RM7035C/RM7065C

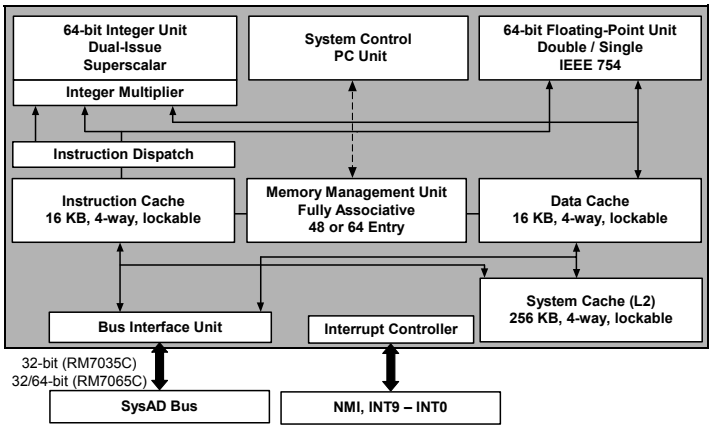
64-Bit MIPS RISC Microprocessors with Integrated L2 Cache

Released
Product Brief

PRODUCT HIGHLIGHTS

- Dual issue symmetric superscalar microprocessor with instruction prefetch optimized for system level price/performance:
  - 466, 533, 600 MHz operating frequency.
  - >1380 Dhrystone 2.1 MIPS @ 600 MHz.
- High-performance system interface:
  - 1600 Mbyte/s peak throughput.
  - 200 MHz maximum frequency using HSTL signaling on the SysAD bus.
  - Multiplexed address/data (SysAD) bus supports 1.5 V, 2.5 V, 3.3 V I/O logic.
  - Processor clock multipliers 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9.
  - Support for 64- or 32-bit interfaces.
- Integrated primary and secondary caches:
  - All are 4-way set associative with 32-byte line size.
  - 16 Kbytes instruction, 16 Kbytes data, 256 Kbytes on-chip secondary.
  - Per line cache locking in primaries and secondary.
  - Fast Packet Cache increases system efficiency in networking applications.
- High-performance floating-point unit - 1600 MFLOPS maximum:
  - Single cycle repeat rate for common single-precision operations and some double-precision operations.
  - Single cycle repeat rate for single-precision combined multiply-add operations.
  - Two cycle repeat rate for double-precision multiply and double-precision combined multiply-add operations.
- MIPS IV superset instruction set architecture:
  - Data PREFETCH instruction allows the processor to overlap cache miss latency and instruction execution.
  - Single-cycle floating-point multiply-add.
- Integrated memory management unit:
  - Fully associative joint TLB (shared by I and D translations).
  - 64/48 dual entries map 128/96 pages.
  - Variable page size.
- Embedded application enhancements:
  - Specialized DSP integer Multiply-Accumulate instructions, (MAD/MADU) and three-operand multiply instruction (MUL).
  - I&D Test/Break-point (Watch) registers for emulation & debug.
  - Performance counter for system and software tuning & debug.
  - 14 fully prioritized vectored interrupts - 10 external, 2 internal, 2 software.

BLOCK DIAGRAM



PACKAGING

- Fully Static 0.13μ CMOS design with dynamic power down logic.
- RM7035C is available in a 128-pin ExposedPad (ePad) package (20 x 20 mm), pin-compatible with the RM5231A 128-pin ePad product.
- RM7065 package options:
  - 256-pin TBGA package, 27 x 27 mm, pin compatible with the RM7065A TBGA product.
  - 216-pin enhanced exposed pad (eePad) package (24 x 24 mm) pin compatible with the RM5261A ePad product.
- Lead-free (Pb-free) options available.

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PMC-SIERRA

Device	CPU Frequency (MHz)	I/D Cache	Integrated L2 Cache Support	External Bus Width
RM7035C	466,533,600	16KB/16KB	256 KB	32-bit
RM7065C	466,533,600	16KB/16KB	256 KB	64-bit

Device	External Bus Frequency (MHz)	VccInt (V)	VccIO (V)	Package
RM7035C	200	1.3	2.5/3.3	128-pin ePad
RM7065C	200	1.3	2.5/3.3	256-pin TBGA or 216-pin eePad

DEVELOPMENT TOOLS

EVALUATION BOARDS AND COMPANION CHIPS

- ITE (RM7035C only):
  - System controller: IT8172G
  - Evaluation board: IT8172 PDK-BSP
- Marvell Semiconductor (RM7065C only):
  - System controllers: MV-64340, GT-64240, GT-96122
  - Evaluation platforms: EV-64340, EV-64240. Both Marvell evaluation boards feature the RM7000C, which features the same CPU core as the RM7065C. The RM7065C does not provide L3 cache functionality.
- Momentum Computer
  - Evaluation platform: Ocelot C. Features RM7000C.

LOGIC ANALYZERS AND EMULATION

- HP
- Tektronix
- Corelis
- Crescent Heart Software

OPERATING SYSTEMS

- Linux by MontaVista and Red Hat
- VxWorks by Wind River Systems
- Nucleus by Accelerated Technology
- Neutrino by QNX Software Systems

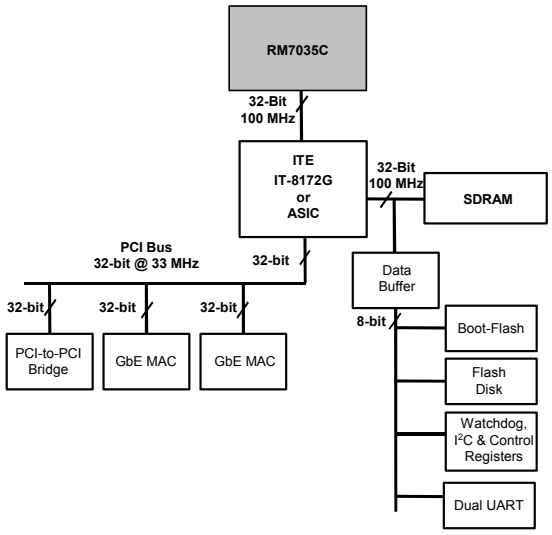
COMPILER SUITES

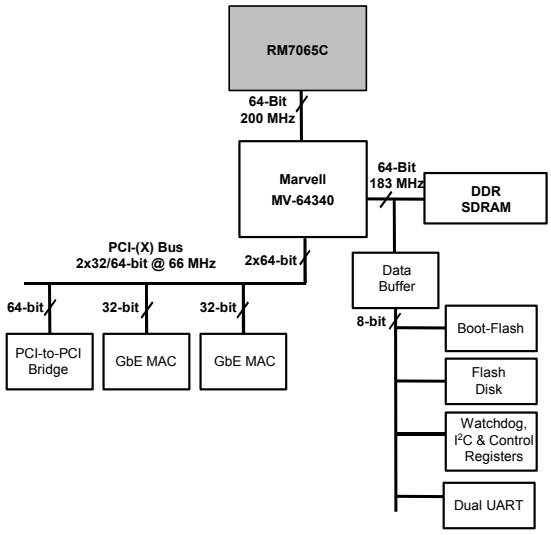
- GNU
- MIPS Technologies
- Green Hills Software
- Red Hat

APPLICATIONS

- Voice Gateways
- Multi-Service Access Platforms
- DSLAMs/Access Concentrators
- Remote Access Switches
- Web Switches
- Layer 3 Switches
- Backbone Switches/Routers

TYPICAL APPLICATIONS





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RM7035C-466L-D004 RM7065C-466G-D004 RM7065C-600G-D004

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