Isolated Switching Regulator with Quad-Channel Isolators

Data Sheet **ADuM4470/ADuM4471/ADuM4472/ADuM4473/ADuM4474**

FEATURES

- Isolated PWM feedback with built in compensation
- Primary side transformer driver for up to 2.5 W output power with 5 V input voltage
- Regulated adjustable output: 3.3 V to 24 V
- Up to 80% efficiency
- Quad dc-to-25 Mbps (NRZ) signal isolation channels
- 200 kHz to 1 MHz adjustable oscillator
- Soft start function at power-up
- Pulse-by-pulse overcurrent protection
- Thermal shutdown
- 5000 V rms isolation
- High common-mode transient immunity: >25 kV/µs
- 20-lead SOIC package with 8.3 mm creepage
- High temperature operation: 105°C

APPLICATIONS

- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Process controls
- RS-232/RS-422/RS-485 transceivers

FUNCTIONAL BLOCK DIAGRAM

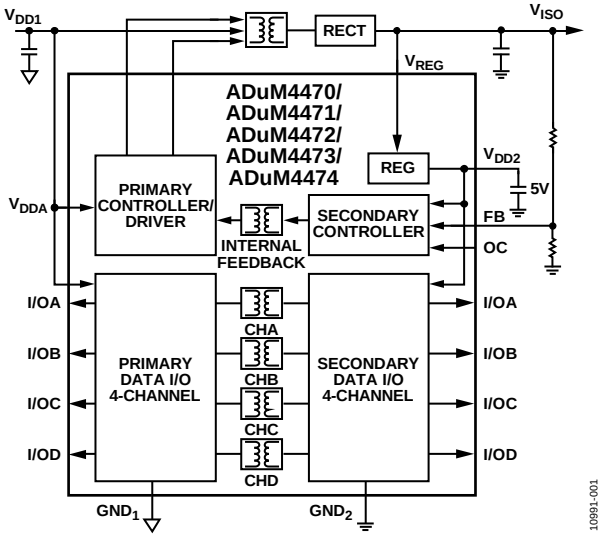

Figure 1.

GENERAL DESCRIPTION

The ADuM4470/ADuM4471/ADuM4472/ADuM4473/ADuM4474[1] are quad-channel, digital isolators with a regulated dc-to-dc isolated power supply controller and an internal MOSFET driver. The dc-to-dc controller has an internal isolated PWM feedback from the secondary side, based on the *i*Coupler® chip scale transformer technology and complete loop compensation. This eliminates the need to use an optocoupler for feedback and compensates the loop for stability.

The ADuM447x isolators provide a more stable output voltage and higher efficiency compared to unregulated isolated dc-to-dc power supplies. The fully integrated feedback and loop compensation in a wide-body SOIC package provide a smaller form factor and 8.3 mm creepage distance solution.

The regulated feedback provides a relatively flat efficiency curve over the full output power range. The ADuM447x enable a dc-to-dc converter with a 3.3 V to 24 V isolated output voltage range from either a 5.0 V or a 3.3 V input voltage, with an output power of up to 2.5 W.

The ADuM447x isolators provide four independent isolation channels in a variety of channel configurations and data rates. (The x in ADuM447x throughout this data sheet stands for the ADuM4470/ADuM4471/ADuM4472/ADuM4473/ADuM4474.)

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7075 329 B2. Other patents pending.

Rev. 0 **Document Feedback**

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REVISION HISTORY

12/12—Revision 0: Initial Version

BLOCK DIAGRAMS OF I/O CHANNELS

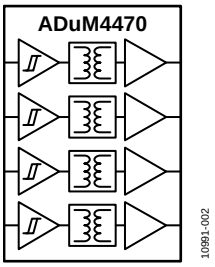

Figure 2. ADuM4470

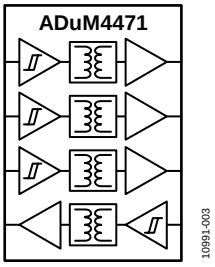

Figure 3. ADuM4471

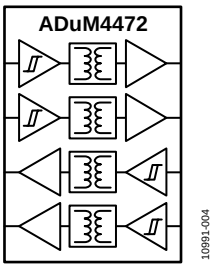

Figure 4. ADuM4472

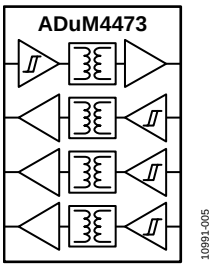

Figure 5. ADuM4473

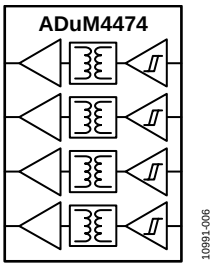

Figure 6. ADuM4474

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ (V_{DD1} = V_{DDA}) ≤ 5.5 V; V_{DD2} = V_{REG} = V_{ISO} = 5.0 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 48. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{DD2} = V_{REG} = V_{ISO} = 5.0 V.

Table 1. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	4.5	5.0	5.5	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	400	500		mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			72		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM4470			14	30	mA	
ADuM4471			15	30	mA	
ADuM4472			16	30	mA	
ADuM4473			17	30	mA	
ADuM4474			18	30	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			44		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			46		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			48		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			50		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			52		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			390		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			388		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			386		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			384		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			382		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			550		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	45	60	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/μs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/μs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

3.0 V ≤ V_{DD1} = V_{DDA} ≤ 3.6 V; V_{DD2} = V_{REG} = V_{ISO} = 3.3 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 48. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 3.3 V, V_{DD2} = V_{REG} = V_{ISO} = 3.3 V.

Table 2. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.6		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	250			mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			68		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1MHz
ADuM4470			9	20	mA	
ADuM4471			10	20	mA	
ADuM4472			11	20	mA	
ADuM4473			11	20	mA	
ADuM4474			12	20	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			28		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			29		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			31		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			32		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			34		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			244		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			243		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			241		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			240		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			238		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			350		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}	1.6			V	
Logic Low Input Threshold	V_{IL}			0.4	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	3.3		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		60	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	60	70	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			45	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			8	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{DD2} = V_{REG} = V_{ISO} = 3.3 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 48. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{DD2} = V_{REG} = V_{ISO} = 3.3 V.

Table 3. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	3.0	3.3	3.6	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO (LINE)}$		1	10	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	2	%	I_{ISO} = 50 mA to 200 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		100		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	400			mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			70		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM4470			9	30	mA	
ADuM4471			10	30	mA	
ADuM4472			11	30	mA	
ADuM4473			11	30	mA	
ADuM4474			12	30	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			33		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			393		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			392		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			390		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			389		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			375		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			350		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	3.3		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	50	70	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			8	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/15 V SECONDARY ISOLATED SUPPLY

4.5 V ≤ V_{DD1} = V_{DDA} ≤ 5.5 V; V_{REG} = V_{ISO} = 15 V; V_{DD2} = 5.0 V; f_{SW} = 500 kHz; all voltages are relative to their respective grounds; see the application schematic in Figure 49. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDA} = 5.0 V, V_{REG} = V_{ISO} = 15 V, V_{DD2} = 5.0 V.

Table 4. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Isolated Output Voltage	V_{ISO}	13.8	15	16.2	V	I_{ISO} = 0 mA, $V_{ISO} = V_{FB} \times (R1 + R2)/R2$
Feedback Voltage Setpoint	V_{FB}	1.15	1.25	1.37	V	I_{ISO} = 0 mA
V_{DD2} Linear Regulator						
Regulator Voltage		4.5	5.0	5.5	V	V_{REG} = 7 V to 15 V, I_{DD2} = 0 mA to 50 mA
Dropout Voltage			0.5	1.5		I_{DD2} = 50 mA
Line Regulation	$V_{ISO (LINE)}$		1	20	mV/V	I_{ISO} = 50 mA, V_{DD1}[1] = V_{DDA}[2] = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	3	%	I_{ISO} = 20 mA to 80 mA
Output Ripple	$V_{ISO (RIP)}$		200		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Output Noise	$V_{ISO (NOISE)}$		500		mV p-p	20 MHz bandwidth, C_{OUT} = 0.1 µF‖47 µF, I_{ISO} = 100 mA
Switching Frequency	f_{SW}		1000		kHz	R_{OC} = 50 kΩ
			200		kHz	R_{OC} = 270 kΩ
		192	318	515	kHz	V_{OC} = V_{DD2} (open-loop)
Switch On-Resistance	R_{ON}		0.5		Ω	
Undervoltage Lockout, V_{DDA}, V_{DD2} Supplies						
Positive Going Threshold	V_{UV+}		2.8		V	
Negative Going Threshold	V_{UV-}		2.6		V	
Hysteresis	V_{UVH}		0.2		V	
DC to 2 Mbps Data Rate[3]						
Maximum Output Supply Current[4]	$I_{ISO (MAX)}$	100			mA	f ≤ 1 MHz, V_{ISO} = 5.0 V
Efficiency at Maximum Output Current[5]			78		%	I_{ISO} = $I_{ISO (MAX)}$, f ≤ 1 MHz
*i*Coupler DATA CHANNELS						
DC to 2 Mbps Data Rate						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (Q)}$					I_{ISO} = 0 mA, f ≤ 1 MHz
ADuM4470			25	45	mA	
ADuM4471			27	45	mA	
ADuM4472			29	45	mA	
ADuM4473			31	45	mA	
ADuM4474			33	45	mA	
25 Mbps Data Rate (CRIZ Grade Only)						
I_{DD1} Supply Current, No V_{ISO} Load	$I_{DD1 (D)}$					
ADuM4470			73		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4471			83		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4472			93		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4473			102		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
ADuM4474			112		mA	I_{ISO} = 0 mA, C_L = 15 pF, f = 12.5 MHz
Available V_{ISO} Supply Current[6]	$I_{ISO (LOAD)}$					f_{SW} = 500 kHz
ADuM4470			91		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4471			89		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4472			86		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4473			83		mA	C_L = 15 pF, f = 12.5 MHz
ADuM4474			80		mA	C_L = 15 pF, f = 12.5 MHz
I_{DD1} Supply Current, Full V_{ISO} Load			425		mA	C_L = 0 pF, f = 0 MHz, V_{DD1} = V_{DDA} = 5 V, I_{ISO} = 400 mA

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}	−20	+0.01	+20	µA	
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DDA} − 0.3, V_{ISO} − 0.3	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDA} − 0.5, V_{ISO} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxH}
			0.0	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxH}
AC SPECIFICATIONS						
ADuM447xARIZ						
Minimum Pulse Width	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}		55	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50	ns	C_L = 15 pF, CMOS signal levels
ADuM447xCRIZ						
Minimum Pulse Width	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		25			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PLH}, t_{PHL}	30	45	60	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			6	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels	t_{PSKCD}			6	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing Directional Channels	t_{PSKCD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DDA} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] V_{DD1} is the power supply for the push-pull transformer.
[2] V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] The contributions of supply current values for all four channels are combined at identical data rates.
[4] The V_{ISO} supply current is available for external use when all data rates are below 2 Mbps. At data rates above 2 Mbps, the data I/O channels draw additional current proportional to the data rate. Additional supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. The dynamic I/O channel load must be treated as an external load and included in the V_{ISO} power budget.
[5] The power demands of the quiescent operation of the data channels were not separated from the power supply section. Efficiency includes the quiescent power consumed by the I/O channels as part of the internal power consumption.
[6] This current is available for driving external loads at the V_{ISO} output. All channels are simultaneously driven at a maximum data rate of 25 Mbps with full capacitive load representing the maximum dynamic load conditions. Refer to the Power Consumption section for calculation of available current at less than the maximum data rate.

PACKAGE CHARACTERISTICS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[2]
Thermal Shutdown						
Thermal Shutdown Threshold	TS_{SD}		150		°C	T_J rising
Thermal Shutdown Hysteresis	TS_{SD-HYS}		20		°C	

[1] The device is considered a 2-terminal device: Pin 1 to Pin 10 are shorted together; and Pin 11 to Pin 20 are shorted together.
[2] See the Thermal Analysis section for thermal model definitions.

REGULATORY APPROVALS (PENDING)

Table 6.

UL	CSA	VDE
Recognized under the UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 5000 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage Reinforced insulation per CSA60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Reinforced insulation per IEC 60601-1 250 V rms (353 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM447x is proof tested by applying an insulation test voltage of ≥6000 V rms for 1 sec (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each of the ADuM447x is proof tested by applying an insulation test voltage of ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 7.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	>8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	>8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure maintenance of the safety data. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 8.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			1273	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 7)			
Case Temperature		T_S	150	°C
Side 1, Side 2 P_{VDDA}, P_{VREG} Power Dissipation		P_{VDDA}, P_{VREG}	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

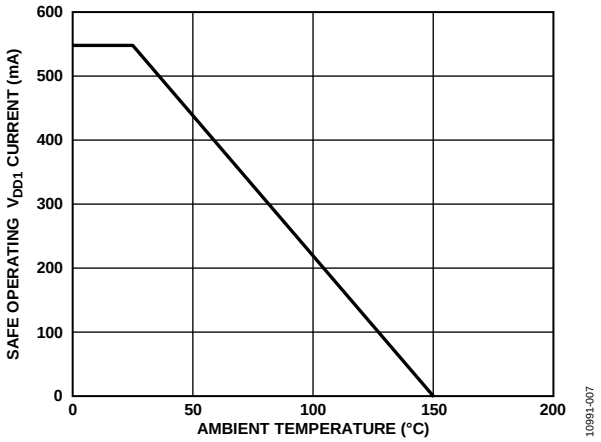

Figure 7. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 9.

Parameter	Symbol	Min	Max	Unit
Temperature				
Operating Temperature	T_A	−40	+105	°C
Supply Voltage				
V_{DD1} at $V_{ISO} = 3.3$ V	V_{DD1}	3.0	3.6	V
V_{DD1} at $V_{ISO} = 3.3$ V	V_{DD1}	4.5	5.5	V
V_{DD1} at $V_{ISO} = 5.0$ V	V_{DD1}	4.5	5.5	V
Load				
Minimum Load	$I_{ISO(MIN)}$	10		mA

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages	
V_{DDA}, V_{DD2} [1, 2]	−0.5 V to +7.0 V
V_{REG}, X1, X2[1]	−0.5 V to +20.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID})	−0.5 V to +V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})	−0.5 V to V_{DDO} +0.5 V
Average Output Current per Pin	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DD1} is the power supply for the push-pull transformer, and V_{DDA} is the power supply of Side 1 of the ADuM447x.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	848	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform	848	V peak	50-year minimum lifetime
DC Voltage	848	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

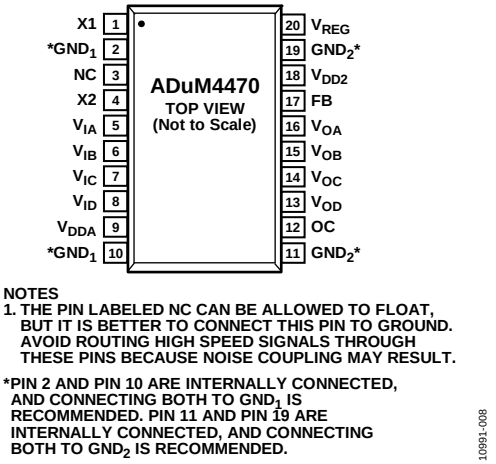

Figure 8. ADuM4470 Pin Configuration

Table 12. ADuM4470 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 8).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{IC}	Logic Input C.
8	V_{ID}	Logic Input D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{OD}	Logic Output D.
14	V_{OC}	Logic Output C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

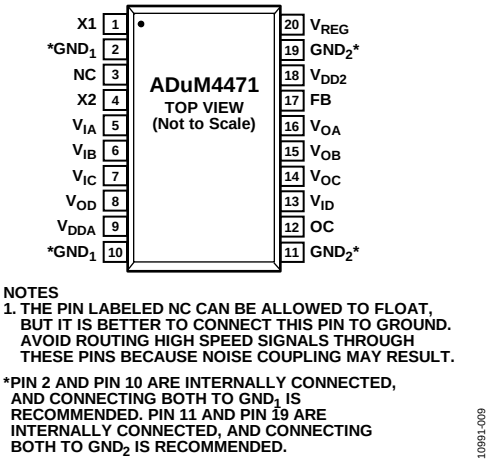

Figure 9. ADuM4471 Pin Configuration

Table 13. ADuM4471 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 9).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{IC}	Logic Input C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{OC}	Logic Output C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

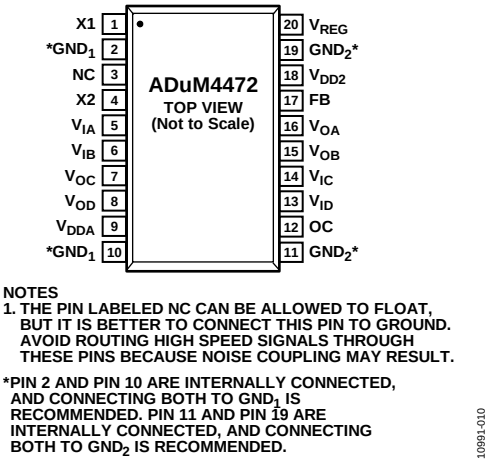

Figure 10. ADuM4472 Pin Configuration

Table 14. ADuM4472 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 10).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{IB}	Logic Input B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{OB}	Logic Output B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

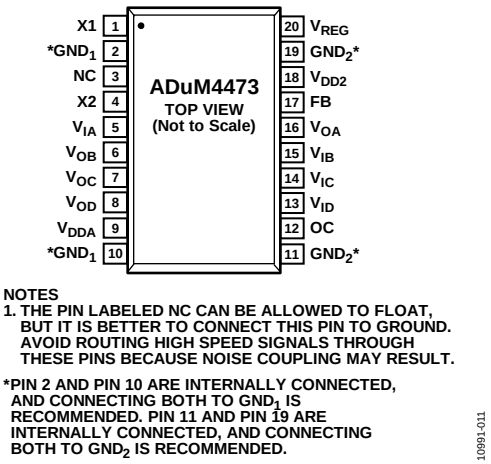

Figure 11. ADuM4473 Pin Configuration

Table 15. ADuM4473 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 11).
4	X2	Transformer Driver Output 2.
5	V_{IA}	Logic Input A.
6	V_{OB}	Logic Output B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{IB}	Logic Input B.
16	V_{OA}	Logic Output A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

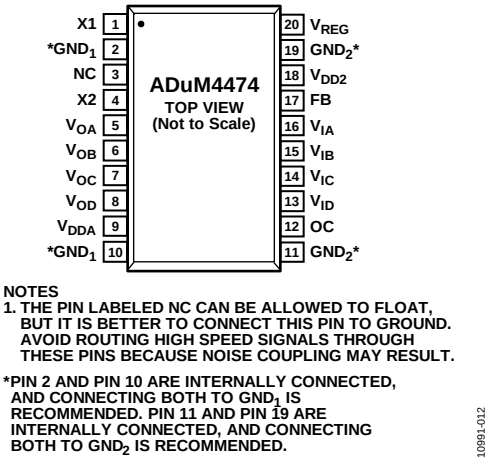

Figure 12. ADuM4474 Pin Configuration

Table 16. ADuM4474 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	Transformer Driver Output 1.
2, 10	GND_1	Ground Reference for Isolator Primary.
3	NC	This pin is not connected internally (see Figure 12).
4	X2	Transformer Driver Output 2.
5	V_{OA}	Logic Output A.
6	V_{OB}	Logic Output B.
7	V_{OC}	Logic Output C.
8	V_{OD}	Logic Output D.
9	V_{DDA}	Primary Supply Voltage 3.0 V to 5.5 V. Connect to V_{DD1}. Connect a 0.1 µF bypass capacitor from V_{DDA} to GND_1.
11, 19	GND_2	Ground Reference for Isolator Side 2.
12	OC	Oscillator Control Pin. When OC = logic high = V_{DD2}, the secondary controller runs open-loop. To regulate the output voltage, connect a resistor between the OC pin and GND_2, and the secondary controller runs at a frequency of 200 kHz to 1 MHz, as programmed by the resistor value.
13	V_{ID}	Logic Input D.
14	V_{IC}	Logic Input C.
15	V_{IB}	Logic Input B.
16	V_{IA}	Logic Input A.
17	FB	Feedback Input from the Secondary Output Voltage, V_{ISO}. Use a resistor divider from V_{ISO} to the FB pin to make the V_{FB} voltage equal to the 1.25 V internal reference level using the $V_{ISO} = V_{FB} \times (R1 + R2)/R2$ formula. The resistor divider is required even in open-loop mode to provide soft start.
18	V_{DD2}	Internal Supply Voltage Pin for the Secondary Side. When a sufficient external voltage is supplied to V_{REG}, the internal regulator regulates the V_{DD2} pin to 5.0 V. Otherwise, V_{DD2} should be in the 3.0 V to 5.5 V range. Connect a 0.1 µF bypass capacitor from V_{DD2} to GND_2.
20	V_{REG}	Input of the Internal Regulator to Power the Secondary Side Controller. V_{REG} should be in the 5.5 V to 15 V range to regulate the V_{DD2} output to 5.0 V.

TYPICAL PERFORMANCE CHARACTERISTICS

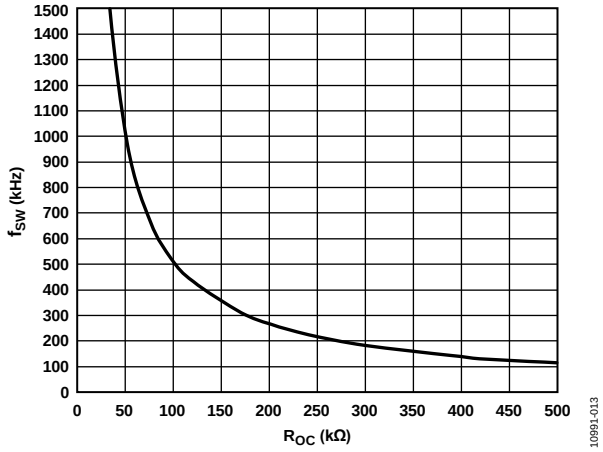

Figure 13. Switching Frequency (f_{SW}) vs. R_{OC} Resistance

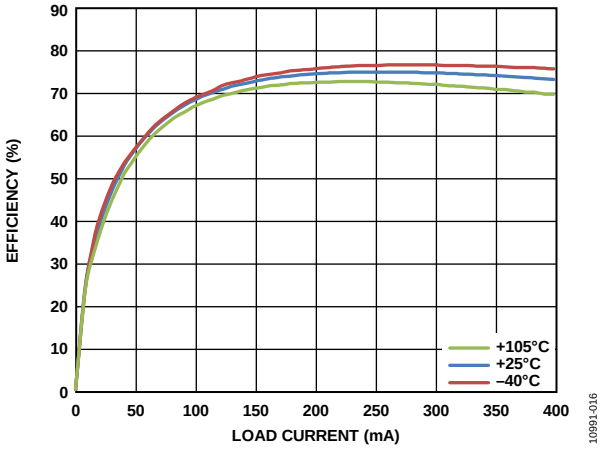

Figure 16. 5 V Input to 5 V Output Efficiency over Temperature with Coilcraft Transformer (CR7983-CL) at 500 kHz f_{SW}

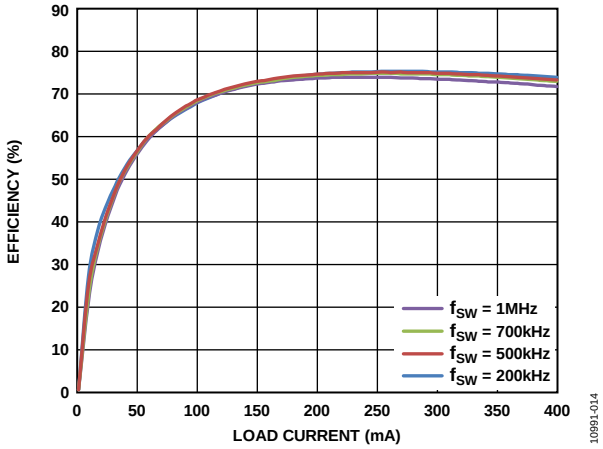

Figure 14. Typical Efficiency at 5 V Input to 5 V Output at Various Switching Frequencies with 1:2 Coilcraft Transformer (CR7983-CL)

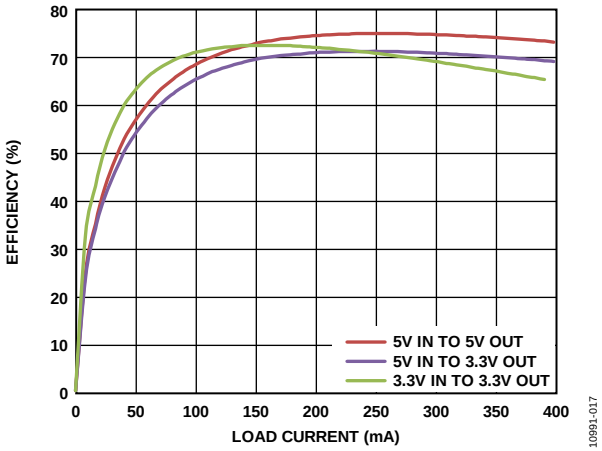

Figure 17. Single-Supply Efficiency with Coilcraft Transformer (CR7983-CL) at 500 kHz f_{SW}

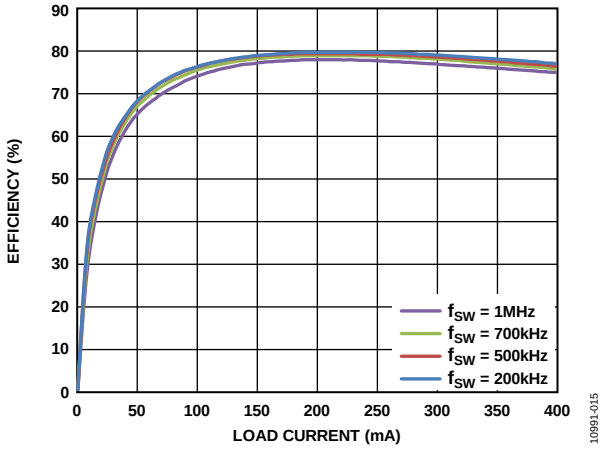

Figure 15. Typical Efficiency at 5 V Input to 5 V Output at Various Switching Frequencies with1:2 Halo Transformer (TGSAD-260V8LF)

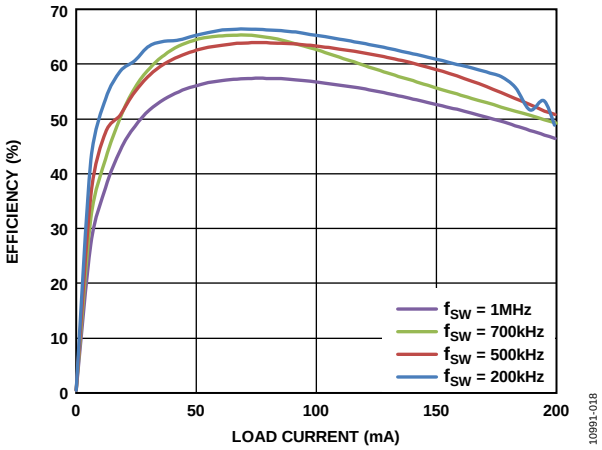

Figure 18. Typical Efficiency at 3.3 V Input to 5 V Output at Various Switching Frequencies with 1:3 Coilcraft Transformer (CR7984-CL)

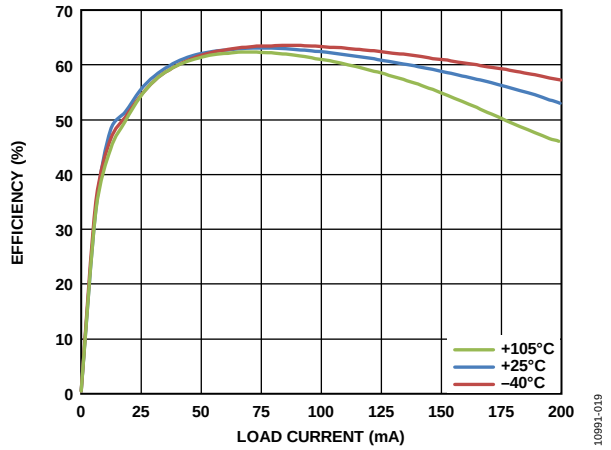

Figure 19. Typical Efficiency at 3.3 V In to 5 V Out over Temperature with 1:3 Coilcraft Transformer (CR7984-CL) at 500 kHz f_{sw}

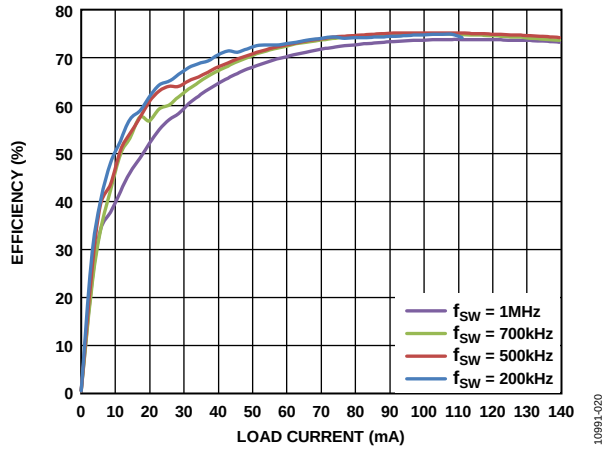

Figure 20. 5 V Input to 15 V Output Efficiency at Various Switching Frequencies with 1: 3 Coilcraft Transformer (CR7984-CL)

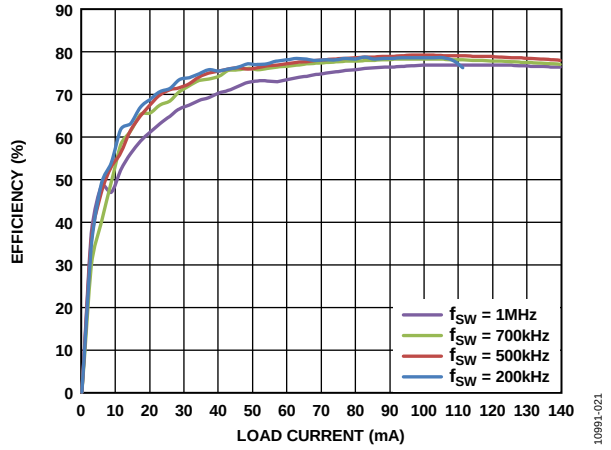

Figure 21. 5 V Input to 15 V Output Efficiency at Various Switching Frequencies with 1:3 Halo Transformer (TGSAD-290V8LF)

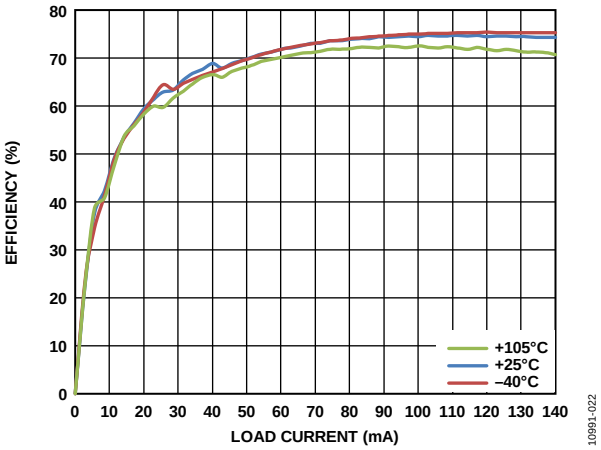

Figure 22. 5 V Input to 15 V Output Efficiency over Temperature with Coilcraft Transformer (CR7984-CL) at 500 kHz f_{SW}

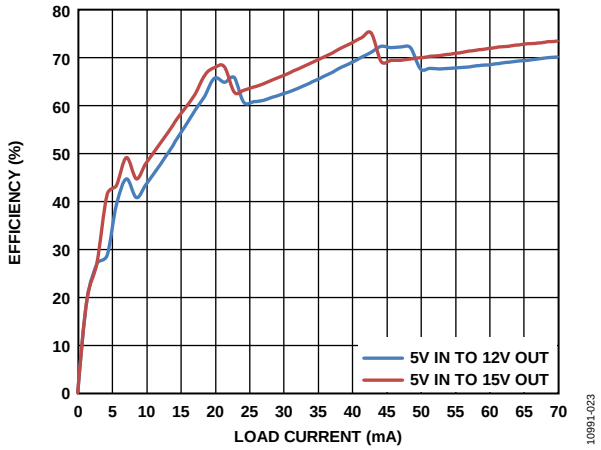

Figure 23. Double-Supply Efficiency with Coilcraft Transformer (CR7985-CL) at 500 kHz f_{SW}

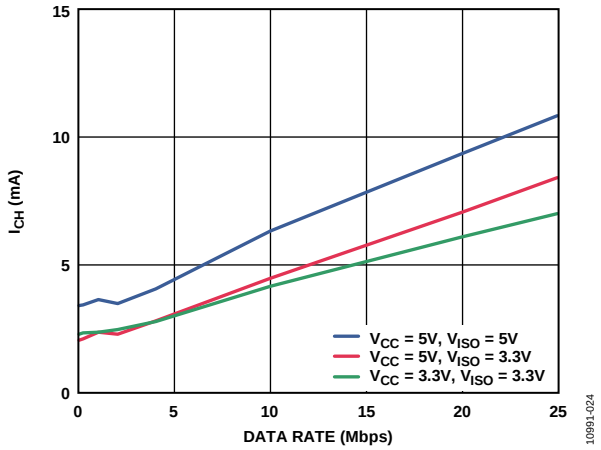

Figure 24. Typical Single-Supply I_{CH} Supply Current per Forward Data Channel (15 pF Output Load)

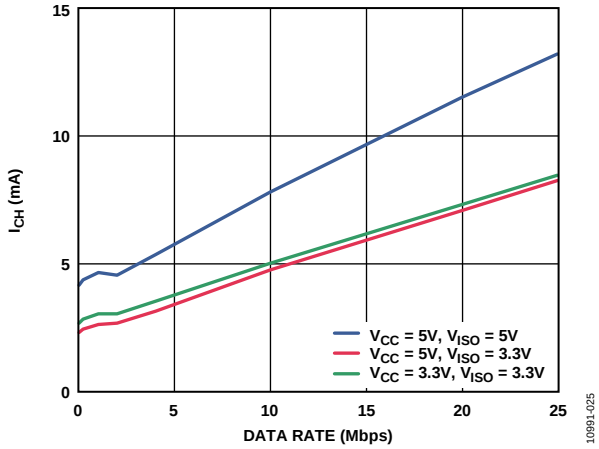

Figure 25. Typical Single-Supply I_{CH} Supply Current per Reverse Data Channel (15 pF Output Load)

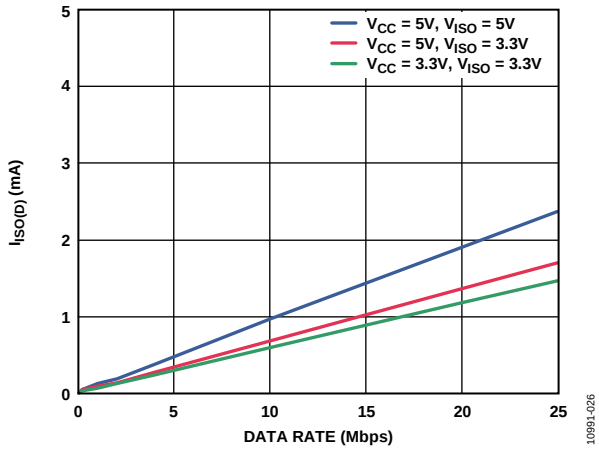

Figure 26. Typical Single-Supply $I_{ISO(D)}$ Dynamic Supply Current per Output Channel (15 pF Output Load)

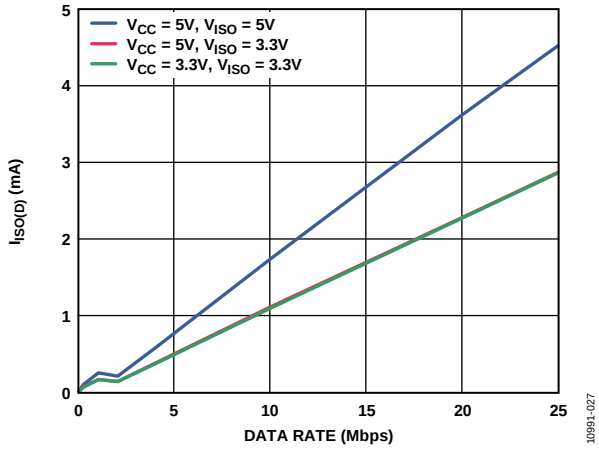

Figure 27. Typical Single-Supply $I_{ISO(D)}$ Dynamic Supply Current per Input Channel (15 pF Output Load)

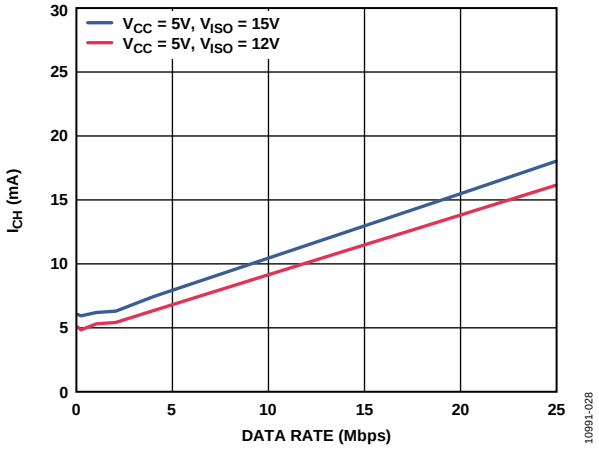

Figure 28. Typical Double-Supply Current I_{CH} Per Forward Data Channel (15 pF Output Load)

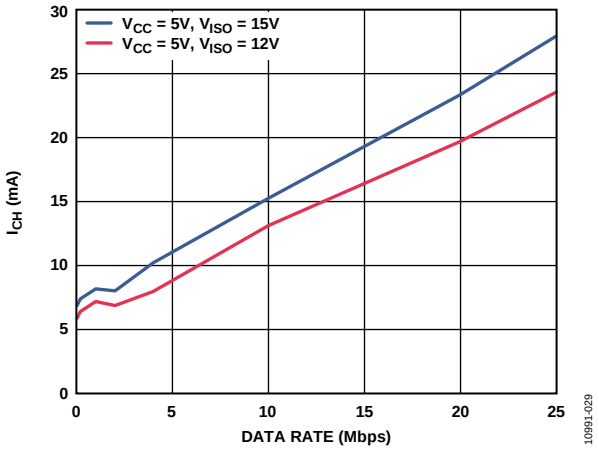

Figure 29. Typical Double-Supply I_{CH} Supply Current per Reverse Data Channel (15 pF Output Data)

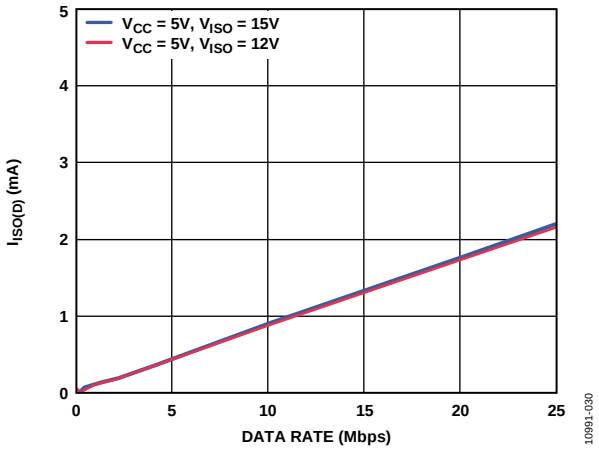

Figure 30. Typical Double-Supply $I_{ISO(D)}$ Dynamic Supply Current per Output Channel (15 pF Output Load)

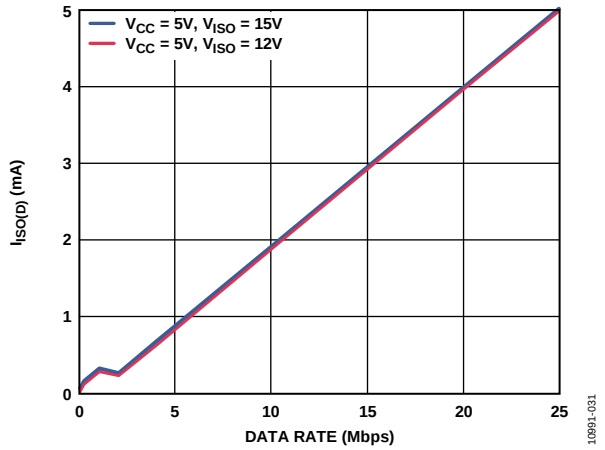

Figure 31. Typical Double-Supply $I_{ISO(D)}$ Dynamic Supply Current per Input Channel

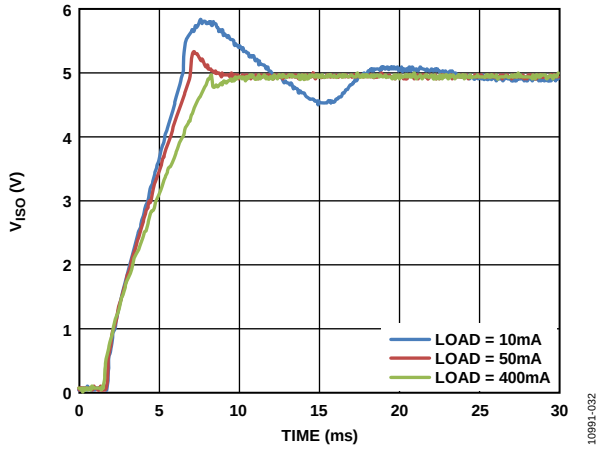

Figure 32. Typical V_{ISO} Startup 5 V Input to 5 V Output with 10 mA, 50 mA, and 400 mA Output Load

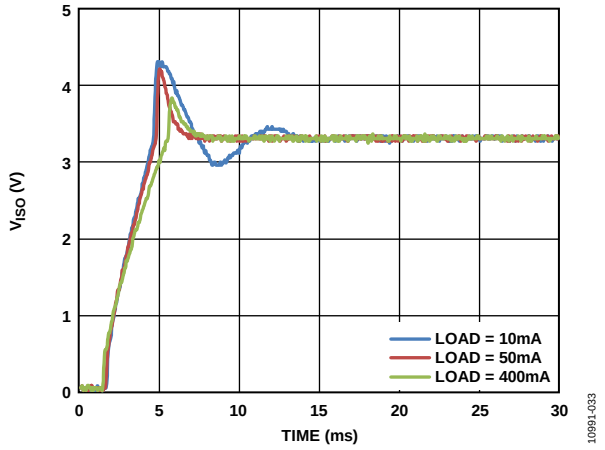

Figure 33. Typical V_{ISO} Startup 5 V Input to 3.3 V Output with 10 mA, 50 mA, and 400 mA Output Load

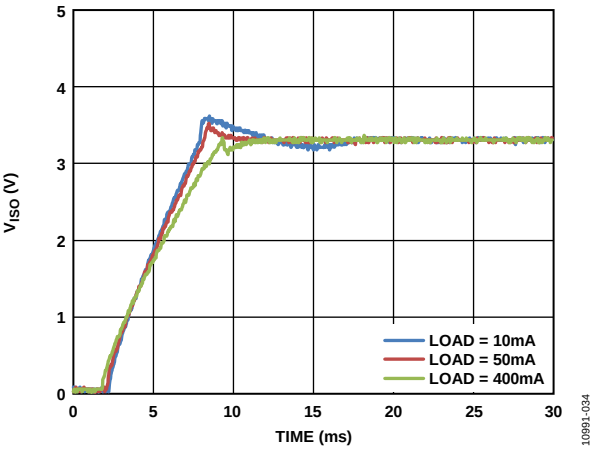

Figure 34. Typical V_{ISO} Startup 3.3 V Input to 3.3 V Output with 10 mA, 50 mA, and 250 mA Output Load

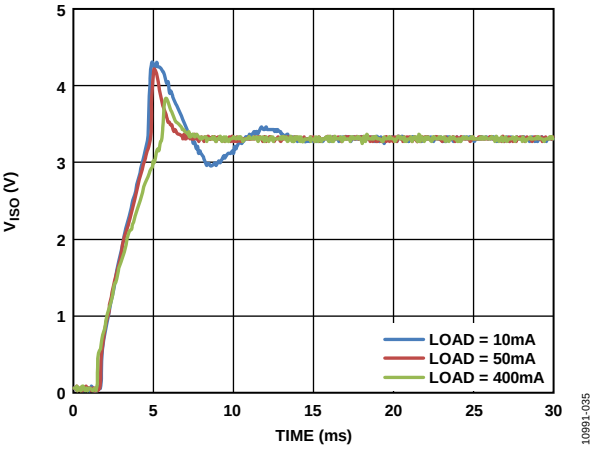

Figure 35. Typical V_{ISO} Startup 5 V Input to 15 V Output with 10 mA, 20 mA, and 100 mA Output Load

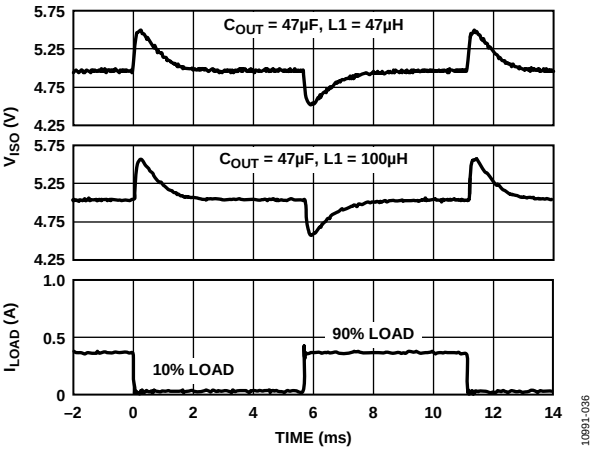

Figure 36. Typical V_{ISO} Load Transient Response 5 V Input to 5 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW}

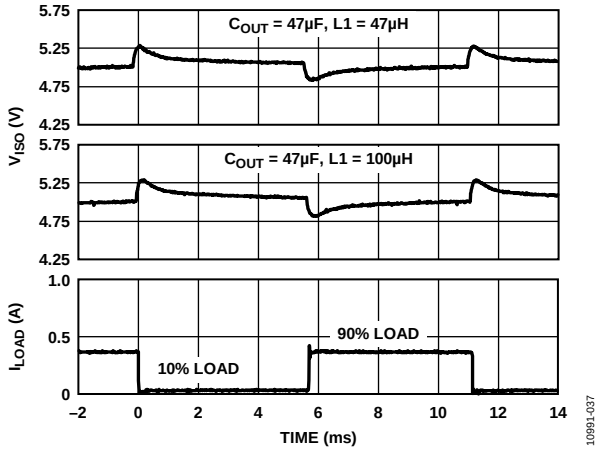

Figure 37. Typical V_{ISO} Load Transient Response 5 V Input to 5 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

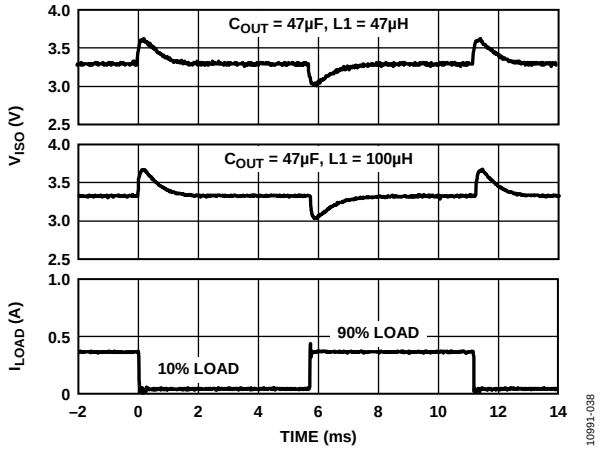

Figure 38. Typical V_{ISO} Load Transient Response 5 V Input to 3.3 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW}

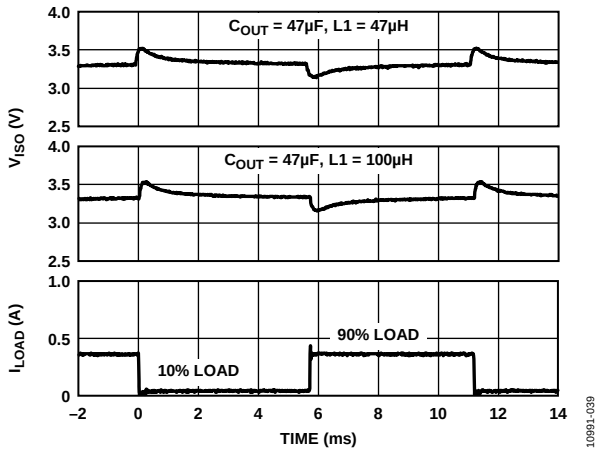

Figure 39. Typical V_{ISO} Load Transient Response 5 V Input to 3.3 V Output at 10% to 90% of 400 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

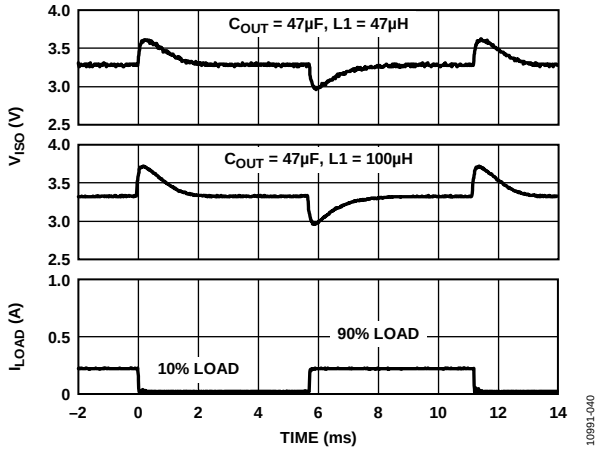

Figure 40. Typical V_{ISO} Load Transient Response 3.3 V Input to 3.3 V Output at 10% to 90% of 250 mA Load at 500 kHz f_{SW}

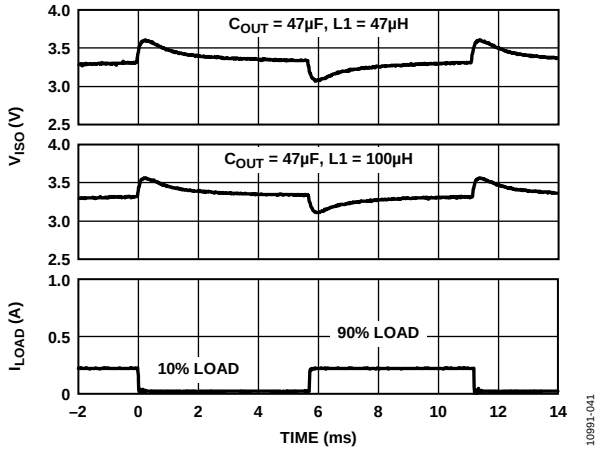

Figure 41. Typical V_{ISO} Load Transient Response 3.3 V Input to 3.3 V Output at 10% to 90% of 250 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

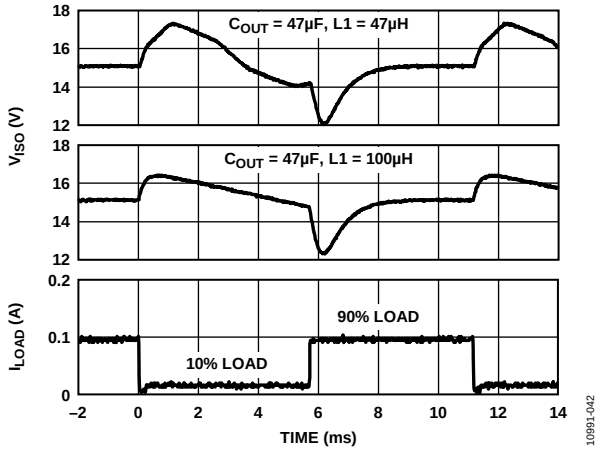

Figure 42. Typical V_{ISO} Load Transient Response 5 V Input to 15 V Output at 10% to 90% of 100 mA Load at 500 kHz f_{SW}

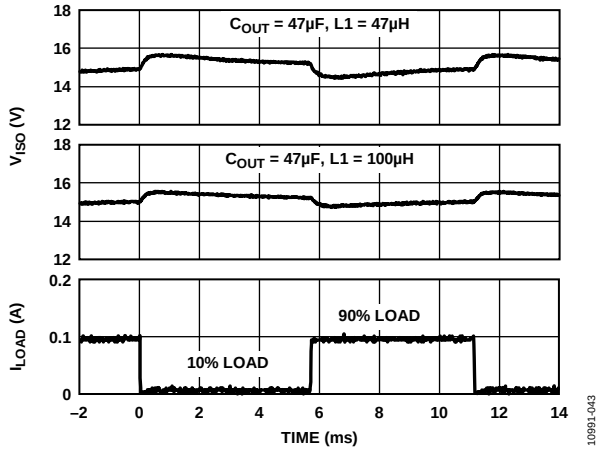

Figure 43. Typical V_{ISO} Load Transient Response 5 V Input to 15 V Output at 10% to 90% of 100 mA Load at 500 kHz f_{SW} with 0.1 µF Feedback Capacitor

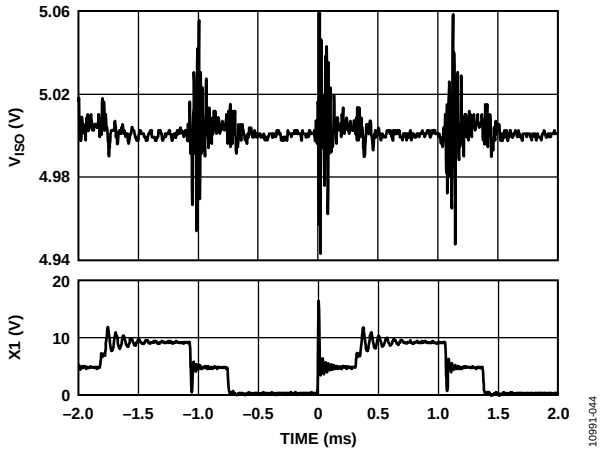

Figure 44. Typical V_{ISO} Output Ripple, 5 V Input to 5 V Output at 400 mA Load at 500 kHz f_{SW}

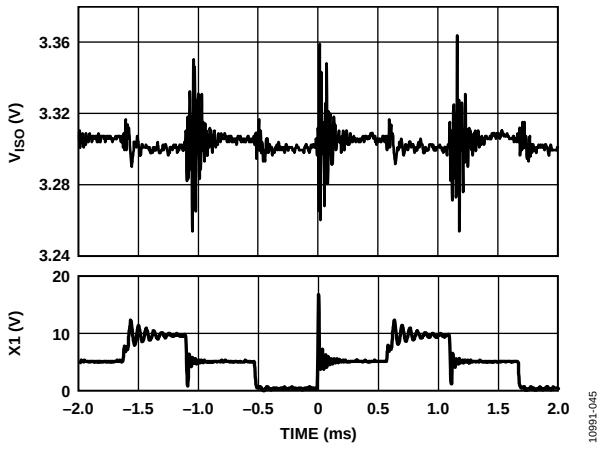

Figure 45. Typical V_{ISO} Output Ripple, 5 V Input to 3.3 V Output at 400 mA Load at 500 kHz f_{SW}

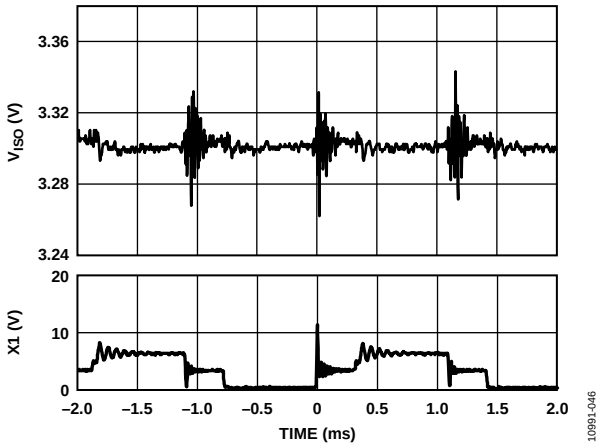

Figure 46. Typical V_{ISO} Output Ripple, 3.3 V Input to 3.3 V Output at 250 mA Load at 500 kHz f_{SW}

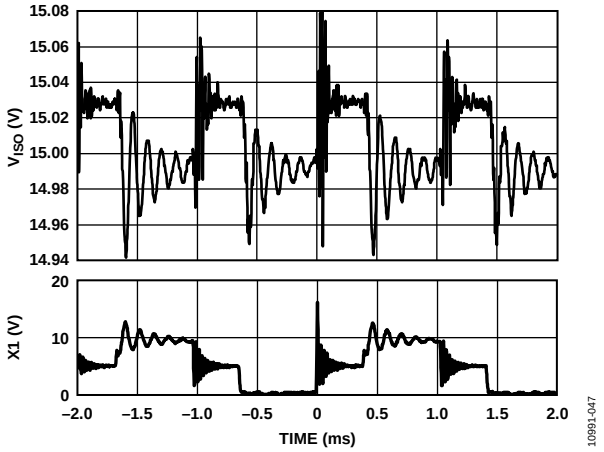

Figure 47. Typical V_{ISO} Output Ripple, 5 V Input to 15 V Output at 100 mA Load at 500 kHz f_{SW}

APPLICATIONS INFORMATION

THEORY OF OPERATION

The dc-to-dc converter section of the ADuM447x uses a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DD1} power is supplied to an oscillating circuit that switches current to the primary of an external power transformer using internal push-pull switches at the X1 and X2 pins. Power transferred to the secondary side of the transformer is full-wave rectified with external Schottky diodes (D1 and D2), filtered with the L1 inductor and C_{OUT} capacitor, and regulated to the isolated power supply voltage from 3.3 V to 15 V. The secondary (V_{ISO}) side controller regulates the output by using a feedback voltage, V_{FB}, from a resistor divider on the output and creating a PWM control signal that is sent to the primary (V_{DD1}) side by a dedicated *i*Coupler data channel labeled V_{FB}. The primary side PWM converter varies the duty cycle of the X1 and X2 switches to modulate the oscillator circuit and control the power being sent to the secondary side. This feedback allows for significantly higher power and efficiency.

The ADuM447x implements undervoltage lockout (UVLO) with hysteresis on the V_{DDA} and V_{DD2} power inputs. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

A minimum load current of 10 mA is recommended to ensure optimum load regulation. Smaller loads can generate excess noise on the output because of short or erratic PWM pulses. Excess noise generated this way can cause regulation problems in some circumstances.

APPLICATION SCHEMATICS

The ADuM447x have three main application schematics (see Figure 48 to Figure 50). Figure 48 has a center-tapped secondary and two Schottky diodes providing full wave rectification for a single output, typically for power supplies of 3.3 V, 5 V, 12 V, and 15 V. For single supplies when V_{ISO} = 3.3 V or V_{ISO} = 5 V, see the note in Figure 48 about connecting together V_{REG}, V_{DD2}, and V_{ISO}. Figure 49 is a voltage doubling circuit that can be used for a single supply whose output exceeds 15 V, which is the largest supply that can be connected to the regulator input, Pin V_{REG}, of the part. With Figure 49, the output voltage can be as high as 24 V and the V_{REG} pin only about 12 V. When using the circuit shown in Figure 49, to obtain an output voltage lower than 10 V (for example, V_{DD1} = 3.3 V, V_{ISO} = 5 V), connect V_{REG} to V_{ISO} directly. Figure 50, which also uses a voltage doubling secondary circuit, shows an example of a coarsely regulated, positive power supply and an unregulated, negative power supply for outputs of approximately ±5 V, ±12 V, and ±15 V. For any circuit in Figure 48, Figure 49, or Figure 50, the isolated output voltage (V_{ISO}) can be set using the voltage dividers, R1 and R2 (with values of 1 kΩ to 100 kΩ), in the application schematics using the following equation:

$$V_{ISO} = V_{FB} \times \frac{R1 + R2}{R2}$$

where V_{FB} is the internal feedback voltage, which is approximately 1.25 V.

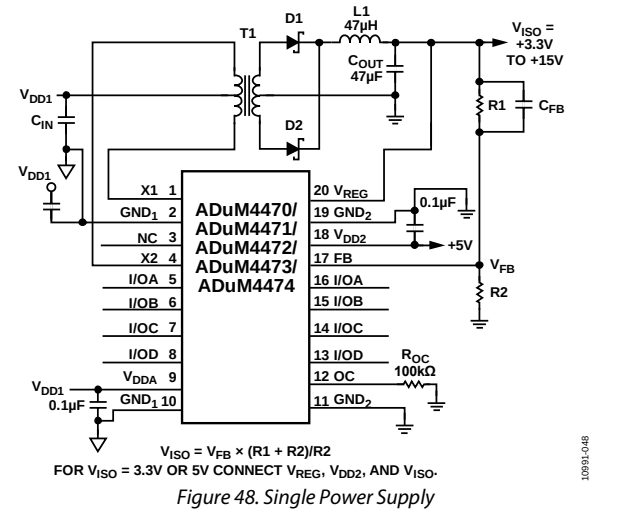

Figure 48. Single Power Supply

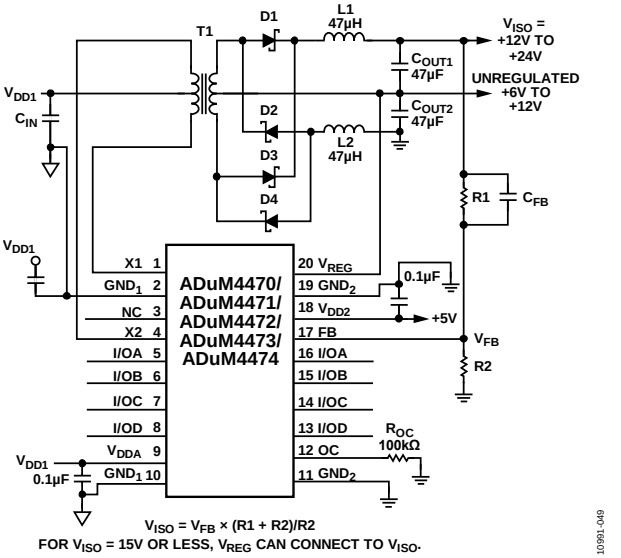

Figure 49. Doubling Power Supply

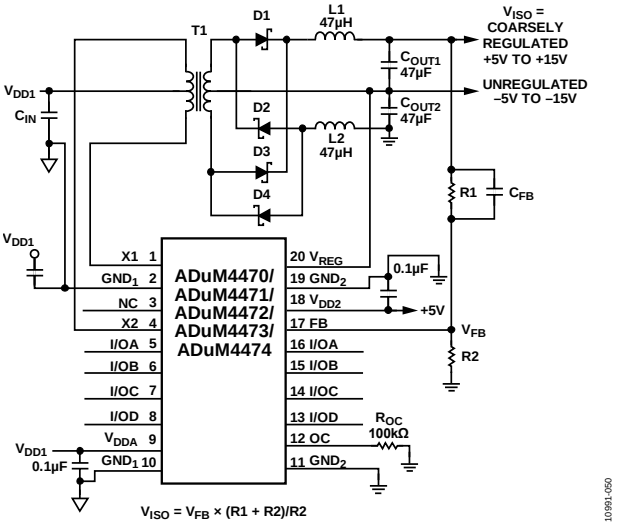

Figure 50. Positive and Unregulated Negative Supply

TRANSFORMER DESIGN

Transformers that have been designed for use in the circuits shown in Figure 48, Figure 49, and Figure 50 are listed in Table 17. The design of a transformer for the ADuM447x can differ from some isolated dc-to-dc converter designs that do not regulate the output voltage. The output voltage is regulated by a PWM controller in the ADuM47x that varies the duty cycle of the primary side switches in response to a secondary side feedback voltage, V_{FB}, received through an isolated digital channel. The internal controller has a limit of 40% maximum duty cycle.

TRANSFORMER TURNS RATIO

To determine the transformer turns ratio, and taking into account the losses for the primary switches and the losses for the secondary diodes and inductors, the external transformer turns ratio for the ADuM447x can be calculated by

$$\frac{N_S}{N_P} = \frac{V_{ISO} + V_D}{V_{DD1(MIN)} \times D \times 2} \quad (1)$$

where:
N_S/N_P is the primary to secondary turns ratio.
V_{ISO} is the isolated output supply voltage.
V_D is the Schottky diode voltage drop (0.5 V maximum).
$V_{DD1(MIN)}$ is the minimum input supply voltage.
D is the duty cycle = 0.30 for a 30% typical duty cycle, 40% is maximum, and a multiplier factor of 2 is used for the push-pull switching cycle.

For example, using the circuit in Figure 48 and the 5 V to 5 V reference design in Table 17, with $V_{DD1\,(MIN)}$ = 4.5 V, the turns ratio is N_S/N_P = 2.

For a similar 3.3 V input to 3.3 V output, isolated single power supply, and with $V_{DD1(MIN)}$ = 3.0 V, the turns ratio is also N_S/N_P = 2. Therefore, the same transformer turns ratio N_S/N_P = 2 can be used for the three single power applications (5 V to 5 V, 5 V to 3.3 V, and 3.3 V to 3.3 V).

In Figure 49, the circuit uses double windings and diode pairs to create a doubler circuit; therefore, half the output voltage, $V_{ISO}/2$, is used in the equation:

$$\frac{N_S}{N_P} = \frac{\frac{V_{ISO}}{2} + V_D}{V_{DD1(MIN)} \times D \times 2} \quad (2)$$

N_S/N_P is the primary to secondary turns ratio.
$V_{ISO}/2$ is used in the equation because the circuit uses two pairs of diodes creating a doubler circuit.
V_D is the Schottky diode voltage drop (0.5 V maximum).
$V_{DD1(MIN)}$ is the minimum input supply voltage.
D is duty cycle, which equals 0.30 for a 30% typical duty cycle, 40% is maximum, and a multiplier factor of 2 is used for the push-pull switching cycle.

For example, using the circuit in Figure 49 and the 5 V to 15 V reference design in Table 17, with $V_{DD1(MIN)}$ = 4.5 V, the turns ratio is N_S/N_P = 3.

In Figure 50, the circuit also uses double windings and diode pairs to create a doubler circuit; however, because a positive and negative output voltage is created, V_{ISO} is used in the equation:

$$\frac{N_S}{N_P} = \frac{V_{ISO} + V_D}{V_{DD1(MIN)} \times D \times 2} \quad (3)$$

where:
N_S/N_P is the primary to secondary turns ratio.
V_{ISO} is the isolated output supply voltage and is used in the equation because the circuit uses two pairs of diodes, creating a doubler circuit with a positive and negative output.
V_D is the Schottky diode voltage drop (0.5 V maximum).
$V_{DD1(MIN)}$ is the minimum input supply voltage, and a multiplier factor of 2 is used for the push-pull switching cycle.
D is the duty cycle; in this case, a higher duty cycle of D = 0.35 for a 35% typical duty cycle (40% is maximum) was used in the Figure 50 circuit to reduce the maximum voltages seen by the diodes for a ±15 V supply.

For example, using the circuit in Figure 50 and the +5 V to ±15 V reference design in Table 17, with $V_{DD1(MIN)}$ = 4.5 V, the turns ratio is N_S/N_P = 5.

TRANSFORMER ET CONSTANT

The next transformer design factor to consider is the ET constant. This constant determines the minimum V × µs constant of the transformer over the operating temperature. ET values of 14 V × µs and 18 V × µs were selected for the ADuM447x designs listed in Table 17 using the following equation:

$$ET(MIN) = \frac{V_{DD1(MAX)}}{f_{SW(MIN)} \times 2} \quad (4)$$

where:
$V_{DD1(MAX)}$ is the maximum input supply voltage.
$f_{SW(MIN)}$ is the minimum primary switching frequency = 300 kHz in startup, and a multiplier factor of 2 is used for the push-pull switching cycle.

TRANSFORMER PRIMARY INDUCTANCE AND RESISTANCE

Another important characteristic of the transformer for designs with the ADuM447x is the primary inductance. Transformers for the ADuM447x are recommended to have between 60 µH to 100 µH of inductance per primary winding. Values of primary inductance in this range are needed for smooth operation of the ADuM447x pulse-by-pulse current-limit circuit, which can help protect against buildup of saturation currents in the transformer. If the inductance is specified for the total of both primary windings, for example, as 400 µH, the inductance of one winding is ¼ of two equal windings, or 100 µH.

Another important characteristic of the transformer for designs with the ADuM447x is primary resistance. Primary resistance as low as is practical (less than 1 Ω) helps reduce losses and improves efficiency. The dc primary resistance can be measured and specified, and is shown for the transformers in Table 17.

TRANSFORMER ISOLATION VOLTAGE

Isolation voltage and isolation type should be determined for the requirements of the application and then specified. The transformers in Table 17 have been specified for 2500 V rms for supplemental or basic isolation and for 1500 V rms functional isolation. Other isolation levels and isolation voltages can be specified and requested from the manufacturers in Table 17 or from other manufacturers.

SWITCHING FREQUENCY

The ADuM447x switching frequency can be adjusted from 200 kHz to 1 MHz by changing the value of the R_{OC} resistor shown in Figure 48, Figure 49, and Figure 50. The value of the R_{OC} resistor needed for the desired switching frequency can be determined from the switching frequency vs. the R_{OC} resistance curve shown in Figure 13. The output filter inductor value and output capacitor value for the ADuM447x application schematics have been designed to be stable over the switching frequency range from 500 kHz to 1 MHz, when loaded from 10% to 90% of the maximum load.

The ADuM447x also has an open-loop mode where the output voltage is not regulated and is dependent on the transformer turns ratio, N_S/N_P, and the conditions of the output, including output load current and the losses in the dc-to-dc converter circuit. This open-loop mode is selected when the OC pin is connected high to the V_{DD2} pin. In open-loop mode, the switching frequency is 318 kHz.

TRANSIENT RESPONSE

The load transient response of the output voltage of the ADuM447x for 10% to 90% of the full load is shown in Figure 36 to Figure 43 for the application schematics in Figure 48 to Figure 50. The response shown is slow but stable and can have more output change than desired for some applications. The output voltage change with load transient has been reduced, and the output has been shown to remain stable by adding more inductance to the output circuits, as shown in the second V_{ISO} output waveform in Figure 36 to Figure 43.

For additional improvement in transient response, add a 0.1 µF ceramic capacitor (C_{FB}) in parallel with the high feedback resistor. As shown in Figure 36 to Figure 43, this value helps reduce the overshoot and undershoot during load transients.

Table 17. Transformer Reference Designs

Part No.	Manufacturer	Turns Ratio, PRI:SEC	ET Constant (V × µs Min)	Total Primary Inductance (µH)	Total Primary Resistance (Ω)	Isolation Voltage (rms)	Isolation Type	Reference
CR7983-CL	Coilcraft	1CT:2CT	18	256	0.2	5000	Reinforced	Figure 48
CR7984-CL	Coilcraft	1CT:3CT	18	256	0.2	5000	Reinforced	Figure 49
CR7985-CL	Coilcraft	1CT:5CT	18	256	0.2	5000	Reinforced	Figure 50
TGRAD-560V8LF	Halo Electronics	1CT:2CT	14	398	0.8	5000	Supplemental	Figure 48
TGRAD-590V8LF	Halo Electronics	1CT:3CT	14	398	0.8	5000	Supplemental	Figure 49

COMPONENT SELECTION

Power supply bypassing is required at the input and output supply pins. Note that a low ESR ceramic bypass capacitor of 0.1 µF is required on Side 1 between Pin 9 and Pin 10, and on Side 2 between Pin 18 and Pin 19, as close to the chip pads as possible.

The power supply section of the ADuM447x uses a high oscillator frequency to efficiently pass power through the external power transformer. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor; ripple suppression and proper regulation require a large value capacitor. To suppress noise and reduce ripple, large-valued ceramic capacitors of X5R or X7R dielectric type are recommended. The recommended capacitor value is 10 µF for V_{DD1} and 47 µF for V_{ISO}. These capacitors have a low ESR and are available in moderate 1206 or 1210 sizes for voltages up to 10 V. For output voltages larger than 10 V, two 22 µF ceramic capacitors can be used in parallel. See Table 18 for suggested components.

Inductors must be selected based on the value and supply current needed. Most applications with switching frequencies between 500 kHz and 1 MHz and load transients between 10% and 90% of full load are stable with the 47 µH inductor value listed in Table 18. Values as large as 200 µH can be used for power supply applications with a switching frequency as low as 200 kHz to help stabilize the output voltage or for improved load transient response (see Figure 36 to Figure 39). Inductors in a small 1212 or 1210 size are listed in Table 18 with a 47 µH value and a 0.41 A current rating to handle the majority of applications below a 400 mA load, and with a 100 µH value and a 0.34 A current rating to handle a load to 300 mA.

Schottky diodes are recommended for their low forward voltage to reduce losses and their high reverse voltage of up to 40 V to withstand the peak voltages available in the doubling circuit shown in Figure 49 and Figure 50.

Table 18. Suggested Components

Part Number	Manufacturer	Value
GRM32ER71A476KE15L	Murata	47 µF, 10 V, X7R, 1210
GRM32ER71C226KEA8L	Murata	22 µF, 16 V, X7R, 1210
GRM31CR71A106KA01L	Murata	10 µF, 10 V, X7R, 1206
MBR0540T1-D	ON Semiconductor	0.5 A, 40 V, Schottky, SOD-123
LQH3NPN470MM0	Murata	47 µH, 0.41 A, 1212
ME3220-104KL	Coilcraft	100 µH, 0.34 A, 1210
LQH6PPN470M43	Murata	47 µH, 1.10 A, 2424
LQH6PPN101M43	Murata	100 µH, 0.80 A, 2424

PRINTED CIRCUIT BOARD (PCB) LAYOUT

Note that the total lead length between the ends of the low ESR capacitor and the V_{DDx} and GND_x pins must not exceed 2 mm. See Figure 51 for the recommended PCB layout.

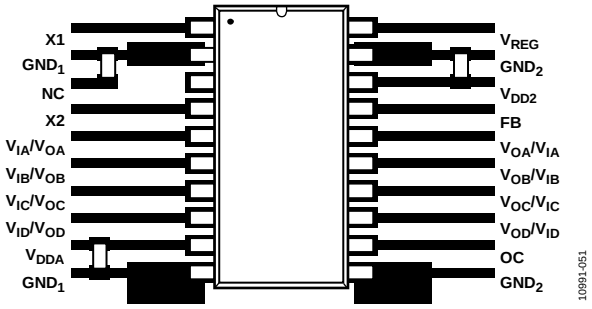

Figure 51. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins, exceeding the absolute maximum ratings specified in Table 10, thereby leading to latch-up and/or permanent damage.

The ADuM447x are power devices that dissipate about 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the devices primarily depend on heat dissipation into the PCB through the GND_x pins. If the devices are used at high ambient temperatures, take care to provide a thermal path from the GND_x pins to the PCB ground plane. The board layout shows enlarged pads for the GND_x pins (Pin 2 and Pin 10 on Side 1 and Pin 11 and Pin 19 on Side 2). Large diameter vias should be implemented from the pad to the ground planes and power planes to increase thermal conductivity and to reduce inductance. Multiple vias in the thermal pads can significantly reduce temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

THERMAL ANALYSIS

The ADuM447x consist of two internal die attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} from Table 5. The value of θ_{JA} is based on measurements taken with the parts mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM447x operate at a full load across the full temperature range without derating the output current. However, following the recommendations in the Printed Circuit Board (PCB) Layout section decreases thermal resistance to the PCB, allowing increased thermal margins in high ambient temperatures. The ADuM447x has an thermal shutdown circuit that shuts down the dc-to-dc converter and the outputs of the ADuM447x when a die temperature of about 160°C is reached. When the die cools below about 140°C, the ADuM447x dc-to-dc converter and outputs turn on again.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component (see Figure 52). The propagation delay to a logic low output may differ from the propagation delay to a logic high output.

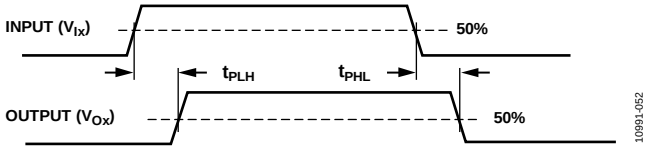

Figure 52. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM447x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM447x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 17) by the watchdog timer circuit. This situation should occur in the ADuM447x devices only during power-up and power-down operations.

The limitation on the ADuM447x magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3.3 V operating condition of the ADuM447x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM447x and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 53.

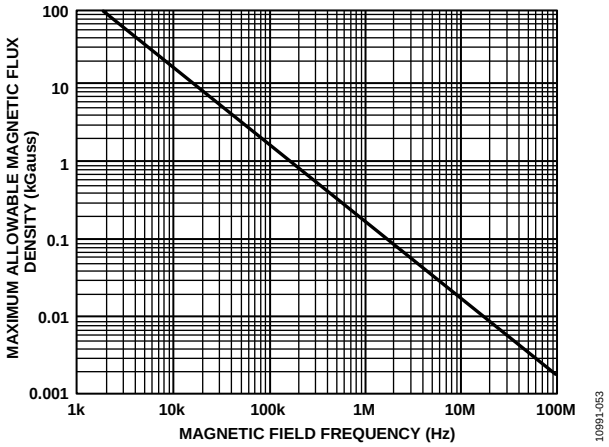

Figure 53. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM447x transformers. Figure 54 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 54, the ADuM447x are extremely immune and can be affected only by extremely large currents operated at a high frequency that is very close to the component. For the 1 MHz example, a 0.5 kA current needs to be placed 5 mm away from the ADuM447x to affect component operation.

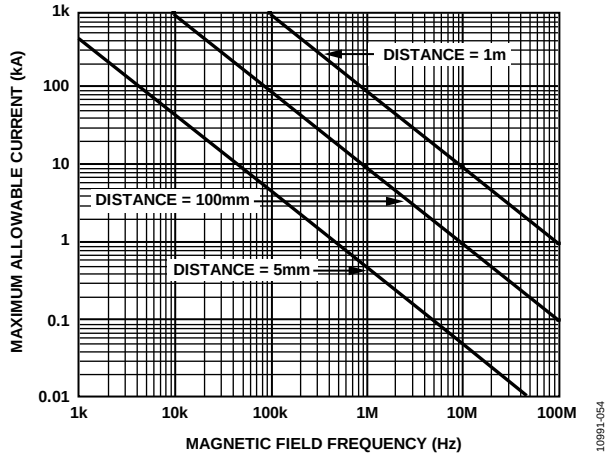

Figure 54. Maximum Allowable Current for Various Current-to-ADuM447x Spacings

In combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages that are sufficiently large to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The V_{DDA} power supply input provides power to the *i*Coupler data channels, as well as to the power converter. For this reason, the quiescent currents drawn by the data converter and the primary and secondary I/O channels cannot be determined separately. All of these quiescent power demands have been combined into the $I_{DDA\,(Q)}$ current, as shown in Figure 55. The total I_{DD} supply current is equal to the sum of the quiescent operating current; the dynamic current, $I_{DDA\,(D)}$, demanded by the I/O channels; and any external I_{ISO} load.

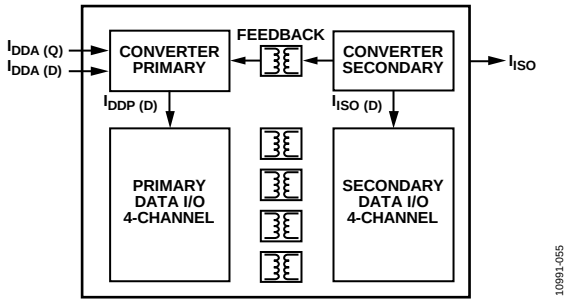

Figure 55. Power Consumption Within the ADuM447x

Dynamic I/O current is consumed only when operating a channel at speeds higher than the refresh rate of f_r. The dynamic current of each channel is determined by its data rate. Figure 24 and Figure 28 show the current for a channel in the forward direction, meaning that the input is on the V_{DDA} and V_{DD2} side of the part. Figure 25 and Figure 29 show the current for a channel in the reverse direction, meaning that the input is on the V_{ISO} side of the part. Figure 24, Figure 25, Figure 28, or Figure 29 assume a typical 15 pF output load.

The following relationship allows the total I_{DD1} current to be

$$I_{DD1} = (I_{ISO} \times V_{ISO})/(E \times V_{DD1}) + \Sigma\, I_{CHn};\ n = 1 \text{ to } 4 \quad (5)$$

where:
I_{DD1} is the total supply input current.
I_{ISO} is the current drawn by the secondary side external load.
E is the power supply efficiency at the given output load from Figure 17 or Figure 23 at the V_{ISO}, V_{DDA}, and V_{DD2} condition of interest.
I_{CHn} is the current drawn by a single channel determined from Figure 24, Figure 25, Figure 28, or Figure 29, depending on channel direction.

The maximum external load can be calculated by subtracting the dynamic output load from the maximum allowable load.

$$I_{ISO\,(LOAD)} = I_{ISO\,(MAX)} - \Sigma\, I_{ISO\,(D)n};\ n = 1 \text{ to } 4 \quad (6)$$

where:
$I_{ISO\,(LOAD)}$ is the current available to supply an external secondary side load.
$I_{ISO\,(MAX)}$ is the maximum external secondary side load current available at V_{ISO}.
$I_{ISO\,(D)n}$ is the dynamic load current drawn from V_{ISO} by an output or input channel, as shown for a single supply in Figure 26 or Figure 27 or for a double supply in Figure 30 or Figure 31.

The preceding analysis assumes a 15 pF capacitive load on each data output. If the capacitive load is larger than 15 pF, the additional current must be included in the analysis of I_{DD1} and $I_{ISO\,(LOAD)}$.

POWER CONSIDERATIONS

Soft Start Mode and Current-Limit Protection

When the ADuM447x first receives power from V_{DDA}, it is in soft start mode, and the output voltage, V_{ISO}, is increased gradually while it is below the start-up threshold. In soft start mode, the width of the PWM signal is increased gradually by the primary converter to limit the peak current during V_{ISO} power-up. When the output voltage is larger than the start-up threshold, the PWM signal can be transferred from the secondary controller to the primary converter, and the dc-to-dc converter switches from soft start mode to the normal PWM control mode. If a short circuit occurs, the push-pull converter shuts down for about 2 ms and then enters soft start mode. If, at the end of soft start, a short circuit still exists, the process is repeated, which is called hiccup mode. If the short circuit is cleared, the ADuM447x enters normal operation.

The ADuM447x also have a pulse-by-pulse current limit, which is active in startup and normal operation and protects the primary switches, X1 and X2, from exceeding approximately 1.2 A peak. This current limit also protects the transformer windings.

Data Channel Power Cycle

The ADuM447x data input channels on the primary side and the data input channels on the secondary side are protected from premature operation by UVLO circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive, and all input channel drivers and refresh circuits are idle. Outputs are held in a low state. This is to prevent transmission of undefined states during power-up and power-down operations.

During the application of power to V_{DDA}, the primary side circuitry is held idle until the UVLO preset voltage is reached. At that time, the data channels are initialized to their default low output state until they receive data pulses from the secondary side.

The primary side input channels sample the input and send a pulse to the inactive secondary output. The secondary side converter begins to accept power from the primary, and the V_{ISO} voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data, either a transition or a dc refresh pulse, is received from the corresponding primary side input. It can take up to 1 µs after the secondary side is initialized for the state of the output to correlate with the primary side input.

Secondary side inputs sample their state and transmit it to the primary side. Outputs are valid one propagation delay after the secondary side becomes active.

Because the rate of charge of the secondary side is dependent on the soft start cycle, loading conditions, input voltage, and output voltage level selected, take care in the design to allow the converter to stabilize before valid data is required.

When power is removed from V_{DDA}, the primary side converter and coupler shut down when the UVLO level is reached. The secondary side stops receiving power and starts to discharge. The outputs on the secondary side hold the last state that they received from the primary until either the UVLO level is reached and the outputs are placed in their default low state, or the outputs detect a lack of activity from the inputs and the outputs are set to their default value before the secondary power reaches UVLO.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices, Inc., conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM447x. Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 11 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages that are higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADuM447x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is dc, bipolar ac, or unipolar ac. Figure 56, Figure 57, and Figure 58 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage.

In the case of dc or unipolar ac voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 11 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the dc or unipolar ac voltage cases. Treat any cross-insulation voltage waveform that does not conform to Figure 57 or Figure 58 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 11.

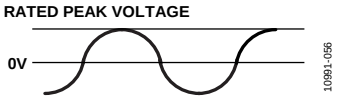

Figure 56. Bipolar AC Waveform

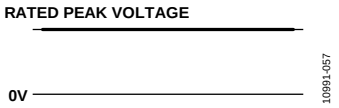

Figure 57. DC Waveform

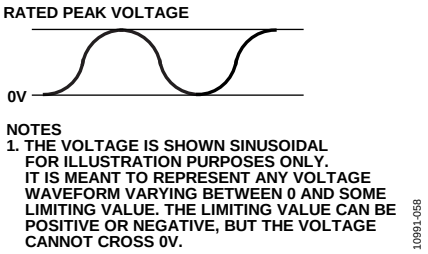

Figure 58. Unipolar AC Waveform

OUTLINE DIMENSIONS

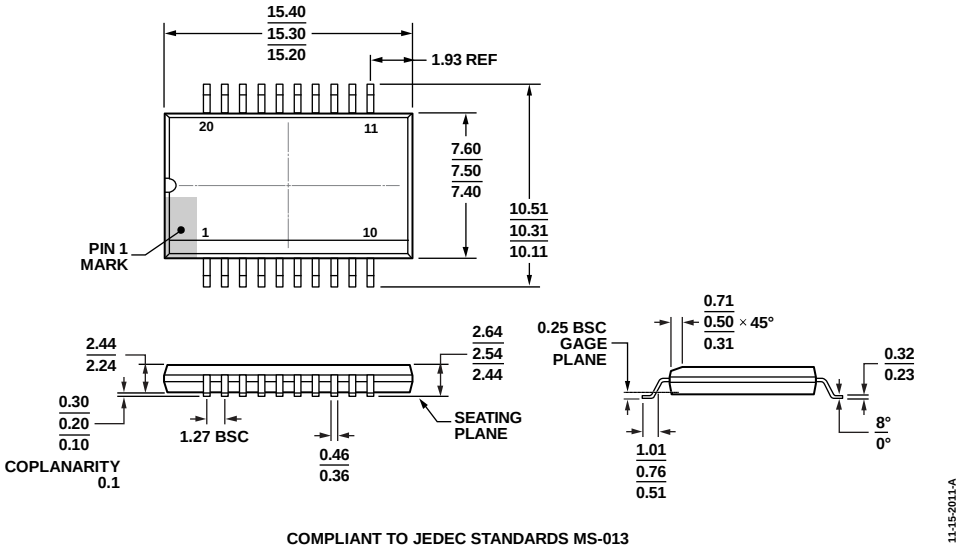

Figure 59. 20-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{ISO} Side	Maximum Data Rate (Mbps)	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuM4470ARIZ	4	0	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4470ARIZ-RL	4	0	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4470CRIZ	4	0	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4470CRIZ-RL	4	0	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4471ARIZ	3	1	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4471ARIZ-RL	3	1	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4471CRIZ	3	1	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4471CRIZ-RL	3	1	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4472ARIZ	2	2	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4472ARIZ-RL	2	2	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4472CRIZ	2	2	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4472CRIZ-RL	2	2	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4473ARIZ	1	3	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4473ARIZ-RL	1	3	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4473CRIZ	1	3	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4473CRIZ-RL	1	3	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4474ARIZ	0	4	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4474ARIZ-RL	0	4	1	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000
ADuM4474CRIZ	0	4	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body	RI-20-1	
ADuM4474CRIZ-RL	0	4	25	−40°C to +105°C	20-Lead SOIC_IC Wide Body 13″ Tape and Reel	RI-20-1	1,000

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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