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April 2012

FDB2552 F085

N-Channel PowerTrench® MOSFET 150V, 37A, 36m Ω

Features

- $r_{DS(ON)} = 32m\Omega$ (Typ.), $V_{GS} = 10V$, $I_D = 16A$
- $Q_{q}(tot) = 39nC (Typ.), V_{GS} = 10V$
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- RoHS Compliant



Applications

- DC/DC Converters and Off-line UPS
- · Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42V Automotive Load Control
- Electronic Valve Train Systems



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain to Source Voltage	150	V
V _{GS}	Gate to Source Voltage	±20	V
	Drain Current	27	^
	Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 10V$)	37	A
I _D	Continuous (T _C = 100°C, V _{GS} = 10V)	26	А
	Continuous ($T_{amb} = 25^{\circ}C$, $V_{GS} = 10V$) with $R_{\theta JA} = 43^{\circ}C/W$	5	А
	Pulsed	See Figure 4	А
E _{AS}	Single Pulse Avalanche Energy (Note 1)	390	mJ
	Power dissipation	150	W
P_{D}	Derate above 25°C	1.0	W/°C
T _J , T _{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220, TO-263	1.0	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220, TO-263 (Note 2)	62	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in ² copper pad area	43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB2552	FDB2552_F085	TO-263AB	330mm	24mm	800 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

Parameter	Test Co	onditions	Min	Тур	Max	Units
acteristics						
Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_C$	GS = 0V	150	-	-	V
Zero Gate Voltage Drain Current	V _{DS} = 120V		-	-	1	
	$V_{GS} = 0V$	$T_{\rm C} = 150^{\rm o}{\rm C}$	-	-	250	μΑ
Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA
	Drain to Source Breakdown Voltage Zero Gate Voltage Drain Current	acteristics Drain to Source Breakdown Voltage $I_D = 250\mu A$, V_C Zero Gate Voltage Drain Current $V_{DS} = 120V$ $V_{GS} = 0V$				acteristics Drain to Source Breakdown Voltage $I_D = 250\mu A, V_{GS} = 0V$ 150 Zero Gate Voltage Drain Current $V_{DS} = 120V$ 1 $V_{GS} = 0V$ $V_{CS} = 150^{\circ}C$ 250

On Characteristics

V _{GS(TH)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	-	4	V
•		$I_D = 16A, V_{GS} = 10V$	-	0.032	0.036	
r _{DS(ON)}	Drain to Source On Resistance	$I_D = 16A, V_{GS} = 10V,$ $T_J = 175^{\circ}C$	-	0.084	0.097	Ω

Dynamic Characteristics

C _{ISS}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	2800	-	pF
Coss	Output Capacitance			-	285	-	pF
C _{RSS}	Reverse Transfer Capacitance			-	55	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$			39	51	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 2V$	$V_{DD} = 75V$	-	5.2	6.8	nC
Q_{gs}	Gate to Source Gate Charge	ı	I _D = 16A	-	13.5	-	nC
$\begin{array}{c} Q_{gs} \\ Q_{gs2} \\ Q_{gd} \end{array}$	Gate Charge Threshold to Plateau	I	$I_g = 1.0 \text{mA}$	-	8.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	8.3	-	nC

Switching Characteristics $(V_{GS} = 10V)$

t _{ON}	Turn-On Time		-	-	62	ns
t _{d(ON)}	Turn-On Delay Time		-	12	-	ns
t _r	Rise Time	V _{DD} = 75V, I _D = 16A	-	29	-	ns
t _{d(OFF)}	Turn-Off Delay Time	$V_{GS} = 10V$, $R_{GS} = 8.2\Omega$	-	36	-	ns
t _f	Fall Time		-	29	-	ns
t _{OFF}	Turn-Off Time		-	-	97	ns

Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 16A	-	-	1.25	V
	Source to Drain Diode voltage	I _{SD} = 8A	-	-	1.0	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$	-	-	90	ns
Q _{RR}	Reverse Recovered Charge	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$	-	-	242	nC

- Notes: 1: Starting $T_J = 25^{\circ}C$, L = 7.8mH, $I_{AS} = 10A$. 2: Pulse Width = 100s

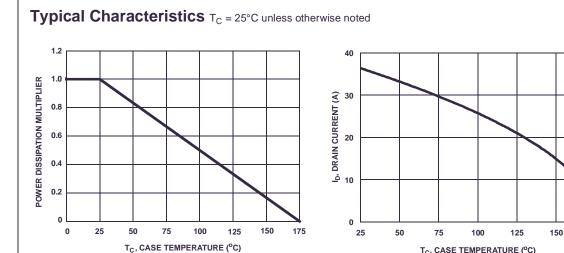


Figure 1. Normalized Power Dissipation vs **Ambient Temperature**

Figure 2. Maximum Continuous Drain Current vs **Case Temperature**

T_C, CASE TEMPERATURE (°C)

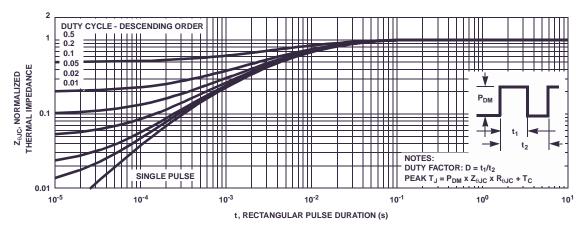


Figure 3. Normalized Maximum Transient Thermal Impedance

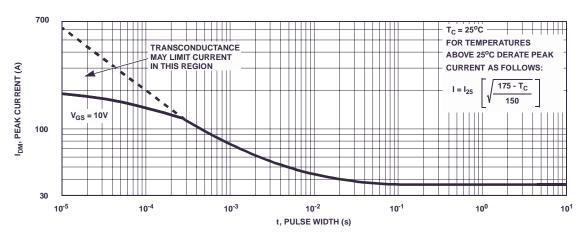
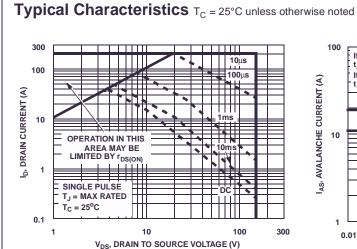


Figure 4. Peak Current Capability



If $R \neq 0$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $STARTING T_J = 25°C$ $STARTING T_J = 150°C$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$ $t_{AV} = (L/R) ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) + 1]$

 $t_{AV} = (L)(I_{AS})/(1.3*RATED BV_{DSS} - V_{DD})$

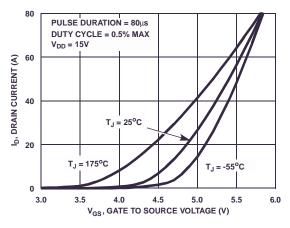
If R = 0

Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability



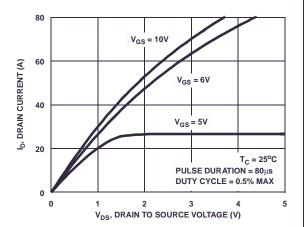
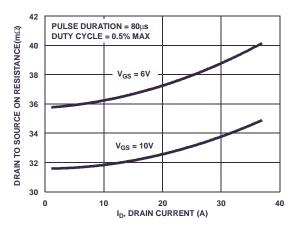


Figure 7. Transfer Characteristics

Figure 8. Saturation Characteristics



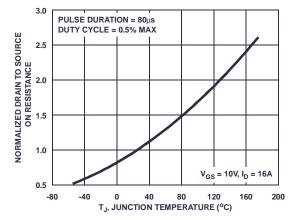


Figure 9. Drain to Source On Resistance vs Drain Current

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

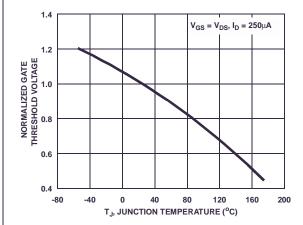


Figure 11. Normalized Gate Threshold Voltage vs
Junction Temperature

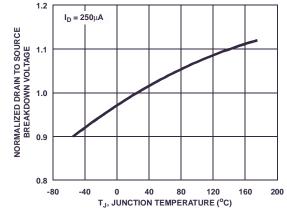


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

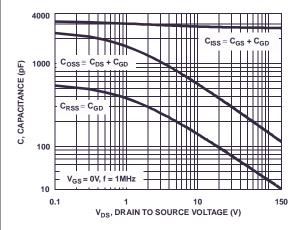


Figure 13. Capacitance vs Drain to Source Voltage

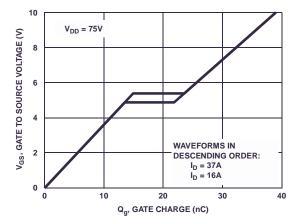


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

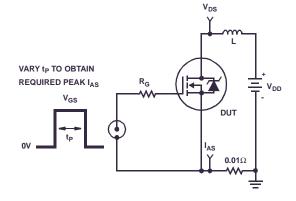


Figure 15. Unclamped Energy Test Circuit

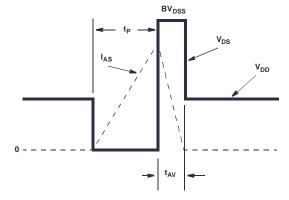


Figure 16. Unclamped Energy Waveforms

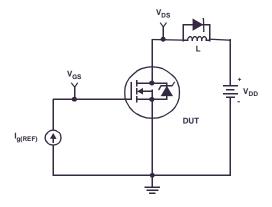


Figure 17. Gate Charge Test Circuit

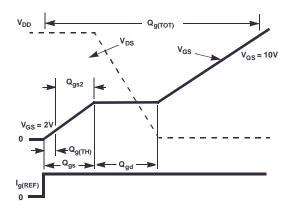


Figure 18. Gate Charge Waveforms

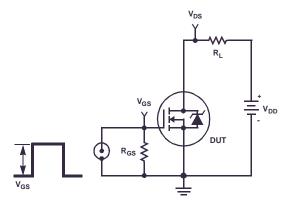


Figure 19. Switching Time Test Circuit

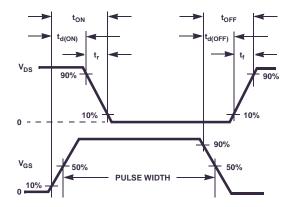


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

- Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
- 2. The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- 6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared

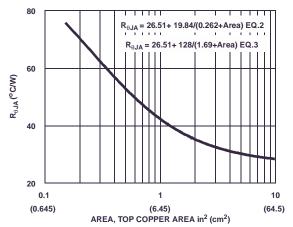
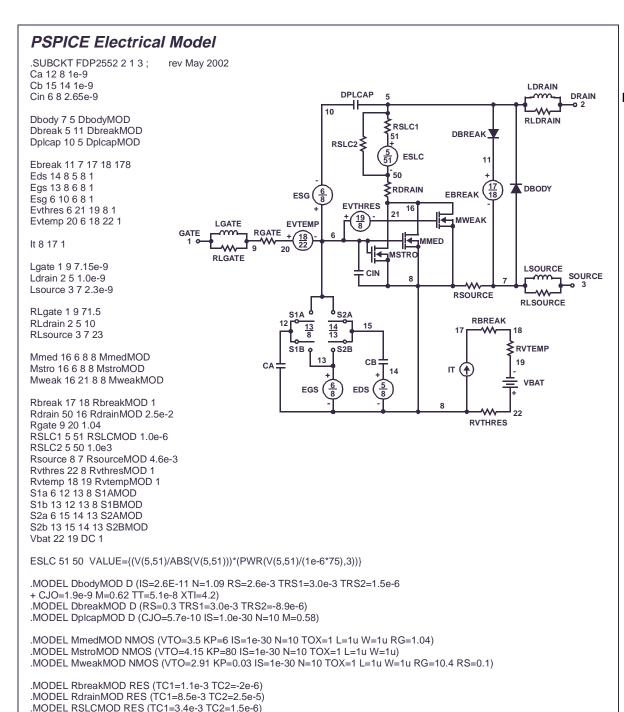


Figure 21. Thermal Resistance vs Mounting
Pad Area



.MODEL RvtempMOD RES (TC1=-4.1e-3 TC2=1.5e-6)

.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6) .MODEL RvthresMOD RES (TC1=-4.3e-3 TC2=-1.6e-5)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.0 VOFF=-4.0) .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.0 VOFF=-6.0)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2)

Note: For further discussion of the PSPICE model, consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model REV May 2002 template FDP2552 n2,n1,n3 electrical n2,n1,n3 var i iscl dp..model dbodymod = (isl=2.6e-11,nl=1.09,rs=2.6e-3,trs1=3.0e-3,trs2=1.5e-6,cjo=1.9e-9,m=0.62,tt=5.1e-8,xti=4.2) dp..model dbreakmod = (rs=0.3.trs1=3.0e-3.trs2=-8.9e-6)dp..model dplcapmod = (cjo=5.7e-10,isl=10.0e-30,nl=10,m=0.58) $m..model mmedmod = (type=_n,vto=3.5,kp=6,is=1e-30, tox=1)$ m..model mstrongmod = (type=_n,vto=4.15,kp=80,is=1e-30, tox=1) m..model mweakmod = (type= n, vto=2.91, kp=0.03, is=1e-30, tox=1, rs=0.1)I DRAIN sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-6.0,voff=-4.0) DPLCAP DRAIN sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-4.0,voff=-6.0) 10 sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5) RLDRAIN sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2) ≹RSLC1 c.ca n12 n8 = 1e-9c.cb n15 n14 = 1e-9 RSLC2 ≥ ISCL c.cin n6 n8 = 2.65e-9DBREAK 3 dp.dbody n7 n5 = model=dbodymod **≨**RDRAIN dp.dbreak n5 n11 = model=dbreakmod $ESG\left(\frac{6}{8}\right)$ DBODY dp.dplcap n10 n5 = model=dplcapmod **EVTHRES** 21 MWFAK LGATE **EVTEMP** spe.ebreak n11 n7 n17 n18 = 178 GATE **RGATE** 1822 FRREAK $^{\circ}$ spe.eds n14 n8 n5 n8 = 1 MMED I₉ ₩-20 spe.egs n13 n8 n6 n8 = 1 **€** MSTR RLGATE spe.esg n6 n10 n6 n8 = 1 CIN spe.evthres n6 n21 n19 n8 = 1 SOURCE spe.evtemp n20 n6 n18 n22 = 1 RSOURCE RLSOURCE i.it n8 n17 = 1RBREAK <u>14</u> 13 I.lgate n1 n9 = 7.15e-918 I.ldrain n2 n5 = 1.0e-9**₹**RVTEMP o S2B S₁B I.lsource n3 n7 = 2.3e-9СВ 19 IT 14 res.rlgate n1 n9 = 71.5 VRAT 5 8 res.rldrain n2 n5 = 10**FGS** FDS res.rlsource n3 n7 = 23 **RVTHRES** m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u res.rbreak n17 n18 = 1, tc1=1.1e-3,tc2=-2e-6 res.rdrain n50 n16 = 2.5e-2, tc1=8.5e-3,tc2=2.5e-5 res.rgate n9 n20 = 1.04 res.rslc1 n5 n51 = 1.0e-6, tc1=3.4e-3,tc2=1.5e-6 res.rslc2 n5 n50 = 1.0e3 res.rsource n8 n7 = 4.6e-3, tc1=4.0e-3,tc2=1.0e-6 res.rvthres n22 n8 = 1, tc1=-4.3e-3,tc2=-1.6e-5 res.rvtemp n18 n19 = 1, tc1=-4.1e-3,tc2=1.5e-6 sw vcsp.s1a n6 n12 n13 n8 = model=s1amod sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc=1 equations { i (n51->n50) +=iscl (v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/75))**3))

SPICE Thermal Model JUNCTION REV 23 May 2002 FDP2552T CTHERM1 TH 6 1e-2 CTHERM2 6 5 1.5e-2 CTHERM3 5 4 2e-2 RTHERM1 CTHERM1 CTHERM4 4 3 2.1e-2 CTHERM5 3 2 2.2e-2 CTHERM6 2 TL 9e-2 6 RTHERM1 TH 6 2.7e-2 RTHERM2 6 5 2.8e-2 RTHERM3 5 4 7.8e-2 RTHERM2 CTHERM2 RTHERM4 4 3 9e-2 RTHERM5 3 2 2.7e-1 RTHERM6 2 TL 2.87e-1 5 SABER Thermal Model SABER thermal model FDP2552T RTHERM3 CTHERM3 template thermal_model th tl thermal_c th, tl ctherm.ctherm1 th 6 =1e-2 ctherm.ctherm2 6 5 =1.5e-2 ctherm.ctherm3 5 4 =2e-2 ctherm.ctherm4 4 3 =2.1e-2 ctherm.ctherm5 3 2 =2.2e-2 RTHERM4 CTHERM4 ctherm.ctherm6 2 tl =9e-2 rtherm.rtherm1 th 6 = 2.7e-2 3 rtherm.rtherm2 6 5 = 2.8e-2 rtherm.rtherm3 5 4 =7.8e-2 rtherm.rtherm4 4 3 =9e-2 CTHERM5 RTHFRM5 rtherm.rtherm5 3 2 =2.7e-1 rtherm.rtherm6 2 tl =2.87e-1 2 RTHERM6 CTHERM6 CASE tl





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