

32-bit XLP Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog

Operating Conditions

- 2.5V to 3.6V, -40°C to +85°C, DC to 72 MHz
- 2.5V to 3.6V, -40°C to +105°C, DC to 72 MHz

Core: 72 MHz/116 DMIPS MIPS32® M4K®

- MIPS16e[®] mode for up to 40% smaller code size
- Code-efficient (C and Assembly) architecture
- Single-cycle (MAC) 32x16 and two-cycle 32x32 multiply

Clock Management

- · 0.9% internal oscillator
- · Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- · Independent Watchdog Timer
- Fast wake-up and start-up

Power Management

- Various power management options for extreme power reduction (VBAT, Deep Sleep, Sleep, and Idle)
- Deep Sleep current: 673 nA (typical)
- · Integrated POR and BOR
- Programmable High/Low-Voltage Detect (HLVD) on VDD

Audio Interface Features

- Data communication: I²S, LJ, RJ, and DSP modes
- Control interface: SPI and I²C
- Master clock:
 - Generation of fractional clock frequencies
 - Can be synchronized with USB clock
 - Can be tuned in run-time

Advanced Analog Features

- · ADC Module:
 - 10-bit 1.1 Msps rate with one S&H
 - Up to 10 analog inputs on 28-pin devices and 13 analog inputs on 44-pin devices
- Flexible and independent ADC trigger sources
- Charge Time Measurement Unit (CTMU):
 - Supports mTouch™ capacitive touch sensing
 - Provides high-resolution time measurement (1 ns)
 - On-chip temperature measurement capability
- Comparators:
 - Up to three Analog Comparator modules
 - Programmable references with 32 voltage points

Timers/Output Compare/Input Capture

- Five General Purpose Timers:
 - Five 16-bit and up to two 32-bit Timers/Counters
- · Five Output Compare (OC) modules
- · Five Input Capture (IC) modules
- · Peripheral Pin Select (PPS) to allow function remap
- Real-Time Clock and Calendar (RTCC) module

Communication Interfaces

- USB 2.0-compliant Full-speed OTG controller
- Two UART modules (17.5 Mbps):
 - Supports LIN 2.0 protocols and IrDA® support
- Two 4-wire SPI modules (25 Mbps)
- Two I²C modules (up to 1 Mbaud) with SMBus support
- · PPS to allow function remap
- Parallel Master Port (PMP)

Direct Memory Access (DMA)

- Four channels of hardware DMA with automatic data size detection
- · Two additional channels dedicated for USB
- Programmable Cyclic Redundancy Check (CRC)

Input/Output

- 10 mA source/sink on all I/O pins and up to 14 mA on nonstandard VOH
- 5V-tolerant pins
- · Selectable open drain, pull-ups, and pull-downs
- · External interrupts on all I/O pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 2 -40°C to +105°C) (planned)
- Class B Safety Library, IEC 60730 (planned)

Debugger Development Support

- · In-circuit and in-application programming
- 4-wire MIPS[®] Enhanced JTAG interface
- · Unlimited program and six complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan

Integrated Software Libraries and Tools

- C/C++ compiler with native DSP/fractional support
- MPLAB[®] Harmony Integrated Software Framework
- USB stack

Packages

Туре	SOIC	QI	TQFP	
Pin Count	28	28	44	44
I/O Pins (up to)	21	21	34	34
Contact/Lead Pitch	1.27	0.65	0.65	0.80
Dimensions	17 90x10 30x2 65	6x6x0.9	8x8x0 9	10x10x1 0

Note: All dimensions are in millimeters (mm) unless specified.

TABLE 1: PIC32MX1XX 28/44-PIN XLP (GENERAL PURPOSE) FAMILY FEATURES

					_	_		Remappable Peripherals						©		els)															
Device	Pins	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Pins	Timers ⁽²⁾ /Capture/ Compare/PWM	UART	SPIN ² S	External Interrupts ⁽³⁾	Analog Comparators	I ² Стм	dWd	DMA Channels (Programmable/Dedicated)	СТМО	10-bit 1 Msps ADC (Channels)	RTCC	suid O/I	JTAG	VBAT	Packages												
PIC32MX154F128B	28			20										10		21		N	SOIC, QFN												
PIC32MX154F128D	44	400.40	20	30	F /F /F /F			5	3		Y	4/2	V	13	Υ	35	Υ	Ν	TQFP, QFN												
PIC32MX155F128B	28	128+12	128+12	128+12	120+12	120+12	120+12	120+12	120+12	120+12	120+12	120+12	120+12	120+12	32	19	5/5/5/5	2	2	3	3	2	'	4/2	Y	9	Y	20		Υ	SOIC, QFN
PIC32MX155F128D	44			29										12		35		Υ	TQFP, QFN												
PIC32MX174F256B	28			20										10		21		N	SOIC, QFN												
PIC32MX174F256D	44	256.12	64	30	E/E/E/E	2	2	5	3	2	Υ	4/2	Y	13	Υ	35	Υ	N	TQFP, QFN												
PIC32MX175F256B	28	256+12	64	19	5/5/5/5			5	3		ľ	4/2	r	9	Y	20	1	Υ	SOIC, QFN												
PIC32MX175F256D	44			29										12		35		Υ	TQFP, QFN												

Note 1: This device features 12 KB of Boot Flash memory.

2: Four out of five timers are remappable.

3: Four out of five external interrupts are remappable.

TABLE 2: PIC32MX2XX 28/44-PIN XLP (USB) FAMILY FEATURES

				_		•	1)	()	_	_	=	<u>-</u>		Re	mappabl	e Per	ipher	als					©		els)					
Device	Pins	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Pins	Timers ⁽²⁾ /Capture/ Compare/PWM	UART	SPI/I ² S	External Interrupts ⁽³⁾	Analog Comparators	USB On-The-Go (OTG)	I ² Стм	PMP	DMA Channels (Programmable/Dedicated)	СТМО	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	VBAT	Packages										
PIC32MX254F128B	28			17											9		17		N	SOIC, QFN										
PIC32MX254F128D	44	400 40		29	- /- /- /-	2		_		.,		Y	4/0		13	.,	35	,,	Ν	TQFP, QFN										
PIC32MX255F128B	28	128+12	128+12 32	32	16	5/5/5/5	2	2	5	3	Y	2	Y	4/2	Υ	8	Y	16	Υ	Υ	SOIC, QFN									
PIC32MX255F128D	44			28											12		35	•	Υ	TQFP, QFN										
PIC32MX274F256B	28			17											9		17		N	SOIC, QFN										
PIC32MX274F256D	44	050.40	0.4	29	E/E/E			_		V	0	, , , , , , , , , , , , , , , , , , ,	4/0	\ \ \	13	V	35	,	Ν	TQFP, QFN										
PIC32MX275F256B	28	256+12	64	16	5/5/5	2	2	5	3	Y	(2	Y	4/2	Y	8	Υ	16	Y	Υ	SOIC, QFN										
PIC32MX275F256D	44			28											12		35		Υ	TQFP, QFN										

Note 1: This device features 12 KB of Boot Flash memory.

2: Four out of five timers are remappable.

3: Four out of five external interrupts are remappable.

Pin Diagrams

TABLE 3: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITH VBAT

28-PIN SOIC (TOP VIEW)^(1,2,3) PIC32MX155F128B PIC32MX175F256B

Pin#	Full Pin Name							
1	MCLR							
2	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA1/RA0							
3	VREF-/AN1/RPA1/ASCL1/CTED2/PMRD/RA1							
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0							
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12//RB1							
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2							
7	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/RB3							
8	Vss							
9	OSC1/CLKI/RPA2/RA2							
10	OSC2/CLKO/RPA3/PMA0/RA3							
11	SOSCI/RPB4/RB4 ⁽⁴⁾							
12	SOSCO/RPA4/T1CK/CTED9/RA4							
13	VDD							
14	PGED3/RPB5/ASDA2/PMD7/RB5							

Pin#	Full Pin Name
15	PGEC3/RPB6/ASCL2/PMD6/RB6
16	TDI/RPB7/CTED3/PMD5/INT0/RB7
17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
19	Vss
20	VCAP
21	PGED1/RPB10/CTED11/PMD2/RB10
22	PGEC1/TMS/RPB11/PMD1/RB11
23	AN12/PMD0/RB12
24	VBAT
25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
27	AVss
28	AVDD

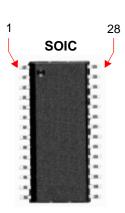
Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.

- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: Shaded pins are 5V tolerant.
- 4: This is an input-only pin.

TABLE 4: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITHOUT VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX154F128B PIC32MX174F256B



Pin#	Full Pin Name
1	MCLR
2	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA1/RA0
3	VREF-/AN1/RPA1/ASCL1/CTED2/RA1
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12//RB1
6	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
7	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
8	Vss
9	OSC1/CLKI/RPA2/RA2
10	OSC2/CLKO/RPA3/PMA0/RA3
11	SOSCI/RPB4/RB4 ⁽⁴⁾
12	SOSCO/RPA4/T1CK/CTED9/RA4
13	VDD
14	PGED3/RPB5/ASDA2/PMD7/RB5

Pin#	Full Pin Name
15	PGEC3/RPB6/ASCL2/PMD6/RB6
16	TDI/RPB7/CTED3/PMD5/INT0/RB7
17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
19	Vss
20	VCAP
21	PGED1/RPB10/CTED11/PMD2/RB10
22	PGEC1/TMS/RPB11/PMD1/RB11
23	AN12/PMD0/RB12
24	AN11/RPB13/CTPLS/PMRD/RB13
25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
27	AVss
28	AVDD

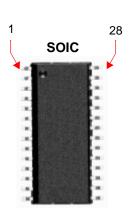
Note

- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.
- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: Shaded pins are 5V tolerant.
- 4: This is an input-only pin.

TABLE 5: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX255F128B PIC32MX275F256B



	T
Pin#	Full Pin Name
1	MCLR
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3
8	Vss
9	OSC1/CLKI/RPA2/RA2
10	OSC2/CLKO/RPA3/PMA0/RA3
11	SOSCI/RPB4/CTED11/RB4 ⁽⁴⁾
12	SOSCO/RPA4/T1CK/CTED9/RA4
13	VDD
14	TMS/RPB5/USBID/PMRD/RB5

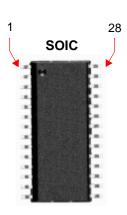
Pin #	Full Pin Name
15	VBUS
16	TDI/RPB7/CTED3/PMD5/INT0/RB7
17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
19	Vss
20	VCAP
21	D+
22	D-
23	Vusb3v3
24	VBAT
25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
27	AVss
28	AVDD

- Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.
 - Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
 - Shaded pins are 5V tolerant. 3:
 - This is an input-only pin.

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES WITHOUT VBAT

28-PIN SOIC (TOP VIEW)(1,2,3)

PIC32MX254F128B PIC32MX274F256B



Pin#	Full Pin Name
1	MCLR
2	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0
3	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1
4	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
5	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1//RB1
6	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
7	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
8	Vss
9	OSC1/CLKI/RPA2/RA2
10	OSC2/CLKO/RPA3/PMA0/RA3
11	SOSCI/RPB4/CTED11/RB4 ⁽⁴⁾
12	SOSCO/RPA4/T1CK/CTED9/RA4
13	VDD
14	TMS/RPB5/USBID/RB5

Pin#	Full Pin Name
15	VBUS
16	TDI/RPB7/CTED3/PMD5/INT0/RB7
17	TCK/RPB8/SCL1/CTED10/PMD4/RB8
18	TDO/RPB9/SDA1/CTED4/PMD3/RB9
19	Vss
20	VCAP
21	D+
22	D-
23	VUSB3V3
24	AN11/RPB13/CTPLS/PMRD/RB13
25	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
26	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
27	AVss
28	AVDD

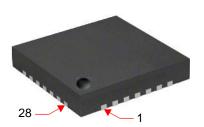
Note

- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions
- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: Shaded pins are 5V tolerant.
- 4: This is an input-only pin.

TABLE 7: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITH VBAT

28-PIN QFN (TOP VIEW)(1,2,3.4)

PIC32MX155F128D PIC32MX175F256D



Pin#	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/RB3
5	Vss
6	OSC1/CLKI/RPA2/RA2
7	OSC2/CLKO/RPA3/PMA0/RA3
8	SOSCI/RPB4/RB4 ⁽⁵⁾
9	SOSCO/RPA4/T1CK/CTED9/RA4
10	VDD
11	PGED3/RPB5/ASDA2/PMD7/RB5
12	PGEC3/RPB6/ASCL2/PMD6/RB6
13	TDI/RPB7/CTED3/PMD5/INT0/RB7
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8

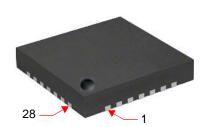
Pin#	Full Pin Name
15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
16	Vss
17	VCAP
18	PGED1/RPB10/CTED11/PMD2/RB10
19	PGEC1/TMS/RPB11/PMD1/RB11
20	AN12/PMD0/RB12
21	VBAT
22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
24	AVss
25	AVDD
26	MCLR
27	VREF+/AN0/C3INC/RPA0ASDA1//CTED1/PMA1/RA0
28	VREF-/AN1/RPA1/ASCL1/CTED2/PMRD/RA1

- Note
- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions
- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.
- 5: This is an input-only pin.

TABLE 8: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES WITHOUT VBAT

28-PIN QFN (TOP VIEW)(1,2,3.4)

PIC32MX154F128B PIC32MX174F256B



Pin#	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
5	Vss
6	OSC1/CLKI/RPA2/RA2
7	OSC2/CLKO/RPA3/PMA0/RA3
8	SOSCI/RPB4/RB4 ⁽⁵⁾
9	SOSCO/RPA4/T1CK/CTED9/RA4
10	VDD
11	PGED3/RPB5/ASDA2/PMD7/RB5
12	PGEC3/RPB6/ASCL2/PMD6/RB6
13	TDI/RPB7/CTED3/PMD5/INT0/RB7
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8

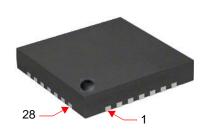
Pin#	Full Pin Name
15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
16	Vss
17	VCAP
18	PGED1/RPB10/CTED11/PMD2/RB10
19	PGEC1/TMS/RPB11/PMD1/RB11
20	AN12/PMD0/RB12
21	AN11/RPB13/CTPLS/PMRD/RB13
22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
24	AVss
25	AVDD
26	MCLR
27	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA1/RA0
28	VREF-/AN1/RPA1/ASCL1/CTED2/RA1

- Note
- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.
- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.
- 5: This is an input-only pin.

TABLE 9: PIN NAMES FOR 28-PIN USB DEVICES WITH VBAT

28-PIN QFN (TOP VIEW)(1,2,3,4)

PIC32MX255F128B PIC32MX275F256B



Pin#	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1/RB1
3	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
4	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMWR/RB3
5	Vss
6	OSC1/CLKI/RPA2/RA2
7	OSC2/CLKO/RPA3/PMA0/RA3
8	SOSCI [/] RPB4/CTED11/RB4 ⁽⁵⁾
9	SOSCO/RPA4/T1CK/CTED9/RA4
10	VDD
11	TMS/RPB5/USBID/PMRD/RB5
12	VBUS
13	TDI/RPB7/CTED3/PMD5/INT0/RB7
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8

Pin#	Full Pin Name
15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
16	Vss
17	VCAP
18	D+
19	D-
20	VUSB3V3
21	VBAT
22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
24	AVss
25	AVDD
26	MCLR
27	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0
28	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1

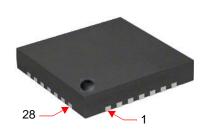
Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.

- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.
- 5: This is an input-only pin.

PIN NAMES FOR 28-PIN USB DEVICES WITHOUT VBAT **TABLE 10:**

28-PIN QFN (TOP VIEW)(1,2,3,4)

PIC32MX254F128B PIC32MX274F256B



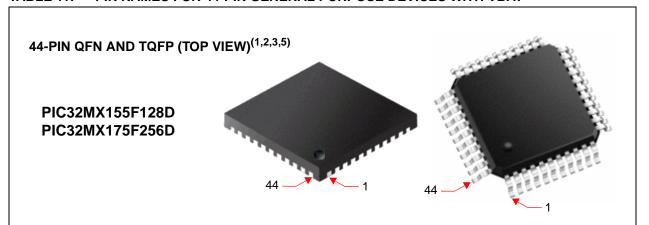
Pin#	Full Pin Name
1	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
2	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMD1/RB1
3	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
4	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
5	Vss
6	OSC1/CLKI/RPA2/RA2
7	OSC2/CLKO/RPA3/PMA0/RA3
8	SOSCI/RPB4/CTED11/RB4 ⁽⁵⁾
9	SOSCO/RPA4/T1CK/CTED9/RA4
10	VDD
11	TMS/RPB5/USBID/RB5
12	VBUS
13	TDI/RPB7/CTED3/PMD5/INT0/RB7
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8

Pin#	Full Pin Name
15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
16	Vss
17	VCAP
18	D+
19	D-
20	VUSB3V3
21	AN11/RPB13/CTPLS/PMRD/RB13
22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMA1/RB14
23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
24	AVss
25	AVDD
26	MCLR
27	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMD7/RA0
28	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMD6/RA1

Note

- The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.
- Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information. 2:
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Shaded pins are 5V tolerant. 4:
- This is an input-only pin.

TABLE 11: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES WITH VBAT



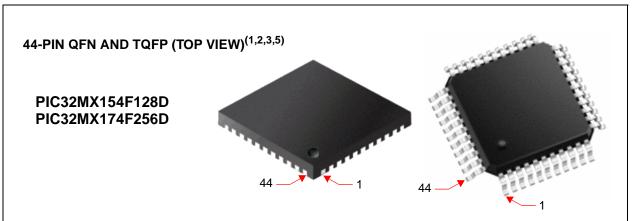
Pin#	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9
2	RPC6/PMA1/RC6
3	RPC7/PMCS1/RC7
4	RPC8/PMD5/RC8
5	RPC9/CTED7/PMD6/RC9
6	Vss
7	VCAP
8	PGED1/RPB10/CTED11/PMA8/RB10
9	PGEC1/TMS/RPB11/PMA9/RB11
10	AN12/PMD0/RB12
11	VBAT
12	PGED4/PMA10/RA10
13	PGEC4/TCK/CTED8/PMD3/RA7
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15
16	AVss
17	AVDD
18	MCLR
19	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/RA0
20	VREF-/AN1/RPA1/ASCL1/CTED2/RA1
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1

Pin#	Full Pin Name
23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMA2/RB3
25	AN6/RPC0/RC0
26	AN7/RPC1/RC1
27	AN8/RPC2/PMWR/RC2
28	Vad
29	Vss
30	OSC1/CLKI/RPA2/RA2
31	OSC2/CLKO/RPA3/RA3
32	TDO/RPA8/PMD2/RA8
33	SOSCI/RPB4/RB4
34	SOSCO/RPA4/T1CK/CTED9/RA4
35	TDI/RPA9/PMD1/RA9
36	RPC3/PMRD/RC3
37	RPC4/PMD4/RC4
38	RPC5/PMD7/RC5
39	Vss
40	Vod
41	PGED3/RPB5/ASDA2/PMA3/RB5
42	PGEC3/RPB6/ASCL2/PMA6/RB6
43	RPB7/CTED3/PMA5/INT0/RB7
44	RPB8/SCL1/CTED10/PMA4/RB8

Note

- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.
- Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.

TABLE 12: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES WITHOUT VBAT



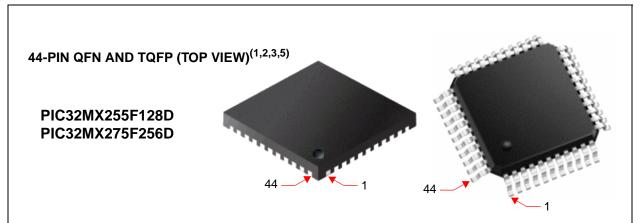
Pin#	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9
2	RPC6/PMA1/RC6
3	RPC7/PMCS1/RC7
4	RPC8/PMD5/RC8
5	RPC9/CTED7/PMD6/RC9
6	Vss
7	VCAP
8	PGED1/RPB10/CTED11/PMA8/RB10
9	PGEC1/TMS/RPB11/PMA9/RB11
10	AN12/PMD0/RB12
11	AN11/RPB13/CTPLS/PMRD/RB13
12	PGED4/PMA10/RA10
13	PGEC4/TCK/CTED8/PMD3/RA7
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15
16	AVss
17	AVDD
18	MCLR
19	VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/RA0
20	VREF-/AN1/RPA1/ASCL1/CTED2/RA1
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/RB0
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/RB1

	Pin#	Full Pin Name
	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMA2/RB3
	25	AN6/RPC0/RC0
	26	AN7/RPC1/RC1
	27	AN8/RPC2/PMWR/RC2
	28	VDD
	29	Vss
	30	OSC1/CLKI/RPA2/RA2
	31	OSC2/CLKO/RPA3/RA3
Ī	32	TDO/RPA8/PMD2/RA8
	33	SOSCI/RPB4/CTED11/RB4
	34	SOSCO/RPA4/T1CK/RA4
	35	TDI/RPA9/PMD1/RA9
	36	RPC3/RC3
	37	RPC4/PMD4/RC4
	38	RPC5/PMD7/RC5
	39	Vss
	40	VDD
	41	PGED3/RPB5/ASDA2/PMA3/RB5
	42	PGEC3/RPB6/ASCL2/PMA6/RB6
	43	RPB7/CTED3/PMA5/INT0/RB7
ſ	44	RPB8/SCL1/CTED10/PMA4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions.

- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.

TABLE 13: PIN NAMES FOR 44-PIN USB DEVICES WITH VBAT



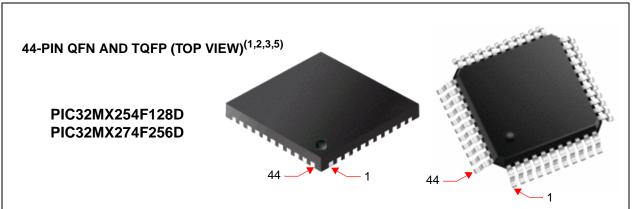
Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9
2	RPC6/PMA1/RC6
3	RPC7/PMCS1/RC7
4	RPC8/PMD5/RC8
5	RPC9/CTED7/PMD6/RC9
6	Vss
7	VCAP
8	D+
9	D-
10	Vusb3v3
11	VBAT
12	PGED4/PMD0/RA10
13	PGEC4/TCK/CTED8/PMD3/RA7
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15
16	AVss
17	AVDD
18	MCLR
19	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA3/RA0
20	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMA6/RA1
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMA10/RB0
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMA9/RB

Pin#	Full Pin Name							
23	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMA8/RB2							
24	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/CTPLS/PMA2 B3							
25	AN6/RPC0/RC0							
26	AN7/RPC1/RC1							
27	AN8/RPC2/PMWR/RC2							
28	VDD							
29	Vss							
30	OSC1/CLKI/RPA2/RA2							
31	OSC2/CLKO/RPA3/RA3							
32	TDO/RPA8/PMD2/RA8							
33	SOSCI/RPB4/CTED11/RB4							
34	SOSCO/RPA4/T1CK/CTED9/RA4							
35	TDI/RPA9/PMD1/RA9							
36	AN12/RPC3/PMRD/RC3							
37	RPC4/PMD4/RC4							
38	RPC5/PMD7/RC5							
39	Vss							
40	VDD							
41	TMS/RPB5/USBID/RB5							
42	VBUS							
43	RPB7/CTED3/PMA5/INT0/RB7							
44	RPB8/SCL1/CTED10/PMA4/RB8							

Note

- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions
- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.

TABLE 14: PIN NAMES FOR 44-PIN USB DEVICES WITHOUT VBAT



Pin#	Full Pin Name
1	RPB9/SDA1/CTED4/PMA7/RB9
2	RPC6/PMA1/RC6
3	RPC7/PMCS1/RC7
4	RPC8/PMD5/RC8
5	RPC9/CTED7/PMD6/RC9
6	Vss
7	VCAP
8	D+
9	D-
10	VUSB3V3
11	AN11/RPB13/CTPLS/PMRD/RB13
12	PGED4/PMD0/RA10
13	PGEC4/TCK/CTED8/PMD3/RA7
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/RB14
15	AN9/C3INA/RPB15/SCK2/CTED6/PMA0/RB15
16	AVss
17	AVDD
18	MCLR
19	PGED3/VREF+/AN0/C3INC/RPA0/ASDA1/CTED1/PMA3/RA0
20	PGEC3/VREF-/AN1/RPA1/ASCL1/CTED2/PMA6/RA1
21	PGED2/AN2/C1IND/C2INB/C3IND/RPB0/PMA10/RB0
22	PGEC2/AN3/C1INC/C2INA/LVDIN/RPB1/CTED12/PMA9/RB1

Pin#	Full Pin Name
23	PGED1/AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMA8/RB2
24	PGEC1/AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMA2/RB3
25	AN6/RPC0/RC0
26	AN7/RPC1/RC1
27	AN8/RPC2/PMWR/RC2
28	VDD
29	Vss
30	OSC1/CLKI/RPA2/RA2
31	OSC2/CLKO/RPA3/RA3
32	TDO/RPA8/PMD2/RA8
33	SOSCI/RPB4/CTED11/RB4
34	SOSCO/RPA4/T1CK/RA4
35	TDI/RPA9/PMD1/RA9
36	AN12/RPC3/RC3
37	RPC4/PMD4/RC4
38	RPC5/PMD7/RC5
39	Vss
40	VDD
41	TMS/RPB5/USBID/RB5
42	VBUS
43	RPB7/CTED3/PMA5/INT0/RB7
44	RPB8/SCL1/CTED10/PMA4/RB8

Note

- 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and 12.3 "Peripheral Pin Select" for restrictions
- 2: Every I/O port pin (RAx-RBx) can be used as a change notification pin (CNAx-CNBx). See 12.0 "I/O Ports" for more information.
- 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: Shaded pins are 5V tolerant.

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Referenced Sources

This device data sheet is based on the following individual chapters of the "PIC32 Family Reference Manual". These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32

website: http://www.microchip.com/pic32

- Section 1. "Introduction" (DS60001127)
- Section 2. "CPU" (DS60001113)
- Section 3. "Memory Organization" (DS60001115)
- Section 4. "Prefetch Cache" (DS60001119)
- Section 5. "Flash Program Memory" (DS60001121)
- Section 6. "Oscillator Configuration" (DS60001112)
- Section 7. "Resets" (DS60001118)
- Section 8. "Interrupt Controller" (DS60001108)
- Section 9. "Watchdog Timer and Power-up Timer" (DS60001114)
- Section 10. "Power-Saving Features" (DS60001130)
- Section 12. "I/O Ports" (DS60001120)
- Section 13. "Parallel Master Port (PMP)" (DS60001128)
- Section 14. "Timers" (DS60001105)
- Section 15. "Input Capture" (DS60001122)
- Section 16. "Output Compare" (DS60001111)
- Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104)
- Section 19. "Comparator" (DS60001110)
- Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109)
- Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107)
- Section 23. "Serial Peripheral Interface (SPI)" (DS60001106)
- Section 24. "Inter-Integrated Circuit (I²C)" (DS60001116)
- Section 27. "USB On-The-Go (OTG)" (DS60001126)
- Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125)
- Section 31. "Direct Memory Access (DMA) Controller" (DS60001117)
- Section 32. "Configuration" (DS60001124)
- Section 33. "Programming and Diagnostics" (DS60001129)
- Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167)
- Section 38. "High/Low Voltage Detect (HLVD)" (DS number pending)

NOTES:

1.0 DEVICE OVERVIEW

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX1XX/2XX 28/44-pin XLP Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/44-pin XLP Family of devices.

Table 1-1 through Table 1-16 list the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM

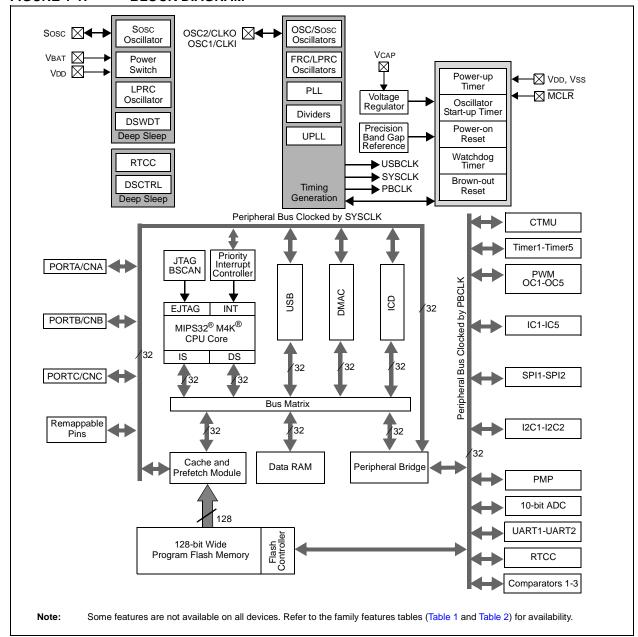


TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

	Pin Number ⁽¹⁾										
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description					
	Analog-to-Digital Converter										
AN0	27	2	19	I	Analog	Analog input channels.					
AN1	28	3	20	I	Analog						
AN2	1	4	21	I	Analog						
AN3	2	5	22	I	Analog						
AN4	3	6	23	I	Analog						
AN5	4	7	24	I	Analog						
AN6	_	_	25	I	Analog						
AN7	_	_	26	I	Analog						
AN8	_	_	27	I	Analog						
AN9	23	26	15	I	Analog						
AN10	22	25	14	I	Analog						
AN11 ⁽³⁾	21	24	11	I	Analog						
AN12	20 ⁽²⁾	23 ⁽²⁾	10	I	Analog]					

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

TTL = TTL input buffer

Analog = Analog input O = Output

P = PowerI = Input

PPS = Peripheral Pin Select

--=N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for General Purpose devices only.

3: This pin is not available on VBAT devices.

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

	Pin Number ⁽¹⁾				ı	
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description
					Oscillators	
CLKI	6	9	30	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	7	10	31	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	6	9	30	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	7	10	31	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	8	11	33	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	9	12	34	0	_	32.768 kHz low-power oscillator crystal output.
REFCLKI	PPS	PPS	PPS	I	ST	Reference Input Clock
REFCLKO	PPS	PPS	PPS	0	_	Reference Output Clock

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer O = Output PPS = Peripheral Pin Select

Analog = Analog input

P = Power I = Input — = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

TABLE 1-3: IC1 THROUGH IC5 PINOUT I/O DESCRIPTIONS

	Pi	n Number ⁽	(1)			
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description
				In	put Captui	re
IC1	PPS	PPS	PPS	I	ST	Input Capture Input 1-5
IC2	PPS	PPS	PPS	I	ST	
IC3	PPS	PPS	PPS	I	ST	
IC4	PPS	PPS	PPS	I	ST	
IC5	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

Analog = Analog input

P = Power

TTL = TTL input buffer

O = Output PPS = Peripheral Pin Select I = Input — = N/A

TABLE 1-4: OC1 THROUGH OC5 PINOUT I/O DESCRIPTIONS

	Pi	n Number ⁽	(1)		Buffer Type	Description
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type		
				Ou	tput Comp	are
OC1	PPS	PPS	PPS	0	_	Output Compare Output 1-5
OC2	PPS	PPS	PPS	0	_	
OC3	PPS	PPS	PPS	0	_	
OC4	PPS	PPS	PPS	0	_	
OC5	PPS	PPS	PPS	0	_	
OCFA	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

TTL = TTL input buffer

Analog = Analog input

P = Power

O = Output

I = InputPPS = Peripheral Pin Select --=N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS TABLE 1-5:

	Pi	in Number ⁽	(1)			Description
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type		
				Exte	rnal Interr	upts
INT0	13	16	43	I	ST	External Interrupt 0-4
INT1	PPS	PPS	PPS	I	ST	
INT2	PPS	PPS	PPS	I	ST	
INT3	PPS	PPS	PPS	I	ST	
INT4	PPS	PPS	PPS	I	ST	

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

TTL = TTL input buffer

Analog = Analog input

P = Power

O = Output

PPS = Peripheral Pin Select

I = Input--=N/A

TABLE 1-6: PORTA THROUGH PORTC PINOUT I/O DESCRIPTIONS

	Pi	in Number	(1)			
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description
					PORT A	
RA0	27	2	19	I/O	ST	PORTA is a bidirectional I/O port
RA1	28	3	20	I/O	ST	
RA2	6	9	30	I/O	ST	
RA3	7	10	31	I/O	ST	
RA4	9	12	34	I/O	ST	
RA7	_	_	13	I/O	ST	
RA8	_	_	32	I/O	ST	
RA9	_	_	35	I/O	ST	
RA10	_	_	12	I/O	ST	
					PORTB	
RB0	1	4	21	I/O	ST	PORTB is a bidirectional I/O port
RB1	2	5	22	I/O	ST	
RB2	3	6	23	I/O	ST	
RB3	4	7	24	I/O	ST	
RB4	8	11	33	I/O	ST	
RB5	11	14	41	I/O	ST	
RB6	12 ⁽²⁾	15 ⁽²⁾	42 ⁽⁴⁾	I/O	ST	
RB7	13	16	43	I/O	ST	
RB8	14	17	44	I/O	ST	
RB9	15	18	1	I/O	ST	
RB10	18 ⁽⁴⁾	21 ⁽⁴⁾	8(4)	I/O	ST	
RB11	19 ⁽⁴⁾	22 ⁽⁴⁾	9(4)	I/O	ST	
RB12	20 ⁽⁴⁾	23 ⁽⁴⁾	10 ⁽⁴⁾	I/O	ST	
RB13	21 ⁽³⁾	24(3)	11 ⁽³⁾	I/O	ST	
RB14	22	25	14	I/O	ST	
RB15	23	26	15	I/O	ST	

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

TTL = TTL input buffer

Analog = Analog input

P = Power

O = Output

PPS = Peripheral Pin Select

I = Input— = N/A

- 2: Pin number for General Purpose devices only.
- 3: This pin is not available for devices with VBAT.
- 4: This pin is not available for devices with USB.

TABLE 1-6: PORTA THROUGH PORTC PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pi	n Number ⁽	1)			
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description
RC0	_	_	25	I/O	ST	PORTC is a bidirectional I/O port
RC1	_	_	26	I/O	ST	
RC2	_	_	27	I/O	ST	
RC3	_	_	36	I/O	ST	
RC4	_	-	37	I/O	ST	
RC5	_	_	38	I/O	ST	
RC6	_	_	2	I/O	ST	
RC7	_		3	I/O	ST	
RC8	_		4	I/O	ST	
RC9	_	_	5	I/O	ST	

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

Analog = Analog input O = Output

P = Power I = Input

TTL = TTL input buffer

PPS = Peripheral Pin Select --=N/ANote 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

- 2: Pin number for General Purpose devices only.
- 3: This pin is not available for devices with VBAT.
- 4: This pin is not available for devices with USB.

TABLE 1-7: TIMER1 THROUGH TIMER5 AND RTCC PINOUT I/O DESCRIPTIONS

	Pi	in Number ⁽	[1)	Pin Type	Buffer Type	Description				
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP							
				Timer1	through 1	Fimer5				
T1CK	9	12	34	I	ST	Timer1-5 External Clock Input				
T2CK	PPS	PPS	PPS	I	ST					
T3CK	PPS	PPS	PPS	I	ST					
T4CK	PPS	PPS	PPS	I	ST					
T5CK	PPS	PPS	PPS	I	ST					
	Real-Time Clock and Calendar									
RTCC	4	7	24	0	ST	Real-Time Clock Alarm Output				

Legend: CMOS = CMOS compatible input or output Analog = Analog input ST = Schmitt Trigger input with CMOS levels O = Output

O = Output I = Input PPS = Peripheral Pin Select — = N/A

P = Power

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

TABLE 1-8: UART1 AND UART2 PINOUT I/O DESCRIPTIONS

TTL = TTL input buffer

TTL = TTL input buffer

	Pin Number ⁽¹⁾								
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description			
Universal Asynchronous Receiver Transmitter 2									
U1CTS	PPS	PPS	PPS	I	ST	UART1 Clear to Send			
U1RTS	PPS	PPS	PPS	0	1	UART1 Ready to Send			
U1RX	PPS	PPS	PPS	I	ST	UART1 Receive			
U1TX	PPS	PPS	PPS	0	1	UART1 Transmit			
		ι	Iniversal A	synchr	onous Rec	eiver Transmitter 2			
U2CTS	PPS	PPS	PPS	I	ST	UART2 Clear to Send			
U2RTS	PPS	PPS	PPS	0	_	UART2 Ready to Send			
U2RX	PPS	PPS	PPS	I	ST	UART2 Receive			
U2TX	PPS	PPS	PPS	0		UART2 Transmit			

Legend: CMOS = CMOS compatible input or output Analog = Analog input ST = Schmitt Trigger input with CMOS levels O = Output

Analog = Analog input P = Power O = Output I = Input PPS = Peripheral Pin Select — = N/A

TABLE 1-9: SPI1 AND SPI2 PINOUT I/O DESCRIPTIONS

	Pi	in Number ⁽	(1)						
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type		Description			
Serial Peripheral Interface 1									
SCK1	22	25	14	I/O	ST	Synchronous Serial Clock Input/Output for SPI1			
SDI1	PPS	PPS	PPS	- 1	ST	SPI1 Data In			
SDO1	PPS	PPS	PPS	0	_	SPI1 Data Out			
SS1	PPS	PPS	PPS	I/O	ST	SPI1 Slave Synchronization or Frame Pulse I/O			
			s	erial Pe	ripheral In	iterface 2			
SCK2	23	26	15	I/O	ST	Synchronous Serial Clock Input/Output for SPI2			
SDI2	PPS	PPS	PPS	I	ST	SPI2 Data In			
SDO2	PPS	PPS	PPS	0	_	SPI2 Data Out			
SS2	PPS	PPS	PPS	I/O	ST	SPI2 Slave Synchronization or Frame Pulse I/O			

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

O = Output

Analog = Analog input

P = Power I = Input

TTL = TTL input buffer

PPS = Peripheral Pin Select

--=N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

TABLE 1-10: **I2C1 AND I2C2 PINOUT I/O DESCRIPTIONS**

Pin Name	Pi	in Number ⁽	(1)	Pin Type	Buffer Type	Description			
	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP						
Inter-Integrated Circuit 1									
SCL1	14	17	44	I/O	ST	Synchronous Serial Clock Input/Output for I2C1			
SDA1	15	18	1	I/O	ST	Synchronous Serial Data Input/Output for I2C1			
ASCL1	28	3	20	I/O	ST	Alternative Synchronous Serial Clock Input/Output for I2C1			
ASDA1	27	2	19	I/O	ST	Alternative Synchronous Serial Data Input/Output for I2C1			
				Inter-In	tegrated C	Circuit 2			
SCL2	4	7	24	I/O	ST	Synchronous Serial Clock Input/Output for I2C2			
SDA2	3	6	23	I/O	ST	Synchronous Serial Data Input/Output for I2C2			
ASCL2	12 ⁽²⁾	15 ⁽²⁾	42 ⁽²⁾	I/O	ST	Alternative Synchronous Serial Clock Input/Output for I2C2			
ASDA2	11 ⁽²⁾	14 ⁽²⁾	41 ⁽²⁾	I/O	ST	Alternative Synchronous Serial Data Input/Output for I2C2			

Legend: CMOS = CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels Analog = Analog input

P = Power

TTL = TTL input buffer

O = Output

2: This pin is not available for devices with USB.

I = InputPPS = Peripheral Pin Select --=N/A

TABLE 1-11: COMPARATOR 1, COMPARATOR 2, AND COMPARATOR VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

	Pin Number ⁽¹⁾								
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description			
			Co	or Voltage	Reference				
VREF-	28	3	20	I	Analog	Comparator Voltage Reference (Low)			
VREF+	27	2	19	I	Analog	Comparator Voltage Reference (High)			
CVREFOUT	22	25	14	0	Analog	Comparator Voltage Reference Output			
Comparator 1									
C1INA	4	7	24	I	Analog	Comparator 1 Positive Input			
C1INB	3	6	23	I	Analog	Comparator 1 Selectable Negative Input			
C1INC	2	5	22	I	Analog				
C1IND	1	4	21	I	Analog				
C1OUT	PPS	PPS	PPS	0	_	Comparator 1 Output			
				С	omparator	2			
C2INA	2	5	22	I	Analog	Comparator 2 Positive Input			
C2INB	1	4	21	I	Analog	Comparator 2 Selectable Negative Input			
C2INC	4	7	24	I	Analog				
C2IND	3	6	23	I	Analog				
C2OUT	PPS	PPS	PPS	0	_	Comparator 2 Output			
				С	omparator	3			
C3INA	23	26	15	I	Analog	Comparator 3 Positive Input			
C3INB	22	25	14	I	Analog	Comparator 3 Selectable Negative Input			
C3INC	27	2	19	ı	Analog				
C3IND	1	4	21	I	Analog				
C3OUT	PPS	PPS	PPS	0		Comparator 3 Output			

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power I = Input--- = N/A

TABLE 1-12: PARALLEL MASTER PORT PINOUT I/O DESCRIPTIONS

	Pi	in Number ⁽	[1)							
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description				
	Parallel Master Port									
PMA0	7	10	15	I/O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)				
PMA1	27 ⁽²⁾ 22 ⁽³⁾	2 ⁽²⁾ 25 ⁽³⁾	2	I/O	TTL/ST	Parallel Master Port Address bit 1 Input (Buffered Slave modes) and Output (Master modes)				
PMA2	_	_	24	0	_	Parallel Master Port Address (Demultiplexed Master				
PMA3	_	_	41 ⁽²⁾ 19 ⁽³⁾	0	_	modes)				
PMA4	_	_	44	0	_					
PMA5	_	_	43	0	_					
PMA6	_	_	42 ⁽²⁾ 20 ⁽³⁾	0	_					
PMA7	_	_	1	0	_					
PMA8	_	_	8 ⁽²⁾ 23 ⁽³⁾	0	_					
PMA9	_	_	9 ⁽²⁾ 22 ⁽³⁾	0	_					
PMA10	_	_	12 ⁽²⁾ 21 ⁽³⁾	0	_					
PMCS1	23	26	3	0	_	Parallel Master Port Chip Select 1 Strobe				
PMD0	20 ⁽²⁾	23 ⁽²⁾ 4 ⁽³⁾	10 ⁽²⁾ 12 ⁽³⁾	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)				
PMD1	19 ⁽²⁾ 2 ⁽³⁾	22 ⁽²⁾ 5 ⁽³⁾	35	I/O	TTL/ST					
PMD2	18 ⁽²⁾ 3 ⁽³⁾	21 ⁽²⁾ 6 ⁽³⁾	32	I/O	TTL/ST					
PMD3	15	18	13	I/O	TTL/ST					
PMD4	14	17	37	I/O	TTL/ST					
PMD5	13	16	4	I/O	TTL/ST					
PMD6	12 ⁽²⁾	15 ⁽²⁾	_	1/0	TTL/OT					
	28 ⁽³⁾	3(3)	5	I/O	TTL/ST					
PMD7	11 ⁽²⁾ 27 ⁽³⁾	14 ⁽²⁾ 2 ⁽³⁾	38	I/O	TTL/ST					
PMRD	21 ^(2,5)	24 ^(2,5)	11 ⁽⁴⁾ 36 ⁽⁵⁾	0	_	Parallel Master Port Read Strobe				
PMWR	22 ⁽²⁾ 4 ⁽³⁾	25 ⁽²⁾ 7 ⁽³⁾	27	0	_	Parallel Master Port Write Strobe				
		1		1	1	1				

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

O = Output

P = PowerI = Input

TTL = TTL input buffer

PPS = Peripheral Pin Select

Analog = Analog input

--=N/A

2: Pin number for General Purpose devices only.

- 3: Pin number for USB devices only.
- 4: Pin number for devices with VBAT only.
- 5: Pin number for devices without VBAT only.

TABLE 1-13: **USB PINOUT I/O DESCRIPTIONS**

	Piı	n Number ⁽¹	1,2)		Pin Buffer Type Type	
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP			Description
				Unive	ersal Seria	l Bus
VBUS	12	15	42	I	Analog	USB Bus Power Monitor
VUSB3V3	20	23	10	Р	_	USB Internal Transceiver Supply. This pin must be connected to VDD.
VBUSON	PPS	PPS	PPS	0	_	USB Host and OTG Bus Power Control Output
D+	18	21	8	I/O	Analog	USB D+
D-	19	22	9	I/O	Analog	USB D-
USBID	11	14	41	I	ST	USB OTG ID Detect
USBON	14	17	44	0	_	ON Signal for External VBUS Source

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

O = Output

P = PowerI = Input

TTL = TTL input buffer

PPS = Peripheral Pin Select --=N/A

Analog = Analog input

- 2: All pins are only available on USB devices.
- 3: Pin number for devices without VBAT.
- 4: Pin number for devices with USB only.
- 5: Pin number for devices without USB.

TABLE 1-14: CTMU PINOUT I/O DESCRIPTIONS

	Pin Number ⁽¹⁾					
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type	Buffer Type	Description
			Cha	arge Tin	ne Measur	ement Unit
CTED1	27	2	19	I	ST	CTMU External Edge Input 1-13
CTED2	28	3	20	I	ST	
CTED3	13	16	43	I	ST	
CTED4	15	18	1	I	ST	
CTED5	22	25	14	I	ST	
CTED6	23	26	15	ı	ST	
CTED7	1	_	5	I	ST	
CTED8		_	13	I	ST	
CTED9	9	12	34(2)	I	ST	
CTED10	14	17	44	I	ST	
CTED11	8 ⁽⁴⁾	11 ⁽⁴⁾	33 ⁽⁴⁾		ST	
	18 ⁽⁵⁾	21 ⁽⁵⁾	8(5)		31	
CTED12	2	5	22		ST	
CTED13	3	6	23	I	ST	
CTPLS	4(2)	7 ⁽²⁾	24(2)	0	_	CTMU Pulse Output
	21 ⁽³⁾	24 ⁽³⁾	11 ⁽³⁾			

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

TTL = TTL input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power I = Input — = N/A

- 2: Pin number for devices with VBAT only.
- 3: Pin number for devices without VBAT.
- 4: Pin number for devices with USB only.
- 5: Pin number for devices without USB.

TABLE 1-15: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

	Pin Number ⁽¹⁾							
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP	Pin Type		Description		
				Pow	er and Gro	ound		
AVDD	25	28	17	Р	_	Positive supply for analog modules. This pin must be connected at all times.		
AVss	24	27	16	Р	_	Ground reference for analog modules		
VDD	10	13	28, 40	Р	_	Positive supply for peripheral logic and I/O pins		
VCAP	17	20	7	Р	_	CPU logic filter capacitor connection		
Vss	5, 16	8, 19	6, 29, 39	Р	_	Ground reference for logic and I/O pins. This pin must be connected at all times.		
LVDIN	2	5	22			Low-Voltage Detect pin		
VBAT	21 ⁽²⁾	24 ⁽²⁾	11 ⁽²⁾			Positive supply for the battery backed section. It is recommended to connect this pin to VDD if VBAT mode is not used (i.e., not connected to the battery).		
Voltage Reference								
VREF+	27	2	19	I	Analog	Analog voltage reference (high) input		
VREF-	28	3	20	I	Analog	Analog voltage reference (low) input		

Legend:CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levelsAnalog = Analog input
O = OutputP = Power
I = Input

TTL = TTL input buffer PPS = Peripheral Pin Select --= N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for devices with VBAT only.

TABLE 1-16: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

	Pi	in Number	(1)	Pin Type	Buffer Type	Description					
Pin Name	28-pin QFN	28-pin SOIC	44-pin QFN/ TQFP								
	Power and Ground										
TMO	19 ⁽²⁾	22 ⁽²⁾	9(2)		ОТ	ITAO Tantura da antantuin					
TMS	11(3)	14(3)	41(3)		ST	JTAG Test mode select pin					
TCK	14	17	13	I	ST	JTAG test clock input pin					
TDI	13	16	35	0		JTAG test data input pin					
TDO	15	18	32	0		JTAG test data output pin					
	Programming/Debugging										
DOED4	18 ⁽²⁾	21 ⁽²⁾	8(2)	1/0	ST	Data I/O pin for Programming/Debugging					
PGED1	₃ (3)	6 ⁽³⁾	23 ⁽³⁾	I/O		Communication Channel 1					
PGEC1	19 ⁽²⁾	22(2)	g (2)	- 1	ST	Clock input pin for Programming/Debugging Communication Channel 1					
FGECT	4 ⁽³⁾	7 ⁽³⁾	24 ⁽³⁾								
PGED2	1	4	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2					
PGEC2	2	5	22	ı	ST	Clock input pin for Programming/Debugging Communication Channel 2					
PGED3	11 ⁽²⁾	14(2)	41(2)	I/O	ST	Data I/O pin for Programming/Debugging					
FGEDS	27 ⁽³⁾	2 ⁽³⁾	19 ⁽³⁾	1/0	5	Communication Channel 3					
PGEC3	12 ⁽²⁾	15 ⁽²⁾	42 ⁽²⁾	_	ST	Clock input pin for Programming/					
I GLOS	28 ⁽³⁾	3(3)	20 ⁽³⁾	'	51	Debugging Communication Channel 3					
PGED4	_	_	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4					
PGEC4	_	_	13	ı	ST	Clock input pin for Programming/ Debugging Communication Channel 4					
MCLR	26	1	18	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.					

Legend: CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels TTL = TTL input buffer

O = Output PPS = Peripheral Pin Select

Analog = Analog input

P = Power I = Input — = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for General Purpose devices only.

3: Pin number for USB devices only.

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/44-pin XLP Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see 2.2 "Decoupling Capacitors")
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 "Decoupling Capacitors")
- VCAP pin (see 2.3 "Capacitor on Internal Voltage Regulator (VCAP)")
- MCLR pin (see 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins, used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see 2.5 "ICSP Pins")
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 "External Oscillator Pins")

The following pins may be required:

 VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

Note:

The AVDD and AVss pins must be connected, regardless of ADC use and the ADC voltage reference source.

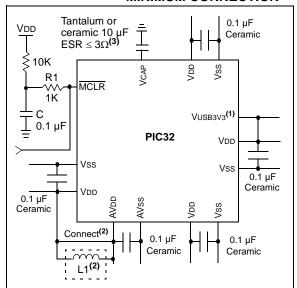
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The
 decoupling capacitors should be placed as close
 to the pins as possible. It is recommended that
 the capacitors be placed on the same side of the
 board as the device. If space is constricted, the
 capacitor can be placed on another layer on the
 PCB using a via; however, ensure that the trace
 length from the pin to the capacitor is within onequarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF.
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: If the USB module is not used, this pin must be connected to VDD.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 3Ω and the inductor capacity greater than 10 mA.

Where:

$$f=\frac{FCNV}{2} \qquad \text{(i.e., ADC conversion rate/2)}$$

$$f=\frac{1}{(2\pi\sqrt{LC})}$$

$$L=\left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

1: Aluminum or electrolytic capacitors should not be used. ESR $\leq 3\Omega$ from -40°C to 125°C @ SYSCLK frequency (i.e., MIPS).

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μ F to 47 μ F. This capacitor should be located as close to the device as possible.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

2.3.1 INTERNAL REGULATOR MODE

A low-ESR (3 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to 33.0 "Electrical Characteristics" for additional information on CEFC specifications.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

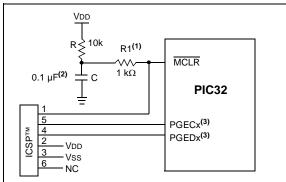
- · Device Reset
- · Device programming and debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



- Note 1: $\frac{470\Omega \leq R1 \leq 1\Omega}{MCLR} \text{ from the external capacitor C, in the event of } \frac{MCLR}{MCLR} \text{ pin breakdown, due to Electrostatic Discharge} \\ \frac{(ESD)}{MCLR} \text{ pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.}$
 - The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.
 - No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE $^{\text{TM}}$.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

- "Using MPLAB® ICD 3" (poster) (DS50001765)
- "MPLAB® ICD 3 Design Advisory" (DS50001764)
- "MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" (DS50001616)
- "Using MPLAB® REAL ICE™ Emulator" (poster) (DS50001749)

2.6 **JTAG**

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

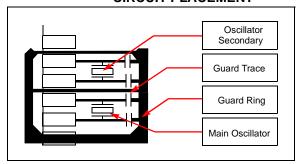
Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to 8.0 "Oscillator Configuration" for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION

```
Crystal manufacturer recommended: CI = C2 = 15 \ pF
Therefore:
CLOAD = \left\{ \left( \ [CIN + CI] \ ^* \ [COUT + C2] \ \right) / \ [CIN + CI + C2 + COUT] \right\} \\ + estimated \ oscillator \ PCB \ stray \ capacitance \\ = \left\{ \left( \ [5 + 15][5 + 15] \right) / [5 + 15 + 15 + 5] \right\} + 2.5 \ pF \right. \\ = \left\{ \left( \ [20][20]) / \ [40] \right\} + 2.5 \\ = 10 + 2.5 = 12.5 \ pF
Rounded to the nearest standard value or 13 pF in this example for Primary Oscillator crystals "C1" and "C2".
```

The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

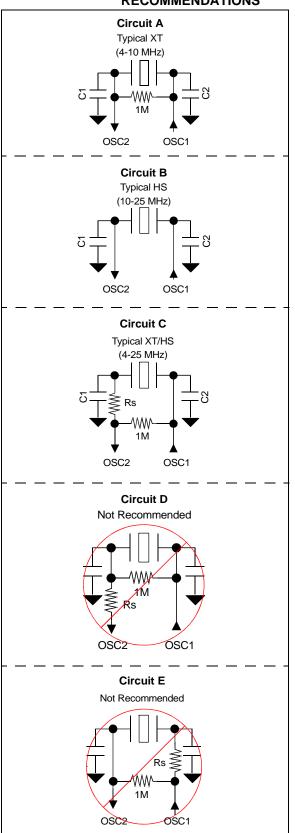
- Select a crystal with a lower "minimum" power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing "ESR" rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator.
 The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit "C" in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to ~VDD-0.6V. When measuring the oscillator signal you must use a FET scope probe or a probe with ≤ 1.5 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.8.1.1 Additional Microchip References

- AN588 "PICmicro® Microcontroller Oscillator Design Guide"
- AN826 "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"
- AN849 "Basic PICmicro® Oscillator Design"

FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.

FIGURE 2-5: REMOTE SENSING APPLICATION

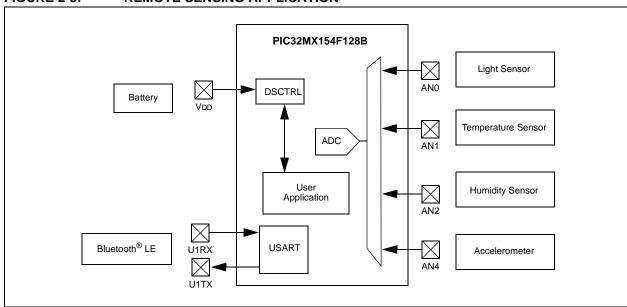
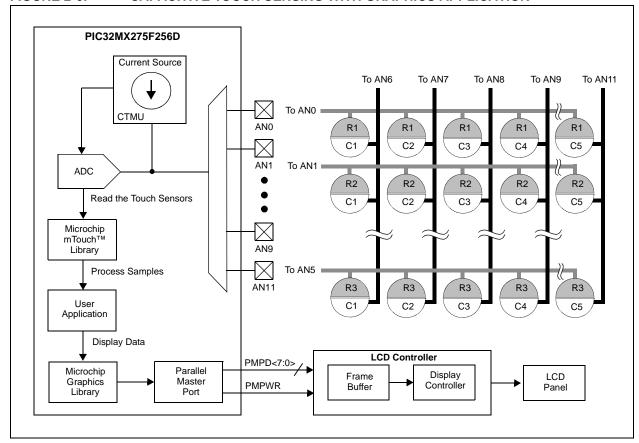


FIGURE 2-6: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION



NOTES:

3.0 CPU

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2.** "CPU" (DS60001113), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). Resources for the MIPS32® M4K® Processor Core are available at: www.imgtec.com.

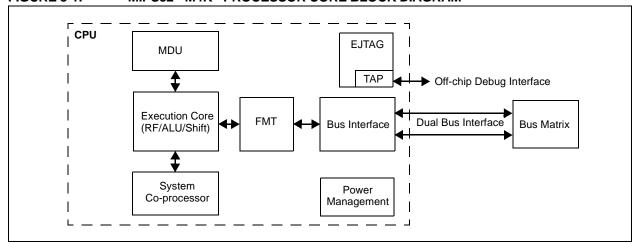
The MIPS32[®] M4K[®] Processor Core is the heart of the PIC32MX1XX/2XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the destinations.

3.1 Features

- 5-stage pipeline
- · 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
- Multiply-accumulate and multiply-subtract instructions
- Targeted multiply instruction
- Zero/One detect instructions
- WAIT instruction
- Conditional move instructions (MOVN, MOVZ)
- Vectored interrupts
- Programmable exception vector base
- Atomic interrupt enable/disable
- Bit field manipulation instructions

- MIPS16e® code compression
 - 16-bit encoding of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8-bit and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- · Simple dual bus interface
 - Independent 32-bit address and data buses
 - Transactions can be aborted to improve interrupt latency
- Autonomous multiply/divide unit
 - Maximum issue rate of one 32x16 multiply per clock
 - Maximum issue rate of one 32x32 multiply every other clock
 - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension-dependent)
- Power control
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- · EJTAG debug and instruction trace
 - Support for single stepping
 - Virtual instruction and data address/value
 - Breakpoints

FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM



3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e[®] Support
- · Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- · Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32® M4K® PROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul rt) (div rs)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU,	16 bits	1	1
MSUB/MSUBU	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 $^{\circledR}$ architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then

adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr ⁽¹⁾	Reports the address for the most recent address-related exception.
9	Count ⁽¹⁾	Processor cycle count.
10	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
11	Compare ⁽¹⁾	Timer interrupt control.
12	Status ⁽¹⁾	Processor status and control.
12	IntCtl ⁽¹⁾	Interrupt system status and control.
12	SRSCtl ⁽¹⁾	Shadow register set status and control.
12	SRSMap ⁽¹⁾	Provides mapping from vectored interrupt to a shadow set.
13	Cause ⁽¹⁾	Cause of last general exception.
14	EPC ⁽¹⁾	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration Register 1.
16	Config2	Configuration Register 2.
16	Config3	Configuration Register 3.
17-22	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
23	Debug ⁽²⁾	Debug control and exception status.
24	DEPC ⁽²⁾	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX1XX/2XX XLP Family core.
30	ErrorEPC ⁽¹⁾	Program counter at last error.
31	DESAVE ⁽²⁾	Debug handler scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see 29.0 "Power-Saving Features".

3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

4.0 MEMORY ORGANIZATION

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 3.** "**Memory Organization**" (DS60001115), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/44-pin XLP Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/44-pin XLP Family devices to execute from data memory.

Key features include:

- · 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- · Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- · Separate Boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 PIC32MX1XX/2XX 28/44-pin XLP Family Memory Layout

PIC32MX1XX/2XX 28/44-pin XLP Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/44-pin XLP Family devices are illustrated in Figure 4-1 and Figure 4-2.

Table 4-1 provides SFR memory map details.

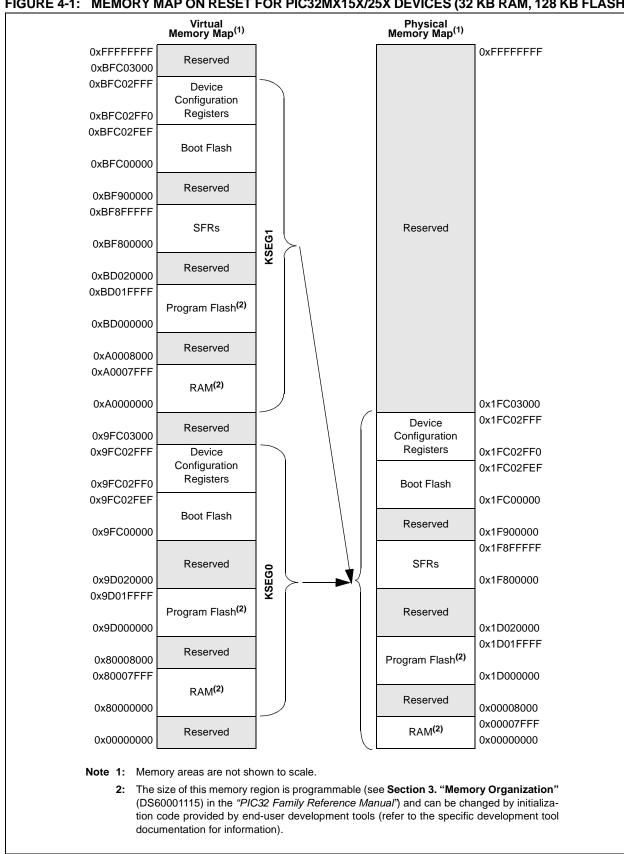


FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX15X/25X DEVICES (32 KB RAM, 128 KB FLASH)

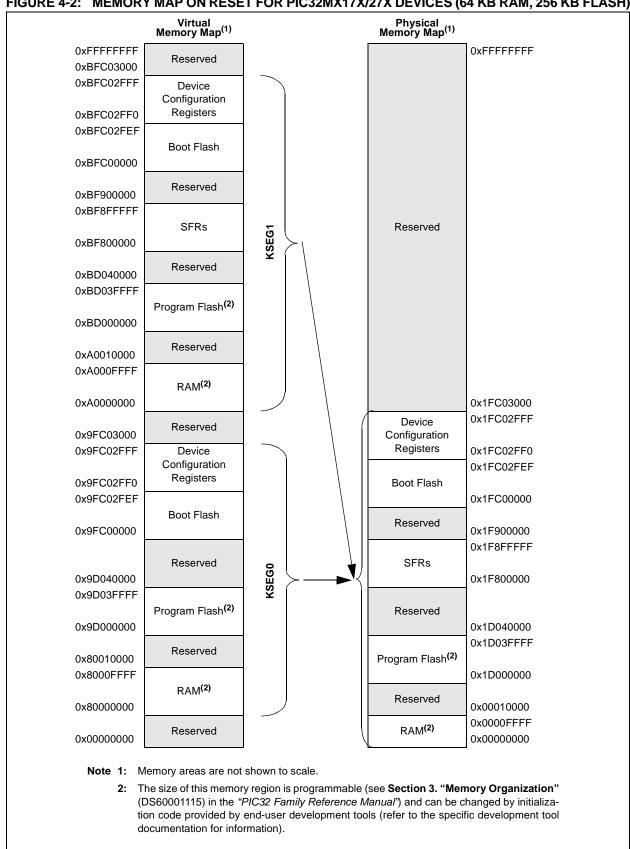


FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX17X/27X DEVICES (64 KB RAM, 256 KB FLASH)

TABLE 4-1: SFR MEMORY MAP

	Virtual A	Address
Peripheral	Base	Offset Start
Deep Sleep Controller		0x0000
RTCC		0x0200
Timer1-Timer5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
I2C1 and I2C2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC	0	0x9000
CVREF	0xBF80	0x9800
Comparator		0xA000
СТМИ		0xA200
Oscillator, Reset		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Watchdog Timer		0xF600
PPS		0xFA00
HLVD		0xFC00
Interrupts		0x1000
Bus Matrix		0x2000
DMA		0x3000
Prefetch	0xBF88	0x4000
USB		0x5000
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x2FF0

4.2 Bus Matrix Control Registers

TABLE 4-2: BUS MATRIX REGISTER MAP

ess (Φ								Ві	ts								
Virtual Address (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000		31:16	_	_	-	_		BMX CHEDMA	_	_	_	_	_	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS	001F
2000	BIVIACOIN	15:0	_	_	_	_	_	_	_	_	_	BMX WSDRM	_	_	_	BMXARB<2:0>			0041
2010	BMXDKPBA ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
2010	DIVINDINI DA.	15:0								BMXDKP	BA<15:0>								0000
2020	BMXDUDBA ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
2020	BIVIABOBBA	15:0								BMXDUD	BA<15:0>								0000
2030	BMXDUPBA ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
2030	BIVIXBOI BA	15:0								BMXDUP	BA<15:0>								0000
2040	BMXDRMSZ	31:16								BMXDRM	97/31:05								xxxx
		15:0								DIVINDICIVI	02<01.0>								xxxx
2050	BMXPUPBA ⁽¹⁾	31:16	_	_	_	_		_	_	_		_	_	_		BMXPUP	3A<19:16>		0000
2030	BIVIXI OI BA	15:0								BMXPUP	BA<15:0>								0000
2060	BMXPFMSZ	31:16		BMXPFMSZ<31:0>									xxxx						
2000	DIVINI I WISE	15:0												xxxx					
2070	BMXBOOTSZ	31:16		BMXBOOTSZ<31:0>										0000					
2070	DIVINDOOTS2	15:0								DIVINDOO	02<31.0>								0000

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-0
31:24	_	_	_	_	_	BMX CHEDMA	_	_
	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
23:16		_	_	BMX ERRIXI	BMX ERRICD	BMX ERRDMA	BMX ERRDS	BMX ERRIS
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
	U-0	R/W-1	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1
7:0	_	BMX WSDRM	_	_	_	E	BMXARB<2:0:	>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared

bit 31-27 Unimplemented: Read as '0'

bit 26 BMXCHEDMA: BMX PFM Cacheability for DMA Access bit

- 1 = Enable Program Flash memory (data) cacheability for DMA accesses (requires cache to have data caching enabled)
- 0 = Disable program Flash memory (data) cacheability for DMA accesses (hits are still read from the cache, but misses do not update the cache)
- bit 25-21 Unimplemented: Read as '0'
- bit 20 BMXERRIXI: Enable Bus Error from IXI bit
 - 1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus
 - 0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus
- bit 19 BMXERRICD: Enable Bus Error from ICD Debug Unit bit
 - 1 = Enable bus error exceptions for unmapped address accesses initiated from ICD
 - 0 = Disable bus error exceptions for unmapped address accesses initiated from ICD
- bit 18 BMXERRDMA: Bus Error from DMA bit
 - 1 = Enable bus error exceptions for unmapped address accesses initiated from DMA
 - 0 = Disable bus error exceptions for unmapped address accesses initiated from DMA
- bit 17 BMXERRDS: Bus Error from CPU Data Access bit (disabled in Debug mode)
 - 1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access
 - 0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access
- bit 16 BMXERRIS: Bus Error from CPU Instruction Access bit (disabled in Debug mode)
 - 1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access
 - 0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access
- bit 15-7 Unimplemented: Read as '0'
- bit 6 BMXWSDRM: CPU Instruction or Data Access from Data RAM Wait State bit
 - 1 = Data RAM accesses from CPU have one wait state for address setup
 - 0 = Data RAM accesses from CPU have zero wait states for address setup
- bit 5-3 Unimplemented: Read as '0'
- bit 2-0 BMXARB<2:0>: Bus Matrix Arbitration Mode bits
 - 111 = Reserved (using these Configuration modes will produce undefined behavior)

:

- 011 = Reserved (using these Configuration modes will produce undefined behavior)
- 010 = Arbitration Mode 2
- 001 = Arbitration Mode 1 (default)
- 000 = Arbitration Mode 0

REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
31:24	_	_	-	_		_	_	_				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23:16	_	_	_	_	_	_	_	_				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0				
15:8		BMXDKPBA<15:8>										
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
7:0				BMXDK	PBA<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDKPBA<15:10>: DRM Kernel Program Base Address bits

When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 BMXDKPBA<9:0>: Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	_			_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
15:8	BMXDUDBA<15:8>							
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				BMXDU	DBA<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUDBA<15:10>: DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 BMXDUDBA<9:0>: Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	_	_	-	_				_			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:16	_	_	_	_	_	_	_	_			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0			
15:8	BMXDUPBA<15:8>										
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7:0				BMXDU	PBA<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUPBA<15:10>: DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 BMXDUPBA<9:0>: Read-Only bits

This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R	R	R	R	R	R	R	R			
31:24	BMXDRMSZ<31:24>										
22:40	R	R	R	R	R	R	R	R			
23:16	BMXDRMSZ<23:16>										
45.0	R	R	R	R	R	R	R	R			
15:8	BMXDRMSZ<15:8>										
7.0	R	R	R	R	R	R	R	R			
7:0				BMXDR	MSZ<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 BMXDRMSZ<31:0>: Data RAM Memory (DRM) Size bits

Static value that indicates the size of the Data RAM in bytes:

0x00008000 = Device has 32 KB RAM 0x00010000 = Device has 64 KB RAM

REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	_	_	_	_		_	_	_	
00:40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	_	_	_	_		BMXPUPE	3A<19:16>		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	
15:8		BMXPUPBA<15:8>							
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
7:0				BMXPU	PBA<7:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-20 Unimplemented: Read as '0'

bit 19-11 BMXPUPBA<19:11>: Program Flash (PFM) User Program Base Address bits

bit 10-0 BMXPUPBA<10:0>: Read-Only bits

This value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXPFMSZ.

REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R	R	R	R	R	R	R	R			
31:24		BMXPFMSZ<31:24>									
22,46	R	R	R	R	R	R	R	R			
23:16	BMXPFMSZ<23:16>										
45.0	R	R	R	R	R	R	R	R			
15:8				BMXPFN	//SZ<15:8>						
7.0	R	R	R	R	R	R	R	R			
7:0				BMXPF	MSZ<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 BMXPFMSZ<31:0>: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes:

0x00020000 = Device has 128 KB Flash 0x00040000 = Device has 256 KB Flash

REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R	R	R	R	R	R	R	R
31:24				BMXBOO	TSZ<31:24>			
22,46	R	R	R	R	R	R	R	R
23:16				BMXBOO	TSZ<23:16>			
45.0	R	R	R	R	R	R	R	R
15:8				BMXBOO	OTSZ<15:8>			
7.0	R	R	R	R	R	R	R	R
7:0				BMXBO	OTSZ<7:0>	_		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 BMXBOOTSZ<31:0>: Boot Flash Memory (BFM) Size bits

Static value that indicates the size of the Boot PFM in bytes:

0x00003000 = Device has 12 KB Boot Flash

NOTES:

5.0 FLASH PROGRAM MEMORY

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Program Memory" (DS60001121), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/44-pin XLP Family devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program the Flash memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming[™] (ICSP[™])

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5.** "Flash Program Memory" (DS60001121) in the "PIC32 Family Reference Manual".

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "PIC32 Flash Programming Specification" (DS60001145), which can be downloaded from the Microchip web site (www.microchip.com).

Note:

The Flash page size on PIC32MX-1XX/2XX 28/44-pin XLP Family devices is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

5.1 Flash Controller Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

ess		0								Bit	s								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F400	NVMCON ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
F400	NVMCON	15:0	WR	WREN	WRERR	LVDERR	LVDSTAT				_	_	_	_		NVMO	P<3:0>	•	0000
F410	NVMKEY	31:16								NVMKEY	′~21·0~								0000
1410	IN VIVINL I	15:0								IN V IVIINE I	<31.0>								0000
F420	NVMADDR ⁽¹⁾	31:16								NVMADD	D ~21·0~								0000
1 420	NVIVIADDIX.,	15:0								INVIVIADDI	1231.02								0000
F430	NVMDATA	31:16								NVMDATA	\ -21·0\								0000
1 430	NVIVIDATA	15:0								INVIVIDATA	1<31.0>								0000
E440	NVMSRCADDR	31:16	•		•		•	•	NI.	/MSDCAL	DR<31:0>		•		•	•	•		0000
1 440	INVINISICADDR	15:0							IN	VIVISITOAL	<0.10>								0000

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	-	_	_	-	-	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	-	_	_	-	-	_
45.0	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
15:8	WR	WREN	WRERR ⁽¹⁾	LVDERR ⁽¹⁾	LVDSTAT ⁽¹⁾	_	_	_
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	1	1	_		NVMOF	P<3:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 WR: Write Control bit

This bit is writable when WREN = 1 and the unlock sequence is followed.

1 = Initiate a Flash operation. Hardware clears this bit when the operation completes

0 = Flash operation is complete or inactive

bit 14 WREN: Write Enable bit

This is the only bit in this register reset by a device Reset.

1 = Enable writes to WR bit and enables HLVD circuit

0 = Disable writes to WR bit and disables HLVD circuit

bit 13 **WRERR:** Write Error bit⁽¹⁾

This bit is read-only and is automatically set by hardware.

1 = Program or erase sequence did not complete successfully

0 = Program or erase sequence completed normally

bit 12 LVDERR: Low-Voltage Detect Error bit (LVD circuit must be enabled)⁽¹⁾

This bit is read-only and is automatically set by hardware.

1 = Low-voltage detected (possible data corruption, if WRERR is set)

0 = Voltage level is acceptable for programming

bit 11 LVDSTAT: Low-Voltage Detect Status bit (LVD circuit must be enabled)⁽¹⁾

This bit is read-only and is automatically set and cleared by the hardware.

1 = Low-voltage event is active

0 = Low-voltage event is not active

bit 10-4 Unimplemented: Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits

These bits are writable when WREN = 0.

1111 = Reserved

•

.

0111 = Reserved

0110 = No operation

0101 = Program Flash Memory (PFM) erase operation: erases PFM, if all pages are not write-protected

0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected

0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected

0010 = No operation

0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected

0000 = No operation

Note 1: This bit is cleared by setting NVMOP == 'b0000, and initiating a Flash operation (i.e., WR).

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
31:24				NVMKE	Y<31:24>			
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
23:16				NVMKE	Y<23:16>			
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
15:8				NVMK	EY<15:8>			
7.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
7:0				NVMK	EY<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24				NVMADI	DR<31:24>			
22.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16				NVMADI	DR<23:16>			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8				NVMAD	DR<15:8>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0				NVMAD	DR<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 NVMADDR<31:0>: Flash Address bits

Bulk/Chip/PFM Erase: Address is ignored.
Page Erase: Address identifies the page to erase.
Row Program: Address identifies the row to program.
Word Program: Address identifies the word to program.

REGISTER 5-4: NVMDATA: FLASH PROGRAM DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24				NVMDA	TA<31:24>			
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16				NVMDA:	TA<23:16>			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8				NVMDA	ATA<15:8>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0				NVMD	ATA<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMDATA<31:0>:** Flash Programming Data bits

Note: The bits in this register are only reset by a Power-on Reset (POR).

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24				NVMSRCA	DDR<31:24	>		
22.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16				NVMSRCA	DDR<23:16	>		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8				NVMSRC	ADDR<15:8>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0				NVMSRC	ADDR<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 NVMSRCADDR<31:0>: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

NOTES:

6.0 RESETS

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7.** "**Resets**" (DS60001118), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

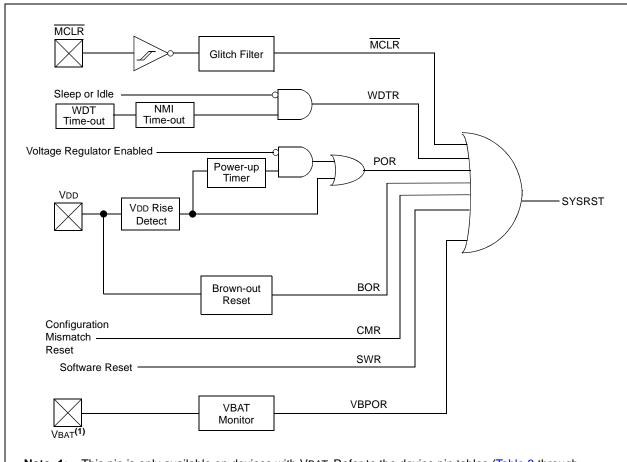
The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- VBAT Power-on Reset (VBPOR)
- Master Clear Reset pin (MCLR)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- · Configuration Mismatch Reset (CMR)

All device Reset will set a corresponding Status bit in the RCON register (see Register 6-1) to indicate the type of reset.

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



Note 1: This pin is only available on devices with VBAT. Refer to the device pin tables (Table 3 through Table 14) for availability.

6.1 Reset Control Registers

TABLE 6-1: RESET CONTROL REGISTER MAP

ess											Bits								8
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F040	RCON	31:16	_	_	_	_	BCFGERR	BCFGFAIL	_	_	_	_	_	_	-	_	VBPOR ⁽³⁾	VBAT ⁽³⁾	C802
F040	RCON	15:0	_	_	_	_	_	DPSLP	CMR	_	EXTR	SWR	_	WDTO	SLEEP	IDLE	BOR	POR	0003
EOEO	RSWRST	31:16	_	1	1	-		_	_	_	I	1	1	I	I	I	_		0000
1 030	KOWKOI	15:0	_	1	1	_	1	1	_	_	_	_	-	-		-	_	SWRST	0000
EOGO	RNMICON	31:16	_	1	1	_	1	1	_	WDTO	SWNMI	_	-	-	GNMI	HLVD	CF	WDTS	0000
1 000	KINIVICON	15:0								NMI	CNT<15:0>	•							0000
E070	PWRCON	31:16	-		1	_	_	_	_	_	_	_	-	1	1	1	_		0000
1 070	FWICON	15:0	_	-	1	-	1	_	_	_	-	-	-	I	I	-	_	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

- 2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
- 3: This bit is only available on devices with VBAT.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	RW-0, HC	R/W-0, HC	U-0	U-0
31:24	_	_	-	_	BCFGERR	BCFGFAIL	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1, HS	R/W-1, HS
23:16	_	_	_	_	_	_	VBPOR ⁽²⁾	VBAT ⁽²⁾
45.0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
15:8	_	_	_	_	_	DPSLP ⁽¹⁾	CMR	_
7.0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
7:0	EXTR	SWR	_	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

Legend: HS = Hardware Set HC = Hardware Cleared

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0' bit **Unimplemented:** Read as '0'

bit 27 BCFGERR: Primary Configuration Registers Error Flag bit

1 = An error occurred during a read of the primary configuration registers0 = No error occurred during a read of the primary configuration registers

bit 26 BCFGFAIL: Primary/Secondary Configuration Registers Error Flag bit

1 = An error occurred during a read of the primary and alternate configuration registers 0 = No error occurred during a read of the primary and alternate configuration registers

bit 25-18 Unimplemented: Read as '0'

bit 17 **VBPOR:** VBPOR Mode Flag bit⁽²⁾

1 = A VBAT domain POR has occurred

0 = A VBAT domain POR has not occurred

bit 16 VBAT: VBAT Mode Flag bit⁽²⁾

1 = A POR exit from VBAT has occurred (a true POR must be established with the valid VBAT voltage on the VBAT pin)

0 = A POR exit from VBAT has not occurred

bit 15-11 Unimplemented: Read as '0'

bit 10 **DPSLP:** Deep Sleep Mode Flag bit⁽¹⁾

1 = Deep Sleep mode has occurred

0 = Deep Sleep mode has not occurred

bit 9 CMR: Configuration Mismatch Reset Flag bit

1 = A Configuration Mismatch Reset has occurred

0 = A Configuration Mismatch Reset has not occurred

bit 8 Unimplemented: Read as '0'

bit 7 **EXTR:** External Reset (MCLR) Pin Flag bit

1 = Master Clear (pin) Reset has occurred

0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit

1 = Software Reset was executed

0 = Software Reset was not executed

bit 5 Unimplemented: Read as '0'

Note 1: User software must clear this bit to view the next detection.

2: This bit is only available on devices with VBAT.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

- bit 4 WDTO: Watchdog Timer Time-out Flag bit
 - 1 = WDT Time-out has occurred
 - 0 = WDT Time-out has not occurred
- bit 3 SLEEP: Wake From Sleep Flag bit
 - 1 = Device was in Sleep mode
 - 0 = Device was not in Sleep mode
- bit 2 IDLE: Wake From Idle Flag bit
 - 1 = Device was in Idle mode
 - 0 = Device was not in Idle mode
- bit 1 BOR: Brown-out Reset Flag bit⁽¹⁾
 - 1 = Brown-out Reset has occurred
 - 0 = Brown-out Reset has not occurred
- bit 0 **POR:** Power-on Reset Flag bit⁽¹⁾
 - 1 = Power-on Reset has occurred
 - 0 = Power-on Reset has not occurred
- Note 1: User software must clear this bit to view the next detection.
 - 2: This bit is only available on devices with VBAT.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	_				_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	-	_	_	_
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
7:0	_	_	_	_	_	_	_	SWRST ^(1,2)

Legend: HC = Hardware Cleared

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-1 Unimplemented: Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit^(1,2)

1 = Enable software Reset event

0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details

2: Once this bit is set, any read of the RSWRST register will cause a reset to occur.

REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
31.24	_	_	_	_	1	_	_	WDTO
23:16	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	SWNMI	_	_	_	GNMI	HLVD	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.6				NMIC	NT<15:8>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0				NMIC	NT<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-25 Unimplemented: Read as '0'

bit 24 WDTO: Watchdog Timer Time-Out Flag bit

1 = WDT time-out has occurred and caused a NMI

0 = WDT time-out has not occurred

Setting this bit will cause a WDT NMI event, and MNICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger.

1 = An NMI will be generated0 = An NMI will not be generated

bit 22-20 Unimplemented: Read as '0'

bit 19 GNMI: General NMI bit

1 = A general NMI event has been detected or a user-initiated NMI event has occurred

0 = A general NMI event has not been detected

Setting GNMI to a '1' causes a user-initiated NMI event. This bit is also set by writing 0x4E to the NMIKEY<7:0> (INTCON<31:24>) bits.

bit 18 **HLVD:** High/Low-Voltage Detect bit

1 = HLVD has detected a low-voltage condition and caused an NMI

0 = HLVD has not detected a low-voltage condition

bit 17 CF: Clock Fail Detect bit

1 = FSCM has detected clock failure and caused an NMI

0 = FSCM has not detected clock failure

Setting this bit will cause a a CF NMI event.

bit 16 WDTS: Watchdog Timer Time-out in Sleep Mode Flag bit

1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep

0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

bit 15-0 NMICNT<15:0>: NMI Reset Counter Value bits

These bits specify the reload value used by the NMI reset counter.

111111111111111-000000000000000 = Number of SYSCLK cycles before a device Reset occurs (1) 0000000000000 = No delay between NMI assertion and device Reset event

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) is cleared before this counter reaches '0', no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section** 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.

REGISTER 6-4: PWRCON: POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	_	_	_	_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	1	_	_			_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
7:0	_	_	_	_	_	_	_	VREGS

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-1 Unimplemented: Read as '0'

bit 0 VREGS: Voltage Regulator Stand-by Enable bit

1 = Voltage regulator will remain active during Sleep

0 = Voltage regulator will go to Stand-by mode during Sleep

NOTES:

7.0 INTERRUPT CONTROLLER

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/44-pin XLP Family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

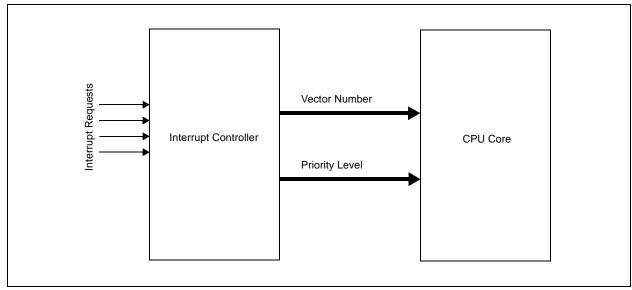
The PIC32MX1XX/2XX 28/44-pin XLP Family interrupt module includes the following features:

- Up to 64 interrupt sources
- · Up to 44 interrupt vectors
- · Single and multi-vector mode operations
- · Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Software can generate any interrupt
- User-configurable Interrupt Vector Table (IVT) location
- · User-configurable interrupt vector spacing

Note: The dedicated shadow register set is not present on PIC32MX1XX/2XX 28/44-pin XLP Family devices.

A simplified block diagram of the Interrupt Controller module is illustrated in Figure 7-1.

FIGURE 7-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



INTERRUPT IRQ, VECTOR AND BIT LOCATION **TABLE 7-1:**

Interrupt Source ⁽¹⁾	IRQ	Vector		Persistent								
interrupt Source(*)	#	#	Flag	Enable	Priority	Sub-priority	Interrupt					
Highest Natural Order Priority												
CT – Core Timer Interrupt	0	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No					
CS0 – Core Software Interrupt 0	1	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No					
CS1 – Core Software Interrupt 1	2	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No					
INT0 – External Interrupt	3	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No					
T1 – Timer1	4	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No					
IC1E - Input Capture 1 Error	5	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes					
IC1 – Input Capture 1	6	5	IFS0<6>	IEC0<6>	IPC1<12:10>	IPC1<9:8>	Yes					
OC1 – Output Compare 1	7	6	IFS0<7>	IEC0<7>	IPC1<20:18>	IPC1<17:16>	No					
INT1 – External Interrupt 1	8	7	IFS0<8>	IEC0<8>	IPC1<28:26>	IPC1<25:24>	No					
T2 – Timer2	9	8	IFS0<9>	IEC0<9>	IPC2<4:2>	IPC2<1:0>	No					
IC2E - Input Capture 2	10	9	IFS0<10>	IEC0<10>	IPC2<12:10>	IPC2<9:8>	Yes					
IC2 – Input Capture 2	11	9	IFS0<11>	IEC0<11>	IPC2<12:10>	IPC2<9:8>	Yes					
OC2 – Output Compare 2	12	10	IFS0<12>	IEC0<12>	IPC2<20:18>	IPC2<17:16>	No					
INT2 – External Interrupt 2	13	11	IFS0<13>	IEC0<13>	IPC2<28:26>	IPC2<25:24>	No					
T3 – Timer3	14	12	IFS0<14>	IEC0<14>	IPC3<4:2>	IPC3<1:0>	No					
IC3E - Input Capture 3	15	13	IFS0<15>	IEC0<15>	IPC3<12:10>	IPC3<9:8>	Yes					
IC3 – Input Capture 3	16	13	IFS0<16>	IEC0<16>	IPC3<12:10>	IPC3<9:8>	Yes					
OC3 – Output Compare 3	17	14	IFS0<17>	IEC0<17>	IPC3<20:18>	IPC3<17:16>	No					
INT3 – External Interrupt 3	18	15	IFS0<18>	IEC0<18>	IPC3<28:26>	IPC3<25:24>	No					
T4 – Timer4	19	16	IFS0<19>	IEC0<19>	IPC4<4:2>	IPC4<1:0>	No					
IC4E – Input Capture 4 Error	20	17	IFS0<20>	IEC0<20>	IPC4<12:10>	IPC4<9:8>	Yes					
IC4 – Input Capture 4	21	17	IFS0<21>	IEC0<21>	IPC4<12:10>	IPC4<9:8>	Yes					
OC4 – Output Compare 4	22	18	IFS0<22>	IEC0<22>	IPC4<20:18>	IPC4<17:16>	No					
INT4 – External Interrupt 4	23	19	IFS0<23>	IEC0<23>	IPC4<28:26>	IPC4<25:24>	No					
T5 – Timer5	24	20	IFS0<24>	IEC0<24>	IPC5<4:2>	IPC5<1:0>	No					
IC5E – Input Capture 5 Error	25	21	IFS0<25>	IEC0<25>	IPC5<12:10>	IPC5<9:8>	Yes					
IC5 – Input Capture 5	26	21	IFS0<26>	IEC0<26>	IPC5<12:10>	IPC5<9:8>	Yes					
OC5 – Output Compare 5	27	22	IFS0<27>	IEC0<27>	IPC5<20:18>	IPC5<17:16>	No					
AD1 – ADC1 Convert done	28	23	IFS0<28>	IEC0<28>	IPC5<28:26>	IPC5<25:24>	Yes					
FSCM – Fail-Safe Clock Monitor	29	24	IFS0<29>	IEC0<29>	IPC6<4:2>	IPC6<1:0>	No					
RTCC – Real-Time Clock and Calendar	30	25	IFS0<30>	IEC0<30>	IPC6<12:10>	IPC6<9:8>	No					
FCE – Flash Control Event	31	26	IFS0<31>	IEC0<31>	IPC6<20:18>	IPC6<17:16>	No					
CMP1 – Comparator Interrupt	32	27	IFS1<0>	IEC1<0>	IPC6<28:26>	IPC6<25:24>	No					
CMP2 – Comparator Interrupt	33	28	IFS1<1>	IEC1<1>	IPC7<4:2>	IPC7<1:0>	No					
CMP3 – Comparator Interrupt	34	29	IFS1<2>	IEC1<2>	IPC7<12:10>	IPC7<9:8>	No					
USB – USB Interrupts	35	30	IFS1<3>	IEC1<3>	IPC7<20:18>	IPC7<17:16>	Yes					
SPI1E - SPI1 Fault		31	IFS1<4>	IEC1<4>	IPC7<28:26>	IPC7<25:24>	Yes					
SPI1RX – SPI1 Receive Done	37	31	IFS1<5>	IEC1<5>	IPC7<28:26>	IPC7<25:24>	Yes					
SPI1TX - SPI1 Transfer Done	38	31	IFS1<6>	IEC1<6>	IPC7<28:26>	IPC7<25:24>	Yes					

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/44-Pin XLP (General Purpose) Family Features" and TABLE 2: "PIC32MX2XX 28/44-Pin XLP (USB) Family Features" for the lists of available peripherals.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾		Vector		Persistent				
interrupt Source(*)	#	#	Flag	Enable	Priority	Sub-priority	Interrupt	
U1E – UART1 Fault	39	32	IFS1<7>	IEC1<7>	IPC8<4:2>	IPC8<1:0>	Yes	
U1RX – UART1 Receive Done	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>	Yes	
U1TX – UART1 Transfer Done	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>	Yes	
I2C1B – I2C1 Bus Collision Event	42	33	IFS1<10>	IEC1<10>	IPC8<12:10>	IPC8<9:8>	Yes	
I2C1S - I2C1 Slave Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>	Yes	
I2C1M – I2C1 Master Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>	Yes	
CNA – PORTA Input Change Interrupt	45	34	IFS1<13>	IEC1<13>	IPC8<20:18>	IPC8<17:16>	Yes	
CNB – PORTB Input Change Interrupt	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>	Yes	
CNC – PORTC Input Change Interrupt		34	IFS1<15>	IEC1<15>	IPC8<20:18>	IPC8<17:16>	Yes	
PMP – Parallel Master Port	48	35	IFS1<16>	IEC1<16>	IPC8<28:26>	IPC8<25:24>	Yes	
PMPE – Parallel Master Port Error		35	IFS1<17>	IEC1<17>	IPC8<28:26>	IPC8<25:24>	Yes	
SPI2E - SPI2 Fault		36	IFS1<18>	IEC1<18>	IPC9<4:2>	IPC9<1:0>	Yes	
SPI2RX – SPI2 Receive Done		36	IFS1<19>	IEC1<19>	IPC9<4:2>	IPC9<1:0>	Yes	
SPI2TX – SPI2 Transfer Done		36	IFS1<20>	IEC1<20>	IPC9<4:2>	IPC9<1:0>	Yes	
U2E – UART2 Error		37	IFS1<21>	IEC1<21>	IPC9<12:10>	IPC9<9:8>	Yes	
U2RX – UART2 Receiver	54	37	IFS1<22>	IEC1<22>	IPC9<12:10>	IPC9<9:8>	Yes	
U2TX – UART2 Transmitter	55	37	IFS1<23>	IEC1<23>	IPC9<12:10>	IPC9<9:8>	Yes	
I2C2B – I2C2 Bus Collision Event	56	38	IFS1<24>	IEC1<24>	IPC9<20:18>	IPC9<17:16>	Yes	
I2C2S - I2C2 Slave Event	57	38	IFS1<25>	IEC1<25>	IPC9<20:18>	IPC9<17:16>	Yes	
I2C2M - I2C2 Master Event	58	38	IFS1<26>	IEC1<26>	IPC9<20:18>	IPC9<17:16>	Yes	
CTMU - CTMU Event	59	39	IFS1<27>	IEC1<27>	IPC9<28:26>	IPC9<25:24>	Yes	
DMA0 - DMA Channel 0	60	40	IFS1<28>	IEC1<28>	IPC10<4:2>	IPC10<1:0>	No	
DMA1 – DMA Channel 1	61	41	IFS1<29>	IEC1<29>	IPC10<12:10>	IPC10<9:8>	No	
DMA2 – DMA Channel 2	62	42	IFS1<30>	IEC1<30>	IPC10<20:18>	IPC10<17:16>	No	
DMA3 – DMA Channel 3	63	43	IFS1<31>	IEC1<31>	IPC10<28:26>	IPC10<25:24>	No	
		Lowes	st Natural O	rder Priority				

Note 1: Not all interrupt sources are available on all devices. See TABLE 1: "PIC32MX1XX 28/44-Pin XLP (General Purpose) Family Features" and TABLE 2: "PIC32MX2XX 28/44-Pin XLP (USB) Family Features" for the lists of available peripherals.

7.1 Interrupt Control Registers

TABLE 7-2: INTERRUPT REGISTER MAP

ess		Bit Range		Bits															
Virtual Address (BF88_#)	Register Name ⁽¹⁾		31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1000	INTCON	31:16	_	_	_	_	-	_	_	_	_	_	_	_	_	_	_	_	0000
1000	INTOON	15:0	_	_	_	MVEC	1		TPC<2:0>		_	_	_	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT ⁽³⁾	31:16	_		_	_	I	1	_	1	_	_	_	-	_	_		_	0000
1010	INTOTAL	15:0	_	_	_	_	1		SRIPL<2:0> — —				VEC<5:0>						0000
1020	IPTMR	31:16		IPTMR<31:0>															0000
1020	II TIVIIX	15:0	000 OO														0000		
1030	IFS0	31:16	FCEIF	RTCCIF	FSCMIF	AD1IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
1030	11 30	15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INTOIF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	0000
1040	11 31	15:0	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USBIF ⁽²⁾	CMP3IF	CMP2IF	CMP1IF	0000
1060	IEC0	31:16	FCEIE	RTCCIE	FSCMIE	AD1IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
1000	ILCO	15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INTOIE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	0000
1070	ILC1	15:0	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USBIE ⁽²⁾	CMP3IE	CMP2IE	CMP1IE	0000
1090	IPC0	31:16	1		_	INT0IP<2:0>			INT0IS<1:0>		_	_	_	CS1IP<2:0>			CS1IS<1:0>		0000
1090	IFCU	15:0	-	1	_		CS0IP<2:0>		CS0IS<1:0>		_	_	_	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	_	_	_	INT1IP<2:0>			INT1IS<1:0>		_	_	_	OC1IP<2:0>			OC1IS<1:0>		0000
TUAU	IFCT	15:0	_		_	IC1IP<2:0>			IC1IS<1:0>		_	_	_	T1IP<2:0>		T1IS<1:0>		0000	
1000	IPC2	31:16	_	_	_	INT2IP<2:0>			INT2IS<1:0>		_	_	_	OC2IP<2:0>		OC2IS<1:0>		0000	
10B0	IPC2	15:0	_	_	_		IC2IP<2:0>		IC2IS<1:0>		_	_	_	T2IP<2:0>		T2IS<1:0>		0000	
1000	IPC3	31:16		_	_	INT3IP<2:0>			INT3IS<1:0>		_	_	_	OC3IP<2:0>		OC3IS<1:0>		0000	
10C0	IPC3	15:0		_	_		IC3IP<2:0>		IC3IS<1:0>		_	_	_	T3IP<2:0>		T3IS<1:0>		0000	
1000	IPC4	31:16 — — INT4IP<2:0>			INT4IS<1:0>		_	_	_	OC4IP<2:0>		OC4IS<1:0>		0000					
10D0	IPC4	15:0	_	_	_	IC4IP<2:0>			IC4IS<1:0>		_	_	_	T4IP<2:0>		T4IS<1:0>		0000	
1000	IDCE	31:16	_	_	_	AD1IP<2:0>			AD1IS<1:0>		_	_	_	OC5IP<2:0>		OC5IS<1:0>		0000	
10E0	IPC5	15:0	_	-	_	IC5IP<2:0>			IC5IS<1:0>		_	_	_	T5IP<2:0>		T5IS<1:0>		0000	
1050	IDCe	31:16	_	_	_	(CMP1IP<2:0>	•	CMP1IS	S<1:0>	_	_	_	FCEIP<2:0>			FCEIS	S<1:0>	0000
10F0 IP0	IPC6	15:0	_	-	_	F	RTCCIP<2:0>			RTCCIS<1:0>		_	_	FSCMIP<2:0>		FSCMIS<1:0>		0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

^{2:} These bits are not available on PIC32MX1XX devices.

^{3:} This register does not have associated CLR, SET, INV registers.

TABLE 7-2: INTERRUPT REGISTER MAP (CONTINUED)

ess		ø								Bits									
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1100	IPC7	31:16	_	_	_		SPI1IP<2:0>		SPI1IS	i<1:0>	_	_	_	U	SBIP<2:0> ⁽²	2)	USBIS-	<1:0> ⁽²⁾	0000
1100	IPC/	15:0		_	_	(CMP3IP<2:0>	•	CMP3IS	S<1:0>	_	_	_	С	MP2IP<2:0:	>	CMP2I	S<1:0>	0000
1110	IPC8	31:16		_	_		PMPIP<2:0>		PMPIS	<1:0>	_	_	_	(CNIP<2:0>		CNIS	<1:0>	0000
1110	IPC8	15:0		_	_		I2C1IP<2:0>		I2C1IS	<1:0>	_	_	_		U1IP<2:0>		U1IS	<1:0>	0000
1120	IPC9	31:16		_	_	(CTMUIP<2:0	•	CTMUIS	S<1:0>	_	_	_	12	2C2IP<2:0>		12C2IS	S<1:0>	0000
1120	IFC9	15:0		_	_		U2IP<2:0>		U2IS<	<1:0>	_	_	_	S	PI2IP<2:0>		SPI2IS	S<1:0>	0000
1120	IPC10	31:16	_	_	_	I	DMA3IP<2:0>	•	DMA3IS	S<1:0>	_	_	_	D	MA2IP<2:0:	>	DMA2I	S<1:0>	0000
1130	IFC IU	15:0	_	_	-		DMA1IP<2:0>	,	DMA1IS	S<1:0>	-	_	_	D	MA0IP<2:0:	>	DMA0I	S<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

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- 2: These bits are not available on PIC32MX1XX devices.
- 3: This register does not have associated CLR, SET, INV registers.

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_		_	_	1	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	_	_	_		_	_
45.0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
15:8	_	_	_	MVEC	_		TPC<2:0>	
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0' bit 15-13 **Unimplemented:** Read as '0'

bit 12 MVEC: Multi Vector Configuration bit

1 = Interrupt controller configured for Multi-vectored mode
 0 = Interrupt controller configured for Single-vectored mode

bit 11 Unimplemented: Read as '0'

bit 10-8 TPC<2:0>: Interrupt Proximity Timer Control bits

111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer 110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer 101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer 100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer 111 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer 110 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer

001 = Interrupts of group priority 1 start the Interrupt Proximity timer

000 = Disables Interrupt Proximity timer

bit 7-5 Unimplemented: Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge0 = Falling edge

bit 3 INT3EP: External Interrupt 3 Edge Polarity Control bit

1 = Rising edge0 = Falling edge

bit 2 INT2EP: External Interrupt 2 Edge Polarity Control bit

1 = Rising edge 0 = Falling edge

bit 1 INT1EP: External Interrupt 1 Edge Polarity Control bit

1 = Rising edge 0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit

1 = Rising edge0 = Falling edge

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_			_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	_	_	-		_	_
15.0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	_	_	_	_	_	S	SRIPL<2:0> ⁽¹⁾	
7.0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_			VEC	<5:0> ⁽¹⁾		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

bit 10-8 SRIPL<2:0>: Requested Priority Level bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0' bit 5-0 **VEC<5:0>:** Interrupt Vector bits⁽¹⁾

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24				IPTMF	<31:24>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10				IPTMF	?<23:16>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.6				IPTMI	R<15:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				IPTM	R<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS09	IFS08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 IFS31-IFS00: Interrupt Flag Status bits

1 = Interrupt request has occurred

0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.6	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 IEC31-IEC00: Interrupt Enable bits

1 = Interrupt is enabled0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	_	_	_		IP03<2:0>		IS03	<1:0>
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	_	_	_		IP02<2:0>		IS02	<1:0>
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
13.6	_	_	_		IP01<2:0>		IS01	<1:0>
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	_	_	_		IP00<2:0>		IS00-	<1:0>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-29 Unimplemented: Read as '0'

bit 28-26 IP03<2:0>: Interrupt Priority bits

111 = Interrupt priority is 7

:

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 IS03<1:0>: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 Unimplemented: Read as '0'

bit 20-18 IP02<2:0>: Interrupt Priority bits

111 = Interrupt priority is 7

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 IS02<1:0>: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 Unimplemented: Read as '0'

bit 12-10 IP01<2:0>: Interrupt Priority bits

111 = Interrupt priority is 7

•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)

```
bit 9-8
           IS01<1:0>: Interrupt Subpriority bits
           11 = Interrupt subpriority is 3
           10 = Interrupt subpriority is 2
           01 = Interrupt subpriority is 1
           00 = Interrupt subpriority is 0
bit 7-5
           Unimplemented: Read as '0'
bit 4-2
           IP00<2:0>: Interrupt Priority bits
           111 = Interrupt priority is 7
           010 = Interrupt priority is 2
           001 = Interrupt priority is 1
           000 = Interrupt is disabled
bit 1-0
           IS00<1:0>: Interrupt Subpriority bits
           11 = Interrupt subpriority is 3
           10 = Interrupt subpriority is 2
           01 = Interrupt subpriority is 1
           00 = Interrupt subpriority is 0
```

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

8.0 OSCILLATOR CONFIGURATION

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX XLP family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the "PIC32 Family Reference Manual", which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX1XX/2XX XLP oscillator system has the following modules and features:

- A total of five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery
- Dedicated On-Chip PLL for USB modules
- · Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

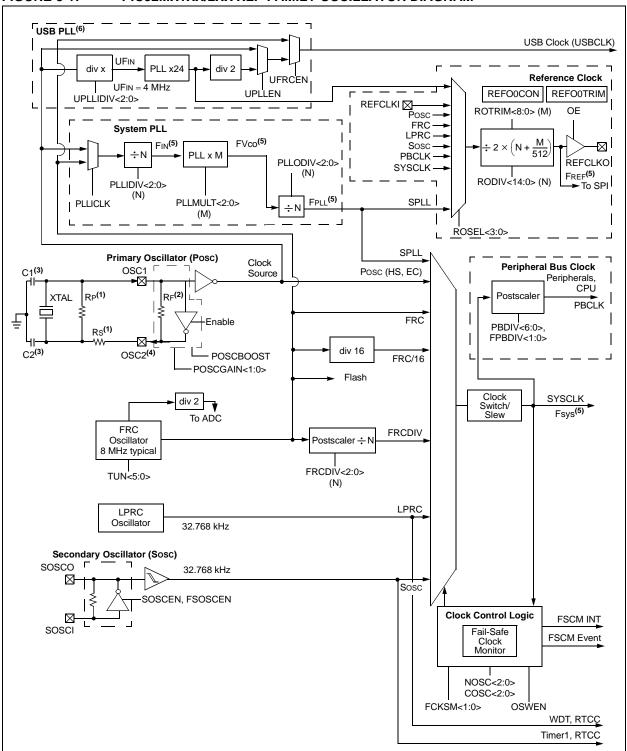
A block diagram of the oscillator system is provided in Figure 8-1.

8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MX1XX/2XX XLP oscillator system includes a Fail-safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the BFRC oscillator and triggers a NMI. The BFRC is an untuned 8 MHz oscillator that will drive the SYSCLK during FSCM event. When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode both the SYSCLK and the FSCM halt, which prevents FSCM detection.

FIGURE 8-1: PIC32MX1XX/2XX XLP FAMILY OSCILLATOR DIAGRAM



Notes: 1. A series resistor, Rs, may be required for AT strip cut crystals, or to eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.

- 2. The internal feedback resistor, RF, is typically in the range of 2 to 10 M Ω .
- 3. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for help in determining the best oscillator components.
- 4. PB0CLK divided by 2 is available on the OSC2 pin in certain clock modes.
- 5. Refer to Table 33-19 in 33.0 "Electrical Characteristics" for frequency limitations.
- 6. The USB PLL is only available on PIC32MX2XX XLP devices.

8.2 Oscillator Control Registers

TABLE 8-1: OSCILLATOR CONFIGURATION REGISTER MAP

SS											Bits								_
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets ⁽¹⁾
F000	OSCCON	31:16	_		_		_	F	FRCDIV<2:0	>	DRMEN	_	SLP2SPD	_		_		_	0020
F000	OSCCON	15:0		(COSC<2:0>		_		NOSC<2:0>		CLKLOCK	_	_	SLPEN	CF	UFRCEN	SOSCEN	OSWEN	xx0x
F010	OSCTUN	31:16	_	1	_	_	_	_	_	_	_	_	_	_	1	_	_	_	0000
F010	OSCIUN	15:0	_	1	_	-	_	_	_	_	_	_			TU	N<5:0>		•	00xx
F020	SPLLCON	31:16	_	1	_	-	_	P	LLODIV<2:0	>	_	_	_	_	_	ı	PLLMULT<2:0>	•	01xx
FU2U	SPLLCON	15:0	_	_	_	_	_	F	PLLIDIV<2:0	>	PLLICLK	_	_	_	_	_	_	_	0x0x
F030	UPLLCON	31:16	_	_	_	_	_	UP	LLODIV<2:0	> ⁽¹⁾	_	_	_	_	_	U	PLLMULT<2:0	>	01xx
F030	UPLLCON	15:0	_	_	_	_	_	UF	PLLIDIV<2:0:	_{>} (1)	_	_	_		_	_	_	_	0x0x
E090	REFO0CON	31:16	_								RODIV<14:0)>							0000
F000	KEFOOCON	15:0	ON	_	SIDL	OE	RSLP	_	DIVSWEN	ACTIVE	_	_	_	_		ROS	EL<3:0>		0000
E000	REFO0TRIM	31:16					ROTRIM<8:0	>				_	_	_	_	_	_	_	0000
F090	KEFOOTKIN	15:0	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
F0A0	PB0DIV	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FUAU	FBUDIV	15:0	_	_	_	_	PBDIVRDY	_	_	_	_				PBDIV<6:0)>			8801
F0C0	CLKSTAT	31:16	_	_	_	_	_	_	_	_	_	_	_		_	_	_	_	0000
FUCU	CLNSIAI	15:0	_	_	_	_	_	_	_	UPLLRDY	SPLLRDY	_	LPRCRDY	SOSCRDY		POSCRDY	SPLLRDY	FRCRDY	0000

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

lote 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
31:24	_	-		-	1	F	FRCDIV<2:0>	
22.40	R/W-0	U-0	R/W-y	U-0	U-0	U-0	U-0	U-0
23:16	DRMEN	_	SLP2SPD	_	_	_	_	_
45.0	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
15:8	_		COSC<2:0>				NOSC<2:0>	
7.0	R/W-0	U-0	U-0	R/W-0	R/W-0, HS	R/W-y	R/W-y	R/W-y
7:0	CLKLOCK	_	_	SLPEN	CF	UFRCEN	SOSCEN	OSWEN ⁽¹⁾

Legend:y = Value set from Configuration bits on PORHS = Hardware SetR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-27 Unimplemented: Read as '0'

bit 26-24 FRCDIV<2:0>: Internal Fast RC (FRC) Oscillator Clock Divider bits

111 = FRC divided by 256

110 = FRC divided by 64

101 = FRC divided by 32

100 = FRC divided by 16

011 = FRC divided by 8 010 = FRC divided by 4

001 = FRC divided by 2

000 = FRC divided by 1 (default setting)

bit 23 DRMEN: Dream Mode Enable bit

1 = Dream mode is enabled

0 = Dream mode is disabled

bit 22 Unimplemented: Read as '0'

bit 21 SLP2SPD: Sleep Two-speed Start-up Control bit

1 = Use FRC as SYSCLK until the selected clock is ready

0 = Use the selected clock directly

bit 20-15 Unimplemented: Read as '0'

bit 14-12 COSC<2:0>: Current Oscillator Selection bits

111 = Reserved

110 = Reserved

101 = Internal Low-Power RC (LPRC) Oscillator

100 = Secondary Oscillator (Sosc)

011 = Reserved

010 = Primary Oscillator (Posc) (HS or EC)

001 = System PLL (SPLL)

000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

bit 11 Unimplemented: Read as '0'

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Reserved
 - 110 = Reserved
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Reserved
 - 010 = Primary Oscillator (Posc) (HS or EC)
 - 001 = System PLL (SPLL)
 - 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (DEVCFG1<2:0>).

- bit 7 CLKLOCK: Clock Selection Lock Enable bit
 - 1 = Clock and PLL selections are locked
 - 0 = Clock and PLL selections are not locked and may be modified
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 SLPEN: Sleep Mode Enable bit
 - 1 = Device will enter Sleep mode when a WAIT instruction is executed
 - 0 = Device will enter Idle mode when a WAIT instruction is executed
- - 1 = FSCM has detected a clock failure
 - 0 = No clock failure has been detected
- bit 2 UFRCEN: USB FRC Clock Enable bit
 - 1 = Enable FRC as the USB clock source
 - 0 = Use the Primary Oscillator or UPLL as the USB clock source
- bit 1 SOSCEN: Secondary Oscillator (Sosc) Enable bit
 - 1 = Enable Secondary Oscillator
 - 0 = Disable Secondary Oscillator
- bit 0 **OSWEN:** Oscillator Switch Enable bit⁽¹⁾
 - 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
 - 0 = Oscillator switch is complete
- **Note 1:** The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	-	1	_	_
22.46	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	-	_	_
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	-	_	_
7.0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_			TUN<	5:0> ⁽¹⁾		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-6 Unimplemented: Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits⁽¹⁾

100000 = Center frequency -2%

100001 =

•

•

111111 =

000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

000001 =

•

•

011110 =

011111 = Center frequency +2%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.

REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
31:24	_	_	1		_	F	PLLODIV<2:0	>
00.40	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
23:16	_	_	_	_	_	F	PLLMULT<2:0	>
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
15.6	_	_	_	_	_		PLLIDIV<2:0>	•
7.0	R/W-y	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	PLLICLK	_	1	1	_	_	1	1

Legend:y = Value set from Configuration bits on PORR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-27 Unimplemented: Read as '0'

bit 26-24 PLLODIV<2:0>: System PLL Output Clock Divider bits

111 = PLL Divide by 16

110 = PLL Divide by 12

101 = PLL Divide by 8

100 = PLL Divide by 6

011 = PLL Divide by 4

010 = PLL Divide by 3 001 = PLL Divide by 2

000 = PLL Divide by 1

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 30-3 in **30.0 "Special Features"** for information.

bit 23-19 Unimplemented: Read as '0'

bit 18-16 PLLMULT<2:0>: System PLL Multiplier bits

111 = Multiply by 24

110 = Multiply by 21

101 = Multiply by 20

100 = Multiply by 19

011 = Multiply by 18

010 = Multiply by 17

001 = Multiply by 16

000 = Multiply by 15

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 30-3 in 30.0 "Special Features" for information.

bit 15-11 Unimplemented: Read as '0'

- Note 1: Writes to this register require an unlock sequence. Refer to **Section 42**. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.
 - 2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

bit 10-8 PLLIDIV<2:0>: System PLL Input Clock Divider bits

111 = Divide by 12 110 = Divide by 10 101 = Divide by 6 100 = Divide by 5 011 = Divide by 4 010 = Divide by 3 001 = Divide by 2

000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 30-3 in 30.0 "Special Features" for information. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set to Divide-by-1.

bit 7 PLLICLK: System PLL Input Clock Source bit

1 = FRC is selected as the input to the System PLL

0 = Posc is selected as the input to the System PLL

The POR default is specified by the FPLLICLK Configuration bit in the DEVCFG2 register. Refer to Register 30-3 in **30.0** "Special Features" for information.

bit 6-0 Unimplemented: Read as '0'

- Note 1: Writes to this register require an unlock sequence. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.
 - 2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

REGISTER 8-4: UPLLCON: USB PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
31:24	-	-	_	_	_	U	PLLODIV<2:0)>
22.40	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
23:16	-	-	_	_	_	U	PLLMULT<2:0)>
15.0	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
15:8	-	-	_	_	_	L	JPLLIDIV<2:0	>
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0						_		

Legend:y = Value set from Configuration bits on PORR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

```
bit 31-27 Unimplemented: Read as '0'
```

bit 26-24 UPLLODIV<2:0>: USB PLL Output Clock Divider bits

111 = PLL Divide by 16

110 = PLL Divide by 12

101 = PLL Divide by 8

100 = PLL Divide by 6

011 = PLL Divide by 4

010 = PLL Divide by 3

001 = PLL Divide by 2

000 = PLL Divide by 1

bit 23-19 Unimplemented: Read as '0'

bit 18-16 UPLLMULT<2:0>: USB PLL Multiplier bits

111 = Multiply by 24

110 = Multiply by 21

101 = Multiply by 20

100 = Multiply by 19

011 = Multiply by 18

010 = Multiply by 17

001 = Multiply by 16

000 = Multiply by 15

bit 15-11 Unimplemented: Read as '0'

bit 10-8 UPLLIDIV<2:0>: USB PLL Input Clock Divider bits

111 = Divide by 12

110 = Divide by 10

101 = Divide by 6

100 = Divide by 5

011 = Divide by 4

010 = Divide by 3

001 = Divide by 3

000 = Divide by 1

bit 7-0 Unimplemented: Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to Section 42. "Oscillators with Enhanced PLL" (DS60001250) in the "PIC32 Family Reference Manual" for details.

REGISTER 8-5: REFO0CON: REFERENCE OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	_			I	RODIV<14:8	>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10				RODI\	/<7:0>			
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
15:8	ON ⁽¹⁾	-	SIDL	OE	RSLP ⁽²⁾	-	DIVSWEN	ACTIVE ⁽¹⁾
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0						ROSEL	<3:0> ⁽³⁾	

Legend:HC = Hardware ClearedHS = Hardware SetR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31 Unimplemented: Read as '0'

bit 30-16 RODIV<14:0> Reference Clock Divider bits

The value selects the reference clock divider bits (see Figure 8-1 for details). A value of '0' selects no divider.

bit 15 ON: Output Enable bit⁽¹⁾

1 = Reference Oscillator Module enabled

0 = Reference Oscillator Module disabled

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Peripheral Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on REFCLKOx pin

0 = Reference clock is not driven out on REFCLKOx pin

bit 11 RSLP: Reference Oscillator Module Run in Sleep bit⁽²⁾

1 = Reference Oscillator Module output continues to run in Sleep

0 = Reference Oscillator Module output is disabled in Sleep

bit 10 Unimplemented: Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress

0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit⁽¹⁾

1 = Reference clock request is active

0 = Reference clock request is not active

bit 7-4 Unimplemented: Read as '0'

bit 3-0 ROSEL<3:0>: Reference Clock Source Select bits(3)

1111 = Reserved

:

1001 = Reserved

1000 = REFCLKI

0111 = System PLL output

0110 = USB PLL output

0101 = Sosc

0100 = LPRC

0011 = FRC

0010 = Posc

0001 = PBCLK

0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.

2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 8-6: REFOOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24				ROTRIN	√8:1>			
00.40	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	ROTRIM<0>	_	_	_	_	_	_	_
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	-
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_	_	_	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-23 ROTRIM<8:0>: Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value 111111110 = 510/512 divisor added to RODIV value

•

•

100000000 = 256/512 divisor added to RODIV value

•

•

000000010 = 2/512 divisor added to RODIV value

000000001 = 1/512 divisor added to RODIV value 000000000 = 0 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '0'

- **Note 1:** While the ON bit (REFO0CON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.
 - 2: Do not write to this register when the ON bit (REFO0CON<15>) is not equal to the ACTIVE bit (REFO0CON<8>).
 - 3: Specified values in this register do not take effect if RODIV<14:0> bits (REFO0CON<30:16>) = 0.

REGISTER 8-7: PB0DIV: PERIPHERAL BUS CLOCK 0 DIVISOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_		1	-	1
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	-	_	-
45.0	U-0	U-0	U-0	U-0	R-1	U-0	U-0	U-0
15:8	_	_	_	_	PBDIVRDY	-	_	-
7.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
7:0	_	_	_	_	_	_	PBDIV	/<1:0>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-12 Unimplemented: Read as '0'

bit 11 PBDIVRDY: Peripheral Bus 'x' Clock Divisor Ready bit

1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written

0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-2 Unimplemented: Read as '0'

bit 1-0 **PBDIV<1:0>:** Peripheral Bus 'x' Clock Divisor Control bits

11 = PBCLKx is SYSCLK divided by 8 10 = PBCLKx is SYSCLK divided by 4

01 = PBCLKx is SYSCLK divided by 2 00 = PBCLKx is SYSCLK divided by 1

Note: Writes to this register require an unlock sequence. Refer to Section 42. "Oscillators with Enhanced PLL"

(DS60001250) in the "PIC32 Family Reference Manual" for details.

REGISTER 8-8: CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	_	_	-		1
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
15:8	_	_	_	_	_	_	_	UPLLRDY
7.0	R-0	U-0	R-0	R-0	U-0	R-0	R-0	R-0
7:0	SPLLRDY	_	LPRCRDY	SOSCRDY	_	POSCRDY	DIVSPLLRDY	FRCRDY

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-9 Unimplemented: Read as '0'

bit 8 UPLLRDY: USB PLL (UPLL) Ready Status bit

1 = UPLL is ready 0 = UPLL is not ready

bit 7 SPLLRDY: System PLL (SPLL) Ready Status bit

1 = SPLL is ready0 = SPLL is not ready

bit 6 Unimplemented: Read as '0'

bit 5 LPRCRDY: Low-Power RC (LPRC) Oscillator Ready Status bit

1 = LPRC is stable and ready

0 = LPRC is disabled or not operating

bit 4 SOSCRDY: Secondary Oscillator (Sosc) Ready Status bit

1 = Sosc is stable and ready

0 = Sosc is disabled or not operating

bit 3 Unimplemented: Read as '0'

bit 2 POSCRDY: Primary Oscillator (Posc) Ready Status bit

1 = Posc is stable and ready

0 = Posc is disabled or not operating

bit 1 DIVSPLLRDY: Divided System PLL Ready Status bit

1 = Divided System PLL is ready0 = Divided System PLL is not ready

bit 0 FRCRDY: Fast RC (FRC) Oscillator Ready Status bit

1 = FRC is stable and ready

0 = FRC is disabled for not operating

REGISTER 8-9: CLKDIAG: USER CLOCK DIAGNOSTIC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	-	1		_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	-	_	_	_
7.0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	UPLLSTOP	SPLLSTOP	LPRCSTOP	FRCSTOP	SOSCSTOP	POSCSTOP

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-6 Unimplemented: Read as '0'

bit 5 UPLLSTOP: USB PLL (UPLL) Clock Stop Control Value bit

1 = UPLL clock source is stopped 0 = UPLL clock source runs as normal

bit 4 SPLLSTOP: System PLL (SPLL) Clock Stop Control Value bit

1 = SPLL clock source is stopped 0 = SPLL clock source runs as normal

bit 3 LPRCSTOP: Low-Power RC Oscillator (LPRC) Clock Stop Control Value bit

1 = LPRC clock source is stopped 0 = LPRC clock source runs as normal

bit 2 FRCSTOP: Fast RC Oscillator (FRC) Clock Stop Control Value bit

1 = FRC clock source is stopped 0 = FRC clock source runs as normal

bit 1 SOSCSTOP: Secondary Oscillator (Sosc) Clock Stop Control Value bit

1 = Sosc clock source is stopped 0 = Sosc clock source runs as normal

bit 0 POSCSTOP: Primary Oscillator (Posc) Clock Stop Control Value bit

1 = Posc clock source is stopped0 = Posc clock source runs as normal

9.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 31. "Direct Memory Access (DMA) Controller" (DS60001117), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

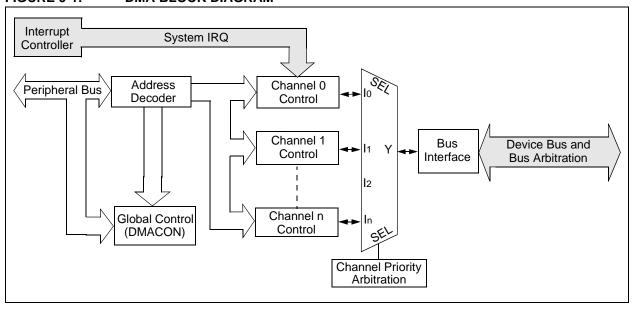
The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32, such as Peripheral Bus devices: SPI, UART, PMP, etc., or memory itself. Figure 9-1 show a block diagram of the DMA Controller module.

The DMA Controller module has the following key features:

- · Four identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination

- · Fixed priority channel arbitration
- Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt)
 DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- · CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable





9.1 DMA Control Registers

TABLE 9-1: DMA GLOBAL REGISTER MAP

ess		0								Bi	ts								ž.
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
2000	DMACON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3000	DIVIACON	15:0	ON	_	_	SUSPEND	DMABUSY	_	_	_	_	_	_	_	_	_	_	_	0000
2010	DMASTAT	31:16		_	-	_	_	_	1	-	_	_	_	_	_	-	_		0000
3010	DIVIASTAT	15:0	_	1	1		_	_	I	I	_	_	_	-	RDWR	DI	MACH<2:0>	(2)	0000
3020	DMAADDR	31:16								DMAADD	D-31·0>								0000
3020	DIVIARDUR	15:0								DIVIAADL	/1\<01.0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information

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TABLE 9-2: DMA CRC REGISTER MAP

ess										Bi	ts				_	_			
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2020	DCRCCON	31:16	_	_	BYTO	<1:0>	WBO	_	_	BITO	_	_	_	_	_	_	_	_	0000
3030	DCRCCON	15:0	_	_	_			PLEN<4:0>			CRCEN	CRCAPP	CRCTYP	_	_	С	RCCH<2:0	>	0000
2040	DCRCDATA	31:16								DCRCDA	TA -21:05								0000
3040	DURUDATA	15:0								DURUDA	1A<31:0>								0000
2050	DCRCXOR	31:16	•	•	•	•	•		•	DCRCXC	D -21:0>				•			•	0000
3030	DCKCXOK	15:0								DCRCXC	VK<01:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

DS6	
JS60001	
140z	
1404A-page	
age	
95	

sse										Ві	ts								
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	DCH0CON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_		_	_	0000
3060	DCHUCON	15:0	CHBUSY		_	_	_	_	_	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	_	CHEDET	CHPR	I<1:0>	0000
3070	DCH0ECON	31:16	_	_	_	_	_	_	_	_				CHAIR	Q<7:0>				00FF
3070	DOI IOLOOIY	15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	_	_	_	FF00
3080	DCH0INT	31:16	_		_	_	_		_		CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
	20	15:0	_		_	_	_	_	_	_	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3090	DCH0SSA	31:16 15:0								CHSSA	<31:0>								0000
		31:16																	0000
30A0	DCH0DSA	15:0								CHDSA	N<31:0>								0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
30B0	DCH0SSIZ	15:0								CHSSIZ	Z<15:0>								0000
2000	DOLIODOI7	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3000	DCH0DSIZ	15:0	•		•		•		•	CHDSIZ	Z<15:0>		•					•	0000
2000	DCLIGCDED	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3000	DCH0SPTR	15:0								CHSPTI	R<15:0>								0000
20E0	DCH0DPTR	31:16		_	_	1		1	_	_	1	I	_	1	1	1	1		0000
JULU	DOTTODETT	15:0								CHDPTI	R<15:0>								0000
30F0	DCH0CSIZ	31:16	_		_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
001 0	DOI 100012	15:0								CHCSIZ	Z<15:0>								0000
3100	DCH0CPTR	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0.00		15:0								CHCPTI	R<15:0>								0000
3110	DCH0DAT	31:16	_		_	_	_		_	_	_	_	_		_	_	_	_	0000
		15:0	_											CHPDA					0000
3120	DCH1CON	31:16	_			_		_							_		_	_	0000
		15:0	CHBUSY							CHCHNS	CHEN	CHAED	CHCHN	CHAEN		CHEDET	CHPR	l<1:0>	0000
3130	DCH1ECON	31:16	_		_	-		_	_	_	050005	CARORT	DATEN	CHAIR					00FF
		15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	-	OLITAIE	- CLIEDIE	FF00
3140	DCH1INT	31:16 15:0	_		_		_		_	_	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE CHERIF	0000
		31:16	_	_	_	_	_	_	_	_	CHODIF	СПОПІР	CHUDIF	CUDUIL	CUBCIL	CHCCIF	CHIAIF	CHEKIF	0000
3150	DCH1SSA	15:0								CHSSA	<31:0>								0000
		31:16																	0000
3160	DCH1DSA	15:0								CHDSA	<31:0>								0000
		15.0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

SS										Bi	ts								
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0470	DOL14 0017	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3170	DCH1SSIZ	15:0								CHSSIZ	'<15:0>								0000
3180	DCH1DSIZ	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3100	DOITIDGIZ	15:0								CHDSIZ	′ <15:0>								0000
3190	DCH1SPTR	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0100		15:0								CHSPTF	R<15:0>								0000
31A0	DCH1DPTR	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0.7.10		15:0							1	CHDPT	R<15:0>							1	0000
31B0	DCH1CSIZ	31:16	_	_	_	_	_		_	_	_	_	_	_	_	_		_	0000
		15:0								CHCSIZ									0000
31C0	DCH1CPTR	31:16	_	_	_	_	_		_			_	_	_	_	_		_	0000
		15:0								CHCPT	₹<15:0>								0000
31D0	DCH1DAT	31:16			_				_	_	_	_	_			_		_	0000
		15:0		_	_	_	_		_	_				CHPDA					0000
31E0	DCH2CON	31:16	— —		_	_			_	-	- CUEN		— —	— CHAEN		- CHEDET		-	0000
		15:0 31:16	CHBUSY		_				_	CHCHNS	CHEN	CHAED	CHCHN	CHAEN		CHEDET	CHPR	1<1:0>	0000
31F0	DCH2ECON	15:0	_		_	CHSIR			_	_	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	_		_	00FF FF00
		31:16	_	_	_	—	Q<1.0>	_	_	_	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
3200	DCH2INT	15:0									CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIE	CHCCIF	CHTAIF	CHERIF	0000
		31:16									OHODII	OHOHII	OHDDII	OHDHIII	OFIDOR	Orioon	OTTIVAL	OFFERM	0000
3210	DCH2SSA	15:0								CHSSA	<31:0>								0000
		31:16																	0000
3220	DCH2DSA	15:0								CHDSA	<31:0>								0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3230	DCH2SSIZ	15:0								CHSSIZ	' <15:0>								0000
20.45	D 01 10 D 0: -	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3240	DCH2DSIZ	15:0								CHDSIZ	2 <15:0>								0000
2050	DOLLOODED	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3250	DCH2SPTR	15:0								CHSPTE	R<15:0>								0000
2260	DCUSDDID	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3260	DCH2DPTR	15:0								CHDPT	R<15:0>								0000
3270	DCH2CSIZ	31:16	_	_	_	_	_		_	_	_	_	_	_	_	_	_	_	0000
3210	DONZOSIZ	15:0								CHCSIZ	' <15:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

TABLE 9-3:

3330 DCH3CSIZ 31:16 — — — — — — — — — — — — — — — — — — —	3320 DCH3DPTR 15:0 CHDPTR<15:0> 000																			
3330 DCH3CSIZ 31:16 — — — — — — — — — — — — — — — — — — —	3330 DCH3CSIZ 31:16 — — — — — — — — — — — — — — — — — — —	2220	DCH3DDTB	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_		- 000
DCH3CSIZ 15:0 CHCSIZ<15:0> 0000	CHCSIZ< 15:0 CHCSIZ< 15:0 CHCSIZ< 15:0 OCC	3320	DCI ISDF TK	15:0								CHDPT	R<15:0>							000
15:0 CHCSIZ<15:0> 0000 3340 DCH3CPTR	15:0 CHCSIZ<15:0> 000 3340 DCH3CPTR	2220	DCH3CSIZ	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_ -	- 000
3350 DCH3DAT 31:16 — — — — — — — — — — — — — — — — — — —	3350 DCH3DAT 31:16 — — — — — — — — — — — — — — — — — — —											CHCSIZ	Z<15:0>							000
3350 DCH3DAT 31:16 — — — — — — — — — — — — — — — — — — —	3350 DCH3DAT 31:16 — — — — — — — — — — — — — — — — — — —	2240	DCLISCOTO	31:16	_		_	_	_	_	_	_	_	_	_	_	_	_		- 000
3350 DCH3DAT 15:0 — — — — — — — — — — — — — — — — — — —	3350 DCH3DAT 15:0 — — — — — — — — — — — — — — — — — — —	3340	DCH3CPTR	15:0	•							CHCPT	R<15:0>							000
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more	Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more	2250	DCUADAT	31:16	_		_	_	_	_	_	_	_	_	_	_	_	_		- 000
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more	Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more	3350	DCH3DAI	15:0	_	_	_	_	_	_	_	_		•	•	CHPD	AT<7:0>			000
								, -	Ü		i viituui aaa	iresses, piu	s offsets of (ux4, uxo ar	iu uxc, ies	Joodavory. O		, -		ioi illoic

ω _		4																	10
Virtual Addre (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
		31:16	_	-	_	_	_	_	-	_	_	_	-	1	-	-	-	_	0000
3280	DCH2CPTR	15:0								CHCPTI	R<15:0>								0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3290	DCH2DAT	15:0	_	_	_	_	_	_	_	_				CHPDA	T<7:0>				0000
	DOLLOGO 1	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
32A0	DCH3CON	15:0	CHBUSY	_	-	_	_	_	_	CHCHNS	CHEN	CHAED	CHCHN	CHAEN		CHEDET	CHPR	I<1:0>	0000
32B0	DCH3ECON	31:16	_	_	_	_	_	_	1	_				CHAIR	Q<7:0>				OOFF
3200	DOI ISLOON	15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	_		_	FF00
32C0	DCH3INT	31:16	_	_	_	_	_	_	_	_	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
3200	DOMINI	15:0	_	_	_	_	_	_	_	_	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16 15:0								CHSSA	\<31:0>								0000
32E0	DCH3DSA	31:16 15:0								CHDSA	\<31:0>								0000
	D.01100017	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		0000
32F0	DCH3SSIZ	15:0								CHSSIZ	Z<15:0>		<u> </u>						0000
2200	DCH3DSIZ	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3300	DCH3D3IZ	15:0								CHDSIZ	Z<15:0>								0000
3310	DCH3SPTR	31:16	_	_	_	_	_	_		_	_	_	_	_		_		_	0000
5510	DO11001 110	15:0				I				CHSPTI	R<15:0>							I	0000
3320	DCH3DPTR	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
	J	15:0								CHDPTI	R<15:0>								0000
		31.16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	nnnn

Bits

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DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

REGISTER 9-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_			_	_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	_	_	SUSPEND	DMABUSY	_	_	_
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** DMA On bit⁽¹⁾

1 = DMA module is enabled 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0' bit 12 **SUSPEND:** DMA Suspend bit

1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus

0 = DMA operates normally

bit 11 DMABUSY: DMA Module Busy bit

1 = DMA module is active

0 = DMA module is disabled and not actively transferring data

bit 10-0 Unimplemented: Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 9-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	-	_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
7:0	_	_	_	_	RDWR	[DMACH<2:0>	•

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0' bit 3 **RDWR:** Read/Write Status bit

1 = Last DMA bus access was a read0 = Last DMA bus access was a write

bit 2-0 DMACH<2:0>: DMA Channel bits

These bits contain the value of the most recent active DMA channel.

REGISTER 9-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.04	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
31:24				DMAADDF	?<31:24>								
22.40	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
23:16	DMAADDR<23:16>												
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
15:8	DMAADDR<15:8>												
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
7:0	DMAADDR<7:0>												

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 DMAADDR<31:0>: DMA Module Address bits

These bits contain the address of the most recent DMA access.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
31:24			BYTO	<1:0>	WBO ⁽¹⁾	-	_	BITO
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	_	_	_			PLEN<4:0>		
7.0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
7:0	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	_	_	(CRCCH<2:0>	•

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-28 BYTO<1:0>: CRC Byte Order Selection bits

- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)
- bit 27 WBO: CRC Write Byte Order Selection bit (1)
 - 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
 - 0 = Source data is written to the destination unaltered
- bit 26-25 Unimplemented: Read as '0'
- bit 24 BITO: CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = $\underline{1}$ (CRC module is in IP Header mode):

- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)
- bit 23-13 Unimplemented: Read as '0'
- bit 12-8 PLEN<4:0>: Polynomial Length bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

- bit 7 CRCEN: CRC Enable bit
 - 1 = CRC module is enabled and channel transfers are routed through the CRC module
 - 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

- bit 6 CRCAPP: CRC Append Mode bit⁽¹⁾
 - 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
 - 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5 **CRCTYP:** CRC Type Selection bit
 - 1 = The CRC module will calculate an IP header checksum
 - 0 = The CRC module will calculate a LFSR CRC
- bit 4-3 Unimplemented: Read as '0'
- bit 2-0 CRCCH<2:0>: CRC Channel Select bits
 - 111 = Reserved
 - 110 = Reserved
 - 101 = Reserved
 - 100 = Reserved
 - 011 = CRC is assigned to Channel 3
 - 010 = CRC is assigned to Channel 2
 - 001 = CRC is assigned to Channel 1
 - 000 = CRC is assigned to Channel 0
- Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 9-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
31.24	DCRCDATA<31:24>												
22.46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16	DCRCDATA<23:16>												
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
15:8	DCRCDATA<15:8>												
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7:0	DCRCDATA<7:0>												

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 DCRCDATA<31:0>: CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Bits greater than PLEN will return '0' on any read.

REGISTER 9-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
31:24	DCRCXOR<31:24>												
22,46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16	DCRCXOR<23:16>												
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
15:8	DCRCXOR<15:8>												
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7:0		DCRCXOR<7:0>											

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 DCRCXOR<31:0>: CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

- 1 = Enable the XOR input to the Shift register
- 0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		_	_				_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
15:8	CHBUSY	_	_	_	_	_	_	CHCHNS ⁽¹⁾
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
7:0	CHEN ⁽²⁾	CHAED	CHCHN	CHAEN	_	CHEDET	CHPF	RI<1:0>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 CHBUSY: Channel Busy bit

1 = Channel is active or has been enabled

0 = Channel is inactive or has been disabled

bit 14-9 Unimplemented: Read as '0'

bit 8 **CHCHNS**: Chain Channel Selection bit⁽¹⁾

1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)

0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 CHEN: Channel Enable bit(2)

1 = Channel is enabled

0 = Channel is disabled

bit 6 CHAED: Channel Allow Events If Disabled bit

1 = Channel start/abort events will be registered, even if the channel is disabled

0 = Channel start/abort events will be ignored if the channel is disabled

bit CHCHN: Channel Chain Enable bit

1 = Allow channel to be chained

0 = Do not allow channel to be chained

bit 4 CHAEN: Channel Automatic Enable bit

1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete

0 = Channel is disabled on block transfer complete

bit 3 Unimplemented: Read as '0'

bit 2 CHEDET: Channel Event Detected bit

1 = An event has been detected

0 = No events have been detected

bit 1-0 CHPRI<1:0>: Channel Priority bits

11 = Channel has priority 3 (highest)

10 = Channel has priority 2

01 = Channel has priority 1

00 = Channel has priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 9-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	_	_	_	_	_	_
22,46	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
23:16				CHAIRQ<	<7:0> ⁽¹⁾			
15.0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
15:8	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
7.0	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	_		_

Legend:S = Settable bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit 23-16 CHAIRQ<7:0>: Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•

•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 CHSIRQ<7:0>: Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

.

.

00000001 = Interrupt 1 will initiate a DMA transfer 00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 CFORCE: DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 CABORT: DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 PATEN: Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 SIRQEN: Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 AIRQEN: Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 Unimplemented: Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		_	_	-	_		_	_
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit 23 CHSDIE: Channel Source Done Interrupt Enable bit

1 = Interrupt is enabled

0 = Interrupt is disabled

bit 22 CHSHIE: Channel Source Half Empty Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 21 CHDDIE: Channel Destination Done Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 20 CHDHIE: Channel Destination Half Full Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 19 CHBCIE: Channel Block Transfer Complete Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 18 CHCCIE: Channel Cell Transfer Complete Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 17 CHTAIE: Channel Transfer Abort Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 16 CHERIE: Channel Address Error Interrupt Enable bit

1 = Interrupt is enabled0 = Interrupt is disabled

bit 15-8 Unimplemented: Read as '0'

bit 7 CHSDIF: Channel Source Done Interrupt Flag bit

1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)

0 = No interrupt is pending

bit 6 CHSHIF: Channel Source Half Empty Interrupt Flag bit

1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)

0 = No interrupt is pending

bit 5 CHDDIF: Channel Destination Done Interrupt Flag bit

1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)

0 = No interrupt is pending

REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
 - 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
 - 0 = No interrupt is pending
- bit 3 CHBCIF: Channel Block Transfer Complete Interrupt Flag bit
 - 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
 - 0 = No interrupt is pending
- bit 2 CHCCIF: Channel Cell Transfer Complete Interrupt Flag bit
 - 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
 - 0 = No interrupt is pending
- bit 1 CHTAIF: Channel Transfer Abort Interrupt Flag bit
 - 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
 - 0 = No interrupt is pending
- bit 0 CHERIF: Channel Address Error Interrupt Flag bit
 - 1 = A channel address error has been detected (either the source or the destination address is invalid)
 - 0 = No interrupt is pending

REGISTER 9-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
31:24				CHSSA<	31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16	CHSSA<23:16>												
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
15:8		CHSSA<15:8>											
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7:0		CHSSA<7:0>											

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 CHSSA<31:0> Channel Source Start Address bits

Channel source start address.

Note: This must be the physical address of the source.

REGISTER 9-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
31:24				CHDSA<	31:24>								
22.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16	CHDSA<23:16>												
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
15:8	CHDSA<15:8>												
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7:0	CHDSA<7:0>												

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 CHDSA<31:0>: Channel Destination Start Address bits

Channel destination start address.

Note: This must be the physical address of the destination.

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
			_	_	1		-	_	
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_	_	_	_	_	_	_	_	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	CHSSIZ<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	CHSSIZ<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSSIZ<15:0>: Channel Source Size bits

111111111111111 = 65,535 byte source size

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0000000000000010 = 2 byte source size

00000000000000001 = 1 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	_	_	_	_	_	_	_	_		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
	_	_	_	_	_	_	_	_		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	CHDSIZ<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	CHDSIZ<7:0>									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHDSIZ<15:0>: Channel Destination Size bits

111111111111111 = 65,535 byte destination size

•

00000000000000010 = 2 byte destination size

00000000000000001 = 1 byte destination size

REGISTER 9-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_	_	_	_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15:8				CHSPTR	<15:8>			
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				CHSPTF	R<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHSPTR<15:0>: Channel Source Pointer bits

111111111111111 = Points to byte 65,535 of the source

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0000000000000000 = Points to byte 1 of the source 000000000000000 = Points to byte 0 of the source

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24		_	_	_	-		-	-		
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	_	_	_	_	_	_	_	_		
15.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
15:8				CHDPTR	<15:8>					
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0		
7:0	CHDPTR<7:0>									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHDPTR<15:0>: Channel Destination Pointer bits

111111111111111 = Points to byte 65,535 of the destination

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REGISTER 9-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24		_	_	_	_		1	_		
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	_	_	_	_	_	_	_	_		
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8				CHCSIZ	<15:8>					
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	CHCSIZ<7:0>									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHCSIZ<15:0>: Channel Cell Size bits

111111111111111 = 65,535 bytes transferred on an event

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0000000000000010 = 2 bytes transferred on an event 0000000000000001= 1 byte transferred on an event

REGISTER 9-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	1		-	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
15:8				CHCPTR	<15:8>			
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				CHCPTF	R<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CHCPTR<15:0>: Channel Cell Progress Pointer bits

111111111111111 = 65,535 bytes have been transferred since the last event

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Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 9-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24	_	_	_	_		_	_	_		
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	_	_	_	_	_	_	_	_		
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15:8	_	_	_	_	_	_	_	_		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	CHPDAT<7:0>									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 CHPDAT<7:0>: Channel Data Register bits

Pattern Terminate mode:

Data to be matched must be stored in this register to allow a "terminate on match".

All other modes: Unused.

NOTES:

10.0 PREFETCH CACHE

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4.** "**Prefetch Cache**" (DS60001119), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

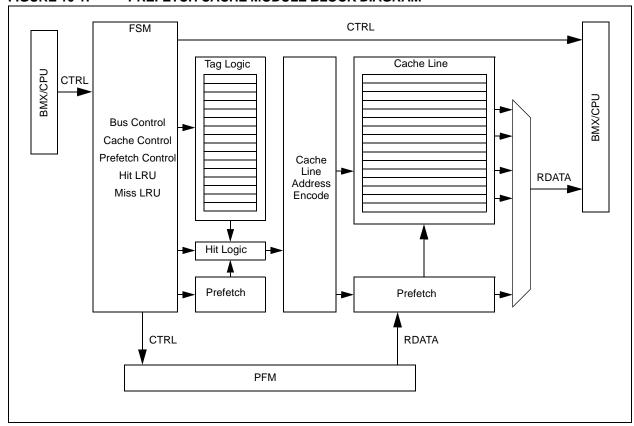
Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

The following are key features of the Prefetch Cache module:

- 16 fully associative lockable cache lines
- 16-byte cache lines
- · Up to four cache lines allocated to data
- Two cache lines with address mask to hold repeated instructions
- Pseudo LRU replacement policy
- · All cache lines are software writable
- 16-byte parallel memory fetch
- · Predictive instruction prefetch

A simplified block diagram of the Prefetch Cache module is illustrated in Figure 10-1.

FIGURE 10-1: PREFETCH CACHE MODULE BLOCK DIAGRAM



10.1 Control Registers

TABLE 10-1: PREFETCH REGISTER MAP

ess		-								Bit	s								
Virtual Address (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	CHECON ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	CHECOH	
1000	OFFICOR	15:0	_	_	_	_	_	_	DCSZ	ː<1:0>		_	PREFE	N<1:0>	_	P	PFMWS<2:0)>	0007
4010	CHEACC ⁽¹⁾	31:16	CHEWEN	_	_	-	-	_	_	-	_	_	_	-	_	_	_	_	0000
.0.0		15:0	_	_	_	-	-	_	_	-	_	_	_	_		CHEID	X<3:0>		00xx
4020	CHETAG ⁽¹⁾		LTAGBOOT	_	_		_	_	_	_				LTAG<				•	xxx0
.020		15:0			1			LTAG<	15:4>			1	I		LVALID	LLOCK	LTYPE	_	xxx2
4030	CHEMSKUJ	31:16	_		_				_	_		_	_	_		_		_	0000
		15:0					LN	MASK<15:5	>						_	_	_	_	xxxx
4040	CHEW0	31:16								CHEW0	<31:0>								XXXX
		15:0																	XXXX
4050	CHEW1	31:16								CHEW1	<31:0>								XXXX
		15:0																	XXXX
4060	CHEW2	31:16 15:0								CHEW2	<31:0>								XXXX
		31:16																	xxxx
4070	CHEW3	15:0								CHEW3	<31:0>								XXXX
		31:16	_		l —	_	_	_	_				CH	HELRU<24:1	6>				0000
4080	CHELRU	15:0								CHELRU	<15·0>				-				0000
		31:16								OHELIKO	<10.02								xxxx
4090	CHEHIT	15:0								CHEHIT	<31:0>								XXXX
		31:16		XXXX															
40A0	CHEMIS	15:0		CHEMIS<31:0>															
		31:16																	xxxx
40C0	CHEPFART	15:0								CHEPFAE	T<31:0>								xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section12.2 "CLR, SET and INV Registers" for more information.

REGISTER 10-1: CHECON: CACHE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		_	_	_	_		_	_
22:40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
23:16	_	_	_	_	_	_	_	CHECOH
45.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	_	_	_	_	_	_	DCSZ	′ <1:0>
7.0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
7:0		_	PREFE	N<1:0>	_	F	PFMWS<2:0>	•

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-17 Unimplemented: Write '0'; ignore read

bit 16 CHECOH: Cache Coherency Setting on a PFM Program Cycle bit

1 = Invalidate all data and instruction lines

0 = Invalidate all data lnes and instruction lines that are not locked

bit 15-10 Unimplemented: Write '0'; ignore read

bit 9-8 DCSZ<1:0>: Data Cache Size in Lines bits

11 = Enable data caching with a size of 4 Lines

10 = Enable data caching with a size of 2 Lines

01 = Enable data caching with a size of 1 Line

00 = Disable data caching

Changing these bits induce all lines to be reinitialized to the "invalid" state.

bit 7-6 **Unimplemented:** Write '0'; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits

11 = Enable predictive prefetch for both cacheable and non-cacheable regions

10 = Enable predictive prefetch for non-cacheable regions only

01 = Enable predictive prefetch for cacheable regions only

00 = Disable predictive prefetch

bit 3 Unimplemented: Write '0'; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSLK Wait States bits

111 = Seven Wait states

110 = Six Wait states

101 = Five Wait states

100 = Four Wait states

011 = Three Wait states

010 = Two Wait states

001 = One Wait state

000 = Zero Wait state

REGISTER 10-2: CHEACC: CACHE ACCESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	CHEWEN	_	_	_	_	_	_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	-	-	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	_
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	_		CHEID	X<3:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 **CHEWEN:** Cache Access Enable bits for registers CHETAG, CHEMSK, CHEW0, CHEW1, CHEW2, and CHEW3

1 = The cache line selected by CHEIDX<3:0> is writeable

0 = The cache line selected by CHEIDX<3:0> is not writeable

bit 30-4 **Unimplemented:** Write '0'; ignore read bit 3-0 **CHEIDX<3:0>:** Cache Line Index bits

The value selects the cache line for reading or writing.

REGISTER 10-3: CHETAG: CACHE TAG REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	LTAGBOOT	_	_	_	_	_	_	_
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23.10				LTAG<1	9:12>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15.6				LTAG<	11:4>			
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0	R/W-1	U-0
7.0		LTAG<	<3:0>		LVALID	LLOCK	LTYPE	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 LTAGBOOT: Line TAG Address Boot bit

1 = The line is in the 0x1D000000 (physical) area of memory

0 = The line is in the 0x1FC00000 (physical) area of memory

bit 30-24 Unimplemented: Write '0'; ignore read

bit 23-4 LTAG<19:0>: Line TAG Address bits

LTAG<19:0> bits are compared against physical address to determine a hit. Because its address range and position of PFM in kernel space and user space, the LTAG PFM address is identical for virtual addresses, (system) physical addresses, and PFM physical addresses.

bit 3 LVALID: Line Valid bit

1 = The line is valid and is compared to the physical address for hit detection

0 = The line is not valid and is not compared to the physical address for hit detection

bit 2 LLOCK: Line Lock bit

1 = The line is locked and will not be replaced

0 = The line is not locked and can be replaced

bit 1 LTYPE: Line Type bit

1 = The line caches instruction words

0 = The line caches data words

bit 0 Unimplemented: Write '0'; ignore read

REGISTER 10-4: CHEMSK: CACHE TAG MASK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_	-	_	_	_
22:40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_		_	_	_
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.6				LMASK<	<10:3>			
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
7.0	I	_MASK<2:0>		_		_	_	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Write '0'; ignore read

bit 15-5 LMASK<10:0>: Line Mask bits

- 1 = Enables mask logic to force a match on the corresponding bit position in the LTAG<19:0> bits (CHETAG<23:4>) and the physical address.
- 0 = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B. Disables mask logic.

bit 4-0 Unimplemented: Write '0'; ignore read

REGISTER 10-5: CHEW0: CACHE WORD 0

		51.1 211 0. 071		•							
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
31:24				CHEW0<	:31:24>						
22.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
23:16	CHEW0<23:16>										
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
15:8				CHEW0-	<15:8>						
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
7:0				CHEWO	<7:0>						

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 10-6: CHEW1: CACHE WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
31:24				CHEW1<	:31:24>						
00:40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
23:16				CHEW1<	:23:16>						
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
15:8				CHEW1	<15:8>						
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
7:0	CHEW1<7:0>										

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CHEW1<31:0>:** Word 1 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 10-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
31:24				CHEW2<	:31:24>							
22:46	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
23:16	CHEW2<23:16>											
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
15:8				CHEW2	<15:8>							
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
7:0	CHEW2<7:0>											

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CHEW2<31:0>:** Word 2 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

REGISTER 10-8: CHEW3: CACHE WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
31:24				CHEW3<	:31:24>							
22,46	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
23:16	CHEW3<23:16>											
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
15:8				CHEW3	<15:8>							
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
7:0	CHEW3<7:0>											

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CHEW3<31:0>:** Word 3 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>) Readable only if the device is not code-protected.

Note: This register is a window into the cache data array and is readable only if the device is not code-protected.

REGISTER 10-9: CHELRU: CACHE LRU REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0					
31.24	-	_	_	_	1	-	-	CHELRU<24>					
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
23.10	CHELRU<23:16>												
45.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
15:8				CHELR	U<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
7.0	CHELRU<7:0>												

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-25 Unimplemented: Write '0'; ignore read

bit 24-0 CHELRU<24:0>: Cache Least Recently Used State Encoding bits

Indicates the pseudo-LRU state of the cache.

REGISTER 10-10: CHEHIT: CACHE HIT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
31:24				CHEHIT<	:31:24>								
00:40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
23:16	CHEHIT<23:16>												
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
15:8				CHEHIT	<15:8>								
7.0	R/W-x	R/W-x	R/W-x R/W-x R/W-			R/W-x	R/W-x	R/W-x					
7:0	CHEHIT<7:0>												

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 CHEHIT<31:0>: Cache Hit Count bits

Incremented each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

REGISTER 10-11: CHEMIS: CACHE MISS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
31.24				CHEMIS<	<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
23.10				CHEMIS<	<23:16>							
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
15:8				CHEMIS	<15:8>							
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
7:0	CHEMIS<7:0>											

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 CHEMIS<31:0>: Cache Miss Count bits

Incremented each time the processor issues an instruction fetch from a cacheable region that misses the prefetch cache. Non-cacheable accesses do not modify this value.

REGISTER 10-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
31.24				CHEPFAB	Γ<31:24>								
22.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
23:16	CHEPFABT<23:16>												
15.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
15:8				CHEPFAB	T<15:8>								
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
7:0	CHEPFABT<7:0>												

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 CHEPFABT<31:0>: Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.

11.0 USB ON-THE-GO (OTG)

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 27. "USB On-The-Go (OTG)" (DS60001126), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, Full-Speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

The clock generator provides the 48 MHz clock required for USB Full-Speed and Low-Speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32 USB module includes the following features:

- USB Full-Speed support for Host and Device
- · Low-speed host support
- USB OTG support
- · Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- · Integrated USB transceiver
- · Transaction handshaking performed by hardware
- · Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note:

The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc., also referred to as USB-IF (www.usb.org). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

FIGURE 11-1: PIC32MX1XX/2XX 28/44-PIN XLP FAMILY FAMILY USB INTERFACE DIAGRAM FRC Oscillator 8 MHz Typical TUN<5:0>(3) Primary Oscillator UFIN(4) (Posc) Div x PLL Div 2 UFRCEN⁽²⁾ OSC1 UPLLIDIV⁽⁵⁾ UPLLEN⁽⁵⁾ OSC2 **USB Module** USB SRP Charge Voltage Comparators Bus X SRP Discharge 48 MHz USB Clock(6) Full Speed Pull-up D+(1) Registers and Control Interface Host Pull-down SIE Transceiver ow Speed Pull-up D-(1) DMA System RAM Host Pull-down ID Pull-up ID⁽¹⁾ VBUSON⁽¹⁾ VUSB3V3 Transceiver Power 3.3V Pins can be used as digital input/output when USB is not enabled. Note 1: This bit field is contained in the OSCCON register. This bit field is contained in the OSCTRM register. 4: USB PLL UFIN requirements: 4 MHz. This bit field is contained in the DEVCFG2 register. A 48 MHz clock is required for proper USB operation.

11.1 USB Control Registers

TABLE 11-1: USB REGISTER MAP

SSe											Bit	s							
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5040	U1OTGIR ⁽²⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3040	OTOTOIC	15:0	_	_	_	_	_	_	_	_	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF	0000
5050	U1OTGIE	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
	0.0.0.2	15:0		_	_			_	_		IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE		VBUSVDIE	0000
5060	U1OTGSTAT ⁽³⁾	31:16		_	_			_	_		_		_	_	_	_		_	0000
		15:0	_	_			_	_	_	_	ID		LSTATE		SESVD	SESEND		VBUSVD	0000
5070	U10TGCON	31:16	_	_			_	_	_	_	_	_	_	_	_	_	_	_	0000
		15:0	_	_			_	_	_	_	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
5080	U1PWRC	31:16	_	_	_	_	_	_	_	_	<u> </u>	_	_		_				0000
		15:0	_	_	_	_	_	_	_	_	UACTPND ⁽⁴⁾	_	_	USLPGRD	USBBUSY	_	USUSPEND	USBPWR	0000
	(2)	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5200	U1IR ⁽²⁾	15:0	_	_	_	_	_	_	_	_	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5210	U1IE	15:0	-	_	-	_	_	_	_	_	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000
		31:16	_								_	_		_			_	—	0000
5220	U1EIR ⁽²⁾	15:0	_	_	_	_	_	_	_	_	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000
		31:16															EUFEF		
5230	U1EIE	31:10	_	_		_	_	_	_		_	_	_	_			CRC5EE	_	0000
3230	OTELE	15:0	1	_	-	1	_	_	_	_	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	EOFEE	PIDEE	0000
5240	U1STAT ⁽³⁾	31:16	I	_	1	1	_	_	_	_	_	1	I	1	ı	_	ı	_	0000
3240	UISTAI	15:0	1	_		1	_	_	_	_		ENDF	PT<3:0>		DIR	PPBI	1	_	0000
		31:16	I	_			_	_	_	_	-	-	1	ı		_	-	_	0000
5250	U1CON	15:0	_	_	_	_	_	_	_	_	JSTATE	SE0	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000
		31:16	_	_	_		_	_			_	_	—	_	_		_	— —	0000
5260	U1ADDR	15:0		_							LSPDEN				VADDR<6:	0>			0000
		31:16		_								_	_	_		_	_	_	0000
5270	U1BDTP1	15:0												 TPTRL<15:9>					0000
		10.0									l		00	11 11KL \ 10.32					3000

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See 12.2 "CLR, SET and INV Registers" for more information.

^{2:} This register does not have associated SET and INV registers.

This register does not have associated CLR, SET and INV registers.

^{4:} Reset value for this bit is undefined.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

ess			Bits o																
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5280	U1FRML ⁽³⁾	31:16	_	_	_	_	_	_	_	_		_	_	_	_	_	_	_	0000
3200	OTIKWE	15:0	_	_	_	_	_	_	_	_				FRML<	7:0>				0000
5290	U1FRMH ⁽³⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3230	OTTTAMIT	15:0		_	_	_	_	_	_	_	_	_	_	_	_		FRMH<2:0>		0000
52A0	U1TOK	31:16	_	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
32/10	OTTOR	15:0	_	_	_	_	_	_	_	_		PID	<3:0>	•		EP	<3:0>		0000
52B0	U1SOF	31:16	_	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
3200	01301	15:0	_	_	_	_	_	_	_	_		•		CNT<7	7 :0>				0000
52C0	U1BDTP2	31:16	_	_	_	_	_	_	_	_	I	_	1	_	_	1	_	1	0000
3200	OIBBIF2	15:0		_	_	_	_	_	_	_				BDTPTRH	H<7:0>				0000
52D0	U1BDTP3	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
32D0	OIBDIF3	15:0	_	_	_	_	_	_	_	_				BDTPTRU	J<7:0>				0000
52E0	U1CNFG1	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
32L0	01014101	15:0		_	_	_	_	_	_	_	UTEYE	UOEMON	_	USBSIDL	_		_	UASUSPND	0001
5300	U1EP0	31:16		_	_	_	_	_	_	_		_	_	_	_	_	_	_	0000
3300	OTELO	15:0		_	_	_	_	_	_	_	LSPD	RETRYDIS	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5310	U1EP1	31:16		_	_	_	_	_	_	_		_	_	_	_	_	_	_	0000
3310	OTELLI	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5320	U1EP2	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0020	OTELL	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5330	U1EP3	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	OTELO	15:0	_	_	_	_	_	_	_	_	-	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340	U1EP4	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0040	OTEL 4	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5350	U1EP5	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3330	OTEI 3	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5360	U1EP6	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3300	OILIO	15:0	_	_	_	_	_	_	_	_	I	_	I	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5370	U1EP7	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3370	O I LI 7	15:0	_	_	_	_	_	_	_	_		_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5380	U1EP8	31:16		_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
3300	OILIO	15:0	_	_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See 12.2 "CLR, SET and INV Registers" for more information.

[:] This register does not have associated SET and INV registers.

^{3:} This register does not have associated CLR, SET and INV registers.

^{4:} Reset value for this bit is undefined.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

ess	Bits																		
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5390	U1EP9	31:16	-	_	_	_	_	_	_	_	_	_	_	_	-	_	_	_	0000
5390	UIEF9	15:0		_	_	_	_	_	_	_	_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	1	_	_	_	_	_	_	_	_	_	_	_	1	_	_	_	0000
55A0	UIEFIU	15:0	I	_	_	1	_	_	_	_	I	1	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	I	_	_	1	_	_	_	_	1	1	-	_	I	_	_	_	0000
3300	OILFII	15:0	I	_	_	1	_	_	_	_	1	1	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	-	_	_	_	_	_	_	_		_	_	_	1	_	_	_	0000
3300	OTET 12	15:0	-	_	_	_	_	_	_	_		_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	-	_	_	_	_	_	_	_		_	_	_	1	_	_	_	0000
33D0	OTET 15	15:0	-	_	_	_	_	_	_	_		_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
53EU	UTEP14	15:0	ı	_	_	_	_	_	_	_	-	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	-	_	_	_	_	_	_	_	_	_	_	_	-	_	_	_	0000
33FU	UILPIS	15:0	I	_	_	-	_	_	_	_	I	1	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See 12.2 "CLR, SET and INV Registers" for more information.

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- 2: This register does not have associated SET and INV registers.
- 3: This register does not have associated CLR, SET and INV registers.
- 4: Reset value for this bit is undefined.

U10TGIR: USB OTG INTERRUPT STATUS REGISTER REGISTER 11-1:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	_	_	-	_	-	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	_	_	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	-	_	_	_	-	_	-	_
7.0	R/WC-0, HS	U-0	R/WC-0, HS					
7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	_	VBUSVDIF

HS = Hardware Settable bit Legend: WC = Write '1' to clear

W = Writable bit R = Readable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 IDIF: ID State Change Indicator bit

> 1 = A change in the ID state was detected 0 = No change in the ID state was detected

bit 6 T1MSECIF: 1 Millisecond Timer bit

> 1 = 1 millisecond timer has expired 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit

1 = USB line state has been stable for 1 ms, but different from last time

0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit

1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up

0 = Activity has not been detected

bit 3 SESVDIF: Session Valid Change Indicator bit

1 = VBUS voltage has dropped below the session end level

0 = VBUS voltage has not dropped below the session end level

bit 2 SESENDIF: B-Device VBUS Change Indicator bit

1 = A change on the session end input was detected

0 = No change on the session end input was detected

bit 1 Unimplemented: Read as '0'

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bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit

1 = A change on the session valid input was detected

0 = No change on the session valid input was detected

REGISTER 11-2: U10TGIE: USB OTG INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	-	-	-	_	_	_	_
22.46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	-		-	-	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	_
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
7:0	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	_	VBUSVDIE

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 IDIE: ID Interrupt Enable bit

1 = ID interrupt is enabled0 = ID interrupt is disabled

bit 6 T1MSECIE: 1 Millisecond Timer Interrupt Enable bit

1 = 1 millisecond timer interrupt is enabled0 = 1 millisecond timer interrupt is disabled

bit 5 LSTATEIE: Line State Interrupt Enable bit

1 = Line state interrupt is enabled

0 = Line state interrupt is disabled

bit 4 ACTVIE: Bus Activity Interrupt Enable bit

1 = Activity interrupt is enabled

0 = Activity interrupt is disabled

bit 3 SESVDIE: Session Valid Interrupt Enable bit

1 = Session valid interrupt is enabled

0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Device Session End Interrupt Enable bit

1 = B-Device session end interrupt is enabled

0 = B-Device session end interrupt is disabled

bit 1 Unimplemented: Read as '0'

bit 0 VBUSVDIE: A-Device VBUS Valid Interrupt Enable bit

1 = A-Device VBUS valid interrupt is enabled

0 = A-Device VBUS valid interrupt is disabled

REGISTER 11-3: U10TGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_	_	-	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	_	_	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	_	_	_	_	_	_	_	_
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
7.0	ID	_	LSTATE	_	SESVD	SESEND	_	VBUSVD

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 ID: ID Pin State Indicator bit

1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle

0 = A "type A" OTG cable has been inserted into the USB receptacle

bit 6 Unimplemented: Read as '0'

bit 5 LSTATE: Line State Stable Indicator bit

1 = USB line state (SE0 (U1CON<6>) bit and JSTATE (U1CON<7>)) bit has been stable for previous 1 ms

0 = USB line state (SE0 and JSTATE) has not been stable for previous 1 ms

bit 4 Unimplemented: Read as '0'

bit 3 SESVD: Session Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A or B device

0 = VBUS voltage is below Session Valid on the A or B device

bit 2 SESEND: B-Device Session End Indicator bit

1 = VBUS voltage is below Session Valid on the B device

0 = VBUS voltage is above Session Valid on the B device

bit 1 Unimplemented: Read as '0'

bit 0 VBUSVD: A-Device VBUS Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A device

0 = VBUS voltage is below Session Valid on the A device

REGISTER 11-4: U10TGCON: USB OTG CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	-	_	_	-	_	1	-
22,16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	-	_		-	_	1	
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	_	_	_	_	_	_	_	_
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit

1 = D+ data line pull-up resistor is enabled

0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

1 = D- data line pull-up resistor is enabled

0 = D- data line pull-up resistor is disabled

bit 5 DPPULDWN: D+ Pull-Down Enable bit

1 = D+ data line pull-down resistor is enabled

0 = D+ data line pull-down resistor is disabled

bit 4 DMPULDWN: D- Pull-Down Enable bit

1 = D- data line pull-down resistor is enabled

0 = D- data line pull-down resistor is disabled

bit 3 VBUSON: VBUS Power-on bit

1 = VBUS line is powered

0 = VBUS line is not powered

bit 2 OTGEN: OTG Functionality Enable bit

1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control

0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 VBUSCHG: VBUS Charge Enable bit

1 = VBUS line is charged through a pull-up resistor

0 = VBUS line is not charged through a resistor

bit 0 VBUSDIS: VBUS Discharge Enable bit

1 = VBUS line is discharged through a pull-down resistor

0 = VBUS line is not discharged through a resistor

REGISTER 11-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	1	_	-	1	_	-	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	1	_	-	1	_	-	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	-	_	_	-	_	_	_	_
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	_	_	USLPGRD	USBBUSY ⁽¹⁾	_	USUSPEND	USBPWR

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

1 = USB bus activity has been detected; however, an interrupt is pending, which has yet to be generated

0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 USLPGRD: USB Sleep Entry Guard bit

1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending

0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit⁽¹⁾

1 = USB module is active or disabled, but not ready to be enabled

0 = USB module is not active and is ready to be enabled

bit 2 Unimplemented: Read as '0'

bit 1 USUSPEND: USB Suspend Mode bit

1 = USB module is placed in Suspend mode

(The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)

0 = USB module operates normally

bit 0 USBPWR: USB Operation Enable bit

1 = USB module is turned on

0 = USB module is disabled

(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

REGISTER 11-6: U1IR: USB INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_			_				_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_		_	_		_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	_	-	-	-	-			_
	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
7:0	STALLIF	ATTACHIF ⁽¹⁾	RESUMEIF ⁽²⁾	IDLEIF	TRNIF ⁽³⁾	SOFIF	UERRIF ⁽⁴⁾	URSTIF ⁽⁵⁾
	O 17 (EEII	711 17101111	I (LOO!VILII	IDEEII	1131411	00111	OLIVI	DETACHIF ⁽⁶⁾

Legend:WC = Write '1' to clearHS = Hardware Settable bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit

1 = In Host mode a STALL handshake was received during the handshake phase of the transaction In Device mode a STALL handshake was transmitted during the handshake phase of the transaction

0 = STALL handshake has not been sent

bit 6 ATTACHIF: Peripheral Attach Interrupt bit⁽¹⁾

1 = Peripheral attachment was detected by the USB module

0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit⁽²⁾

1 = K-State is observed on the D+ or D- pin for 2.5 μ s

0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit

1 = Idle condition detected (constant Idle state of 3 ms or more)

0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit⁽³⁾

1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information

0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit

1 = SOF token received by the peripheral or the SOF threshold reached by the host

0 = SOF token was not received nor threshold reached

bit 1 **UERRIF**: USB Error Condition Interrupt bit⁽⁴⁾

1 = Unmasked error condition has occurred

0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)⁽⁵⁾

1 = Valid USB Reset has occurred

0 = No USB Reset has occurred

DETACHIF: USB Detach Interrupt bit (Host mode)⁽⁶⁾

1 = Peripheral detachment was detected by the USB module

0 = Peripheral detachment was not detected

Note 1: This bit is valid only if the HOSTEN bit is set (see Register 11-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.

- 2: When not in Suspend mode, this interrupt should be disabled.
- 3: Clearing this bit will cause the STAT FIFO to advance.
- 4: Only error conditions enabled through the U1EIE register will set this bit.
- 5: Device mode.
- 6: Host mode.

REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0						
31.24	_	_	_	-	_	_	_	
23:16	U-0	U-0						
23.10	_	_	-	_	_	_	_	_
15:8	U-0	U-0						
15.6	_	_	_	-	_	_	_	
	R/W-0	R/W-0						
7:0	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE ⁽¹⁾	URSTIE ⁽²⁾
	O I , LEIL	711 17 (OT IIL	TREGOMETE	IDELIL	TIME	001 IL	OLIVIC	DETACHIE ⁽³⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 STALLIE: STALL Handshake Interrupt Enable bit

1 = STALL interrupt is enabled0 = STALL interrupt is disabled

bit 6 ATTACHIE: ATTACH Interrupt Enable bit

1 = ATTACH interrupt is enabled0 = ATTACH interrupt is disabled

bit 5 RESUMEIE: RESUME Interrupt Enable bit

1 = RESUME interrupt is enabled0 = RESUME interrupt is disabled

bit 4 IDLEIE: Idle Detect Interrupt Enable bit

1 = Idle interrupt is enabled0 = Idle interrupt is disabled

bit 3 TRNIE: Token Processing Complete Interrupt Enable bit

1 = TRNIF interrupt is enabled 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit

1 = SOFIF interrupt is enabled0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit⁽¹⁾

1 = USB Error interrupt is enabled0 = USB Error interrupt is disabled

URSTIE: USB Reset Interrupt Enable bit(2)

1 = URSTIF interrupt is enabled0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit⁽³⁾

1 = DATTCHIF interrupt is enabled0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE (U1IE<1>) bit must be set.

2: Device mode.

3: Host mode.

bit 0

REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	-	-	-	-	-	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	-	-	-	-	-	_	_	_
	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS
7:0	BTSEF	BMXEF	DMAEF ⁽¹⁾	BTOEF ⁽²⁾	DFN8EF	CRC16EF	CRC5EF ⁽⁴⁾	PIDEF
	DISEF	DIVINE	DIVINEL.,	DIOEF. 7	DINOEF	CINCIDE	EOFEF ^(3,5)	LIDEL

Legend:WC = Write '1' to clearHS = Hardware Settable bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 BTSEF: Bit Stuff Error Flag bit

1 = Packet rejected due to bit stuff error

0 = Packet accepted

bit 6 BMXEF: Bus Matrix Error Flag bit

1 = The base address, of the Buffer Descriptor Table, or the address of an individual buffer pointed to by a Buffer Descriptor Table entry, is invalid.

0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit⁽¹⁾

1 = USB DMA error condition detected

0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit⁽²⁾

1 = Bus turnaround time-out has occurred

0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit

1 = Data field received is not an integral number of bytes

0 = Data field received is an integral number of bytes

bit 2 CRC16EF: CRC16 Failure Flag bit

1 = Data packet rejected due to CRC16 error

0 = Data packet accepted

- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
 - 2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
 - **3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
 - 4: Device mode.
 - 5: Host mode.

REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

- bit 1 CRC5EF: CRC5 Host Error Flag bit⁽⁴⁾
 - 1 = Token packet rejected due to CRC5 error
 - 0 = Token packet accepted **EOFEF:** EOF Error Flag bit^(3,5)
 - 1 = An EOF error condition was detected0 = No EOF error condition was detected
- bit 0 PIDEF: PID Check Failure Flag bit
 - 1 = PID check failed0 = PID check passed
- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
 - 2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
 - 3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
 - 4: Device mode.
 - 5: Host mode.

REGISTER 11-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31:24	_	_	_	_	_	_	_	_
22,46	U-0	U-0						
23:16	_	_	_	_	_	_	_	_
15:8	U-0	U-0						
15.6	_	_	_	_	_	_	_	_
	R/W-0	R/W-0						
7:0	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE ⁽¹⁾	PIDEE
	DISEL	DIVINEE	DIVIALE	DIOLL	DINOEE	CINOTOLL	EOFEE ⁽²⁾	FIDEE

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 BTSEE: Bit Stuff Error Interrupt Enable bit

1 = BTSEF interrupt is enabled0 = BTSEF interrupt is disabled

bit 6 BMXEE: Bus Matrix Error Interrupt Enable bit

1 = BMXEF interrupt is enabled0 = BMXEF interrupt is disabled

bit 5 DMAEE: DMA Error Interrupt Enable bit

1 = DMAEF interrupt is enabled0 = DMAEF interrupt is disabled

bit 4 BTOEE: Bus Turnaround Time-out Error Interrupt Enable bit

1 = BTOEF interrupt is enabled0 = BTOEF interrupt is disabled

bit 3 DFN8EE: Data Field Size Error Interrupt Enable bit

1 = DFN8EF interrupt is enabled0 = DFN8EF interrupt is disabled

bit 2 CRC16EE: CRC16 Failure Interrupt Enable bit

1 = CRC16EF interrupt is enabled0 = CRC16EF interrupt is disabled

bit 1 CRC5EE: CRC5 Host Error Interrupt Enable bit (1)

1 = CRC5EF interrupt is enabled0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit⁽²⁾

1 = EOF interrupt is enabled0 = EOF interrupt is disabled

bit 0 PIDEE: PID Check Failure Interrupt Enable bit

1 = PIDEF interrupt is enabled0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

Note: For an interrupt to propagate the USBIF register, the UERRIE (U1IE<1>) bit must be set.

REGISTER 11-10: U1STAT: USB STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	_	-	-	-	-	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	-	_	_	-	-	-	-	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
7:0		ENDP.	T<3:0>		DIR	PPBI	_	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 ENDPT<3:0>: Encoded Number of Last Endpoint Activity bits

(Represents the number of the Buffer Descriptor Table, updated by the last USB transfer.)

1111 = Endpoint 15

1110 = Endpoint 14

:

•

0001 = Endpoint 1

0000 = Endpoint 0

bit 3 DIR: Last Buffer Descriptor Direction Indicator bit

1 = Last transaction was a transmit (TX) transfer

0 = Last transaction was a receive (RX) transfer

bit 2 PPBI: Ping-Pong Buffer Descriptor Pointer Indicator bit

1 = The last transaction was to the ODD Buffer Descriptor bank

0 = The last transaction was to the EVEN Buffer Descriptor bank

bit 1-0 Unimplemented: Read as '0'

Note: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when the TRNIF (U1IR<3>) bit is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

REGISTER 11-11: U1CON: USB CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04:04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	-		_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	-		_	1			_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	-		_	_
	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	JSTATE	SE0	PKTDIS ⁽⁴⁾	USBRST	HOSTEN ⁽²⁾	RESUME ⁽³⁾	PPBRST	USBEN ⁽⁴⁾
	JOIAIE	350	TOKBUSY ^(1,5)	USDRST	11031EW	KESUME	FEDROI	SOFEN ⁽⁵⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

1 = JSTATE was detected on the USB

0 = No JSTATE was detected

bit 6 SE0: Live Single-Ended Zero flag bit

1 = Single-Ended Zero was detected on the USB

0 = No Single-Ended Zero was detected

bit 5 **PKTDIS:** Packet Transfer Disable bit⁽⁴⁾

1 = Token and packet processing is disabled (set upon SETUP token received)

0 = Token and packet processing is enabled

TOKBUSY: Token Busy Indicator bit (1,5)

1 = Token is being executed by the USB module

0 = No token is being executed

bit 4 USBRST: Module Reset bit⁽⁵⁾

1 = USB reset generated

0 = USB reset terminated

bit 3 HOSTEN: Host Mode Enable bit⁽²⁾

1 = USB host capability is enabled

0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit⁽³⁾

1 = RESUME signaling is activated

0 = RESUME signaling is disabled

- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - 3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

REGISTER 11-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 PPBRST: Ping-Pong Buffers Reset bit
 - 1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
 - 0 = Even/Odd buffer pointers are not Reset
- bit 0 **USBEN:** USB Module Enable bit⁽⁴⁾
 - 1 = USB module and supporting circuitry is enabled0 = USB module and supporting circuitry is disabled
 - **SOFEN:** SOF Enable bit⁽⁵⁾
 1 = SOF token is sent every 1 ms
 - 0 = SOF token is disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - 3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	-	_	_	-	-	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	-	_		_	_	1		_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	_
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	LSPDEN			D	EVADDR<6:0	>		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 LSPDEN: Low-Speed Enable Indicator bit

1 =Next token command to be executed at Low-Speed 0 =Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	_	_	-	_	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	_	_	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	1	-	_	_	-	_	_	_
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				FRML	.<7:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 FRML<7:0>: The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24	-	_	-	_	-	-	-	-		
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	-	_		_	-	1	-	-		
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
15.6	_	_	_	_	_	_	_	_		
7.0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0		
7:0	_	_	_	_	_		FRMH<2:0>			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

bit 2-0 FRMH<2:0>: The Upper 3 bits of the Frame Numbers bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 11-15: U1TOK: USB TOKEN REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		PID<	3:0> ⁽¹⁾	•		EP<	3:0>	•

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 PID<3:0>: Token Type Indicator bits⁽¹⁾

1101 = SETUP (TX) token type transaction 1001 = IN (RX) token type transaction

0001 = OUT (TX) token type transaction

Note: All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits The four bit value must specify a valid endpoint.

Note 1: All other values are reserved and must not be used.

REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	-	_	-	_	_	1	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	-	_	-	_	_	1		_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_	_	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 CNT<7:0>: SOF Threshold Value bits

Typical values of the threshold are:

01001010 = **64-byte** packet

00101010 = 32-byte packet

00011010 = **16-byte** packet

00010010 = 8-byte packet

REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_	_	_
22,16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	-	_	-	_		_	-	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BDTPTRL<15:9>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-1 BDTPTRL<15:9>: Buffer Descriptor Table Base Address bits

This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 Unimplemented: Read as '0'

REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	-	1	1	1	_	-	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	-	1	1	1	1	1	1	1
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	-	_	_	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 BDTPTRH<23:16>: Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	-	-	_	-	-	1	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_	_	_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	_	_	_	_	_	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 BDTPTRU<31:24>: Buffer Descriptor Table Base Address bits

This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	-	_	-	-	-	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	-	_	-	-		_
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.6	_	_	_	_	_	_	_	_
7.0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
7:0	UTEYE	UOEMON	_	USBSIDL	_	_	_	UASUSPND

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 UTEYE: USB Eye-Pattern Test Enable bit

1 = Eye-Pattern Test is enabled0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB OE Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving

0 = OE signal is inactive

bit 5 Unimplemented: Read as '0'

bit 4 USBSIDL: Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 3-1 Unimplemented: Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit

- 1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.
- 0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

REGISTER 11-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	-	_	-	_	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	-	_	-	_		-	_	-
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
13.6	-	_	-	_		-	_	-
7.0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	LSPD	RETRYDIS	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 LSPD: Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)

1 = Direct connection to a Low-Speed device enabled

0 = Direct connection to a Low-Speed device disabled; hub required with PRE_PID

bit 6 RETRYDIS: Retry Disable bit (Host mode and U1EP0 only)

1 = Retry NAKed transactions disabled

0 = Retry NAKed transactions enabled; retry done in hardware

bit 5 Unimplemented: Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit

If EPTXEN = 1 and EPRXEN = 1:

1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed

0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed

Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit

1 = Endpoint n receive is enabled

0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit

1 = Endpoint n transmit is enabled

0 = Endpoint n transmit is disabled

bit 1 EPSTALL: Endpoint Stall Status bit

1 = Endpoint n was stalled

0 = Endpoint n was not stalled

bit 0 EPHSHK: Endpoint Handshake Enable bit

1 = Endpoint Handshake is enabled

0 = Endpoint Handshake is disabled (typically used for isochronous endpoints)

12.0 I/O PORTS

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12.** "I/O Ports" (DS60001120), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions.

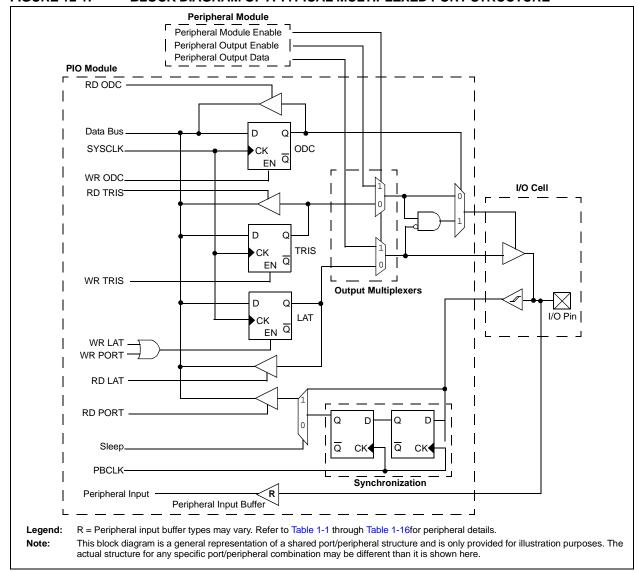
These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

The following are key features of the I/O Ports module:

- Individual output pin open-drain enable/disable
- · Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- · Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



12.1 Parallel I/O (PIO) Ports

All port pins have 10 registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

12.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the "Pin Diagrams" section for the available pins and their functionality.

12.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

12.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

12.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MX1XX/2XX 28/44-pin XLP Family devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 12-3.

12.2 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR, or INV register, the base register must be read.

12.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

12.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

12.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digitalonly peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

12.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

12.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [pin name]R registers, where [pin name] refers to the peripheral pins listed in Table, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX

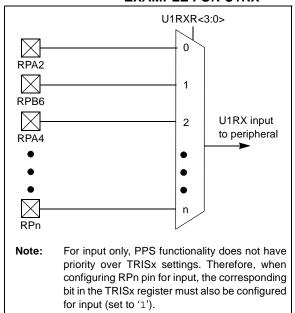


TABLE 12-1: INPUT PIN SELECTION

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPn Pin Selection
INT4	INT4R	INT4R<3:0>	0000 = RPA0 0001 = RPB3
T2CK	T2CKR	T2CKR<3:0>	0010 = RPB4 0011 = RPB15 0100 = RPB7
IC4	IC4R	IC4R<3:0>	0101 = RPC7 ⁽¹⁾ 0110 = RPC0 ⁽¹⁾ 0111 = RPC5 ⁽¹⁾
SS1	SS1R	SS1R<3:0>	1000 = Reserved
REFCLKI	REFCLKIR	REFCLKIR<3:0>	1111 = Reserved
INT3	INT3R	INT3R<3:0>	0000 = RPA1 0001 = RPB5
T3CK	T3CKR	T3CKR<3:0>	0010 = RPB1 0011 = RPB11 ⁽²⁾
IC3	IC3R	IC3R<3:0>	0100 = RPB8 0101 = RPA8 ⁽¹⁾
Ū1CTS	U1CTSR	U1CTSR<3:0>	0110 = RPC8 ⁽¹⁾ 0111 = RPA9 ⁽¹⁾
U2RX	U2RXR	U2RXR<3:0>	1000 = Reserved
SDI1	SDI1R	SDI1R<3:0>	• 1111 = Reserved
INT2	INT2R	INT2R<3:0>	0000 = RPA2
T4CK	T4CKR	T4CKR<3:0>	$\begin{array}{c}$
IC1	IC1R	IC1R<3:0>	0011 = RPB13 ⁽³⁾ 0100 = RPB2
IC5	IC5R	IC5R<3:0>	$0101 = RPC6^{(1)}$
U1RX	U1RXR	U1RXR<3:0>	$0110 = RPC1^{(1)}$ $0111 = RPC3^{(1)}$
U2CTS	U2CTSR	U2CTSR<3:0>	1000 = Reserved
SDI2	SDI2R	SDI2R<3:0>	□:
OCFB	OCFBR	OCFBR<3:0>	• 1111 = Reserved
INT1	INT1R	INT1R<3:0>	0000 = RPA3 0001 = RPB14
T5CK	T5CKR	T5CKR<3:0>	0010 = RPB0 0011 = RPB10 ⁽²⁾ 0100 = RPB9
IC2	IC2R	IC2R<3:0>	0101 = RPC9 ⁽¹⁾ 0110 = RPC2 ⁽¹⁾ 0111 = RPC4 ⁽¹⁾
SS2	SS2R	SS2R<3:0>	1000 = Reserved
OCFA	OCFAR	OCFAR<3:0>	1111 = Reserved

Note 1: This pin is only available on 44-pin devices.

^{2:} This pin is not available on USB devices.

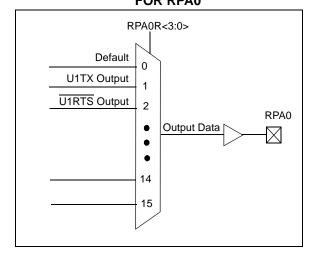
^{3:} This pin is not available on VBAT devices.

12.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [pin name]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0



12.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- · Control register lock sequence
- · Configuration bit select lock

12.3.6.1 Control Register Lock Sequence

Under normal operation, writes to the RPnR and [pin name]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the Configuration bit, IOLOCK (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

12.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [pin name]R registers. The Configuration bit, IOL1WAY (DEVCFG3<29>), blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and reenable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

TABLE 12-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA0	RPA0R	RPA0R<3:0>	0000 = No Connect 0001 = U1TX
RPB3	RPB3R	RPB3R<3:0>	0010 = U2RTS
RPB15	RPB15R	RPB15R<3:0>	0011 = SS1 0100 = VBUSON ⁽⁴⁾
RPB7	RPB7R	RPB7R<3:0>	0101 = OC1 0110 = Reserved
RPC7 ⁽¹⁾	RPC7R	RPC7R<3:0>	0111 = C2OUT
RPC0 ⁽¹⁾	RPC0R	RPC0R<3:0>	1000 = Reserved
RPC5 ⁽¹⁾	RPC5R	RPC5R<3:0>	1111 = Reserved
RPA1	RPA1R	RPA1R<3:0>	0000 = No Connect
RPB5	RPB5R	RPB5R<3:0>	0001 = Reserved 0010 = Reserved
RPB1	RPB1R	RPB1R<3:0>	0011 = SDO1
RPB11 ⁽²⁾	RPB11R	RPB11R<3:0>	0100 = SDO2 0101 = OC2
RPB8	RPB8R	RPB8R<3:0>	0110 = Reserved
RPA8 ⁽¹⁾	RPA8R	RPA8R<3:0>	0111 = C3OUT
RPC8 ⁽¹⁾	RPC8R	RPC8R<3:0>	•
RPA9 ⁽¹⁾	RPA9R	RPA9R<3:0>	1111 = Reserved
RPA2	RPA2R	RPA2R<3:0>	0000 = No Connect
RPB6 ⁽²⁾	RPB6R	RPB6R<3:0>	0001 = Reserved 0010 = Reserved
RPB13 ⁽³⁾	RPB13R	RPB13R<3:0>	0011 = SDO1 0100 = SDO2
RPB2	RPB2R	RPB2R<3:0>	0101 = OC4 0110 = OC5
RPC6 ⁽¹⁾	RPC6R	RPC6R<3:0>	0111 = REFCLKO 1000 = Reserved
RPC1 ⁽¹⁾	RPC1R	RPC1R<3:0>	• • • • • • • • • • • • • • • • • • •
RPC3 ⁽¹⁾	RPC3R	RPC3R<3:0>	• 1111 = Reserved
RPA3	RPA3R	RPA3R<3:0>	0000 = No Connect
RPB14	RPB14R	RPB14R<3:0>	0001 = U1RTS 0010 = U2TX
RPB0	RPB0R	RPB0R<3:0>	0011 = Reserved 0100 = SS2
RPB10 ⁽²⁾	RPB10R	RPB10R<3:0>	0101 = OC3
RPB9	RPB9R	RPB9R<3:0>	0110 = Reserved 0111 = C1OUT
RPC9 ⁽¹⁾	RPC9R	RPC9R<3:0>	1000 = Reserved
RPC2 ⁽¹⁾	RPC2R	RPC2R<3:0>	- -
RPC4 ⁽¹⁾	RPC4R	RPC4R<3:0>	1111 = Reserved

Note 1: This pin is only available on 44-pin devices.

^{2:} This pin is not available on USB devices.

^{3:} This pin is not available on VBAT devices.

^{4:} This pin is only available on USB devices.

12.4 Ports Control Registers

TABLE 12-3: PORTA REGISTER MAP

ess		•								Bits	3								"
Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6000	ANSELA	31:16		_	_	_	_	_	_	Ι		_		_	I	_	_	_	0000
0000		15:0		_	_	_	_	1	_	1			_		_		ANSA1	ANSA0	0003
6010	TRISA	31:16	-	_	_	_	_	_			_	_		_	-	_	_	_	0000
00.0		15:0	-	_	_	_	_	TRISA10 ⁽²⁾	TRISA9 ⁽²⁾	TRISA8 ⁽²⁾	TRISA7 ⁽²⁾	_		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
6020	PORTA	31:16	-	_	_	_	_		_	_	_	_							0000
0020	1 01(1)(15:0	_	_	_	_	_	RA10 ⁽²⁾	RA9 ⁽²⁾	RA8 ⁽²⁾	RA7 ⁽²⁾	_	_	RA4	RA3	RA2	RA1	RA0	xxxx
6030	LATA	31:16		_	_	_	_		_	_	_	_	_	_	1	_	_	_	0000
0000	27(17)	15:0	_	_	_	_	_	LATA10 ⁽²⁾	LATA9 ⁽²⁾	LATA8 ⁽²⁾	LATA7 ⁽²⁾	_	_	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6040	ODCA	31:16	-	_	_	_	_	_	_		_	_		_	-	_	_	_	0000
0040		15:0	-	_	_	_	_	ODCA10 ⁽²⁾	ODCA9 ⁽²⁾	ODCA8 ⁽²⁾	ODCA7 ⁽²⁾	_		ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
6050	CNPUA	31:16	-	_	_	_	_	_	_			_		_	-	_	_	_	0000
0000	0141 071	15:0		_	_	_	_	CNPUA10 ⁽²⁾	CNPUA9 ⁽²⁾	CNPUA8 ⁽²⁾	CNPUA7 ⁽²⁾	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
6060	CNPDA	31:16	-	_	_	_	_	_	_			_		_	-	_	_	_	0000
0000		15:0		_	_	_	_	CNPDA10 ⁽²⁾	CNPDA9 ⁽²⁾	CNPDA8 ⁽²⁾	CNPDA7 ⁽²⁾	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
6070	CNCONA	31:16	_	_	_	_	_	_	_	_	_	_		_	-	_	_	_	0000
0070		15:0	ON	_	SIDL	_	_	_	_		_	_	_	_	_	_	_	_	0000
6080	CNENA	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	SINLINA	15:0	_	_	_	_	_	CNIEA10 ⁽²⁾	CNIEA9 ⁽²⁾	CNIEA8 ⁽²⁾	CNIEA7 ⁽²⁾	_	-	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
6090	CNSTATA	31:16	_	_	_	_	_	_	_	_	_	_		_	_	_	_	_	0000
0090	CNSTATA	15:0	_	_	_	_	_	CNSTATA10 ⁽²⁾	CNSTATA9 ⁽²⁾	CNSTATA8 ⁽²⁾	CNSTATA7 ⁽²⁾	_		CNSTATA4	CNSTATA3	CNSTATA2	CNSTATA1	CNSTATA0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

2: This bit is only available on 44-pin devices.

TABLE 12-4: PORTB REGISTER MAP

ess										Bits									
Virtual Address (BF88_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6100	ANSELB	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0100	ANOLLD	15:0	ANSB15	ANSB14	ANSB13 ⁽³⁾	ANSB12 ⁽²⁾	_	_	_	_	_	_	_	_	ANSB3	ANSB2	ANSB1	ANSB0	EOOF
6110	TRISB	31:16	_	-	_	_	_	_	_	_		_	_	_	_	_	_	_	0000
00		15:0	TRISB15	TRISB14	TRISB13 ⁽³⁾	TRISB12 ⁽²⁾	TRISB11 ⁽²⁾	TRISB10 ⁽²⁾	TRISB9	TRISB8	TRISB7	TRISB6 ⁽²⁾	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
6120	PORTB	31:16	_	_	<u> </u>		<u> </u>	<u> </u>	_	_	_		_						0000
		15:0	RB15	RB14	RB13 ⁽³⁾	RB12 ⁽²⁾	RB11 ⁽²⁾	RB10 ⁽²⁾	RB9	RB8	RB7	RC6 ⁽²⁾	RB5	RB4	RB3	RB2	RB1	RB0	XXXX
6130	LATB	31:16	_	_	— (a)				_	_	_		_		_	_	_	_	0000
		15:0	LATB15	LATB14	LATB13 ⁽³⁾	LATB12 ⁽²⁾	LATB11 ⁽²⁾	LATB10 ⁽²⁾	LATB9	LATB8	LATB7	LATB6 ⁽²⁾	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	XXXX
6140	ODCB	31:16	_	_	— (a)				_	_	_	_	_		_	_	_	_	0000
0.10		15:0	ODCB15	ODCB14	ODCB13 ⁽³⁾	ODCB12 ⁽²⁾	ODCB11 ⁽²⁾	ODCB10 ⁽²⁾	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
6150	CNPUB	31:16	_	_	<u> </u>				_	_	_		_		_	_	_	_	0000
0.00			CNPUB15	CNPUB14	CNPUB13(3)	CNPUB12 ⁽²⁾	CNPUB11(2)	CNPUB10(2)	CNPUB9	CNPUB8	CNPUB7	CNPUB6 ⁽²⁾	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	
6160	CNPDB	31:16	_	_	_				_	_	_		_		_	_	_	_	0000
0.00			CNPDB15	CNPDB14	CNPDB13	CNPDB12 ⁽²⁾	CNPDB11(2)	CNPDB10(2)	CNPDB9	CNPDB8	CNPDB7	CNPDB6 ⁽²⁾	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	
6170	CNCONB	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_	_	0000
		15:0	ON	_	SIDL		_	_	_	_	_	_	_	_	_	_	_	_	0000
6180	CNENB	31:16		_	— (2)	— (2)	— (2)	— (2)		_		— (2)				_			0000
		15:0	CNIEB15	CNIEB14	CNIEB13 ⁽³⁾	CNIEB11 ⁽²⁾	CNIEB11 ⁽²⁾	CNIEB10 ⁽²⁾	CNIEB9	CNIEB8	CNIEB7	CNIEB6 ⁽²⁾	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1		0000
		31:16	_		_	_	_	_		_	_	_				_	_		0000
6190	CNSTATB	15:0	CN STATB15	CN STATB14	CN STATB13 ⁽³⁾	CN STATB12 ⁽²⁾	CN STATB11 ⁽²⁾	CN STATB10 ⁽²⁾	CN STATB9	CN STATB8	CN STATB7	CN STATB6 ⁽²⁾	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

- 2: This bit is not available on USB devices.
- 3: This bit is not available on VBAT devices.

TABLE 12-5: PORTC REGISTER MAP

ess	_	•									Bits								_o
Virtual Address (BF88_#)	Register Name ^(1,2)	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6200	ANSELC	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0200	ANOLLO	15:0	_	_	_	_	_	_	_	_	_	_	_	_	ANSC3	ANSC2	ANSC1	ANSC0	000F
6210	TRISC	31:16	_	_		_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0210	111100	15:0	_	_	_	_	_	_	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
6220	PORTC	31:16	_	_		_	_	_	_	_	_	_	_						0000
0220		15:0	_	_		_	_	_	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
6230	LATC	31:16	_	_	-	_	_	_	_	_	_	_	_	-	_	_	_	_	0000
0200		15:0	_	_	-	_	_	_	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
6240	ODCC	31:16							_	_		_	_	_	_	_	_	_	0000
02 10		15:0	_						ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
6250	CNPUC	31:16	_						_	_		_	_	-	_	_	_		0000
0200		15:0	_						CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
6260	CNPDC	31:16	_						_	_		_	_	-	_	_	_		0000
0200		15:0	_						CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	_		_				_			_			_	_	_		0000
0210		15:0	ON		SIDL				_			_			_	_	_		0000
6280	CNENC	31:16	_						_	_		_	_	-	_	_	_		0000
3200		15:0							CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
6290	CNSTATC	31:16							_	_		_	_	_	_	_	_	_	0000
0230	CINCIAIC	15:0	_	_	_	_	_	_	CNSTATC9	CNSTATC8	CNSTATC7	CNSTATC6	CNSTATC5	CNSTATC4	CNSTATC3	CNSTATC2	CNSTATC1	CNSTATC0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

: PORTC is not available on 28-pin devices.

TABLE 12-6: PERIPHERAL PIN SELECT INPUT REGISTER MAP

SS										В	its								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E404	INT1R	31:16	1	_	_	_	_	_	_	_	1	1	_	_	_	1	_	1	0000
FA04	INTIK	15:0	I	_	_	_	_	_	_	_	1	1	_	_		INT1F	R<3:0>		0000
FA08	INT2R	31:16	1	_	_	_	_	-	_	_	1	1	_	_	_	1	_	1	0000
FAUO	INTZK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		INT2F	R<3:0>		0000
FA0C	INT3R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FAUC	INTOK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		INT3F	R<3:0>		0000
FA10	INT4R	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FAIU	IINT4K	15:0	_	_	_	_	_	_	_	_	_	_	_	_		INT4F	R<3:0>		0000
FA18	T2CKR	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FATO	IZCKK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		T2CKI	R<3:0>		0000
EA40	T3CKR	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FA1C	ISCAR	15:0	-	_	_	_	_	_	_	_	-	_	_	_		T3CKI	R<3:0>		0000
FA20	T4CKR	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FA20	14CKK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		T4CKI	R<3:0>		0000
EA 24	TECKD	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FA24	T5CKR	15:0	-	_	_	_	_	_	_	_	-	_	_	_		T5CKI	R<3:0>		0000
FA28	IC4D	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FAZ8	IC1R	15:0	-	_	_	_	_	_	_	_	-	_	_	_		IC1R	<3:0>		0000
FA2C	ICOD	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FAZC	IC2R	15:0	-	_	_	_	_	_	_	_	-	_	_	_		IC2R	<3:0>		0000
FA30	IC3R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FASU	IUSK	15:0	_	_	_	_	_	_	_	_	_	_	_	_		IC3R	<3:0>		0000
FA34	IC4R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FA34	IC4K	15:0	_	_	_	_	_	_	_	_	_	_	_	_		IC4R	<3:0>		0000
FA38	IC5R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FASO	ICSK	15:0	_	_	_	_	_	_	_	_	_	_	_	_		IC5R	<3:0>		0000
EA 40	OCFAR	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	_	0000
FA48	OUTAK	15:0	-	_	_	_	_	_	_	_		_	_	_		OCFA	R<3:0>		0000
FA4C	OCFBR	31:16	-	_	_	_	_	_	_	_		_	_	_	_	_	_	_	0000
FA4C	OCEBR	15:0	_	_	_	_	_	_	_	_	_	_	_	_		OCFB	R<3:0>		0000
E450	LIADVD	31:16	-	_	_	_	_	_	_	_		_	_	_	_	_	_	_	0000
FA50	U1RXR	15:0	-	_	_	_	_	_	_	_	-	-	_	_		U1RX	R<3:0>		0000

TABLE 12-6: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

sss									`	В	its								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FA54	U1CTSR	31:16		_	_	_	_	_	_	_		_	_	_	_	_	_		0000
FA54	UICISK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		U1CTS	R<3:0>		0000
FA58	U2RXR	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	-	0000
FASo	UZKAK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		U2RX	R<3:0>		0000
FA5C	U2CTSR	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	-	0000
FASC	UZCISK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		U2CTS	R<3:0>		0000
FA84	SDI1R	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	-	0000
1 A04	SDITK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		SDI1F	R<3:0>		0000
FA88	SS1R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1 A00	3311	15:0	-	_	_	_	_	_	_	_	-	_	_	_		SS1R	<3:0>		0000
FA90	SDI2R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FA90	SDIZK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		SDI2F	R<3:0>		0000
FA94	SS2R	31:16	-	_	_	_	_	_	_	_	-	_	_	_	_	_	_	-	0000
FA94	332K	15:0	-	_	_	_	_	_	_	_	-	_	_	_		SS2R	<3:0>		0000
EVBO	REFCLKIR	31:16	-	_	_	_	_	_	-	-	1	_	_	_	_	_	_	-	0000
FAD8	NEFULNIK	15:0	-	_	_	_	_	_	_	_	-	_	_	_		REFCL	(IR<3:0>		0000

PERIPHERAL PIN SELECT OUTPUT REGISTER MAP **TABLE 12-7:**

SSS										Bi	ts								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FB00	RPA0R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
. 200		15:0		_				_		_				_		RPA0	<3:0>		0000
FB04	RPA1R	31:16		_				_		_				_	_	_	_		0000
. 501		15:0	_	_	_	_	_	_	_	_	_	_	_			RPA1	<3:0>		0000
FB08	RPA2R	31:16	_	_	_	_	_	_	_	_	_	_	_			_	_	_	0000
1 000	MITALIN	15:0	_	_	_	_	_	_	_	_	_	_	_			RPA2	<3:0>		0000
FB0C	RPA3R	31:16	_	_	_	_	_	_	_	_	_	_	_		1		_	_	0000
1 500	MIMOR	15:0	_	_	_	_	_	_	_	_	_	_	_			RPA3	<3:0>		0000
FB10	RPA4R	31:16	_	_	_	_	_	_	_	_	_	_	_		1		_	_	0000
1 10	1(17(4)(15:0	_	_	_	_	_	_	_	_	_	_	_			RPA4	<3:0>		0000
FB20	RPA8R ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1 620	KFA0K.	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPA8	<3:0>		0000
FB24	RPA9R ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1 024	KEASK	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPA9	<3:0>		0000
FB2C	RPB0R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		0000
FBZC	KFBUK	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPB0	<3:0>		0000
FB30	RPB1R	31:16	_	_	_	_	_	_	_	-	_	_	_			-	_	_	0000
FB30	KPDIK	15:0	_	_	_	_	_	_	_	-	_	_	_			RPB1	<3:0>		0000
FB34	RPB2R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_		0000
FB34	KFD2K	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPB2	<3:0>		0000
FB38	RPB3R	31:16	_	_	_	_	_	_	_	-	_	_	_		-	-	_	_	0000
FB36	RPB3R	15:0	_	_	_	_	_	_	_	-	_	_	_			RPB3	<3:0>		0000
ED3C	RPB4R	31:16	_	_	_	_	_	_	_	-	_	_	_		-	-	_	_	0000
FB3C	KPD4K	15:0	_	_	-	-	-	_	-		_	-	-			RPB4	<3:0>	·	0000
ED 40	DDDED	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	-	_	_	0000
FB40	RPB5R	15:0	_	_	_	_	_	_	_	1	_	_	_	1		RPB5	<3:0>		0000
ED 44	DDDcD(2)	31:16	_	_	_	_	_	_	_	1	_	_	_	1	_	_	_		0000
FB44	RPB6R ⁽²⁾	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPB6	<3:0>		0000

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

Note 1: This register is only available on 44-pin devices.

This register is only available on USB devices.

2: 3: This register is only available on VBAT devices.

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	TABLE 12-7:	PERIPHERAL PIN SELECT OUTPUT REGISTER MAP ((CONTINUED)
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sse		_								Ві	its								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FB48	RPB7R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
1 1540	KFD/K	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPB7	' <3:0>		0000
FB4C	RPB8R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB4C	KFDOK	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPB8	3<3:0>		0000
FB50	RPB9R	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB30	KFD9K	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPB9	<3:0>		0000
FB54	RPB10R	31:16	1	1	_	1	1	_		1	_	_	_	_	1	-	_	1	0000
FB34	RPBIUR	15:0	1	1	_	1	1	_	_		_	_	_	_		RPB1	0<3:0>		0000
FB58	RPB11R	31:16	1	1	_	1	1	_	_		_	_	_	_	-	_	_	-	0000
FB36	RPBIIR	15:0	1	1	_	1	1	_	_		_	_	_	_		RPB1	1<3:0>		0000
EB60	RPB13R ⁽³⁾	31:16	1	1	_	1	1	_	_		_	_	_	_	-	_	_	-	0000
FB60	RPB13R ^(*)	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPB1	3<3:0>		0000
EDC4	DDD44D	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB64	RPB14R	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPB1	4<3:0>		0000
ED.CO	DDD4ED	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB68	RPB15R	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPB1	5<3:0>		0000
FDCC	DDCcD(1)	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB6C	RPC0R ⁽¹⁾	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPC)<3:0>		0000
ED70	RPC1R ⁽¹⁾	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB70	RPCTR	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPC1	<3:0>		0000
ED74	DDCcD(1)	31:16	-	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB74	RPC2R ⁽¹⁾	15:0	-	_	_	_	_	_	_	_	_	_	_	_		RPC2	2<3:0>		0000
ED.70	DD00D(1)	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB78	RPC3R ⁽¹⁾	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPC3	3<3:0>		0000
ED70	DDC 4D(1)	31:16	1	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB7C	RPC4R ⁽¹⁾	15:0		_	_	_	_	_	_	_	_	_	_	_		RPC4	l<3:0>		0000
FDOG	DD05D(1)	31:16	1	_	_	_	-	_	_	-	_	_	_	_	-	_	_	_	0000
FB80	RPC5R ⁽¹⁾	15:0	_	_	_	_	_	_	_	_	_	_	_	_		RPC5	<3:0>		0000

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

Note 1: This register is only available on 44-pin devices.

2:

This register is only available on USB devices.
This register is only available on VBAT devices.

TABLE 12-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

sse										Ві	its								
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
ED04	RPC6R ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
FB84	RPCoRt	15:0	_	_	_	1	_	-	I		-	_	-	_		RPC	i<3:0>		0000
ED00	RPC7R ⁽¹⁾	31:16	_	_	_	1	_	-	I		-	_	-	_	1	I	_	-	0000
FB88	RPC/R ⁽¹⁾	15:0	_	_	_	1	_	-	I		-	_	-	_		RPC7	'<3:0>		0000
FB8C	RPC8R ⁽¹⁾	31:16	_	_	_	1	_	-	I		-	_	-	_	1	I	_	-	0000
FB6C	RPCoRt	15:0	_	_	_	1	_	-	I		-	_	-	_		RPC	3<3:0>		0000
FB90	RPC9R ⁽¹⁾	31:16	_	_	_	1	_	1	1	1	1	_	1	_	1	1	_	1	0000
FB90	KFC9K ⁽¹⁾	15:0	_	_	_	1	_	1	1	1	1	_	1	_		RPCS	<3:0>		0000

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

This register is only available on 44-pin devices. Note 1:

This register is only available on USB devices.
This register is only available on VBAT devices.

2: 3:

REGISTER 12-1: [pin name]R: PERIPHERAL PIN SELECT INPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_		_	-			_
00:40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_		_			_	_
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	_		[pin name	P R<3:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

bit 3-0 [pin name]R<3:0>: Peripheral Pin Select Input bits

Where [pin name] refers to the pins that are used to configure peripheral input mapping. See Table 12-1 for input pin selection values.

Note: Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

REGISTER 12-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	_	_	_	_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	1	_	_		1	1
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	-	_	_		_	_
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	_		RPnR	<3:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-4 Unimplemented: Read as '0'

bit 3-0 RPnR<3:0>: Peripheral Pin Select Output bits

See Table 12-2 for output pin selection values.

Note: Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

REGISTER 12-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTX REGISTER (x = A, B, C)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	-		_			_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON	_	SIDL	_	-	_	_	_
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_	_	_	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 ON: Change Notice (CN) Control ON bit

1 = CN is enabled 0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 SIDL: Stop in Idle Control bit

1 = Idle mode halts CN operation0 = Idle does not affect CN operation

bit 12-0 Unimplemented: Read as '0'

13.0 TIMER1

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14.** "Timers" (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications.

The following modes are supported:

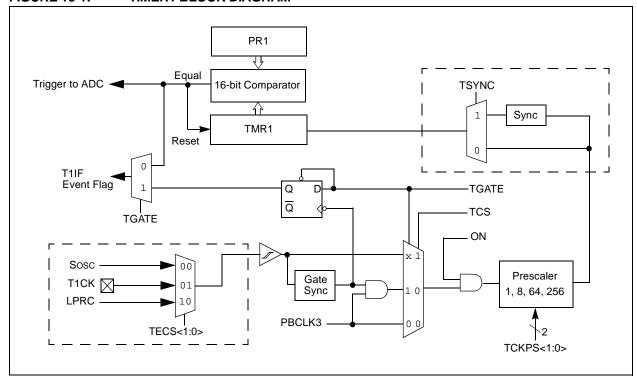
- · Synchronous Internal Timer
- · Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- · Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

Figure 13-1 illustrates a general block diagram of Timer1.

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



13.2 Timer1 Control Registers

TABLE 13-1: TIMER1 REGISTER MAP

Rits Bits Bits	17/1	16/0	Resets									
DO	17/1	16/0	Se									
발표 경기 경기 30/14 29/13 28/12 27/11 26/10 25/9 24/8 23/7 22/6 21/5 20/4 19/3 18/2		10,0	AII									
0600 T1CON 31:16 — — — — — — — — — — — — — — — — — — —	_	_	0000									
0600 TCON	TCS	_	0000									
0610 TMR1 31:16 — — — — — — — — — — — — — — — — — — —	_	_	0000									
15:0 TMR1<15:0>	TMR1<15:0> 000											
0620 PR1 31:16 — — — — — — — — — — — — — — — — —												
0020 PR1 15:0 PR1<15:0>	PR1<15:0> FFFF											

.egend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	-	_	-	-	_	-	_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	-	_			_	-	_	_
15.0	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	_	SIDL	TWDIS	TWIP	_	TECS	S<1:0>
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
7.0	TGATE	_	TCKPS	S<1:0>	_	TSYNC	TCS	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** Timer On bit⁽¹⁾

1 = Timer is enabled

0 = Timer is disabled

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12 TWDIS: Asynchronous Timer Write Disable bit

1 = Writes to Timer1 are ignored until pending write operation completes

0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

1 = Asynchronous write to the Timer1 register in progress

0 = Asynchronous write to Timer1 register is complete

In Synchronous Timer mode:

This bit is read as '0'.

bit 10 Unimplemented: Read as '0'

bit 9-8 TECS<1:0>: Timer1 External Clock Selection bits

11 = Reserved

10 = External clock comes from the LPRC

01 = External clock comes from the T1CK pin

00 = External clock comes from the Sosc

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6 Unimplemented: Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 5-4 TCKPS<1:0>: Timer Input Clock Prescale Select bits

11 = 1:256 prescale value

10 = 1:64 prescale value

01 = 1:8 prescale value

00 = 1:1 prescale value

bit 3 Unimplemented: Read as '0'

bit 2 TSYNC: Timer External Clock Input Synchronization Selection bit

When TCS = 1:

1 = External clock input is synchronized

0 = External clock input is not synchronized

When TCS = 0:

This bit is ignored.

bit 1 TCS: Timer Clock Source Select bit

1 = External clock is defined by the TECS<1:0> bits

0 = Internal peripheral clock

bit 0 Unimplemented: Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

14.0 TIMER2/3, TIMER4/5

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14.** "Timers" (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a freerunning interval timer for various timing applications and counting external events. The following modes are supported:

- · Synchronous internal 16-bit timer
- · Synchronous internal 16-bit gated timer
- · Synchronous external 16-bit timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

- · Synchronous internal 32-bit timer
- · Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

Note: In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through Timer5 in 16-bit

modes. In 32-bit modes, 'x' represents Timer2 or Timer4 and 'y' represents

Timer3 or Timer5.

14.1 Additional Supported Features

- · Selectable clock prescaler
- · Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 and Timer3 only)
- ADC event trigger (Timer3 in 16-bit mode, Timer2/3 in 32-bit mode)
- Fast bit manipulation using CLR, SET and INV registers

Figure 14-1 and Figure 14-2 illustrate block diagrams of Timer2/3 and Timer4/5.

FIGURE 14-1: TIMER2-TIMER5 BLOCK DIAGRAM (16-BIT)

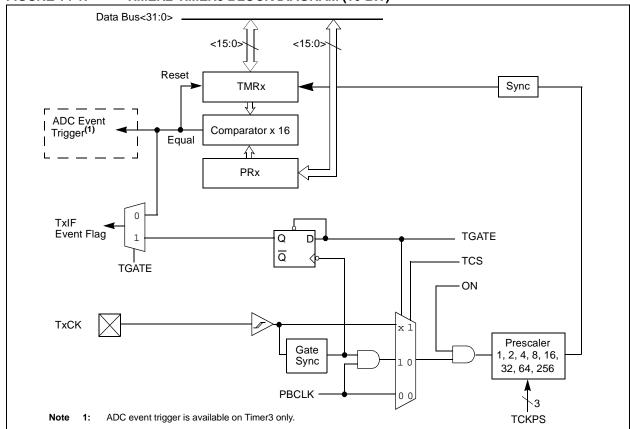
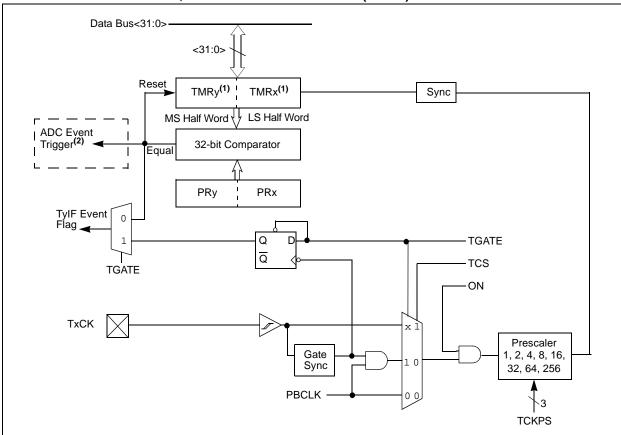


FIGURE 14-2: TIMER2/3, TIMER4/5 BLOCK DIAGRAM (32-BIT)



- **Note 1:** In this diagram, the use of 'x' in registers, TxCON, TMRx, PRx and TxCK, refers to either Timer2 or Timer4; the use of 'y' in registers, TyCON, TMRy, PRy, TyIF, refers to either Timer3 or Timer5.
 - 2: ADC event trigger is available only on the Timer2/3 pair.

14.2 Timer Control Registers

TABLE 14-1: TIMER2-TIMER5 REGISTER MAP

ess										Ві	ts								"
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0800	T2CON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	120011	15:0	ON	_	SIDL	_	_		_		TGATE		TCKPS<2:0:	>	T32	_	TCS	_	0000
0810	TMR2	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0010	TIVITAL	15:0								TMR2	<15:0>								0000
0820	PR2	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0020	1 112	15:0								PR2<	15:0>								FFFF
0A00	T3CON	31:16		_	_	_	_		_		_	_	_	_	_	_	_	_	0000
0,000	130011	15:0	ON	_	SIDL	_	_		_		TGATE		TCKPS<2:0:	>	_	_	TCS	_	0000
0A10	TMR3	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
OATO	TIVITO	15:0								TMR3	<15:0>								0000
0A20	PR3	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0/120	1110	15:0								PR3<	15:0>								FFFF
0000	T4CON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	14001	15:0	ON	_	SIDL	_	_	_	_	_	TGATE		TCKPS<2:0:	>	T32	_	TCS	_	0000
0C10	TMR4	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0010	TIVITY	15:0								TMR4	<15:0>								0000
0C20	PR4	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0020	1 134	15:0								PR4<	15:0>								FFFF
0E00	T5CON	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0200	15001	15:0	ON	_	SIDL	_	_	_	_	_	TGATE		TCKPS<2:0:	>	_	_	TCS	_	0000
0E10	TMR5	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
02.10	· wir to	15:0								TMR5	<15:0>								0000
0E20	PR5	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0220	1 110	15:0								PR5<	15:0>								FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information

TXCON: TYPE B TIMER CONTROL REGISTER REGISTER 14-1:

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	-	-	1	_	_	_
22,46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	-	-	1	-	_	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ^(1,3)	_	SIDL ⁽⁴⁾	_	-	_	_	_
7.0	R/W-0		R/W-0 R/W-0		R/W-0	U-0	R/W-0	U-0
7:0	TGATE ⁽³⁾	Т	CKPS<2:0>(3	3)	T32 ⁽²⁾	_	TCS ⁽³⁾	_

Legend:

W = Writable bit R = Readable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

ON: Timer On bit(1,3) bit 15

> 1 = Module is enabled 0 = Module is disabled

bit 14 Unimplemented: Read as '0' bit 13

SIDL: Stop in Idle Mode bit⁽⁴⁾

1 = Discontinue module operation when the device enters Idle mode 0 = Continue module operation when the device enters Idle mode

bit 12-8 Unimplemented: Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled 0 = Gated time accumulation is disabled

TCKPS<2:0>: Timer Input Clock Prescale Select bits(3) bit 6-4

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

- Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - 3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
 - While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

bit 3 T32: 32-Bit Timer Mode Select bit⁽²⁾

1 = Odd numbered and even numbered timers form a 32-bit timer

0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 Unimplemented: Read as '0'

bit 1 TCS: Timer Clock Source Select bit⁽³⁾

1 = External clock from TxCK pin

0 = Internal peripheral clock

bit 0 Unimplemented: Read as '0'

- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
 - **4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

NOTES:

15.0 WATCHDOG TIMER (WDT)

Note:

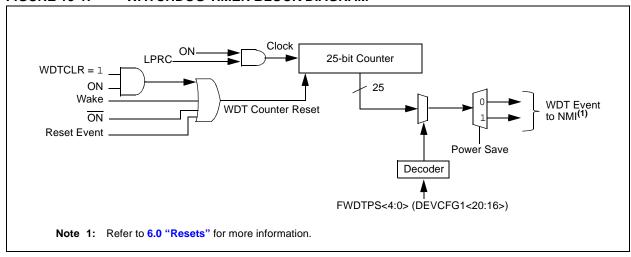
This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9.** "Watchdog, **Deadman, and Power-up Timers**" (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

When enabled, the Watchdog Timer (WDT) operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are key features of the WDT module:

- · Configuration or software controlled
- · User-configurable time-out period
- Can wake up the device from Sleep or Idle mode

FIGURE 15-1: WATCHDOG TIMER BLOCK DIAGRAM



15.1 Watchdog Timer Control Registers

TABLE 15-1: WATCHDOG TIMER REGISTER MAP

ess		ø									Bits								S
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
F000	WDTCON ⁽¹⁾	31:16					WDTCLRKEY<15:0> 0000												
F600	WDTCON	15:0	ON	I	_	RUNDIV<4:0>							xxxx						

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
31:24				WDTCLRI	<ey<15:8></ey<15:8>			
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
23:16				WDTCLR	KEY<7:0>			
45.0	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
15:8	ON ⁽¹⁾	_	_			RUNDIV<4:0)>	
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
7:0	_	_	_	_	_	_	_	WDTWINEN

Legend:y = Values set from Configuration bits on PORR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 WDTCLRKEY<15:0>: Watchdog Timer Clear Key bits

To clear the Watchdog Timer to prevent a time-out, software must write the value 0x5743 to these bits using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit⁽¹⁾

1 = The Watchdog Timer module is enabled 0 = The Watchdog Timer module is disabled

bit 14-13 Unimplemented: Read as '0'

bit 12-8 RUNDIV<4:0>: Watchdog Timer Postscaler Value in Run Mode bits

In Run mode, these bits are set to the values of the WDTPS<4:0> Configuration bits in DEVCFG1.

bit 7-1 Unimplemented: Read as '0'

bit 0 WDTWINEN: Watchdog Timer Window Enable bit

1 = Enable windowed Watchdog Timer0 = Disable windowed Watchdog Timer

Note 1: This bit only has control when FWDTEN (DEVCFG1<23>) = 0.

NOTES:

16.0 DEEP SLEEP WATCHDOG TIMER (DSWDT)

Note:

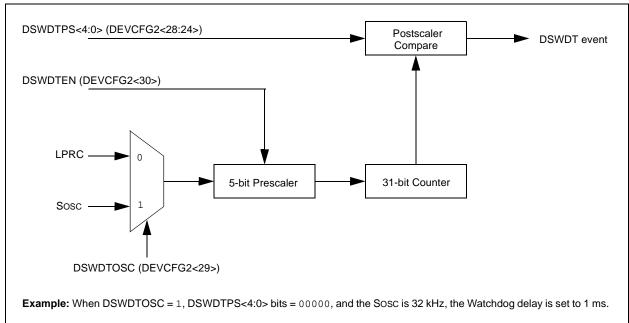
This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9.** "Watchdog, **Deadman, and Power-up Timers**" (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Deep Sleep Watchdog Timer (DSWDT) is a dedicated Watchdog Timer for Deep Sleep mode operations of the device. The DSWDT is very useful in battery-powered applications and in low-power modes of operations.

The primary function of the DSWDT is to automatically exit Deep Sleep mode after a prescribed amount of time has elapsed.

The DSWDT is controlled through the DEVCFG2 Configuration register at boot time (one-time programmable per POR). When enabled through the DSWDTEN bit in DEVCFG2, the DSWDT operates either from the internal Low-Power RC (LPRC) clock or from the Secondary Oscillator (Sosc). The clock selection for the DSWDT is done through the DSWDTOSC bit in the DEVCFG2 register.

FIGURE 16-1: DEEP SLEEP WATCHDOG TIMER BLOCK DIAGRAM



NOTES:

17.0 INPUT CAPTURE

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- · Simple capture event modes:
 - Capture timer value on every rising and falling edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

- · Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

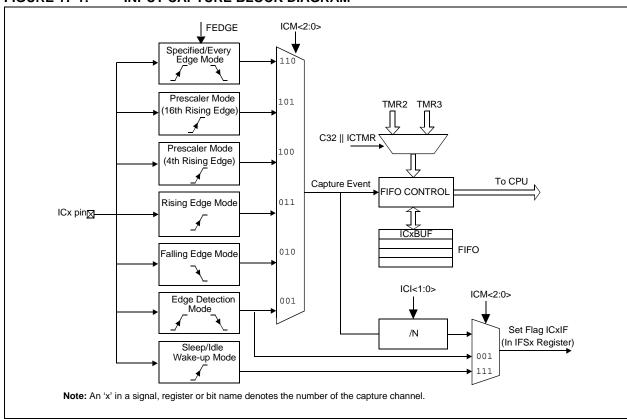
Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- · Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- Input capture can also be used to provide additional sources of external interrupts

Figure 17-1 illustrates a general block diagram of the Input Capture module.

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



17.1 Input Capture Control Registers

TABLE 17-1: INPUT CAPTURE 1-INPUT CAPTURE 5 REGISTER MAP

ess										Bi	ts								(0
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	IC1CON ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_		_	_	_	_	_	_	0000
2000	1010014	15:0	ON	_	SIDL	_	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
2010	IC1BUF	31:16								IC1BUF	<31:0>								xxxx
		15:0		1							10 1107				1	1	1		xxxx
2200	IC2CON ⁽¹⁾	31:16		_	_	_			_		_	_	_	_	_	_	_	_	0000
	.0200.1	15:0	ON	_	SIDL	_	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
2210	IC2BUF	31:16 15:0	IC2BUF<31:0> XXXX XXXX												xxxx				
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
2400	IC3CON ⁽¹⁾	15:0	ON	_	SIDL	_	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>								xxxx
	10.1001(1)	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
2600	IC4CON ⁽¹⁾	15:0	ON	_	SIDL	_	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
2610	IC4BUF	31:16 15:0								IC4BUF	<31:0>				•	•			xxxx
2800	IC5CON ⁽¹⁾	31:16 15:0												0000					
-																			
2810	IC5BUF	31:16 15:0																	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 17-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	
22:40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	_	SIDL	_	_	_	FEDGE	C32
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
7:0	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	

Legend:

bit 8

bit 7

R = Readable bit W = Writable bit U = Unimplemented bit

-n = Bit Value at POR: ('0', '1', x = unknown) P = Programmable bit r = Reserved bit

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** Input Capture Module Enable bit⁽¹⁾

1 = Module is enabled

0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0' bit 13 **SIDL:** Stop in Idle Control bit

1 = Halt in Idle mode

0 = Continue to operate in Idle mode

bit 12-10 Unimplemented: Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)

1 = Capture rising edge first0 = Capture falling edge firstC32: 32-bit Capture Select bit

1 = 32-bit timer resource capture 0 = 16-bit timer resource capture

ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')

0 = Timer3 is the counter source for capture 1 = Timer2 is the counter source for capture

bit 6-5 ICI<1:0>: Interrupt Control bits

11 = Interrupt on every fourth capture event
 10 = Interrupt on every third capture event
 01 = Interrupt on every second capture event

00 = Interrupt on every capture event

bit 4 ICOV: Input Capture Overflow Status Flag bit (read-only)

1 = Input capture overflow has occurred0 = No input capture overflow has occurred

bit 3 ICBNE: Input Capture Buffer Not Empty Status bit (read-only)

1 = Input capture buffer is not empty; at least one more capture value can be read

0 = Input capture buffer is empty

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

bit 2-0 ICM<2:0>: Input Capture Mode Select bits

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode every sixteenth rising edge
- 100 = Prescaled Capture Event mode every fourth rising edge
- 011 = Simple Capture Event mode every rising edge
- 010 = Simple Capture Event mode every falling edge
- 001 = Edge Detect mode every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

18.0 OUTPUT COMPARE

Note:

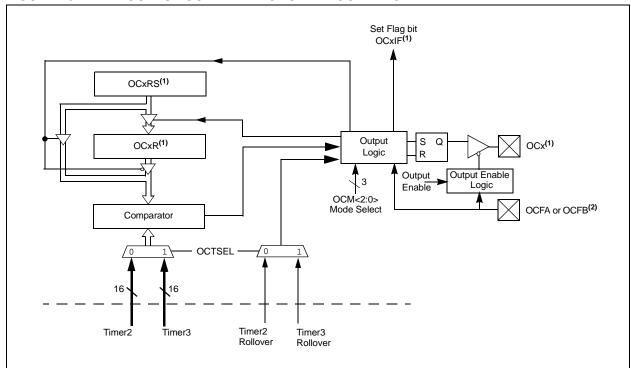
This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features of the Output Compare module:

- Multiple Output Compare Modules in a device
- Programmable interrupt generation on compare event
- · Single and Dual Compare modes
- Single and continuous output pulse generation
- · Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 18-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



- **Note 1:** Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.
 - 2: The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

18.1 Output Compare Control Registers

TABLE 18-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP

ess										Bi	ts								
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	OC1CON	31:16 15:0	– ON	1 1	— SIDL	_		1 1					— OC32	— OCFLT	OCTSEL	1	— OCM<2:0>	_	0000
3010	OC1R	31:16 15:0								OC1R	<31:0>								xxxx
3020	OC1RS	31:16 15:0								OC1RS	<31:0>								xxxx
3200	OC2CON	31:16 15:0	ON		— SIDL	_							— OC32	OCFLT	OCTSEL	_	OCM<2:0>	_	0000
3210	OC2R	31:16 15:0	011		O.D.L					OC2R-			0002	00.2.	001022		OOM (2.0)		xxxx
3220	OC2RS	31:16 15:0								OC2RS	<31:0>								xxxx
3400	OC3CON	31:16 15:0	ON		- SIDL								— OC32	OCFLT	OCTSEL	-	OCM<2:0>	_	0000
3410	OC3R	31:16 15:0								OC3R	<31:0>			•					xxxx
3420	OC3RS	31:16 15:0								OC3RS	<31:0>								xxxx
3600	OC4CON	31:16 15:0	ON		- SIDL	_							— ОС32	OCFLT	OCTSEL	_	OCM<2:0>	_	0000
3610	OC4R	31:16 15:0			•					OC4R	<31:0>			•	1				xxxx
3620	OC4RS	31:16 15:0								OC4RS	<31:0>								xxxx
3800	OC5CON	31:16 15:0	ON	_ _	— SIDL	_ _	_	_ _	_ _	_	_	_ _	— OC32	OCFLT	OCTSEL	_	— OCM<2:0>	_	0000
3810	OC5R	31:16 15:0			I					OC5R-	<31:0>			I					xxxx
3820	OC5RS	31:16 15:0								OC5RS	<31:0>								xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 18-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	-
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	_	SIDL	_	_	_	_	_
7.0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	OC32	OCFLT ⁽²⁾	OCTSEL		OCM<2:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit⁽¹⁾

1 = Output Compare peripheral is enabled

0 = Output Compare peripheral is disabled

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12-6 Unimplemented: Read as '0'

bit 5 OC32: 32-bit Compare Mode bit

1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source

0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 OCFLT: PWM Fault Condition Status bit⁽²⁾

1 = PWM Fault condition has occurred (cleared in hardware only)

0 = No PWM Fault condition has occurred

bit 3 OCTSEL: Output Compare Timer Select bit

1 = Timer3 is the clock source for this Output Compare module

0 = Timer2 is the clock source for this Output Compare module

bit 2-0 OCM<2:0>: Output Compare Mode Select bits

111 = PWM mode on OCx; Fault pin enabled

110 = PWM mode on OCx; Fault pin disabled

101 = Initialize OCx pin low; generate continuous output pulses on OCx pin

100 = Initialize OCx pin low; generate single output pulse on OCx pin

011 = Compare event toggles OCx pin

010 = Initialize OCx pin high; compare event forces OCx pin low

001 = Initialize OCx pin low; compare event forces OCx pin high

000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

NOTES:

19.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note:

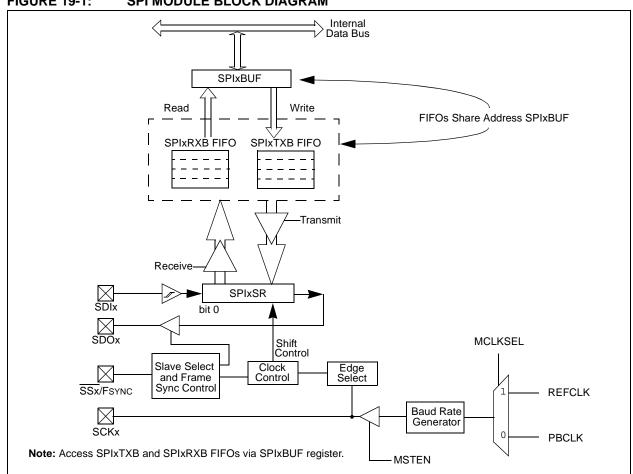
This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23.** "**Serial Peripheral Interface (SPI)**" (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontrollers. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

The following are key features of the SPI module:

- · Master mode and Slave mode support
- · Four clock formats
- · Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
 - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
 - I²S protocol
 - Left-justified
 - Right-justified
 - PCM

FIGURE 19-1: SPI MODULE BLOCK DIAGRAM



19.1 SPI Control Registers

TABLE 19-1: SPI1 AND SPI2 REGISTER MAP

	LL 13-1			0 01 12 1															
ess										Bi	ts								
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5900	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FF	RMCNT<2:0)>	MCLKSEL	_	I	-	_	_	SPIFE	ENHBUF	0000
3000	SFITCON	15:0	ON	_	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISE	EL<1:0>	0000
E010	SPI1STAT	31:16	_	_	_		RXE	BUFELM<4:	0>		_	_	1		TX	BUFELM<4	:0>		0000
5610	SFIISTAI	15:0	_	_	_	FRMERR	SPIBUSY	_	I	SPITUR	SRMT	SPIROV	SPIRBE		SPITBE	_	SPITBF	SPIRBF	0008
5820	SPI1BUF	31:16								DATA-	31.0~								0000
3620	OI IIDOI	15:0					DATA<31:0>								0000				
5830	SPI1BRG	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
3030		15:0		_	_						E	BRG<12:0>							0000
		31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5840	SPI1CON2	15:0	SPI SGNEXT	_	_	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	_	_	_	AUD MONO	_	AUDMO	D<1:0>	0000
E A O O	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FF	RMCNT<2:0)>	MCLKSEL	_	1		_	_	SPIFE	ENHBUF	0000
5A00	SFIZCON	15:0	ON	_	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISE	EL<1:0>	0000
E A 10	SPI2STAT	31:16	_	_	_		RXE	BUFELM<4:	0>		_	-			TX	BUFELM<4	l:0>		0000
5A IU	SFIZSTAT	15:0		_	_	FRMERR	SPIBUSY	_	_	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	0008
5A20	SPI2BUF	31:16								DATA<	31.0~								0000
3A20	31 12D01	15:0								DAIA	.51.02								0000
5430	SPI2BRG	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
JA30	OI IZBICO	15:0		_	_		•				E	BRG<12:0>							0000
		31:16	_	_	_	1	_	_	1		_	_			_	_	_	_	0000
5A40	SPI2CON2	15:0	SPI SGNEXT	_	_	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	_		_	AUD MONO	_	AUDMO	D<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 19-1: SPIXCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	F	RMCNT<2:0)>
00.40	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
23:16	MCLKSEL ⁽²⁾	_	_	_	_	_	SPIFE	ENHBUF ⁽²⁾
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	_	SIDL	DISSDO	MODE32	MODE16	SMP	CKE ⁽³⁾
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	SSEN	CKP ⁽⁴⁾	MSTEN	DISSDI	STXISE	L<1:0>	SRXIS	EL<1:0>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 FRMEN: Framed SPI Support bit

1 = Framed SPI support is enabled (SSx pin used as FSYNC input/output)

0 = Framed SPI support is disabled

bit 30 FRMSYNC: Frame Sync Pulse Direction Control on SSx pin bit (Framed SPI mode only)

1 = Frame sync pulse input (Slave mode)

0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)

1 = Frame pulse is active-high

0 = Frame pulse is active-low

bit 28 MSSEN: Master Mode Slave Select Enable bit

1 = Slave select SPI support enabled. The SS pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.

0 = Slave select SPI support is disabled.

bit 27 FRMSYPW: Frame Sync Pulse Width bit

1 = Frame sync pulse is one character wide

0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in FRAMED_SYNC mode.

111 = Reserved; do not use

110 = Reserved; do not use

101 = Generate a frame sync pulse on every 32 data characters

100 = Generate a frame sync pulse on every 16 data characters

011 = Generate a frame sync pulse on every 8 data characters

010 = Generate a frame sync pulse on every 4 data characters

001 = Generate a frame sync pulse on every 2 data characters 000 = Generate a frame sync pulse on every data character

bit 23 MCLKSEL: Master Clock Enable bit⁽²⁾

1 = REFCLK is used by the Baud Rate Generator

0 = PBCLK is used by the Baud Rate Generator

bit 22-18 Unimplemented: Read as '0'

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit can only be written when the ON bit = 0.

3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

REGISTER 19-1: SPIXCON: SPI CONTROL REGISTER (CONTINUED)

- bit 17 SPIFE: Frame Sync Pulse Edge Select bit (Framed SPI mode only)
 - 1 = Frame synchronization pulse coincides with the first bit clock
 - 0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF**: Enhanced Buffer Enable bit⁽²⁾
 - 1 = Enhanced Buffer mode is enabled
 - 0 = Enhanced Buffer mode is disabled
- bit 15 **ON:** SPI Peripheral On bit⁽¹⁾
 - 1 = SPI Peripheral is enabled
 - 0 = SPI Peripheral is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 SIDL: Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode
- bit 12 DISSDO: Disable SDOx pin bit
 - 1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
 - 0 = SDOx pin is controlled by the module
- bit 11-10 MODE<32.16>: 32/16-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE16	Communication
x	32-bit
1	16-bit
0	8-bit
	x 1

bit 9 SMP: SPI Data Input Sample Phase bit

Master mode (MSTEN = 1):

- 1 = Input data sampled at end of data output time
- 0 = Input data sampled at middle of data output time

Slave mode (MSTEN = 0):

SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

To write a '1' to this bit, the MSTEN value = 1 must first be written.

- bit 8 **CKE**: SPI Clock Edge Select bit⁽³⁾
 - 1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
 - 0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)
- bit 7 SSEN: Slave Select Enable (Slave mode) bit
 - $1 = \overline{SSx}$ pin used for Slave mode
 - $0 = \overline{SSx}$ pin not used for Slave mode, pin controlled by port function.
- bit 6 **CKP:** Clock Polarity Select bit⁽⁴⁾
 - 1 = Idle state for clock is a high level; active state is a low level
 - 0 = Idle state for clock is a low level; active state is a high level
- Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit can only be written when the ON bit = 0.
 - 3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - **4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

REGISTER 19-1: SPIXCON: SPI CONTROL REGISTER (CONTINUED)

- bit 5 MSTEN: Master Mode Enable bit
 - 1 = Master mode
 - 0 = Slave mode
- bit 4 DISSDI: Disable SDI bit
 - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 - 10 = Interrupt is generated when the buffer is empty by one-half or more
 - 01 = Interrupt is generated when the buffer is completely empty
 - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
 - 11 = Interrupt is generated when the buffer is full
 - 10 = Interrupt is generated when the buffer is full by one-half or more
 - 01 = Interrupt is generated when the buffer is not empty
 - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- Note 1: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit can only be written when the ON bit = 0.
 - 3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
 - **4:** When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

REGISTER 19-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_			-	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	_	_	_	_	_	_	_
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.6	SPISGNEXT	_	_	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7.0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	AUDEN ⁽¹⁾	1	_	_	AUDMONO ^(1,2)	1	AUDMOD	<1:0> ^(1,2)

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit

1 = Data from RX FIFO is sign extended

0 = Data from RX FIFO is not sign extended

bit 14-13 Unimplemented: Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit

1 = Frame Error overflow generates error events

0 = Frame Error does not generate error events

bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit

1 = Receive overflow generates error events

0 = Receive overflow does not generate error events

bit 10 SPITUREN: Enable Interrupt Events via SPITUR bit

1 = Transmit underrun generates error events

0 = Transmit underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)

1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data

0 = A ROV is a critical error that stops SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)

1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty

0 = A TUR is a critical error that stops SPI operation

bit 7 AUDEN: Enable Audio CODEC Support bit (1)

1 = Audio protocol enabled

0 = Audio protocol disabled

bit 6-5 Unimplemented: Read as '0'

bit 3 AUDMONO: Transmit Audio Data Format bit (1,2)

1 = Audio data is mono (Each data word is transmitted on both left and right channels)

0 = Audio data is stereo

bit 2 Unimplemented: Read as '0'

bit 1-0 AUDMOD<1:0>: Audio Protocol Mode bit(1,2)

11 = PCM/DSP mode

10 = Right-Justified mode

01 = Left-Justified mode

 $00 = I^2S \text{ mode}$

Note 1: This bit can only be written when the ON bit = 0.

2: This bit is only valid for AUDEN = 1.

REGISTER 19-3: SPIXSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
31:24	_	_	_		R)	XBUFELM<4:0	0>	
22.40	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
23:16	_	_	_		T	(BUFELM<4:0)>	
45.0	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
15:8	_	_	_	FRMERR	SPIBUSY	_	_	SPITUR
7.0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
7:0	SRMT	SPIROV	SPIRBE	-	SPITBE	_	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Set in hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared $x = Bit$ is unk	nown

bit 31-29 Unimplemented: Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 Unimplemented: Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 Unimplemented: Read as '0'

bit 12 FRMERR: SPI Frame Error status bit

1 = Frame error detected0 = No Frame error detected

This bit is only valid when FRMEN = 1.

bit 11 SPIBUSY: SPI Activity Status bit

1 = SPI peripheral is currently busy with some transactions

0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 SPITUR: Transmit Under Run bit

1 = Transmit buffer has encountered an underrun condition

0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)

1 = When SPI module shift register is empty

0 = When SPI module shift register is not empty

bit 6 SPIROV: Receive Overflow Flag bit

1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.

0 = No overflow has occurred

This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

bit 5 SPIRBE: RX FIFO Empty bit (valid only when ENHBUF = 1)

1 = RX FIFO is empty (CRPTR = SWPTR)

0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 Unimplemented: Read as '0'

REGISTER 19-3: SPIXSTAT: SPI STATUS REGISTER

- bit 3 SPITBE: SPI Transmit Buffer Empty Status bit
 - 1 = Transmit buffer, SPIxTXB is empty
 - 0 = Transmit buffer, SPIxTXB is not empty

Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

- bit 2 Unimplemented: Read as '0'
- bit 1 SPITBF: SPI Transmit Buffer Full Status bit
 - 1 = Transmit not yet started, SPITXB is full
 - 0 = Transmit buffer is not full

Standard Buffer Mode:

Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB. Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.

Enhanced Buffer Mode:

Set when CWPTR + 1 = SRPTR; cleared otherwise

- bit 0 SPIRBF: SPI Receive Buffer Full Status bit
 - 1 = Receive buffer, SPIxRXB is full
 - 0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise

20.0 INTER-INTEGRATED CIRCUIT (I²C)

Note:

This data sheet summarizes PIC32MX1XX/2XX features of the 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 24. "Inter-Integrated Circuit (I^2C) " (DS60001116), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

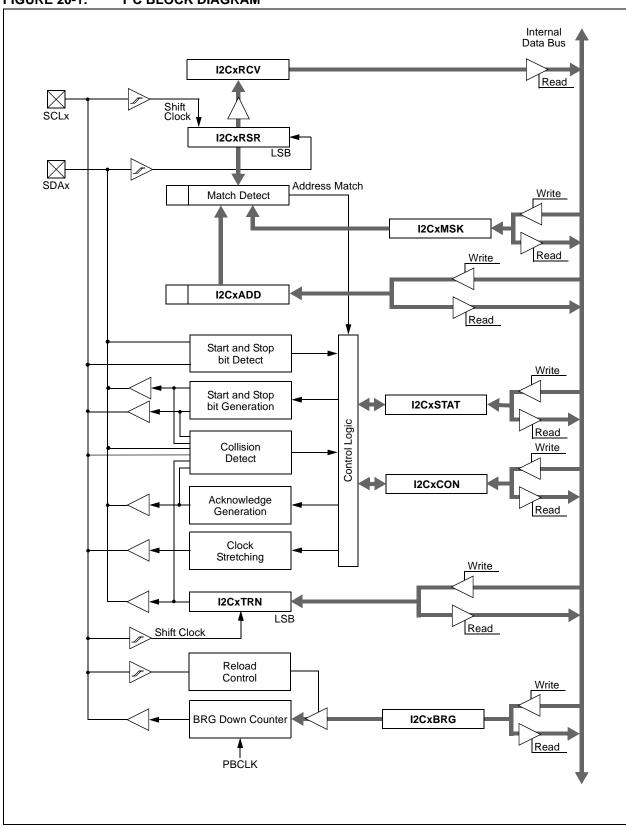
The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard. Figure 20-1 illustrates the I²C module block diagram.

Each I²C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- · Provides support for address bit masking

FIGURE 20-1: I²C BLOCK DIAGRAM



20.1 I²C Control Registers

TABLE 20-1: I2C1 AND I2C2 REGISTER MAP

ess										Bi	ts								(0
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5000	I2C1CON	31:16	_	_	_	-		_	— —	-						_	-		0000
		15:0 31:16	ON	_	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5010	I2C1STAT	15:0	— ACKSTAT	TRSTAT		_		BCL	GCSTAT	ADD10	IWCOL	I2COV	— D А	— Р		R_W	RBF	— TBF	0000
		31:16	—	—		_		— —	—	ADD 10	IVVCOL	12000	D_A	г	<u> </u>	K_VV		—	0000
5020	I2C1ADD	15:0										_	Address	Register			_		0000
		31:16	_	_	_	_	_		_	_		_	_	_	_	_	_	_	0000
5030	I2C1MSK	15:0	_	_	_	_	_	_					Address Ma	ısk Register					0000
5040	IOCADDO	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5040	I2C1BRG	15:0	_	_	_	_					Bau	id Rate Ger	erator Reg	ster					0000
5050	I2C1TRN	31:16	_	_	_	_	_	_	_		_	_	_		-	_	_	_	0000
3030	IZCTTKIN	15:0	_	_	_	_		_	_					Transmit	Register				0000
5060	I2C1RCV	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0000	12011101	15:0	_	_		_	_		_			I	I	Receive	Register		1		0000
5100	I2C2CON	31:16	_	_	_	_	_	_	_	_		_	_	_	_	_	_		0000
		15:0	ON	_	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
5110	I2C2STAT	31:16				_		_	_			-		_	_				0000
			ACKSTAT	TRSTAT		_		BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
5120	I2C2ADD	31:16	_	_	_	_	_		_	_	_	_	A -1 -1	—	_	_	_	_	0000
		15:0 31:16	_	_		_			_	_		_	Address	Register	_	_	_	_	0000
5130	I2C2MSK	15:0							_				Address Ma	sk Register		_		_	0000
		31:16							_	_		_	Address Mic	isk ivegister	_	_	_	_	0000
5140	I2C2BRG	15:0	_	_	_	_					Bau	ıd Rate Ger	erator Red	ster					0000
		31:16	_	_	_	_	_	_	_	_	_		—	_	_	_	_	_	0000
5150	I2C2TRN	15:0	_	_	_	_	_	_	_	— Transmit Register						0000			
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
5160	I2C2RCV	15:0	_	_	_	_	_	_	_	_				Receive	Register				0000

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

REGISTER 20-1: I2CXCON: I²C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00:40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	_	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7.0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
7:0	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend: HC = Cleared in Hardware

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 ON: I²C Enable bit⁽¹⁾

1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins

 $0 = \text{Disables the } I^2\text{C module}$; all $I^2\text{C pins}$ are controlled by PORT functions

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)

1 = Release SCLx clock

0 = Hold SCLx clock low (clock stretch)

If STREN = 1:

Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:

Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

- bit 11 STRICT: Strict I²C Reserved Address Rule Enable bit
 - 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
 - 0 = Strict I²C Reserved Address Rule not enabled
- bit 10 A10M: 10-bit Slave Address bit
 - 1 = I2CxADD is a 10-bit slave address
 - 0 = I2CxADD is a 7-bit slave address
- bit 9 DISSLW: Disable Slew Rate Control bit
 - 1 = Slew rate control disabled
 - 0 = Slew rate control enabled
- bit 8 SMEN: SMBus Input Levels bit
 - 1 = Enable I/O pin thresholds compliant with SMBus specification
 - 0 = Disable SMBus input thresholds
- Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-1: I2CxCON: I²C CONTROL REGISTER (CONTINUED)

- bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
 - 1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
 - 0 = General call address is disabled
- bit 6 STREN: SCLx Clock Stretch Enable bit (when operating as I²C slave)

Used in conjunction with SCLREL bit.

- 1 = Enable software or receive clock stretching
- 0 = Disable software or receive clock stretching
- bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)

Value that is transmitted when the software initiates an Acknowledge sequence.

- 1 = Send a NACK during an Acknowledge sequence
- 0 = Send an ACK during an Acknowledge sequence
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as I²C master, applicable during master receive)
 - 1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence.
 - 0 = Acknowledge sequence not in progress
- bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)
 - 1 = Enables Receive mode for I^2C . Hardware clear at end of eighth bit of master receive data byte.
 - 0 = Receive sequence not in progress
- bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)
 - 1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.
 - 0 = Stop condition not in progress
- bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)
 - 1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.
 - 0 = Repeated Start condition not in progress
- bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)
 - 1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.
 - 0 = Start condition not in progress
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-2: I2CXSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04:04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
15:8	ACKSTAT	TRSTAT	_		_	BCL	GCSTAT	ADD10
7.0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
7:0	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF

Legend:HS = Set in hardwareHSC = Hardware set/clearedR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedC = Clearable bit

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C master, applicable to master transmit operation)
 - 1 = Acknowledge was not received from slave
 - 0 = Acknowledge was received from slave

Hardware set or clear at end of slave Acknowledge.

- bit 14 TRSTAT: Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
 - 1 = Master transmit is in progress (8 bits + ACK)
 - 0 = Master transmit is not in progress

Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

- bit 13-11 Unimplemented: Read as '0'
- bit 10 BCL: Master Bus Collision Detect bit
 - 1 = A bus collision has been detected during a master operation
 - 0 = No collision

Hardware set at detection of bus collision. This condition can only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module.

- bit 9 GCSTAT: General Call Status bit
 - 1 = General call address was received
 - 0 = General call address was not received

Hardware set when address matches general call address. Hardware clear at Stop detection.

- bit 8 ADD10: 10-bit Address Status bit
 - 1 = 10-bit address was matched
 - 0 = 10-bit address was not matched

Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

- bit 7 IWCOL: Write Collision Detect bit
 - 1 = An attempt to write the I2CxTRN register failed because the I 2 C module is busy
 - 0 = No collision

Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

- bit 6 I2COV: Receive Overflow Flag bit
 - 1 = A byte was received while the I2CxRCV register is still holding the previous byte
 - 0 = No overflow

Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
 - 1 = Indicates that the last byte received was data
 - 0 = Indicates that the last byte received was device address

Hardware clear at device address match. Hardware set by reception of slave byte.

REGISTER 20-2: I2CxSTAT: I²C STATUS REGISTER (CONTINUED)

- bit 4 P: Stop bit
 - 1 = Indicates that a Stop bit has been detected last
 - 0 = Stop bit was not detected last

Hardware set or clear when Start, Repeated Start or Stop detected.

- bit 3 S: Start bit
 - 1 = Indicates that a Start (or Repeated Start) bit has been detected last
 - 0 = Start bit was not detected last

Hardware set or clear when Start, Repeated Start or Stop detected.

- bit 2 $\mathbf{R}_{\mathbf{W}}$: Read/Write Information bit (when operating as I^2 C slave)
 - 1 = Read indicates data transfer is output from slave
 - 0 = Write indicates data transfer is input to slave

Hardware set or clear after reception of I²C device address byte.

- bit 1 RBF: Receive Buffer Full Status bit
 - 1 = Receive complete, I2CxRCV is full
 - 0 = Receive not complete, I2CxRCV is empty

Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

- bit 0 TBF: Transmit Buffer Full Status bit
 - 1 = Transmit in progress, I2CxTRN is full
 - 0 = Transmit complete, I2CxTRN is empty

Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

NOTES:

21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107), which available from the Documentation > Reference Manual section of the PIC32 Microchip web site (www.microchip.com/pic32).

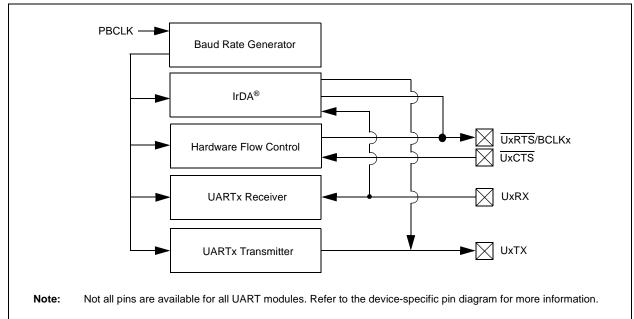
The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX 28/44-pin XLP Family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The UART module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The following are key features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- · Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 33.4 bps to 17.5 Mbps at 72 MHz
- 8-level deep First In First Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- · LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support
- Auto-baud support
- · Ability to receive data during Sleep mode

Figure 21-1 illustrates a simplified block diagram of the UART module.

FIGURE 21-1: UART SIMPLIFIED BLOCK DIAGRAM



21.1 UART Control Registers

TABLE 21-1: UART1 AND UART2 REGISTER MAP

ess		•								Ві	ts								"
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6000	U1MODE ⁽¹⁾	31:16	_	_	_			_	_	1	SLPEN	ACTIVE	_	_	_	CLKSE	L<1:0>	RUNOVF	0000
0000	OTWODE	15:0	ON	-	SIDL	IREN	RTSMD	_	UEN-	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEI	L<1:0>	STSEL	0000
6010	U1STA ⁽¹⁾	31:16	31:16 MASK<7:0> ADDR<7:0>											0000					
6010	UISIA	15:0	UTXISE	L<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISE	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
6020	LIATABEC	31:16	_	_	_	_	_	_	_	_	_	_		_	_	_	_	_	0000
0020	6020 U1TXREG		_	_	_	_	_	_	_	TX8	Transmit Register				0000				
6020	6030 U1RXREG	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6030	UIKAKEG	15:0	_	_	_	_	_	_	_	RX8	Receive Register				0000				
6040	U1BRG ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
6040	UIBKG,	15:0							Baud	Rate Gen	erator Pres	caler							0000
0000	U2MODE ⁽¹⁾	31:16		_	_	_			_	_	SLPEN	ACTIVE	-	_	_	CLKSE	L<1:0>	RUNOVF	0000
6200	UZMODE	15:0	ON	_	SIDL	IREN	RTSMD	_	UEN-	<1:0>	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEI	L<1:0>	STSEL	0000
2040	U2STA ⁽¹⁾	31:16				MASK	<7:0>					l .	<u> </u>	ADDR	<7:0>	l .			0000
6210	U251A**	15:0	UTXISE	L<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISE	EL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
0000	LIOTYDEO	31:16	_	_	_		_	_	_	_	_	_	_	_	_	_	_	_	0000
6220	U2TXREG	15:0	_	_	_	-	_	_	_	TX8		•		Transmit	Register	•			0000
6220	HARVEC	31:16	_	-	_		_	_	_	_		_	_	_	_	_	_	_	0000
0230	U2RXREG	15:0	_	-	_		_	_	-	RX8				Receive	Register				0000
6240	U2BRG ⁽¹⁾	31:16	_	-	_		_	_	_	_	_	_	_	_	_	_	_	_	0000
6240	UZBKG**/	15:0							Baud	Rate Gen	erator Pres	caler							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 21-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31:24	_	_	-	-	_		_	_
00.40	R/W-0	R-0, HS, HC	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
23:16	SLPEN	ACTIVE	_	_	_	CLKSE	RUNOVF	
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	ON	_	SIDL	IREN	RTSMD	_	UEN<	1:0> ⁽¹⁾
7.0	R/W-0	R/W-0						
7:0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL	-<1:0>	STSEL

Legend:HS = Hardware setHC = Hardware clearedR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit 23 SLPEN: Run During Sleep Enable bit

1 = UARTx BRG clock runs during Sleep mode

0 = UARTx BRG clock is turned off during Sleep mode

Note: SLPEN = 1 only applies if CLKSEL = FRC. All clocks, as well as the UART, are disabled in Deep

Sleep mode.

bit 22 ACTIVE: UARTx Module Running Status bit

1 = UARTx module is active (UxMODE register should not be updated)

0 = UARTx module is not active (UxMODE register can be updated)

bit 21-19 Unimplemented: Read as '0'

bit 18-17 CLKSEL<1:0>: UARTx Module Clock Selection bits

11 = BRG clock is PBCLK2

10 = BRG clock is FRC

01 = BRG clock is SYSCLK (turned off in Sleep mode)

00 = BRG clock is PBCLK2 (turned off in Sleep mode)

bit 16 RUNOVF: Run During Overflow Condition Mode bit

1 = When an Overflow Error (OERR) condition is detected, the shift register continues to run to remain synchronized

0 = When an Overflow Error (OERR) condition is detected, the shift register stops accepting new data (Legacy mode)

bit 15 ON: UARTx Enable bit

1 = UARTx module is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits

0 = UARTx module is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx, and LATx registers; UARTx power consumption is minimal

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Discontinue operation when device enters Idle mode

0 = Continue operation in Idle mode

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **12.3** "Peripheral Pin Select" for more information).

REGISTER 21-1: UxMODE: UARTX MODE REGISTER (CONTINUED)

- bit 12 IREN: IrDA® Encoder and Decoder Enable bit
 - 1 = IrDA is enabled
 - 0 = IrDA is disabled
- bit 11 RTSMD: Mode Selection for UxRTS Pin bit
 - $1 = \overline{\text{UxRTS}}$ pin is in Simplex mode
 - $0 = \overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Module Enable bits⁽¹⁾
 - 11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
 - 01 = UxTX, UxRX and \overline{UxRTS} pins are enabled and used; \overline{UxCTS} pin is controlled by corresponding bits in the PORTx register
 - 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
- bit 7 WAKE: Enable Wake-up on Start bit Detect During Sleep Mode bit
 - 1 = Wake-up enabled
 - 0 = Wake-up disabled
- bit 6 LPBACK: UARTx Loopback Mode Select bit
 - 1 = Loopback mode is enabled
 - 0 = Loopback mode is disabled
- bit 5 ABAUD: Auto-Baud Enable bit
 - 1 = Enable baud rate measurement on the next character requires reception of Sync character (0x55); cleared by hardware upon completion
 - 0 = Baud rate measurement disabled or completed
- bit 4 RXINV: Receive Polarity Inversion bit
 - 1 = UxRX Idle state is '0'
 - 0 = UxRX Idle state is '1'
- bit 3 **BRGH:** High Baud Rate Enable bit
 - 1 = High-Speed mode 4x baud clock enabled
 - 0 = Standard Speed mode 16x baud clock enabled
- bit 2-1 PDSEL<1:0>: Parity and Data Selection bits
 - 11 = 9-bit data, no parity
 - 10 = 8-bit data, odd parity
 - 01 = 8-bit data, even parity
 - 00 = 8-bit data, no parity
- bit 0 STSEL: Stop Selection bit
 - 1 = 2 Stop bits
 - 0 = 1 Stop bit
- **Note 1:** These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see 12.3 "Peripheral Pin Select" for more information).

REGISTER 21-2: UxSTA: UARTX STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
31:24	MASK<7:0>												
22.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16	ADDR<7:0>												
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1					
15:8	UTXISE	L<1:0>	UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT					
7.0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0					
7:0	URXISE	L<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-25 MASK<7:0>: UARTx Address Match Mask bits

These bits are used to mask the ADDR<7:0> bits.

11111111 = Corresponding ADDRx bits are used to detect the address match

Note: This setting allows the user to assign individual address as well as a group broadcast address to a UART.

00000000 = Corresponding ADDRx bits are not used to detect the address match.

bit 23-16 ADDR<7:0>: Automatic Address Mask bits

When the ADDEN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 UTXISEL<1:0>: TX Interrupt Mode Selection bits

- 11 = Reserved, do not use
- 10 = Interrupt is generated and asserted while the transmit buffer is empty
- 01 = Interrupt is generated and asserted when all characters have been transmitted
- 00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 UTXINV: Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):

- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):

- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 URXEN: Receiver Enable bit

- 1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module

Note: The event of disabling an enabled receiver will release the RX pin to the PORT function; however, the receive buffers *will not* be reset. Disabling the receiver has no effect on the receive status flags.

bit 11 UTXBRK: Transmit Break bit

- 1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Break transmission is disabled or completed

REGISTER 21-2: UXSTA: UARTX STATUS AND CONTROL REGISTER (CONTINUED)

- bit 10 UTXEN: Transmit Enable bit
 - 1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
 - 0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset

Note: The event of disabling an enabled transmitter will release the TX pin to the PORT function and reset the transmit buffers to empty. Any pending transmission is aborted and data characters in the transmit buffers are lost. All transmit status flags are cleared and the TRMT bit is set

- bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
 - 1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer
- bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit
 - 11 = Reserved
 - 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
 - 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
 - 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)
- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
 - 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
 - 0 = Address Detect mode is disabled
- bit 4 RIDLE: Receiver Idle bit (read-only)
 - 1 = Receiver is Idle
 - 0 = Data is being received
- bit 3 PERR: Parity Error Status bit (read-only)
 - 1 = Parity error has been detected for the current character
 - 0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
 - 1 = Framing error has been detected for the current character
 - 0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit.

This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.

- 1 = Receive buffer has overflowed
- 0 = Receive buffer has not overflowed
- bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
 - 1 = Receive buffer has data, at least one more character can be read
 - 0 = Receive buffer is empty

Figure 21-2 and Figure 21-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 21-2: UART RECEPTION

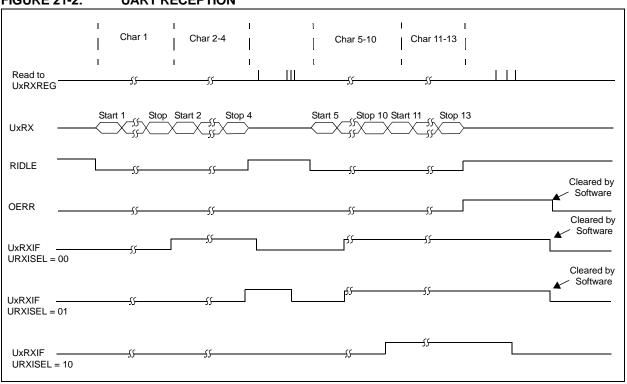
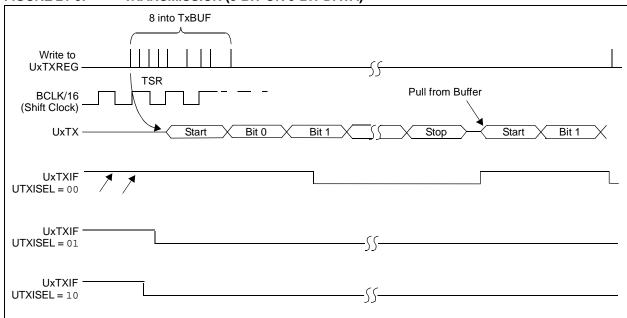


FIGURE 21-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



NOTES:

22.0 PARALLEL MASTER PORT (PMP)

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

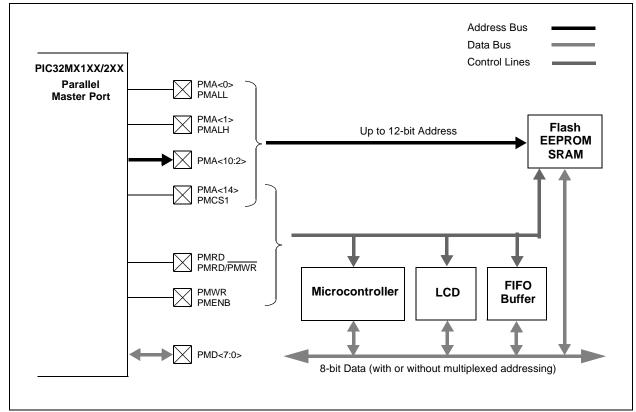
The PMP is a parallel 8-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are key features of the PMP module:

- · Fully multiplexed address/data mode
- Demultiplexed or partially multiplexed address/ data mode
 - Up to 11 address lines with single Chip Select
 - Up to 12 address lines without Chip Select
- One Chip Select line
- Programmable strobe options, any one of these:
 - Individual read and write strobes
 - Read/write strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- · Legacy parallel slave port support
- · Enhanced parallel slave support
 - Address support
 - 4-byte deep auto-incrementing buffer
- · Programmable Wait states
- · Selectable input voltage levels

Figure 22-1 illustrates the PMP module block diagram.

FIGURE 22-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



22.1 PMP Control Registers

TABLE 22-1: PARALLEL MASTER PORT REGISTER MAP

ess										В	its								"
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7000	PMCON	31:16	_	_	_	_	_	_	_	_	RDSTART	_	_	_	_	_	_		0000
7000	TWOON	15:0	ON	_	SIDL	ADRML	JX<1:0>	PMPTTL	PTWREN	PTRDEN	CSF<	<1:0>	ALP	_	CS1P	_	WRSP	RDSP	0000
7010	PMMODE	31:16		_		_	_	_	_	_	_	_	_	_	_	_	_	_	0000
7010	TWINIODE	15:0	BUSY	IRQM	<1:0>	INCM	<1:0>	_	MODE	<1:0>	WAITE	3<1:0>		WAITN	/l<3:0>		WAITE	<1:0>	0000
7020	7020 PMADDR 31			_		_		_	_	_	_	_	_	_	_	_	_	_	0000
7020	FINIADDIN	15:0	_	CS1	_	_	_					A	ADDR<10:0:	>					0000
7030	PMDOUT	31:16												0000					
7030	FINIDOUT	15:0												0000					
7040	PMDIN	31:16								DATAIN	N<31:0>								0000
7040	FIVIDIN	15:0								DATAII	N<31.0>								0000
7050	PMAEN	31:16		_		_	_	_	_	_	_	_	_	_	_	_	_	_	0000
7030	FIVIALIN	15:0	_	PTEN14	_	_	_					ı	PTEN<10:0:	>					0000
7060	PMSTAT	31:16	_	_	_	_	I	_	_	-	_	_	_	-	-	_	_	1	0000
7000	FINISTAT	15:0	IBF	IBOV	_		IB3F	IB2F	IB1F	IB0F	OBE	OBUF		1	OB3E	OB2E	OB1E	OB0E	008F
7070	PMWADDR	31:16	_	_	_	1	I	_	_	-	_	_	1	1	1	_	-	I	0000
7070	FIVIVVADDR	15:0	_	WCS1	_	_	_					W	ADDR<10:0	0>					0000
		31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
7080	PMRADDR	15:0	_	RCS1	_	_						R	ADDR<10:0)>					0000
7000	DMDDIN	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
7090	PMRDIN	15:0								RDATAI	N<15:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

REGISTER 22-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04:04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	-	_	_	_	_
22.40	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	RDSTART	_	_	_	_	_	_	_
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	_	SIDL	ADRML	JX<1:0>	PMPTTL	PTWREN	PTRDEN
7.0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	CSF<	1:0> ⁽²⁾	ALP ⁽²⁾		CS1P ⁽²⁾	_	WRSP	RDSP

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 23 RDSTART: Start Read on PMP Bus bit

This bit is cleared by hardware at the end of the read cycle.

1 = Start a read cycle on the PMP bus

0 = No effect

bit 22-16 Unimplemented: Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾

1 = PMP enabled

0 = PMP disabled, no off-chip access performed

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits

11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used

10 = All 16 bits of address are multiplexed on PMD<7:0> pins

01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>

00 = Address and data appear on separate pins

bit 10 PMPTTL: PMP Module TTL Input Buffer Select bit

1 = PMP module uses TTL input buffers

0 = PMP module uses Schmitt Trigger input buffer

bit 9 PTWREN: Write Enable Strobe Port Enable bit

1 = PMWR/PMENB port enabled

0 = PMWR/PMENB port disabled

bit 8 PTRDEN: Read/Write Strobe Port Enable bit

1 = PMRD/PMWR port enabled

0 = PMRD/PMWR port disabled

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 22-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 7-6 **CSF<1:0>:** Chip Select Function bits⁽²⁾
 - 11 = Reserved
 - 10 = PMCS1 functions as Chip Select
 - 01 = PMCS1 functions as PMA<14>
 - 00 = PMCS1 functions as PMA<14>
- bit 5 ALP: Address Latch Polarity bit⁽²⁾
 - 1 = Active-high (PMALL and PMALH)
 - $0 = Active-low (\overline{PMALL} \text{ and } \overline{PMALH})$
- bit 4 Unimplemented: Read as '0'
- bit 3 **CS1P:** Chip Select 0 Polarity bit⁽²⁾
 - 1 = Active-high (PMCS1)
 - $0 = Active-low (\overline{PMCS1})$
- bit 2 Unimplemented: Read as '0'
- bit 1 WRSP: Write Strobe Polarity bit

For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):

- 1 = Write strobe active-high (PMWR)
- $0 = Write strobe active-low (\overline{PMWR})$

For Master mode 1 (MODE<1:0> = 11):

- 1 = Enable strobe active-high (PMENB)
- 0 = Enable strobe active-low (PMENB)
- bit 0 RDSP: Read Strobe Polarity bit

For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):

- 1 = Read Strobe active-high (PMRD)
- $0 = \text{Read Strobe active-low } (\overline{PMRD})$

For Master mode 1 (MODE<1:0> = 11):

- 1 = Read/write strobe active-high (PMRD/ \overline{PMWR})
- $0 = \text{Read/write strobe active-low } (\overline{PMRD/PMWR})$
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 22-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	_	_	_	_	_	_	-	_	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	_	_	_	_	_	_	_	_	
45.0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	
15:8	BUSY	IRQM	<1:0>	INCM	<1:0>	_	MODE	<1:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	WAITB	<1:0> ⁽¹⁾		WAITM	<3:0> ⁽¹⁾		WAITE<1:0> ⁽¹⁾		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy

0 = Port is not busy

bit 14-13 IRQM<1:0>: Interrupt Request Mode bits

11 = Reserved, do not use

10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)

01 = Interrupt generated at the end of the read/write cycle

00 = No Interrupt generated

bit 12-11 INCM<1:0>: Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)

10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)

01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle⁽²⁾

00 = No increment or decrement of address

bit 10 **Unimplemented:** Read as '0'

bit 9-8 MODE<1:0>: Parallel Port Mode Select bits

11 = Master mode 1 (PMCS1, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<7:0>)

10 = Master mode 2 (PMCS1, PMRD, PMWR, PMA<x:0>, and PMD<7:0>)

01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)

00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 WAITB<1:0>: Data Setup to Read/Write Strobe Wait States bits(1)

11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB

10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB

01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB

00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 WAITM<3:0>: Data Read/Write Strobe Wait States bits(1)

1111 = Wait of 16 TPB

•

0001 = Wait of 2 TPB

0000 = Wait of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

REGISTER 22-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

- bit 1-0 WAITE<1:0>: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾
 - 11 = Wait of 4 TPB
 - 10 = Wait of 3 TPB
 - 01 = Wait of 2 TPB
 - 00 = Wait of 1 TPB (default)

For Read operations:

- 11 = Wait of 3 TPB
- 10 = Wait of 2 TPB
- 01 = Wait of 1 TPB
- 00 = Wait of 0 TpB (default)
- Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 ΤΡΒCLK cycle for a write operation; WAITB = 1 ΤΡΒCLK cycle, WAITE = 0 ΤΡΒCLK cycles for a read operation.
 - 2: Address bit A14 is not subject to auto-increment/decrement if configured as Chip Select CS1.

REGISTER 22-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24		_	_		_	_	_	_	
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	_	_	_	_	_	_	_	_	
45.0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
15:8	_	CS1	_	_	_		ADDR<10:8>	,	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	ADDR<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 14 CS1: Chip Select 1 bit

1 = Chip Select 1 is active 0 = Chip Select 1 is inactive

bit 13-11 **Unimplemented:** Read as '0'

bit 10-0 ADDR<10:0>: Destination Address bits

REGISTER 22-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31:24		-	-	-	-	-	-			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23:16	-	_	_	_	_	_	_	_		
45.0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0		
15:8		PTEN14	_	_	_		PTEN<10:8>			
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0	PTEN<7:0>									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 15-14 PTEN14: PMCS1 Address Port Enable bits

1 = PMA14 functions as either PMA14 or PMCS1⁽¹⁾

0 = PMA14 functions as port I/O

bit 13-11 Unimplemented: Read as '0'

bit 10-2 PTEN<10:2>: PMP Address Port Enable bits

1 = PMA<10:2> function as PMP address lines

0 = PMA<10:2> function as port I/O

bit 1-0 PTEN<1:0>: PMALH/PMALL Address Port Enable bits

1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)

0 = PMA1 and PMA0 pads functions as port I/O

Note 1: The use of this pin as PMA14 or CS1 is selected by the CSF<1:0> bits in the PMCON register.

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.

REGISTER 22-5: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	-	_	_	-	_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
15:8	IBF	IBOV	-	_	IB3F	IB2F	IB1F	IB0F
7.0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
7:0	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E

Legend: HSC = Set by Hardware; Cleared by Software

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 IBF: Input Buffer Full Status bit

1 = All writable input buffer registers are full

0 = Some or all of the writable input buffer registers are empty

bit 14 IBOV: Input Buffer Overflow Status bit

1 = A write attempt to a full input byte buffer occurred (must be cleared in software)

0 = No overflow occurred

bit 13-12 Unimplemented: Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)

0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit

1 = All readable output buffer registers are empty

0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit

1 = A read occurred from an empty output byte buffer (must be cleared in software)

0 = No underflow occurred

bit 5-4 Unimplemented: Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits

1 = Output buffer is empty (writing data to the buffer will clear this bit)

0 = Output buffer contains data that has not been transmitted

REGISTER 22-6: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	-		_	_	_	_	_	_	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	_	_	_	_	_	_	_	_	
45.0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
15:8	_	WCS1	_	_	_	V	VADDR<10:8	>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	WADDR<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 14 WCS1: Chip Select 1 bit

1 = Chip Select 1 is active0 = Chip Select 1 is inactive

bit 14-11 **Unimplemented:** Read as '0' bit 10-0 **WADDR<10:0>:** Address bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

REGISTER 22-7: PMRADDR: PARALLEL PORT READ ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24			_	_	_	_	_	_	
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	_	_	_	_	_	_	_	_	
45.0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
15:8	_	RCS1	_	_	_	F	RADDR<10:8	>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	RADDR<7:0>								

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-15 Unimplemented: Read as '0'

bit 14 RCS1: Chip Select 1 bit

1 = Chip Select 1 is active

0 = Chip Select 1 is inactive (RADDR14 function is selected)

bit 13-11 **Unimplemented:** Read as '0' bit 10-0 **RADDR<13:0>:** Address bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

REGISTER 22-8: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	-	-	_	_	_	_					
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:16	_	_	_	_	_	_	_	_			
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8				RDATAIN<	15:8>						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
		RDATAIN<7:0>									

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 RDATAIN<15:0>: Port Read Input Data bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1' and exclusively for reads. If the

DUALBUF bit is '0', the PMDIN register is used for reads instead of PMRDIN.

23.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

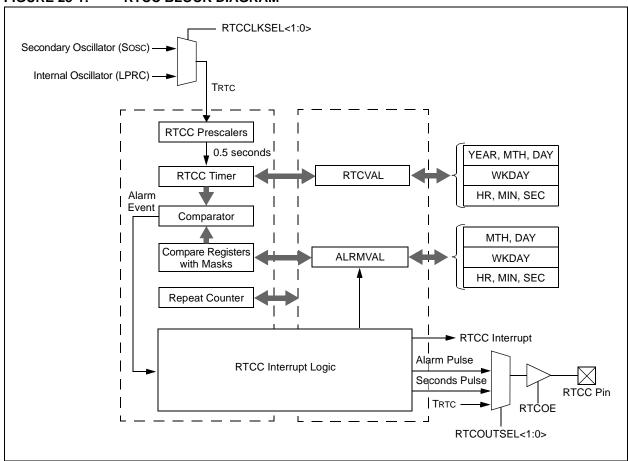
The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The RTCC module can operate in VBAT mode when there is a power loss on the VDD pin. The RTCC will continue to operate if the VBAT pin is powered on (it is usually connected to the battery).

The following are some of the key features of the RTCC module:

- · Time: hours, minutes and seconds
- 24-hour format (military time)
- · Visibility of one-half second period
- · Provides calendar: day, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- · Alarm repeat with decrementing counter
- · Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- · BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- · Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- · Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

FIGURE 23-1: RTCC BLOCK DIAGRAM



23.1 RTCC Control Registers

TABLE 23-1: RTCC REGISTER MAP

																			
ess										1	Bits								"
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0200	RTCCON	31:16	_	_	_	_	_	_					CAL	<9:0>					0000
0200	KICCON	15:0	ON	_	SIDL	_							0000						
0210	RTCALRM	31:16	_	_	1	_	_	1	_	1		_	_	_	_	1	_	_	0000
0210	KTOALKW	15:0	ALRMEN	CHIME	PIV	ALRMSYNC		AMAS	K<3:0>					ARPT	<7:0>				0000
0220	RTCTIME	31:16	_	_	HR1	0<1:0>		HR01	<3:0>		_	М	IN10<2:0>	•		MIN01	<3:0>		xxxx
0220	KTOTIVIL	15:0	_		SEC10<2:	0>		SEC0	1<3:0>			_		_	_	_	_		xx00
0230	RTCDATE	31:16		YEAR	10<3:0>			YEAR)1<3:0>		-	_	_	MONTH10)	MONTH	01<3:0>		xxxx
0230	KIODAIL	15:0	_	_	DAY1	10<1:0>		DAY0	1<3:0>		1	_	_	_	_	V	/DAY01<2:0	>	xx00
0240	ALRMTIME	31:16	_	_	HR1	0<1:0>	HR01<3:0> — MIN10<2:0> MIN01<3:0>				xxxx								
0240	ALIXIVITIVIL	15:0	_		SEC10<2:	0>	SEC01<3:0>				_	xx00							
0250	ALRMDATE	31:16	_	_		_	_		_	_		_	_	MONTH10)	MONTH	01<3:0>		00xx
0230	ALINIDAIL	15:0		DAY1	0<3:0>		DAY01<3:0>				xx0x								

.egend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

REGISTER 23-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
24.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0					
31:24	_	_	_	_	_	_	CAL	_<9:8>					
22,46	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
23:16		CAL<7:0>											
	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0					
15:8	ON ⁽¹⁾	-	SIDL		_	RTCCLK	(SEL<1:0>	RTC OUTSEL<1> ⁽²⁾					
	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0					
7:0	RTC OUTSEL<0>(2)	RTC CLKON	_		RTC WREN ⁽³⁾	RTC SYNC	HALFSEC ⁽⁴⁾	RTCOE					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-26 Unimplemented: Read as '0'

bit 25-16 **CAL<9:0>:** Real-Time Clock Drift Calibration bits, which contain a signed 10-bit integer value 0111111111 = Maximum positive adjustment, adds 511 real-time clock pulses every one minute

•

000000001 = Minimum positive adjustment, adds 1 real-time clock pulse every one minute 0000000000 = No adjustment

1111111111 = Minimum negative adjustment, subtracts 1 real-time clock pulse every one minute

•

1000000000 = Minimum negative adjustment, subtracts 512 real-time clock pulses every one minute

bit 15 **ON**: RTCC On bit⁽¹⁾

1 = RTCC module is enabled

0 = RTCC module is disabled

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Disables RTCC operation when CPU enters Idle mode

0 = Continue normal operation when CPU enters Idle mode

bit 12-11 Unimplemented: Read as '0'

Note 1: The ON bit is only writable when RTCWREN = 1.

2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

3: The RTCWREN bit can be set only when the write sequence is enabled.

4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

REGISTER 23-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER (CONTINUED)

bit 10-9 RTCCLKSEL<1:0>: RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

- 11 = Reserved
- 10 = Reserved
- 01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
- 00 = RTCC uses the internal 32 kHz oscillator (LPRC)
- bit 8-7 RTCOUTSEL<1:0>: RTCC Output Data Select bits⁽²⁾
 - 11 = Reserved
 - 10 = RTCC Clock is presented on the RTCC pin
 - 01 = Seconds Clock is presented on the RTCC pin
 - 00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered
- bit 6 RTCCLKON: RTCC Clock Enable Status bit
 - 1 = RTCC Clock is actively running
 - 0 = RTCC Clock is not running
- bit 5-4 Unimplemented: Read as '0'
- bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit⁽³⁾
 - 1 = Real-Time Clock Value registers can be written to by the user
 - 0 = Real-Time Clock Value registers are locked out from being written to by the user
- bit 2 RTCSYNC: Real-Time Clock Value Registers Read Synchronization bit
 - 1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
 - 0 = Real-time clock value registers can be read without concern about a rollover ripple
- bit 1 HALFSEC: Half-Second Status bit⁽⁴⁾
 - 1 = Second half period of a second
 - 0 = First half period of a second
- bit 0 RTCOE: RTCC Output Enable bit
 - 1 = RTCC output is enabled
 - 0 = RTCC output is not enabled
- **Note 1:** The ON bit is only writable when RTCWREN = 1.
 - 2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
 - 3: The RTCWREN bit can be set only when the write sequence is enabled.
 - 4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

REGISTER 23-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
31.24	_			-				_		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
23.10	_	_	_	_	_	_	_	_		
15.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC	AMASK<3:0> ⁽²⁾					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0	ARPT<7:0> ⁽²⁾									

Legend:

bit 14

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 ALRMEN: Alarm Enable bit (1,2)

1 = Alarm is enabled0 = Alarm is disabled

CHIME: Chime Enable bit⁽²⁾

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF

0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.

When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 ALRMSYNC: Alarm Sync bit

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.

0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits(2)

0000 = Every half-second

0001 = Every second

0010 = Every 10 seconds

0011 = Every minute

0100 = Every 10 minutes

0101 = Every hour

0110 = Once a day

0111 = Once a week

1000 = Once a month

1001 = Once a year (except when configured for February 29, once every four years)

1010 = Reserved

1011 = Reserved

11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

REGISTER 23-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 ARPT<7:0>: Alarm Repeat Counter Value bits⁽²⁾

11111111 = Alarm will trigger 256 times

•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

REGISTER 23-3: RTCTIME: RTC TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31:24	_	_	- HR10<1:0> HR0						
22.40	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:16	_		MIN10<2:0>		MIN01<3:0>				
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15:8	_		SEC10<2:0>			SEC01	<3:0>		
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
7:0		-	-	1	_	1	1	_	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary-Coded Decimal Value of Hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 HR01<3:0>: Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9

bit 23 Unimplemented: Read as '0'

bit 22-20 MIN10<2:0>: Binary-Coded Decimal Value of Minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 MIN01<3:0>: Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9

bit 15 Unimplemented: Read as '0'

bit 14-12 SEC10<2:0>: Binary-Coded Decimal Value of Seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 SEC01<3:0>: Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 23-4: RTCDATE: RTC DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
31:24		YEAR1	0<3:0>		YEAR01<3:0>				
22.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
23:16	_	_	_	MONTH10	MONTH01<3:0>				
45.0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
15:8	_	_	DAY10	0<1:0>		DAY01	<3:0>		
7.0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	
7:0	_	_	_	_	_	V	VDAY01<2:0:	>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-28 YEAR10<3:0>: Binary-Coded Decimal Value of Years bits, 10s place digit; contains a value from 0 to 9

bit 27-24 YEAR01<3:0>: Binary-Coded Decimal Value of Years bits, 1s place digit; contains a value from 0 to 9

bit 23-21 Unimplemented: Read as '0'

bit 20 MONTH10: Binary-Coded Decimal Value of Months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 MONTH01<3:0>: Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 Unimplemented: Read as '0'

bit 13-12 DAY10<1:0>: Binary-Coded Decimal Value of Days bits, 10s place digit; contains a value of 0 to 3

bit 11-8 DAY01<3:0>: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 Unimplemented: Read as '0'

bit 2-0 WDAY01<2:0>: Binary-Coded Decimal Value of Weekdays bits; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 23-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
31:24			HR10	<1:0>		HR01	<3:0>	
22.40	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:16	_		MIN10<2:0>	N10<2:0>		MIN01	<3:0>	
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8	_		SEC10<2:0>			SEC01	<3:0>	
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_	_	_	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary Coded Decimal value of hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 HR01<3:0>: Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9

bit 23 Unimplemented: Read as '0'

bit 22-20 MIN10<2:0>: Binary Coded Decimal value of minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 MIN01<3:0>: Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9

bit 15 Unimplemented: Read as '0'

bit 14-12 SEC10<2:0>: Binary Coded Decimal value of seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 SEC01<3:0>: Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

REGISTER 23-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_		_	_	_	-	_	_
22.40	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:16	_	_	_	MONTH10		MONTH	01<3:0>	
45.0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8	_	_	DAY1	0<1:0>		DAY01	<3:0>	
7.0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
7:0	_	_	_	_	_	V	VDAY01<2:0:	>

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 Unimplemented: Read as '0'

bit 20 MONTH10: Binary Coded Decimal value of months bits, 10s place digit; contains a value of 0 or 1

bit 19-16 MONTH01<3:0>: Binary Coded Decimal value of months bits, 1s place digit; contains a value from 0 to 9

bit 15-14 Unimplemented: Read as '0'

bit 13-12 DAY10<1:0>: Binary Coded Decimal value of days bits, 10s place digit; contains a value from 0 to 3

bit 11-8 DAY01<3:0>: Binary Coded Decimal value of days bits, 1s place digit; contains a value from 0 to 9

bit 7-3 Unimplemented: Read as '0'

bit 2-0 WDAY01<2:0>: Binary Coded Decimal value of weekdays bits; contains a value from 0 to 6

NOTES:

24.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

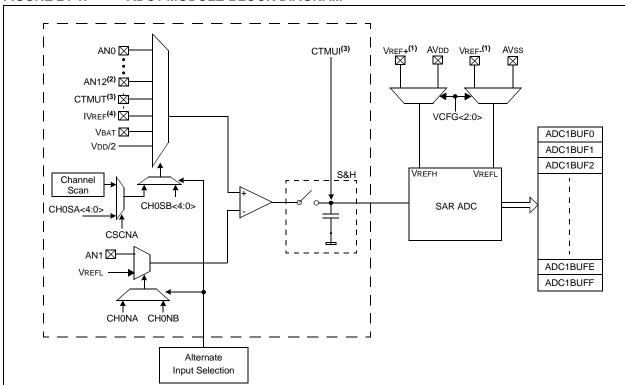
The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed

- · Up to 13 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- · Automatic Channel Scan mode
- Selectable conversion trigger source
- · 16-word conversion result buffer
- · Selectable buffer fill modes
- · Eight conversion result format options
- · Operation during Sleep and Idle modes

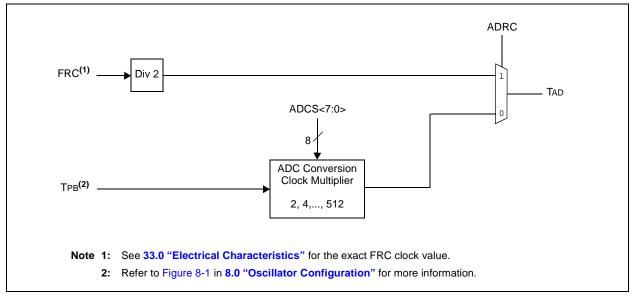
A block diagram of the 10-bit ADC is illustrated in Figure 24-1. Figure 24-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

FIGURE 24-1: ADC1 MODULE BLOCK DIAGRAM



- Note 1: VREF+ and VREF- inputs can be multiplexed with other analog inputs.
 - 2: AN8 is only available on 44-pin devices. AN6, AN7, and AN12 are not available on 28-pin devices.
 - 3: Connected to the CTMU module. See 28.0 "Charge Time Measurement Unit (CTMU)" for more information.
 - 4: Internal precision voltage reference (1.2V).

FIGURE 24-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



24.1 ADC Control Registers

TABLE 24-1: ADC REGISTER MAP

ess		•		Bits 950 950 950 950 950 950 950 950 950 950											"				
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	AD1CON1 ⁽¹⁾	31:16	_	_	-	_	_	-	_	_		-	_	_		_	_	_	0000
9000	AD ICON ICO	15:0	ON	_	SIDL	_	_		FORM<2:0>	>	;	SSRC<2:0>	•	CLRASAM	1	ASAM	SAMP	DONE	0000
9010	AD1CON2 ⁽¹⁾	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
0010	710 100112	15:0	<u> </u>	VCFG<2:0>	•	OFFCAL		CSCNA	_	_	BUFS			SMPI	<3:0>		BUFM	ALTS	0000
9020	AD1CON3 ⁽¹⁾	31:16		_	_	_			_	_	_		_	_	_	_	—	—	0000
		15:0	ADRC	_				SAMC<4:0>						ADCS					0000
9040	AD1CHS ⁽¹⁾	31:16	CH0NB	_				CH0SB<4:0	>		CH0NA					CH0SA<4:0	> I	I	0000
		15:0		_										_	_		-	-	0000
9050	AD1CSSL ⁽¹⁾	31:16 15:0	CSSL15	- -															
			CSSL15	0000															
9070	ADC1BUF0	31:16 15:0		ADC Result Word 0 (ADC1BUF0<31:0>)															
		31:16		ADC Result Word 1 (ADC1BUF1<31:0>) 0000															
9080	ADC1BUF1	15:0							ADC Res	sult Word 1	(ADC1BUF	1<31:0>)							0000
0000	ADC1BUF2	31:16							ADC Dec		(ADC4DUE	0 -24.0- \							0000
9090	ADC IBUF2	15:0							ADC Res	suit vvoid 2	(ADC1BUF	2<31:0>)							0000
9040	ADC1BUF3	31:16							ADC Res	cult Word 3	(ADC1BUF	3~31:0~)							0000
30/10	ADC IDOI 3	15:0							ADO NES	suit vvoid 5	(ADC IDOI	3<31.02)							0000
90B0	ADC1BUF4	31:16							ADC Res	sult Word 4	(ADC1BUF	4<31:0>)							0000
0020	7.50.50.	15:0							7.20 1.00		(7.20.20.	. 10 ,							0000
90C0	ADC1BUF5	31:16							ADC Res	sult Word 5	(ADC1BUF	5<31:0>)							0000
		15:0																	0000
90D0	ADC1BUF6	31:16 15:0							ADC Res	sult Word 6	(ADC1BUF	6<31:0>)							0000
-		31:16																	0000
90E0	ADC1BUF7	15:0		ADC Result Word 7 (ADC1BUF7<31:0>)															
		31:16		0000															
90F0	ADC1BUF8	15:0		ADC Result Word 8 (ADC1BUF8<31:0>)															
2422	4004045	31:16							4505		/A D Q / D / I E								0000
9100	ADC1BUF9	15:0							ADC Res	suit Word 9	(ADC1BUF	9<31:0>)							0000
0110	ADC1BUFA	31:16		ADC Result Word A (ADC1RHFA<31:05)															
9110	ADCIDOFA	15:0		ADC Result Word A (ADC1BUFA<31:0>) 0000 0000															

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Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for details.

TABLE 24-1: ADC REGISTER MAP (CONTINUED)

ess		Φ								В	ts								S
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
9120	ADC1BUFB	31:16							ADC Res	ult Word B	(ADC1BUF	B<31:0>)							0000
3120	ADO IDOI D	15:0							ADO NOS	ait Word B	(//.DO1.DO1	D(01.02)							0000
0130	ADC1BUFC	31:16							ADC Pos	ult Word C	(ADC1BUF	C ~21:0~)							0000
9130	ADCIBUFC	15:0							ADC Res	uit word C	(ADC IBUF	U<31.0 <i>></i>)							0000
0140	ADC1BUFD	31:16							ADC Pos	ult Word D	(ADC1BUF	D-21:0~)							0000
9140	ADC IBOI D	15:0							ADC Nes	uit Word D	(ADC IBOI	D<31.0 <i>></i>)							0000
9150	ADC1BUFE	31:16							ADC Res	ult Word E	(ADC1BUF	E_31:0~\							0000
3130	ADOIDOIL	15:0							ADO NES	ait vvolu L		L<31.02)							0000
9160	ADC1BUFF	31:16	•				•	•	ADC Res	ult Word F	(ADC1BUF	F_31:0~\	•	•		•			0000
3100	ADCIBULL	15:0							ADC RES	Suit VVOIU F	(ADC IDUF	1 <31.0>)							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for details.

REGISTER 24-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31:24		_	_	_			_	_
00:40	U-0	U-0						
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	_	SIDL	_	_	F	FORM<2:0>	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0, HSC	R/C-0, HSC
7:0		SSRC<2:0>		CLRASAM	_	ASAM	SAMP ⁽²⁾	DONE ⁽³⁾

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** ADC Operating Mode bit⁽¹⁾

1 = ADC module is operating

0 = ADC module is not operating

bit 14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12-11 Unimplemented: Read as '0'

bit 10-8 FORM<2:0>: Data Output Format bits

111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)

101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)

100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)

010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)

000 =Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 SSRC<2:0>: Conversion Trigger Source Select bits

111 = Internal counter ends sampling and starts conversion (auto convert)

110 = Reserved

101 = Reserved

100 = Reserved

011 = CTMU ends sampling and starts conversion

010 = Timer 3 period match ends sampling and starts conversion

001 = Active transition on INT0 pin ends sampling and starts conversion

000 = Clearing SAMP bit ends sampling and starts conversion

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

- 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
- 3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 24-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

- bit 4 CLRASAM: Stop Conversion Sequence bit (when the first ADC interrupt is generated)
 - 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
 - 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 Unimplemented: Read as '0'
- bit 2 ASAM: ADC Sample Auto-Start bit
 - 1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
 - 0 = Sampling begins when SAMP bit is set
- bit 1 SAMP: ADC Sample Enable bit⁽²⁾
 - 1 = The ADC sample and hold amplifier is sampling
 - 0 = The ADC sample/hold amplifier is holding
 - When ASAM = 0, writing '1' to this bit starts sampling.

When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

- bit 0 **DONE**: Analog-to-Digital Conversion Status bit⁽³⁾
 - 1 = Analog-to-digital conversion is done
 - 0 = Analog-to-digital conversion is not done or has not started

Clearing this bit will not affect any operation in progress.

- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 24-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_		_	_		_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
15:8		VCFG<2:0>		OFFCAL	_	CSCNA	_	_
7.0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	BUFS	_		SMP	l<3:0>		BUFM	ALTS

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVss

bit 12 OFFCAL: Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 Unimplemented: Read as '0'

bit 10 CSCNA: Input Scan Select bit

1 = Scan inputs

0 = Do not scan inputs

bit 9-8 Unimplemented: Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 Unimplemented: Read as '0'

bit 5-2 SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence

1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

.

0001 = Interrupts at the completion of conversion for each 2^{nd} sample/convert sequence 0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 BUFM: ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8

0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 ALTS: Alternate Input Sample Mode Select bit

1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples

0 = Always use Sample A input multiplexer settings

REGISTER 24-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ADRC	_	_			SAMC<4:0>(1)		
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
7:0				ADCS<	7:0> ⁽²⁾			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 ADRC: ADC Conversion Clock Source bit

1 = Clock derived from FRC

0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 Unimplemented: Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits⁽¹⁾

11111 = **31** TAD

•

•

00001 = 1 TAD

00000 = 0 TAD (Not allowed)

bit 7-0 ADCS<7:0>: ADC Conversion Clock Select bits⁽²⁾

11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD

•

٠

•

00000001 =TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD 00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

Note 1: This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.

2: This bit is not used if the ADRC (AD1CON3<15>) bit = 1.

REGISTER 24-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	CH0NB	_	_			CH0SB<4:0>		
00.40	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	CH0NA	_	_			CH0SA<4:0>		
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	_	_	_	_	_	_
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_		_	_

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 CH0NB: Negative Input Select bit for Sample B

1 = Channel 0 negative input is AN10 = Channel 0 negative input is VREFL

bit 30-29 Unimplemented: Read as '0'

bit 28-24 CH0SB<4:0>: Positive Input Select bits for Sample B

11111 = Reserved

•

10010 = Reserved

10001 = Channel 0 positive input is VDD/2 10000 = Channel 0 positive input is VBAT

01111 = Reserved

01110 = Channel 0 positive input is IVREF⁽¹⁾

01101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)

01100 = Channel 0 positive input is AN12⁽³⁾

•

•

•

00001 = Channel 0 positive input is AN1 00000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting⁽¹⁾

1 = Channel 0 negative input is AN1

0 = Channel 0 negative input is VREFL

bit 22-21 Unimplemented: Read as '0'

Note 1: See 26.0 "Comparator Voltage Reference (CVREF)" for more information.

2: See 28.0 "Charge Time Measurement Unit (CTMU)" for more information.

3: AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

REGISTER 24-4: AD1CHS: ADC INPUT SELECT REGISTER (CONTINUED)

```
bit 20-16

CH0SA<4:0>: Positive Input Select bits for Sample A Multiplexer Setting

11111 = Reserved

10010 = Reserved
10001 = Channel 0 positive input is VDD/2
10000 = Channel 0 positive input is VBAT
01111 = Reserved
01110 = Channel 0 positive input is IVREF(1)
01101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)(2)
01100 = Channel 0 positive input is AN12(3)

•

00001 = Channel 0 positive input is AN1
00000 = Channel 0 positive input is AN1
```

- bit 15-0 **Unimplemented:** Read as '0'
- Note 1: See 26.0 "Comparator Voltage Reference (CVREF)" for more information.
 - 2: See 28.0 "Charge Time Measurement Unit (CTMU)" for more information.
 - 3: AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

REGISTER 24-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24		_	_	_	1		_	_
00:40	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
23:16	_	_	_	_	-	_	CSSL17	CSSL16
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-18 Unimplemented: Read as '0'

bit 17-0 CSSL<17:0>: ADC Input Pin Scan Selection bits(1,2)

1 = Select ANx for input scan0 = Skip ANx for input scan

Note 1: CSSL = ANx, where 'x' = 0-12; CSSL13 selects CTMUT input for scan; CSSL14 selects IVREF for scan; CSSL15 selects Vss for scan; CSSL16 selects VBAT; CSSL17 selects VDD/2.

2: On devices with less than 13 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

NOTES:

25.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer Section 19. to "Comparator" (DS60001110), which is available from the Documentation Reference Manual section the Microchip PIC32 web site (www.microchip.com/pic32).

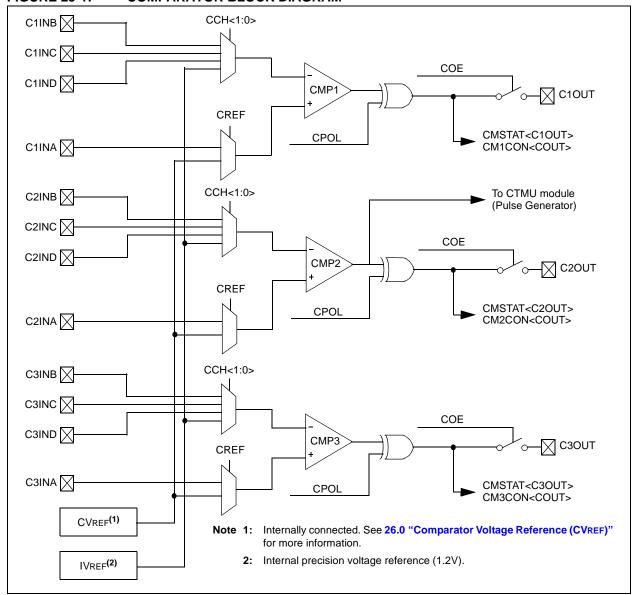
The Analog Comparator module contains three comparators that can be configured in a variety of ways.

The following are key features of the Comparator module:

- Selectable inputs available include:
 - Analog inputs multiplexed with I/O pins
 - On-chip internal absolute voltage reference (IVREF)
 - Comparator voltage reference (CVREF)
- · Outputs can be Inverted
- · Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 25-1.

FIGURE 25-1: COMPARATOR BLOCK DIAGRAM



25.1 Comparator Control Registers

TABLE 25-1: COMPARATOR REGISTER MAP

ess		0								Bi	ts								· s
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
A 000	CM1CON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
A000	CIVITCON	15:0	ON	COE	CPOL	_	_	1	_	COUT	EVPO	L<1:0>	_	CREF	_	_	CCH	<1:0>	00C3
A 01 0	CM2CON	31:16	_	1		_	_	1	_	_	_	_	_	_	_	_	_	_	0000
AUTU	CIVIZCON	15:0	ON	COE	CPOL	_	_	1	_	COUT	EVPO	L<1:0>	_	CREF	_	_	CCH	<1:0>	00C3
4020	CM3CON	31:16	_	1		_	_	1	_	_	_	_	_	_	_	_	_	_	0000
A020	CIVISCOIN	15:0	ON	COE	CPOL	_	_	_		COUT	EVPO	L<1:0>	_	CREF	_	_	CCH-	<1:0>	00C3
A060	CMSTAT	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
A060	CIVISTAI	15:0	_	_	SIDL	_	_		_	_	I	_		_	_	C3OUT	C2OUT	C1OUT	0000

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information

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REGISTER 25-1: CMXCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	_			_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	-		_	_
45.0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
15:8	ON ⁽¹⁾	COE	CPOL ⁽²⁾	_			_	COUT
7.0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
7:0	EVPOL	_<1:0>		CREF	_		CCH	<1:0>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** Comparator ON bit⁽¹⁾

1 = Module is enabled. Setting this bit does not affect the other bits in this register

0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 COE: Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin

0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾

1 = Output is inverted

0 = Output is not inverted

bit 12-9 Unimplemented: Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'

0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output

10 = Comparator interrupt is generated on a high-to-low transition of the comparator output

01 = Comparator interrupt is generated on a low-to-high transition of the comparator output

00 = Comparator interrupt generation is disabled

bit 5 Unimplemented: Read as '0'

bit 4 CREF: Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal CVREF

0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 Unimplemented: Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the IVREF

10 = Comparator inverting input is connected to the CxIND pin

01 = Comparator inverting input is connected to the CxINC pin

00 = Comparator inverting input is connected to the CxINB pin

Note 1: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

REGISTER 25-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	-	_	-	_	_	_	_	_
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	-	_	-	_	_	-	_	_
45.0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
15:8	_	_	SIDL	_	_	_	_	_
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	_	_	_	_	_	C3OUT	C2OUT	C1OUT

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in Idle Control bit

1 = All Comparator modules are disabled when the device enters Idle mode

0 = All Comparator modules continue to operate when the device enters Idle mode

bit 12-3 Unimplemented: Read as '0'

bit 2 C3OUT: Comparator Output bit

1 = Output of Comparator 3 is a '1'

0 = Output of Comparator 3 is a '0'

bit 1 C2OUT: Comparator Output bit

1 = Output of Comparator 2 is a '1'

0 = Output of Comparator 2 is a '0'

bit 0 C10UT: Comparator Output bit

1 = Output of Comparator 1 is a '1'

0 = Output of Comparator 1 is a '0'

26.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20.** "Comparator Voltage Reference (CVREF)" (DS60001109), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

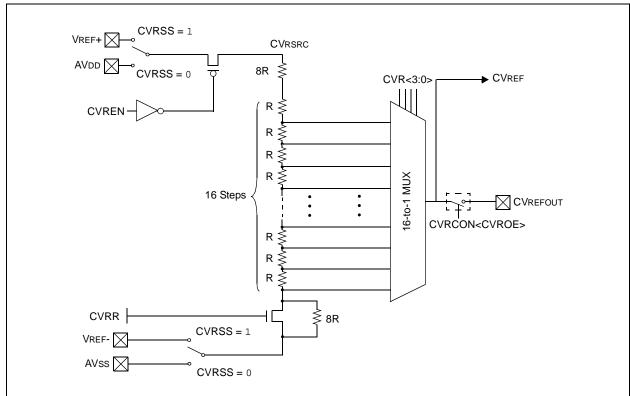
The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/Vss or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- · Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- · Output can be connected to a pin

A block diagram of the module is shown in Figure 26-1.





26.1 Comparator Voltage Reference Control Register

TABLE 26-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#) Register Name ⁽¹⁾				Bits															s
	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9800 CVR	CVDCON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
	CVRCON	15:0	ON	_	_	_	_	_	_	_	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

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REGISTER 26-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	_	_	_	-	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_			1	_	1	_	_
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	ON ⁽¹⁾	_	_	_	_	_	_	_
7.0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	CVROE	CVRR	CVRSS		CVR<	<3:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit⁽¹⁾

1 = Module is enabled

Setting this bit does not affect other bits in the register.

0 = Module is disabled and does not consume current.Clearing this bit does not affect the other bits in the register.

bit 14-7 Unimplemented: Read as '0'

bit 6 CVROE: CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 CVRR: CVREF Range Selection bit

1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size

bit 4 CVRSS: CVREF Source Selection bit

1 = Comparator voltage reference source, CVRSRC = (VREF+) - (VREF-)

0 = Comparator voltage reference source, CVRSRC = AVDD - AVSS

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \le CVR < 3:0 > \le 15$ bits

When CVRR = 1:

 $CVREF = (CVR < 3:0 > /24) \bullet (CVRSRC)$

When CVRR = 0:

 $CVREF = 1/4 \bullet (CVRSRC) + (CVR<3:0>/32) \bullet (CVRSRC)$

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

NOTES:

27.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX XLP family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 38. "High/Low-Voltage Detect (HLVD)", which is available from the Documentation > of Reference Manual section the Microchip PIC32 web site (www.microchip.com/pic32).

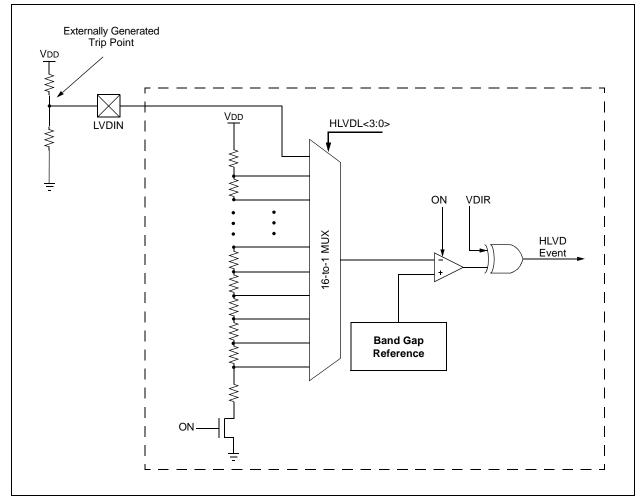
The High/Low-Voltage Detect (HLVD) module is a programmable circuit that can be used to specify both the device voltage trip point and the direction of change. When enabled, a HLVD event will act to disable the Flash controller from executing a programming sequence. This module is used to ensure the supply voltage is sufficient for programming.

The HLVD module is an interrupt-driven supply-level detection. The voltage detection monitors the internal power supply.

The HLVD module provides the following features:

- · Detection hysteresis
- Detection of low-to-high or high-to-low voltage changes
- Generation of Non-Maskable Interrupts (NMI)
- LVDIN pin to provide external voltage trip point

FIGURE 27-1: PROGRAMMABLE HLVD MODULE BLOCK DIAGRAM



27.1 Control Registers

TABLE 27-1: HIGH/LOW-VOLTAGE DETECT REGISTER MAP

ess	_	ø								Bits									S
Virtual Addre (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
1000	HLVDCON	31:16	_						_	_	_		_	_	_				0000
1800	HLVDCON	15:0	ON	_	_	_	VDIR	BGVST	_	HLVDET	_	_	_	_		HLVDL∙	<3:0>		0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 13.2 "CLR, SET, and INV Registers" for more information.

REGISTER 27-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_		_	_	_
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_		_	_
45.0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0
15:8	ON	_	_	_	VDIR ⁽¹⁾	BGVST	_	HLVDET
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	_		HLVDL<	3:0> ⁽¹⁾	

Legend:HS = Hardware SetHC = Hardware ClearedR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15 ON: HLVD Module Enable bit

1 = HLVD module is enabled 0 = HLVD module is disabled

0 = 11EVD module is disabled

bit 14-12 Unimplemented: Read as '0'

bit 11 VDIR: Voltage Change Direction Select bit (1)

1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)

0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 10 BGVST: Band Gap Reference Voltages Stable Status bit

1 = Indicates internal band gap voltage references is stable

0 = Indicates internal band gap voltage reference is not stable

This bit is readable when the HLVD module is disabled (ON = 0).

bit 9 Unimplemented: Read as '0'

bit 8 **HLVDET:** High/Low-Voltage Detection Event Status bit

1 = Indicates HLVD Event interrupt is active

0 = Indicates HLVD Event interrupt is not active

bit 7-4 Unimplemented: Read as '0'

Note 1: To avoid false HLVD events, all HLVD module setting changes should occur only when the module is disabled (ON = 0). See Table 33-6 in the "Electrical Characteristics" chapter for the actual trip points.

REGISTER 27-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

```
bit 3-0 HLVDL<3:0>: High/Low-Voltage Detection Limit Select bits<sup>(1)</sup>

1111 = External LVDIN pin

1110 = Reserved; do not use

1101 = Reserved; do not use

1100 = Reserved; do not use

1011 = Reserved; do not use

1010 = Selects Trip Point 10

1001 = Selects Trip Point 9

1000 = Selects Trip Point 8

0111 = Selects Trip Point 7

0110 = Selects Trip Point 6

0101 = Selects Trip Point 5

0100 = Selects Trip Point 4

0011 = Reserved; do not use
```

0010 = Reserved; do not use 0001 = Reserved; do not use 0000 = Reserved; do not use

Note 1: To avoid false HLVD events, all HLVD module setting changes should occur only when the module is disabled (ON = 0). See Table 33-6 in the "Electrical Characteristics" chapter for the actual trip points.

28.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

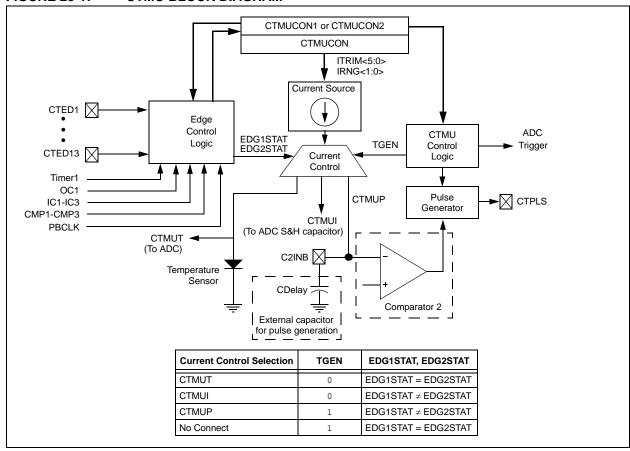
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- · On-chip precision current source
- 16-edge input trigger sources
- · Selection of edge or level-sensitive inputs
- · Polarity control for each edge source
- · Control of edge sequence
- · Control of response to edges
- · High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- · Integrated temperature sensing diode
- Control of current source during auto-sampling
- · Four current source ranges
- · Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 28-1.





28.1 CTMU Control Registers

TABLE 28-1: CTMU REGISTER MAP

ess		•								Bits									
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
4200	CTMUCON	31:16	EDG1MOD	EDG1POL		EDG1S	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG2S	SEL<3:0>		_	_	0000
A200	CTWOCON	15:0	ON	_	CTMUSIDL	TGEN	EDGEN	DGEN EDGSEQEN IDISSEN CTTRIG ITRIM<5:0> IRNG<1:0> 00				0000							

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information

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REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	EDG1MOD	EDG1POL		EDG1S	EL<3:0>		EDG2STAT	EDG1STAT
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
23.10	EDG2MOD	EDG2POL		EDG2S	EL<3:0>		_	_
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.6	ON	_	CTMUSIDL	TGEN ⁽¹⁾	EDGEN	EDGSEQEN	IDISSEN ⁽²⁾	CTTRIG
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0			ITRIM	1<5:0>			IRNG	<1:0>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31 EDG1MOD: Edge1 Edge Sampling Select bit

1 = Input is edge-sensitive

0 = Input is level-sensitive

bit 30 EDG1POL: Edge 1 Polarity Select bit

1 = Edge1 programmed for a positive edge response

0 = Edge1 programmed for a negative edge response

bit 29-26 EDG1SEL<3:0>: Edge 1 Source Select bits

1111 = C3OUT pin is selected

1110 = C2OUT pin is selected

1101 = C1OUT pin is selected

1100 = IC3 Capture Event is selected

1011 = IC2 Capture Event is selected

1010 = IC1 Capture Event is selected

1001 = CTED8 pin is selected

1000 = CTED7 pin is selected

0111 = CTED6 pin is selected

0110 = CTED5 pin is selected

0101 = CTED4 pin is selected

0100 = CTED3 pin is selected

0011 = CTED1 pin is selected

0010 = CTED2 pin is selected

0001 = OC1 Compare Event is selected

0000 = Timer1 Event is selected

bit 25 EDG2STAT: Edge2 Status bit

Indicates the status of Edge2 and can be written to control edge source

1 = Edge2 has occurred

0 = Edge2 has not occurred

- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 33-42) in 33.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 24 EDG1STAT: Edge1 Status bit

Indicates the status of Edge1 and can be written to control edge source

- 1 = Edge1 has occurred
- 0 = Edge1 has not occurred
- bit 23 EDG2MOD: Edge2 Edge Sampling Select bit
 - 1 = Input is edge-sensitive
 - 0 = Input is level-sensitive
- bit 22 EDG2POL: Edge 2 Polarity Select bit
 - 1 = Edge2 programmed for a positive edge response
 - 0 = Edge2 programmed for a negative edge response
- bit 21-18 EDG2SEL<3:0>: Edge 2 Source Select bits
 - 1111 = C3OUT pin is selected
 - 1110 = C2OUT pin is selected
 - 1101 = C1OUT pin is selected
 - 1100 = PBCLK clock is selected
 - 1011 = IC3 Capture Event is selected
 - 1010 = IC2 Capture Event is selected
 - 1001 = IC1 Capture Event is selected
 - 1000 = CTED13 pin is selected
 - 0111 = CTED12 pin is selected
 - 0110 = CTED11 pin is selected
 - 0101 = CTED10 pin is selected
 - 0100 = CTED9 pin is selected
 - 0011 = CTED1 pin is selected
 - 0010 = CTED2 pin is selected
 - 0001 = OC1 Compare Event is selected
 - 0000 = Timer1 Event is selected
- bit 17-16 Unimplemented: Read as '0'
- bit 15 ON: ON Enable bit
 - 1 = Module is enabled
 - 0 = Module is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 CTMUSIDL: Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode
- bit 12 **TGEN:** Time Generation Enable bit⁽¹⁾
 - 1 = Enables edge delay generation
 - 0 = Disables edge delay generation
- bit 11 **EDGEN:** Edge Enable bit
 - 1 = Edges are not blocked
 - 0 = Edges are blocked
- Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 33-42) in 33.0 "Electrical Characteristics" for current values.
 - **4:** This bit setting is not available for the CTMU temperature diode.

REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

- bit 10 EDGSEQEN: Edge Sequence Enable bit
 - 1 = Edge1 must occur before Edge2 can occur
 - 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit⁽²⁾
 - 1 = Analog current source output is grounded
 - 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** Trigger Control bit
 - 1 = Trigger output is enabled
 - 0 = Trigger output is disabled
- bit 7-2 ITRIM<5:0>: Current Source Trim bits
 - 011111 = Maximum positive change from nominal current

011110

•

•

000001 = Minimum positive change from nominal current

000000 = Nominal current output specified by IRNG<1:0>

111111 = Minimum negative change from nominal current

•

.

100010

100001 = Maximum negative change from nominal current

bit 1-0 IRNG<1:0>: Current Range Select bits(3)

- 11 = 100 times base current
- 10 = 10 times base current
- 01 = Base current level
- 00 = 1000 times base current(4)
- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - Refer to the CTMU Current Source Specifications (Table 33-42) in 33.0 "Electrical Characteristics" for current values.
 - **4:** This bit setting is not available for the CTMU temperature diode.

NOTES:

29.0 POWER-SAVING FEATURES

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 10. "Power-Saving Features" (DS60001130), which is available from the Documentation > Reference Manual section of the PIC32 Microchip web site (www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/44-pin XLP Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

29.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

29.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

29.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

29.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- · The CPU is halted
- The system clock source is typically shutdown.
 See 29.3.3 "Peripheral Bus Scaling Method" for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- · On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

29.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

- Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor
 - 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

29.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

29.3.4 DEEP SLEEP MODE

Deep Sleep mode brings the device into its lowest power consumption state without requiring the use of external switches to remove power from the device.

Deep Sleep

In this mode, the CPU, RAM and most peripherals are powered down. Power is maintained to the DSGPR0 register and one or more of the RTCC, DSWDT and DSGPR1 through DSGPR32 registers.

Which of these peripherals is active depends on the state of the following register bits when Deep Sleep mode is entered:

• RTCDIS (DSCON<12>)

This bit must be set to disable the RTCC in Deep Sleep mode (see Register 29-1).

DSWDTEN (DEVCFG2<30>)

This Configuration bit must be set to enable the DSWDT register in Deep Sleep mode (see Register 30-3)

• DSGPREN (DSCON<13>)

This bit must be set to enable the DSGPR1 through DSGPR32 registers in Deep Sleep mode (see Register 29-1).

Note:

The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, the Deep Sleep Control registers must be written twice.

In addition to the conditionally enabled peripherals described above, the MCLR filter and INT0 pin are enabled in Deep Sleep mode.

29.3.5 VBAT MODE

VBAT mode is similar to Deep Sleep mode, except that the device is powered from the VBAT pin. VBAT mode is controlled strictly by hardware, without any software intervention. VBAT mode is initiated when VDD falls **VPOR** (refer the 33.0 "Electrical to Characteristics" for definitions of VDD and VPOR). An external power source must be connected to the VBAT pin before power is removed from VDD to enter VBAT mode. VBAT is the lowest battery-powered mode that can maintain an RTCC. Wake-up from VBAT mode can only occur when VDD is reapplied. The wake-up will appear to be a POR to the rest of the device.

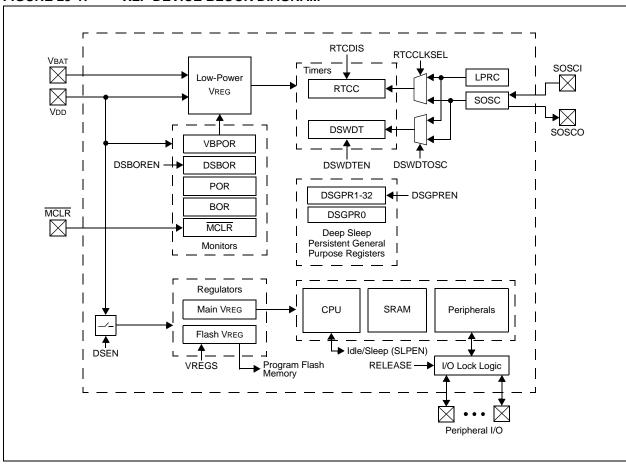
In VBAT mode, the Deep Sleep Watchdog Timer is disabled. The RTCC and DSGPR1 through DSGPR32 registers may be enabled or disabled depending on the state of the RTCDIS bit (DSCON<12>) and the DSGPREN bit (DSCON<13>), respectively. Deep Sleep Persistent General Purpose Register 0 (DSGPR0) is always enabled in VBAT mode.

29.3.6 XLP POWER-SAVING MODES

Figure 29-1 shows a block diagram of the system domain for XLP devices and the related power-saving features. The various blocks are controlled by the following Configuration bit settings and SFRs:

- DSBOREN (DEVCFG2<20>)
- DSEN (DSCON<15>)
- DSGPREN (DSCON<13>)
- DSWDTEN (DEVCFG2<30>)
- DSWDTOSC (DEVCFG2<29>)
- RELEASE (DSCON<0>)
- RTCCLKSEL (RTCCON <9:8>)
- RTCDIS (DSCON<12>)
- SLPEN (OSCCON<4>)
- VREGS (PWRCON<0>)

FIGURE 29-1: XLP DEVICE BLOCK DIAGRAM



29.4 Deep Sleep (DSCTRL) Control Registers

TABLE 29-1: POWER-SAVING MODES REGISTER SUMMARY

SS										E	Bits								_
Virtual Address (BF80_#)	Register Name ⁽²⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets ⁽¹⁾
0000	DSCON	31:16		_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
		15:0	DSEN	_	DSGPREN	RTCDIS	_	_	_	RTCCWDIS	_	_	_	_	_	WAKEDIS	DSBOR	RELEASE	0000
0010	DSWAKE	31:16		_	_	_	_	-	_	_	_	1	-	-	_	_	-	_	0000
		15:0												0000					
0020	DSGPR0 ⁽¹⁾	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0040	DSGPR1	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0044	DSGPR2	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0048	DSGPR3	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
004C	DSGPR4	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0050	DSGPR5	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0054	DSGPR6	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0058	DSGPR7	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
005C	DSGPR8	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0		Deep Sleep Persistent General Purpose bits <15:0> 00										0000					
0060	DSGPR9	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0064	DSGPR10	31:16						De	eep Slee	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000
0068	DSGPR11	31:16													0000				
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	15:0>						0000

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

_egend: — = unimplemented, read as '0'.

e 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

TABLE 29-1: POWER-SAVING MODES REGISTER SUMMARY

sse										E	Bits								£
Virtual Address (BF80_#)	Register Name ⁽²⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets ⁽¹⁾
006C	DSGPR12	31:16		•	•			De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>			•		•	0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0070	DSGPR13	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0074	DSGPR14	31:16											0000						
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0078	DSGPR15	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
007C	DSGPR16	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0080	DSGPR17	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	ieneral Pur	pose bits <	:15:0>						0000
0084	DSGPR18	31:16						De	eep Slee _l	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	ieneral Pur	pose bits <	:15:0>						0000
0088	DSGPR19	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
008C	DSGPR20	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0090	DSGPR21	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0094	DSGPR22	31:16								p Persistent G									0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
0098	DSGPR23	31:16						De	eep Slee	p Persistent G	eneral Purp	ose bits <	31:16>						0000
		15:0								p Persistent G									0000
009C	DSGPR24	31:16								p Persistent G									0000
		15:0								p Persistent G									0000
00A0	DSGPR25	31:16								p Persistent G									0000
		15:0							•	p Persistent G									0000
00A4	DSGPR26	31:16								p Persistent G									0000
		15:0						D	eep Slee	p Persistent G	ieneral Pur	pose bits <	:15:0>						0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

TABLE 29-1: POWER-SAVING MODES REGISTER SUMMARY

sse										E	Bits								1)
Virtual Address (BF80_#)	Register Name ⁽²⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets ⁽¹⁾
00A8	DSGPR27	31:16						D	eep Sleep	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0		Deep Sleep Persistent General Purpose bits <15:0> 00										0000					
00AC	DSGPR28	31:16												0000					
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
00B0	DSGPR29	31:16						D	eep Sleep	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
00B4	DSGPR30	31:16						D	eep Sleep	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000
00B8	DSGPR31	31:16						D	eep Sleep	Persistent Ge	eneral Purp	ose bits <	31:16>						0000
		15:0												0000					
00BC	DSGPR32	31:16	_												0000				
		15:0						D	eep Slee	p Persistent G	eneral Pur	pose bits <	:15:0>						0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

REGISTER 29-1: DSCON: DEEP SLEEP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	_	_	_	_	_	_
45.0	HC, R/W-y	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
15:8	DSEN ⁽¹⁾	_	DSGPREN	RTCDIS	_		1	RTCCWDIS
7.0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
7:0	_	_	_	_	_	WAKEDIS	DSBOR ⁽²⁾	RELEASE

Legend:HC = Hardware Clearedy = Value set from Configuration bits on PORR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0' bit 15 **DSEN:** Deep Sleep Enable bit⁽¹⁾

1 = Deep Sleep mode is entered on a WAIT command

0 = Sleep mode is entered on a WAIT command

bit 14 Unimplemented: Read as '0'

bit 13 DSGPREN: General Purpose Registers Enable bit

1 = General purpose register retention is enabled in Deep Sleep mode

0 = No general purpose register retention in Deep Sleep mode

bit 12 RTCDIS: RTCC Module Disable bit

1 = RTCC module is not enabled

0 = RTCC module is enabled

bit 11-9 Unimplemented: Read as '0'

bit 8 RTCCWDIS: RTCC Wake-up Disable bit

1 = Wake-up from RTCC is disabled

0 = Wake-up from RTCC is enabled

bit 7-3 Unimplemented: Read as '0'

bit 2 WAKEDIS: Wake-up Source Disable bit

1 = External wake-up source is disabled

0 = External wake-up source is enabled

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit⁽²⁾

1 = DSBOREN was enabled and VDD dropped below the DSBOR threshold during Deep Sleep (2)

0 = DSBOREN was disabled, or VDD did not drop below the DSBOR threshold during Deep Sleep

bit 0 RELEASE: I/O Pin State Release bit

1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states

0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

Note 1: To enter Deep Sleep mode, Sleep mode must be executed after setting the DSEN bit.

2: Unlike all other events, a Deep Sleep Brown-out Reset (BOR) event will not cause a wake-up from Deep Sleep mode; this bit is present only as a status bit.

REGISTER 29-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	_	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	-	_	_	_	_	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
15:8	_	_	_	_	_	_	_	DSINT0
7.0	R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0
7:0	DSFLT	_		DSWDT	DSRTC	DSMCLR	_	_

Legend:HS = Hardware SetR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0' bit 8 **DSINT0:** Interrupt-on-Change bit

1 = Interrupt-on-change was asserted during Deep Sleep0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 DSFLT: Deep Sleep Fault Detected bit

1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted

0 = No Fault was detected during Deep Sleep

bit 6-5 Unimplemented: Read as '0'

bit 4 DSWDT: Deep Sleep Watchdog Timer Time-out bit

1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep

0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 DSRTC: Real-Time Clock and Calendar Alarm bit

1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep

0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 DSMCLR: MCLR Event bit

1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep

 $0 = \text{The } \overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 Unimplemented: Read as '0'

Note: All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

REGISTER 29-3: DSGPRX: DEEP SLEEP PERSISTENT GENERAL PURPOSE REGISTER 'x' (x = 0 THROUGH 32)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
31:24			Deep Sle	eep Persisten	General Pur	oose bits		
22.40	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:16			Deep Sle	eep Persisten	General Pur	oose bits		
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15.6			Deep Sle	eep Persisten	General Pur	oose bits		
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
7:0			Deep Sle	eep Persisten	General Pur	oose bits		

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 Deep Sleep Persistent General Purpose bits

Note: The contents of the DSGPR0 register are retained, even in Deep Sleep and VBAT modes. The DSPGR1 through DSPGR32 registers are disabled by default in Deep Sleep and VBAT modes, but can be enabled with the DSGPREN bit (DSCON<13>). All register bits are reset only in the case of a VDD Power-on Reset (POR) event outside of Deep Sleep mode.

29.5 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 29-2 for more information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 29-2: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
СТМИ	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Low-Voltage Detect	HLVDMD	PMD1<20>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Comparator 3	CMP3MD	PMD2<2>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See TABLE 1: "PIC32MX1XX 28/44-Pin XLP (General Purpose) Family Features" and TABLE 2: "PIC32MX2XX 28/44-Pin XLP (USB) Family Features" for the lists of available peripherals.

2: The module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

29.5.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to enabled or disabled peripherals:

- · Control register lock sequence
- · Configuration bit select lock

29.5.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the Configuration bit, PMDLOCK (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

29.5.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The Configuration bit, PMDL1WAY (DEVCFG3<28>), blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

TABLE 29-3: PERIPHERAL MODULE DISABLE REGISTER MAP

ess											Bits								"
Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F240	PMD1	31:16	_	_	_	_		_	_	_	_		_	HLVDMD	1	_	I	_	0000
F240	FINIDI	15:0	_	_	_	CVRMD	_	_	_	CTMUMD	_	_	_	_	-	_	-	AD1MD	0000
F250	PMD2	31:16		-	_	_	-	_	-	_	_		-	_	1	_	ı	_	0000
F230	1 IVID2	15:0	_	_	_	_	_	_	_	_	_	-	_	_	1	CMP3MD	CMP2MD	CMP1MD	0000
F260	PMD3	31:16	_	_	_	_	_	_	_	_	_	-	_	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
F260	I IVIDS	15:0	_	_	_	_	_	_	_	_	_	-	_	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
F270	PMD4	31:16	_	_	_	_		_	_	_	_	_	_	_		_	_	_	0000
F270	I WID4	15:0	_	_	_	_	_	_	_	_	_	-	_	T5MD	T4MD	T3MD	T2MD	T1MD	0000
F280	PMD5	31:16	_	_	_	_	_	_	_	USB1MD	_	_	_	_	_	_	I2C1MD	I2C1MD	0000
1 200	i WiDS	15:0	_	_	_	_		_	SPI2MD	SPI1MD	_	_	_	_		_	U2MD	U1MD	0000
F290	PMD6	31:16	_	_	_	_		_	_	_	_	_	_	_		_	_	PMPMD	0000
1 290	i wibo	15:0	_	_	_	_	_	_	_	_	_	-	_	_	1	_	REFOMD	RTCCMD	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See 12.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

NOTES:

30.0 SPECIAL FEATURES

Note:

This data sheet summarizes the features of the PIC32MX1XX/2XX 28/44-pin XLP Family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Configuration" Section 32. Section (DS60001124) and "Programming and Diagnostics" (DS60001129), which are available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/44-pin XLP Family devices include the following features intended to maximize application flexibility, reliability and minimize cost through elimination of external components.

- · Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming[™] (ICSP[™])

30.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- CFGCON: Configuration Control Register

In addition, the DEVID register (Register 30-6) provides device and revision information.

30.2 Configuration Registers

TABLE 30-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

ess (ø								Bits									S
Virtual Address (BFC0_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
2FF0	DEVCFG3	31:16	_	FUSBIDIO	IOL1WAY	PMDL1WAY	_	_	-	_	Al2C2	AI2C1	_	_	_	_	_	I	xxxx
2110	DE VOI OS	15:0							1	USERID<1	5:0>								xxxx
2FF4	DEVCFG2	31:16	FDSEN	DSWDT EN	DSWD TOSC		DS	SWDTPS<4:	0>		DSBOR EN	_	VBAT BOREN	BOREN	-	FP	LLODIV<2:	0>	xxxx
		15:0	UPLLEN ⁽¹⁾	_	_	_		UPI	LIDIV<2:0	_{>} (1)	FPLLICLK	FF	PLLMUL<2:0	0>	_	FF	PLLIDIV<2:0)>	xxxx
2FF8	DEVCFG1	31:16	_	-	-	-	_	_	FWDTWII	NSZ<1:0>	FWDTEN	WINDIS	WDTS PGM		\	WDTPS<4:0)>		xxxx
		15:0	FCKSM	l<1:0>	FPBDI	/<1:0>	_	OSCIOFNC	POSCM	OD<1:0>	IESO	_	FSOSCEN	_	_	F	NOSC<2:0:	>	xxxx
2550	DEVCFG0	31:16	_	_		CP	_	_	_	BWP	SMCLR	_	_	_		PWP<	7:4> ⁽²⁾		xxxx
ZFFC	DEVOFGU	15:0		PWP	<3:0>		_	_	_	_	_	_	_	ICESE	L<1:0>	JTAGEN	DEBUG	G<1:0>	xxxx

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on PIC32MX2XX devices.

2: PWP<8:7> are only available on devices with 256 KB of Flash.

TABLE 30-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

				,															
ess										Bit	s								£
Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets ⁽¹⁾
F000	CFGCON	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
F200	CFGCON	15:0	_	_	IOLOCK	PMDLOCK	_	_	_	RPFA	_	_	_	_	JTAGEN	_	FAEN	TDOEN	000B
F220	DEVID	31:16		VER<	<3:0>							DEVID<2	7:16>						xxxx ⁽¹⁾
		15:0								DEVID<	15:0>								xxxx ⁽¹⁾
E220	SYSKEY(3)	31:16								SYSKEY	∠31·0 \								0000
1 230	O I OIKE I	15:0								O I OILL I	NO 1.02								0000

.egend: x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

REGISTER 30-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	R/P
31:24	_	_	_	CP	_	_		BWP
22.40	R/P	r-1	r-1	r-1	R/P	R/P	R/P	R/P
23:16	SMCLR	_	_	_		PWP	<7:4>	
45.0	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
15:8		PWP<	:3:0>		_	_	-	_
7.0	r-1	r-1	r-1	R/P	R/P	R/P	R/P	R/P
7:0	_	_	_	ICESEL	<1:0> ⁽²⁾	JTAGEN ⁽¹⁾	DEBU	G<1:0>

Legend:r = Reserved bitP = Programmable bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'<math>-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 30-29 **Reserved:** Write '1' bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.

1 = Protection is disabled0 = Protection is enabled

bit 27-25 Reserved: Write '1'

bit 24 BWP: Boot Flash Write-Protect bit

Prevents Boot Flash memory from being modified during code execution.

1 = Boot Flash is writable

0 = Boot Flash is not writable

bit 23 SMCLR: Soft Master Clear Enable bit

 $1 = \overline{MCLR}$ pin generates a normal system Reset

 $0 = \overline{MCLR}$ pin generates a POR

bit 22-20 Reserved: Write '1'

Note 1: This bit sets the value for the JTAGEN bit in the CFGCON register.

2: The PGEC4/PGED4 pin pair is not available on all devices. Refer to the "Pin Diagrams" section for availability.

REGISTER 30-1: **DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)**

bit 19-12 **PWP<7:0>:** Program Flash Write-Protect bits⁽³⁾

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the one's compliment of the number of write protected program Flash memory pages.

```
11111111 = Disabled
111111110 = 0xBD00_0FFF
111111101 = 0xBD00_1FFF
111111100 = 0xBD00_2FFF
11111011 = 0xBD00_3FFF
111111010 = 0xBD00_4FFF
11111001 = 0xBD00_5FFF
111111000 = 0xBD00_6FFF
11110111 = 0xBD00_7FFF
11110110 = 0xBD00_8FFF
11110101 = 0xBD00_9FFF
11110100 = 0xBD00_AFFF
11110011 = 0xBD00_BFFF
11110010 = 0xBD00_CFFF
11110001 = 0xBD00_DFFF
11110000 = 0xBD00_EFFF
11101111 = 0xBD00_FFFF
10111111 = 0xBD03 FFFF
10111110 = Reserved
000000000 = Reserved
```

- bit 11-5 Reserved: Write '1'
- ICESEL<1:0>: In-Circuit Emulator/Debugger Communication Channel Select bits⁽²⁾ bit 4-3
 - 11 = PGEC1/PGED1 pair is used
 - 10 = PGEC2/PGED2 pair is used
 - 01 = PGEC3/PGED3 pair is used
 - 00 = PGEC4/PGED4 pair is used(2)
- JTAGEN: JTAG Enable bit(1) bit 2
- 1 = JTAG is enabled
 - 0 = JTAG is disabled
- bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
 - 1x = Debugger is disabled
 - 0x = Debugger is enabled
- **Note 1:** This bit sets the value for the JTAGEN bit in the CFGCON register.
 - 2: The PGEC4/PGED4 pin pair is not available on all devices. Refer to the "Pin Diagrams" section for availability.

REGISTER 30-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P	
31.24		_			_	_	FWDTWI	NSZ<1:0>	
22,46	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P	
23:16	FWDTEN	WINDIS	WDTSPGM			WDTPS<4:0>			
15.0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P	
15:8	FCKSM	/l<1:0>	FPBDI'	V<1:0>	_	OSCIOFNC	POSCM	OD<1:0>	
7.0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P	
7:0	IESO	_	FSOSCEN		_	FNOSC<2:0>			

Legend:r = Reserved bitP = Programmable bitR = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-26 Reserved: Write '1'

bit 25-24 FWDTWINSZ<1:0>: Watchdog Timer Window Size bits

11 = Window size is 25%

10 = Window size is 37.5%

01 = Window size is 50%

00 = Window size is 75%

bit 23 FWDTEN: Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software

0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 WINDIS: Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode

0 = Watchdog Timer is in Window mode

bit 21 WDTSPGM: Watchdog Timer Stop During Flash Programming bit

1 = Watchdog Timer stops during Flash programming

0 = Watchdog Timer runs during Flash programming

bit 20-16 WDTPS<4:0>: Watchdog Timer Postscale Select bits

10100 = 1:1048576

10011 = 1:524288

10010 = 1:262144

10001 = 1:131072

10000 = 1:65536

01111 = 1:32768

01110 = 1:16384

01101 = 1:8192

01100 = 1:4096

01011 = 1:2048

01010 = 1:1024

01001 = 1:512

01000 = 1:256

00111 = 1:128

00110 = 1:6400101 = 1:32

00100 = 1:16

00011 = 1:8

00010 = 1:4

00001 = 1:2

00000 = 1:1

All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

REGISTER 30-2: **DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)** bit 15-14 FCKSM<1:0>: Clock Switching and Monitor Selection Configuration bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled bit 13-12 FPBDIV<1:0>: Peripheral Bus Clock Divisor Default Value bits 11 = PBCLK is SYSCLK divided by 8 10 = PBCLK is SYSCLK divided by 4 01 = PBCLK is SYSCLK divided by 2 00 = PBCLK is SYSCLK divided by 1 bit 11 Reserved: Write '1' bit 10 OSCIOFNC: CLKO Enable Configuration bit 1 = CLKO output disabled 0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00) bit 9-8 POSCMOD<1:0>: Primary Oscillator Configuration bits 11 = Primary Oscillator is disabled 10 = HS Oscillator mode is selected 01 = XT Oscillator mode is selected 00 = External Clock mode is selected bit 7 IESO: Internal External Switchover bit 1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled) 0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled) Reserved: Write '1' bit 6 FSOSCEN: Secondary Oscillator Enable bit bit 5 1 = Enable Secondary Oscillator 0 = Disable Secondary Oscillator bit 4-3 Reserved: Write '1' bit 2-0 FNOSC<2:0>: Oscillator Selection bits 111 = Fast RC Oscillator with divide-by-N (FRCDIV) 110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler 101 = Low-Power RC Oscillator (LPRC) 100 = Secondary Oscillator (Sosc) 011 = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL) 010 = Primary Oscillator (XT, HS, EC)⁽¹⁾ 001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL) 000 = Fast RC Oscillator (FRC)

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

REGISTER 30-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
31.24	FDSEN	DSWDTEN	DSWDTOSC		DS	WDTPS<4:0	>	
22,46	R/P	r-1	R/P	R/P	r-1	R/P	R/P	R/P
23:16	DSBOREN	_	VBATBOREN	BOREN	_	FF	PLLODIV<2:0)>
15.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
15:8	UPLLEN ⁽¹⁾	_	_	_	_	UP	LLIDIV<2:0>	(1)
7.0	R/P	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
7:0	FPLLICLK		FPLLMUL<2:0	>	_	F	PLLIDIV<2:0	>

Legend: r = Reserved bit P = Programmable bit R = Readable bit U = Unimplemented bit, read as '0' W = Writable bit -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 FDSEN: Deep Sleep Enable bit
 - 1 = Deep Sleep mode is entered on a WAIT command
 - 0 = Sleep mode is entered on a WAIT command
- bit 30 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
 - 1 = Enable the Deep Sleep Watchdog Timer (DSWDT) during Deep Sleep mode
 - 0 = Disable the DSWDT during Deep Sleep mode
- bit 29 DSWDTOSC: Deep Sleep Watchdog Timer Reference Clock Select bit
 - 1 = Select the LPRC Oscillator as the DSWDT reference clock
 - 0 = Select the Secondary Oscillator as the DSWDT reference clock
- bit 28-24 DSWDTPS<4:0>: Deep Sleep Watchdog Timer Postscale Select bits
 - $11111 = 1:2^{36}$
 - $11110 = 1:2^{35}$
 - $11101 = 1:\overline{2}^{34}$
 - $11100 = 1:2^{33}$ $11011 = 1:2^{32}$
 - $11010 = 1:2^{31}$
 - $11001 = 1.\overline{2}^{30}$
 - $11000 = 1:2^{29}$
 - $10111 = 1:2^{28}$
 - $10110 = 1:2^{27}$
 - $10101 = 1:2^{26}$
 - $10100 = 1.2^{25}$
 - $10011 = 1:2^{24}$
 - $10010 = 1:2^{23}$ $10001 = 1:2^{22}$
 - $10000 = 1:\overline{2^{21}}$
 - $01111 = 1:2^{20}$
 - $01110 = 1:\overline{2}^{19}$

 - $01101 = 1:2^{18}$ $01100 = 1:2^{17}$
 - $01011 = 1:2^{16}$
 - $01010 = 1:\overline{2}^{15}$
 - $01001 = 1:2^{14}$
 - $01000 = 1:2^{13}$
 - $00111 = 1:2^{12}$
 - $00110 = 1:2^{11}$
 - $00101 = 1:2^{10}$
 - $00100 = 1:2^9$
 - $00011 = 1:2^8$
 - $00010 = 1:2^{7}$
 - $00001 = 1:2^6$
 - $00000 = 1:2^5$

Note 1: This bit is only available on PIC32MX2XX devices.

```
REGISTER 30-3:
                      DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)
bit 23
           DSBOREN: Deep Sleep BOR Enable bit
           1 = Enable BOR during Deep Sleep mode
           0 = Disable BOR during Deep Sleep mode
           Reserved: Write '1'
bit 22
           VBATBOREN: VBAT BOR Enable bit
bit 21
           1 = Enable BOR during VBAT mode
           0 = Disable BOR during VBAT mode
bit 20
           BOREN: Brown-Out Reset (BOR) Enable bit
           1 = Enable BOR
           0 = Disable BOR
bit 19
          Reserved: Write '1'
bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits
           111 = PLL output divided by 256
           110 = PLL output divided by 64
           101 = PLL output divided by 32
           100 = PLL output divided by 16
           011 = PLL output divided by 8
           010 = PLL output divided by 4
           001 = PLL output divided by 2
           000 = PLL output divided by 1
           UPLLEN: USB PLL Enable bit<sup>(1)</sup>
bit 15
           1 = Disable and bypass USB PLL
           0 = Enable USB PLL
bit 14-11 Reserved: Write '1'
bit 10-8
          UPLLIDIV<2:0>: USB PLL Input Divider bits<sup>(1)</sup>
           111 = 12x divider
           110 = 10x divider
           101 = 6x \text{ divider}
           100 = 5x \text{ divider}
           011 = 4x \text{ divider}
           010 = 3x \text{ divider}
           010 = 3x \text{ divider}
           001 = 2x \text{ divider}
           000 = 1x \text{ divider}
bit 7
          FPLLICLK: System PLL Input Clock Select bit
           1 = FRC is selected as input to the System PLL
           0 = Posc is selected as input to the System PLL
           FPLLMUL<2:0>: PLL Multiplier bits
bit 6-4
           111 = 24x multiplier
           110 = 21x multiplier
           101 = 20x multiplier
           100 = 19x multiplier
           011 = 18x multiplier
           010 = 17x multiplier
           001 = 16x multiplier
           000 = 15x multiplier
bit 3
           Reserved: Write '1'
Note 1: This bit is only available on PIC32MX2XX devices.
```

REGISTER 30-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 2-0 FPLLIDIV<2:0>: PLL Input Divider bits

111 = 12x divider

110 = 10x divider

101 = 6x divider

100 = 5x divider

011 = 4x divider

010 = 3x divider

001 = 2x divider

000 = 1x divider

Note 1: This bit is only available on PIC32MX2XX devices.

REGISTER 30-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	r-1	R/P	R/P	R/P	r-1	r-1	r-1	r-1			
31:24	_	FUSBIDIO	IOL1WAY	PMDL1WAY	_	_	_	_			
22,46	R/P	R/P	r-1	r-1	r-1	r-1	r-1	r-1			
23:16	Al2C2	Al2C1	_	_	_	_	_	_			
15.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P			
15:8				USERID<1	15:8>						
7.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P			
7:0	USERID<7:0>										

Legend:		r = Reserved bit	P = Programmable bit
	R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
	-n = Value at POR	'1' = Bit is set	0' = Bit is cleared $x = Bit is unknown$

bit 31 Reserved: Write '1'

bit 30 FUSBIDIO: USB USBID Selection bit

1 = USBID pin is controlled by the USB module 0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit

1 = Allow only one reconfiguration0 = Allow multiple reconfigurations

bit 28 PMDI1WAY: Peripheral Module Disable Configuration bit

1 = Allow only one reconfiguration0 = Allow multiple reconfigurations

bit 27-24 Reserved: Write '1'

bit 23 Al2C2: Alternate I/O Select for I2C2 bit

1 = I2C2 uses the SDA2/SCL2 pins 0 = I2C2 uses the ASDA2/ASCL2 pins

bit 22 Al2C1: Alternate I/O Select for I2C1 bit

1 = I2C1 uses the SDA1/SCL1 pins 0 = I2C1 uses the ASDA1/ASCL1 pins

bit 21-16 Reserved: Write '1'

bit 15-0 USERID<15:0>: User ID bits

This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

REGISTER 30-5: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_		_	-	_	_	
22.46	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	_	_	-	_	-	_	_	1
45.0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-1
15:8	_	_	IOLOCK ⁽¹⁾	PMDLOCK ⁽¹⁾	1	_		RPFA
7.0	U-0	U-0	U-0	U-0	R/W-1	U-0	R/W-1	R/W-1
7:0	_	_	1	_	JTAGEN	_	FAEN	TDOEN

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit⁽¹⁾

 ${\tt 1}$ = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.

0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.

bit 12 **PMDLOCK:** Peripheral Module Disable bit⁽¹⁾

1 = Peripheral module is locked. Writes to PMD registers is not allowed.

0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11-9 Unimplemented: Read as '0'

bit 8 RPFA: Reduced Power Flash Access bit

This bit is used for low clock frequency operation.

1 = Enables Low Power Read Circuit

0 = Disables Low Power Read Circuit (which improves flash read access timing)

bit 4 **Unimplemented:** Read as '0'

bit 3 JTAGEN: JTAG Port Enable bit

1 = Enable the JTAG port

0 = Disable the JTAG port

bit 2 **Unimplemented:** Read as '1'

bit 1 FAEN: Flash Access Enable bit

On entry to ICSP (TMOD0) and JTAG Test Mode (TMOD12) hardware clears this bit to prevent the processor (and all other bus initiators) from fetching from (unprogrammed) flash memory. This effectively stalls the initiator accessing the flash. To access the flash this bit must be set first.

1 = Flash is accessible

0 = Flash is not accessible

bit 0 TDOEN: TDO Enable for 2-Wire JTAG bit

1 = 2-wire JTAG protocol uses TDO

0 = 2-wire JTAG protocol does not use TDO

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

REGISTER 30-6: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04:04	R	R	R	R	R	R	R	R
31:24		VER<	3:0> ⁽¹⁾			DEVID<	27:24> ⁽¹⁾	
22.40	R	R	R	R	R	R	R	R
23:16				DEVID<2	23:16> ⁽¹⁾			
45.0	R	R	R	R	R	R	R	R
15:8	DEVID<15:8> ⁽¹⁾							
7.0	R	R	R	R	R	R	R	R
7:0	DEVID<7:0>(1)							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits⁽¹⁾ bit 27-0 **DEVID<27:0>:** Device ID bits⁽¹⁾

Note 1: See the "PIC32 Flash Programming Specification" (DS60001145) for a list of Revision and Device ID values.

30.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX 28/44-pin XLP Family devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX 28/44-pin XLP Family family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 30-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in 33.1 "DC Characteristics".

Note: It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

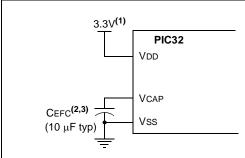
30.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

30.3.2 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX 28/44-pin XLP Family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in 33.1 "DC Characteristics".

FIGURE 30-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



- Note 1: These are typical operating voltages. Refer to 33.1 "DC Characteristics" for the full operating ranges of VDD.
 - **2:** It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.
 - **3:** The typical voltage on the VCAP pin is 1.8V.

30.4 Programming and Diagnostics

PIC32MX1XX/2XX 28/44-pin XLP Family devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

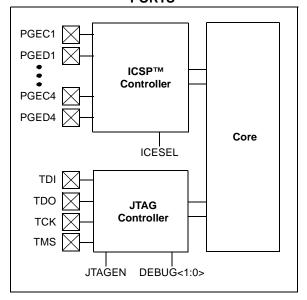
- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

Figure 30-2 illustrates a block diagram of the programming, debugging, and trace ports.

FIGURE 30-2: BLOCK DIAGRAM OF PROGRAMMING,

PROGRAMMING,
DEBUGGING AND TRACE
PORTS



NOTES:

31.0 INSTRUCTION SET

The PIC32MX1XX/2XX XLP instruction set complies with the MIPS32[®] Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- · Core extend instructions
- · Coprocessor 1 instructions
- · Coprocessor 2 instructions

Note: Refer to "MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set" at www.imgtec.com for more information.

PIC32MX1XX/2XX 28/44-PIN XLP FAMILY					
NOTES:					

32.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASMTM Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit™ 3
- · Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

32.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac OS[®] X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- · Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- · Multiple projects
- · Multiple tools
- Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

32.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- · Support for the entire device instruction set
- Support for fixed-point and floating-point data
- · Command-line interface
- · Rich directive set
- · Flexible macro language
- · MPLAB X IDE compatibility

32.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

32.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

32.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- · Command-line interface
- · Rich directive set
- · Flexible macro language
- MPLAB X IDE compatibility

32.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

32.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

32.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

32.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

32.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

32.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEMTM and dsPICDEMTM demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELoq® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

32.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]

33.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/44-pin XLP Family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/44-pin XLP Family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias	
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0.3V to +4.0V
Voltage on VBAT with respect to VSS	0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD ≥ 2.7V (Note 3)	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.7V (Note 3)	0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	
Maximum current out of Vss pin(s)	200 mA
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	150 mA
Maximum current sourced by all ports (Note 2)	150 mA

- Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 33-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.

33.1 DC Characteristics

TABLE 33-1: OPERATING MIPS VS. VOLTAGE

	Vpp Pango	Tomp Pango	Max. Frequency
Characteristic	VDD Range (in Volts) ⁽¹⁾	Temp. Range (in °C)	PIC32MX1XX/2XX 28/44-pin XLP Family
DC5	2.5-3.6V	-40°C to +85°C	72 MHz
DC5a	2.5-3.6V	-40°C to +105°C	72 MHz

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 33-5 for BOR values.

TABLE 33-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Minimum	Typical	Maximum	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	_	+125	°C
Operating Ambient Temperature Range	TA	-40	_	+85	°C
V-temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	_	+140	°C
Operating Ambient Temperature Range	TA	-40	_	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD - S IOH)	PD		PINT + PI/0	0	W
I/O Pin Power Dissipation: $I/O = S ((\{VDD - VOH\} \times IOH) + S (VOL \times IOL))$					
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θ.	JA	W

TABLE 33-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Maximum	Unit	Notes
Package Thermal Resistance, 28-pin SOIC	θЈА	50	_	°C/W	1
Package Thermal Resistance, 28-pin QFN	θЈА	35	_	°C/W	1
Package Thermal Resistance, 44-pin QFN	θЈА	32	_	°C/W	1
Package Thermal Resistance, 44-pin TQFP	θЈА	45	_	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 33-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics	Min. Typ. Max. Units Condit				Conditions
Operati	ng Voltag	e					
DC10	VDD	Supply Voltage (Note 2)	2.5	_	3.6	V	_
DC12	VDR	RAM Data Retention Voltage (Note 1)	2.0	_	_	V	_
DC16	VPOR	VDD Start Voltage (Note 3) to Ensure Internal Power-on Reset Signal	1.75	_	2.1	V	_
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.00005	_	0.115	V/µs	_
DC18	VBAT	Battery Supply Voltage	1.94	_	3.6	V	_

- Note 1: This is the limit to which VDD can be lowered without losing RAM data.
 - 2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 33-5 for BOR values.
 - 3: VDD voltage must remain below VPOR for a minimum of 200 µs to ensure POR.

TABLE 33-5: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-Temp				
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾ Typ. Max. Units Conditions				
BO10	VBOR	BOR Event on VDD transition high-to-low (Note 2)	2.2		2.384	V	

- Note 1: Parameters are for design guidance only and are not tested in manufacturing.
 - 2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

TABLE 33-6: LOW-VOLTAGE DETECT CHARACTERISTICS

DC CHARACTERISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)					
DC CHARACTERISTICS	Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					

Param No.	Symbol	Characteristic		Min.	Тур.	Max.	Units	Conditions
HLV10	VHLVD	HLVD Voltage on VDD	LVDL<3:0> = 0100 ⁽¹⁾	_	3.59	_	V	_
		Transition	LVDL<3:0> = 0101	_	3.44	_	V	_
			LVDL<3:0> = 0110	_	3.13	_	V	_
			LVDL<3:0> = 0111	_	2.92	_	V	_
			LVDL<3:0> = 1000	_	2.81	_	V	_
			LVDL<3:0> = 1001	_	2.60	_	V	_
			LVDL<3:0> = 1010	_	2.50		٧	
HLV11	VHTHL	HLVD Voltage on HLVDIN Pin Transition	LVDL<3:0> = 1111	_	1.20	_	V	_

Note 1: Trip points for values of HLVD<3:0>, from '0000' to '0011' and '1001' to '1110' are not implemented.

TABLE 33-7: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARA	CHARACTERISTICS					
Parameter No.	Typical ⁽³⁾	Max.	Units Conditions			
Operating (Current (IDD)	(Notes 1, 2, 5))			
DC20	1.7		mA	4 MH	z (Note 4)	
DC21	4		mA	1	0 MHz	
DC22	12.5	_	mA	30 MF	Hz (Note 4)	
DC23	20	_	mA	50 MHz (Note 4)		
DC24	29	_	mA	72 MHz		
DC25	100		μΑ	+25°C, 3.3V LPRC (31 kHz) (Note 4)		

- Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.
 - 2: The test conditions for IDD measurements are as follows:
 - Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
 - CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
 - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
 - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to Vss
 - MCLR = VDD
 - CPU executing while(1) statement from Flash
 - · RTCC and JTAG are disabled
 - **3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 4: This parameter is characterized, but not tested in manufacturing.
 - **5:** IPD electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

TABLE 33-8: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACT	ERISTICS		(unless other	erwise stated) mperature -40°C ≤	erating Conditions: 2.5V to 3.6V wise stated) perature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp				
Parameter No.	Typical ⁽²⁾	Max.	Units Conditions						
Idle Current (II	DLE): Core Of	f, Clock on E	Base Current	(Notes 1, 4)					
DC30a	0.6	_	mA		4 MHz (Note 3)				
DC31a	1.5	_	mA		10 MHz				
DC32a	4.5	_	mA		30 MHz (Note 3)				
DC33a	7.5	_	mA		50 MHz (Note 3)				
DC34a	10.5	_	mA		72 MHz				
DC37a	100	_	μA	-40°C LPRC (31 kHz					
DC37b	250	_	μΑ	+25°C 3.3V (Note 3)					
DC37c	380		μA	+85°C					

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD
- RTCC and JTAG are disabled
- 2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3: This parameter is characterized, but not tested in manufacturing.
- 4: IIDLE electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

TABLE 33-9: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARAC	TERISTICS			ird Operating ing temperat	g Conditions: 2.5V to 3.6V (unless otherwise stated) ure $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-Temp
Param. No.	Typical ⁽²⁾	Maximum	Units		Conditions
Power-De	own Curren	t (IPD) (Note	: 1)		
DC40k	_	_	μΑ	-40°C	
DC40I	25	42	μA	+25°C	Sloop (Note 4)
DC40m	240	390	μA	+85°C	Sleep (Note 1)
DC40n	_	_	μA	+105°C	
DC41k	_	_	nA	-40°C	
DC41I	673	800	nA	+25°C	Deep Sleep (Note 5)
DC41m	-	_	nA	+85°C	Deep Sieep (Note 3)
DC41n	-	_	nA	+105°C	
DC42k		_	nA	-40°C	
DC42I		_	nA	+25°C	VBAT (Note 6)
DC42m		_	nA	+85°C	VBAT (Note 0)
DC42n		_	nA	+105°C	
Module D	Differential (Current			
DC44a	5	_	μΑ	3.6V	Watchdog Timer Current: ∆IWDT (Note 3)
DC44b	23	_	μΑ	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC + ΔITMR (Note 3)
DC44c	1000	_	mA	3.6V	ADC Current: ΔIADC (Notes 3, 4)
DC44d	15	_	μA	3.6V	Deadman Timer Current: ΔIDMT
DC44e	0.71	_	μA	3.6V	Deep Sleep Watchdog Timer Current: ΔIDSWDT (Note 3)
DC44f	8.0	_	μΑ	3.6V	RTCC Current: ΔIRTCC (Note 3)

Note 1: The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), VusB3v3 is connected to Vss
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD
- · RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0; IOANCPEN = 0)
- 2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- **4:** Voltage regulator is operational (VREGS = 1).
- 5: The test conditions for Deep Sleep mode current measurements are as follows:
 - All I/O pins are configured as inputs and pulled to Vss
 - DSBOREN, DSWDTEN, and DGPREN are set to '0' and RTCDIS is set to '1'
- **6:** The test conditions for VBAT mode current measurements is as follows:
 - VBATBOREN is set to '0'

TABLE 33-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHA	ARACTER	RISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{Ta} \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq \text{Ta} \leq +105^{\circ}\text{C}$ for V-temp						
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions		
	VIL	Input Low Voltage							
DI10		I/O Pins with PMP	Vss	_	0.15 VDD	V			
		I/O Pins	Vss	_	0.2 VDD	V			
DI18		SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled (Note 4)		
DI19		SDAx, SCLx	Vss	_	0.8	V	SMBus enabled (Note 4)		
	VIH	Input High Voltage							
DI20		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 VDD	_	VDD	V	(Note 4,6)		
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 VDD + 0.8V	_	5.5	V	(Note 4,6)		
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 VDD	_	5.5	V			
DI28		SDAx, SCLx	0.65 VDD	_	5.5	V	SMBus disabled (Note 4,6)		
DI29		SDAx, SCLx	2.1	_	5.5	V	SMBus enabled, $2.0V \le VPIN \le 5.5$ (Note 4,6)		
DI30	ICNPU	Change Notification Pull-up Current	400	250	50	μА	VDD = 3.3V, VPIN = VSS (Note 3,6)		
DI31	ICNPD	Change Notification Pull-down Current ⁽⁴⁾	-400	-250	-50	μΑ	VDD = 3.3V, VPIN = VDD		
	lı∟	Input Leakage Current (Note 3)							
DI50		I/O Ports	_	_	<u>+</u> 1	μΑ	VSS ≤ VPIN ≤ VDD, Pin at high-impedance		
DI51		Analog Input Pins	_	_	<u>+</u> 1	μΑ	VSS ≤ VPIN ≤ VDD, Pin at high-impedance		
DI55		MCLR ⁽²⁾	_	_	<u>+</u> 1	μΑ	$Vss \leq Vpin \leq Vdd$		
DI56		OSC1	_	_	<u>+</u> 1	μА	$ \begin{array}{c} \text{VSS} \leq \text{VPIN} \leq \text{VDD,} \\ \text{XT and HS modes} \end{array} $		

- **Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - **3:** Negative current is defined as current sourced by the pin.
 - **4:** This parameter is characterized, but not tested in manufacturing.
 - **5:** See the "Pin Diagrams" section for the 5V-tolerant pins.
 - **6:** The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

TABLE 33-11: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHA	ARACTER	RISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)							
Param. No.	Symbol	Characteristics	Min. Typ. ⁽¹⁾ Max. Units Conditions							
DI60a	licl	Input Low Injection Current	0	_	₋₅ (2,5)	mA	This parameter applies to all pins, with the exception of the power pins.			
DI60b	lich	Input High Injection Current	0	_	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.			
DI60c	∑lict	Total Input Injection Current (sum of all I/O and Control pins)	-20 ⁽⁶⁾	_	+20 ⁽⁶⁾	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins (IICL + IICH) $\leq \sum$ IICT)			

- **Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 2: VIL source < (Vss 0.3). Characterized but not tested.
 - 3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.
 - **4:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.
 - 5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (Vss 0.3)).
 - 6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 2, IICL = (((Vss 0.3) VIL source) / Rs). If Note 3, IICH = ((IICH source (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (Vss 0.3) ≤ Vsource ≤ (VDD + 0.3), injection current = 0.

TABLE 33-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industriance $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temperature $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$					
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
DO10	VOL	Output Low Voltage I/O Pins	_	_	0.4	V	IOL ≤ 10 mA, VDD = 3.3V	
		Output High Voltage	1.5 ⁽¹⁾	_	_		IOH ≥ -14 mA, VDD = 3.3V	
DO20	Vон	I/O Pins	2.0 ⁽¹⁾	_	_	V	$IOH \ge -12 \text{ mA}, \text{ VDD} = 3.3 \text{V}$	
DO20 VOH			2.4	_	_	V	$IOH \ge -10 \text{ mA}, \text{ VDD} = 3.3 \text{V}$	
			3.0(1)	_	_	,	IOH ≥ -7 mA, VDD = 3.3V	

Note 1: Parameters are characterized, but not tested.

TABLE 33-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)						
Param. No.	Symbol	Characteristics	Min. Typical ⁽¹⁾ Max. Units Conditions							
		Program Flash Memory ⁽³⁾								
D130	EР	Cell Endurance	20,000	_	_	E/W	_			
D131	VPR	VDD for Read	2.5	_	3.6	_				
D132	VPEW	VDD for Erase or Write	2.5	_	3.6	V	_			
D134	TRETD	Characteristic Retention	10	_	_	Year	Provided no other specifications are violated			
D135	IDDP	Supply Current during Programming	_	10	_	mA	_			
	Tww	Word Write Cycle Time	_	471	_	es	See Note 4			
D136	TRW	Row Write Cycle Time	_	8020	_	Cycles	See Note 2,4			
D137	TPE	Page Erase Cycle Time	— 240114 — O See Note 4							
	TCE	Chip Erase Cycle Time	_	640304	_	FRC	See Note 4			

- Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.
 - 2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).
 - **3:** Refer to the "PIC32 Flash Programming Specification" (DS60001145) for operating conditions during programming and erase cycles.
 - 4: This parameter depends on FRC accuracy (See Table 33-20) and FRC tuning values (See Register 8-2).

TABLE 33-14: COMPARATOR SPECIFICATIONS

DC CHA	ARACTERI	Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	-10	_	+10	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	_	VDD	V	AVDD = VDD, AVSS = VSS (Note 2)
D302	CMRR	Common Mode Rejection Ratio	70	_	_	dB	Max VICM = (VDD - 1)V (Note 2)
D303A	TRESP	Large Signal Response Time	_	100	80	ns	AVDD = VDD, AVSS = VSS (Note 1,2)
D303B	TSRESP	Small Signal Response Time	_	50	160	ns	This is defined as an input step of 50 mV with 15 mV of overdrive (Note 2)
D304	ON2ov	Comparator Enabled to Output Valid	_		110	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	1.16	1.2	1.24	V	_
D312	TSET	Internal Comparator Voltage DRC Reference Setting time	_	_	1	μs	(Note 3)

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from Vss to VDD.

- **2:** These parameters are characterized but not tested.
- 3: Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.
- **4:** The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 33-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHA	RACTERI	STICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments		
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	_	1	10	μs	See Note 1		
D313	DACREFH	CVREF Input Voltage	AVss	_	AVDD	V	CVRSRC with CVRSS = 0		
		Reference Range	VREF-	_	VREF+	V	CVRSRC with CVRSS = 1		
D314	DVREF	CVREF Programmable Output Range	0	_	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size		
			0.25 x DACREFH	_	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size		
D315	DACRES	Resolution	_	_	DACREFH/24	_	CVRCON <cvrr> = 1</cvrr>		
			_	_	DACREFH/32	_	CVRCON <cvrr> = 0</cvrr>		
D316	DACACC	Absolute Accuracy ⁽²⁾	_	_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>		
			_	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>		

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

TABLE 33-16: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)					
Param. No.	Symbol	Characteristics	Min. Typical Max. Units Comments					
D321	CEFC	External Filter Capacitor Value	8 10 —			μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.	

^{2:} These parameters are characterized but not tested.

33.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX 28/44-pin XLP Family AC characteristics and timing parameters.

FIGURE 33-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

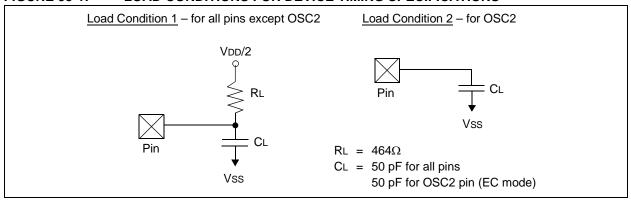


TABLE 33-17: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics	Min. Typical ⁽¹⁾ Max. Units Conditions						
DO50	Cosco	OSC2 pin	_	_	15	pF	In XT and HS modes when an external crystal is used to drive OSC1		
DO56	Сю	All I/O pins and OSC2	50 pF EC mode						
DO58	Св	SCLx, SDAx	_	_	400	pF	In I ² C mode		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 33-2: EXTERNAL CLOCK TIMING

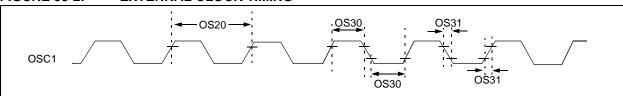


TABLE 33-18: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions		
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC		50	MHz	EC (Note 3)		
OS13		Oscillator Crystal Frequency	10	_	25	MHz	HS (Note 3)		
OS15			32	32.768	100	kHz	Sosc (Note 3)		
OS20	Tosc	Tosc = 1/Fosc = Tcy (Note 2)	_		_	_	See parameter OS10 for Fosc value		
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.375 x Tosc	_	_	ns	EC (Note 3)		
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	_	_	7.5	ns	EC (Note 3)		
OS40	Тоѕт	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	_	1024	_	Tosc	(Note 3)		
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	_	2	_	ms	(Note 3)		
OS42	Gм	External Oscillator Transconductance (Primary Oscillator only)	14	16	18	mA/V	VDD = 3.3V, TA = +25°C (Note 3)		

- **Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.
 - 2: Instruction cycle period (TcY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.
 - 3: This parameter is characterized, but not tested in manufacturing.

TABLE 33-19: PLL CLOCK TIMING SPECIFICATIONS

AC CHA	RACTERI	STICS	(unless of	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp			Industrial	
Param. No.	Symbol	Characteristi	cs ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
OS50	FIN	PLL Voltage Control Oscillator (VCO) Inp Frequency Range		4	ı	5		ECPLL, HSPLL, and FRCPLL modes
OS51	Fsys	On-Chip VCO Syste Frequency	m	60	_	120	MHz	_

-0.25

Note 1: These parameters are characterized, but not tested in manufacturing.

PLL Start-up Time (Lock Time)

(Period Jitter or Cumulative)

CLKO Stability⁽²⁾

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

2

+0.25

ms

%

period

Measured over 100 ms

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$Effective Jitter = \frac{D_{CLK}}{\sqrt{\frac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

TABLE 33-20: INTERNAL FRC ACCURACY

OS52

OS53

TLOCK

DCLK

AC CHA	RACTERISTICS	(unless	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp							
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions				
Internal	Internal FRC Accuracy @ 8.00 MHz ⁽¹⁾									
F20b	FRC -0.9 — +0.9 % —					_				

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE 33-21: INTERNAL LPRC ACCURACY

AC CHA	ARACTERISTICS	(unless	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp								
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions					
LPRC @	LPRC @ 31.25 kHz ⁽¹⁾										
F21	LPRC	-15	_	+15	%	_					

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 33-3: I/O TIMING CHARACTERISTICS

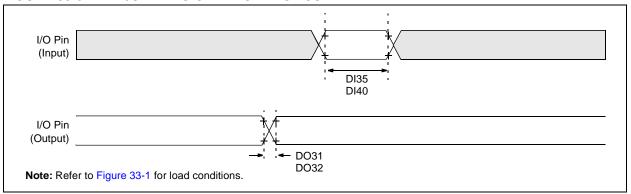


TABLE 33-22: I/O TIMING REQUIREMENTS

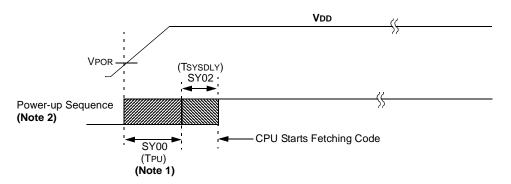
AC CHARACTERISTICS			(unless other	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Param. No. Symbol Characteristic			stics ⁽²⁾	Min.	Typical ⁽¹⁾	Max.	Units	Conditions		
DO31	TioR	Port Output Rise Tir	ne	_	5	15	ns	VDD < 2.0V		
				_	5	10	ns	VDD > 2.0V		
DO32	TioF	Port Output Fall Tim	ie	_	5	15	ns	VDD < 2.0V		
				_	5	10	ns	VDD > 2.0V		
DI35	TINP	INTx Pin High or Lo	w Time	20	_	_	ns	_		
DI40	TRBP	CNx High or Low Ti	me (input)	2	10	_	TSYSCLK	_		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

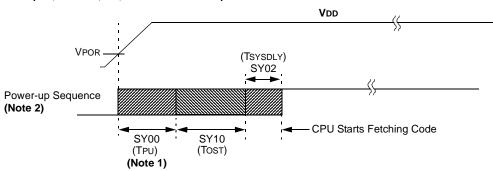
2: This parameter is characterized, but not tested in manufacturing.

FIGURE 33-4: POWER-ON RESET TIMING CHARACTERISTICS

Internal Voltage Regulator Enabled
Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)



Internal Voltage Regulator Enabled Clock Sources = (HS, HSPLL, XT, XTPLL and Sosc)



- Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDD < VDDMIN).
 - 2: Includes interval voltage regulator stabilization delay.

FIGURE 33-5: EXTERNAL RESET TIMING CHARACTERISTICS

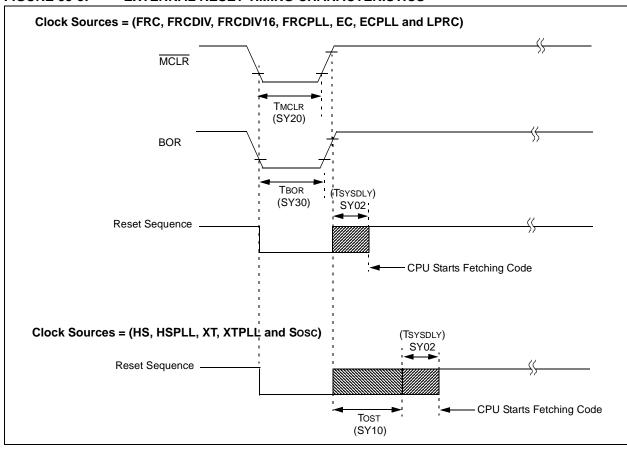


TABLE 33-23: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions	
SY00	Tpu	Power-up Period Internal Voltage Regulator Enabled		400	600	μS	_	
SY02	Tsysdly	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	_	1 μs + 8 SYSCLK cycles	_	_	_	
SY20	TMCLR	MCLR Pulse Width (low)	_	2	_	μS	_	
SY30	TBOR	BOR Pulse Width (low)	_	1	_	μS	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

FIGURE 33-6: TIMER1 - TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS

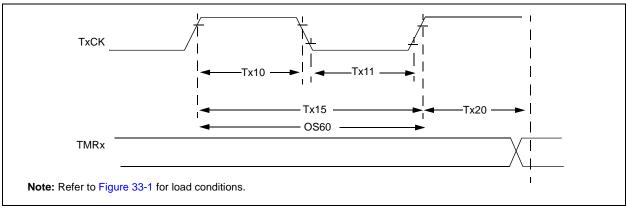


TABLE 33-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS ⁽¹⁾			(un	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)							
/10 011/1			Operating temperature -40°C ≤ TA				+85°C for Industrial				
				-40°C ≤ TA ≤ +105°C for V-temp					temp		
Param.	Symbol	Characteristics ⁽²⁾		Min.		Typical	Max.	Units	Conditions		

Param. No.	Symbol	Charac	teristics ⁽²⁾	Min.	Typical	Max.	Units	Conditions
TA10	ТтхН	TxCK Synchronous, High Time with prescaler		[(12.5 ns or 1 TPB)/N] + 25 ns			ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	_		ns	_
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns			ns	Must also meet parameter TA15
			Asynchronous, with prescaler	10	_		ns	_
TA15	ТтхР	TxCK Input Period	Synchronous, with prescaler	[(Greater of 25 ns or 2 TPB)/N] + 30 ns	_	_	ns	VDD > 2.7V
				[(Greater of 25 ns or 2 TPB)/N] + 50 ns	_	_	ns	VDD < 2.7V
			Asynchronous, with prescaler	20	_		ns	VDD > 2.7V (Note 3)
				50	_	_	ns	VDD < 2.7V (Note 3)
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting the TCS (T1CON<1>) bit)		32	_	50	kHz	_
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		_	_	1	Трв	_

Note 1: Timer1 is a Type A timer.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

TABLE 33-25: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp

Param. No.	Symbol	Characteristics ⁽¹⁾		acteristics ⁽¹⁾ Min.		Units	Condit	ions
TB10	ТтхН	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	_	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8,
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPB)/N] + 25 ns	_	ns	Must also meet parameter TB15	16, 32, 64, 256)
TB15	TTXP	TxCK Input	Synchronous, with prescaler	[(Greater of [(25 ns or 2 TPB)/N] + 30 ns	_	ns	VDD > 2.7V	
		Period		[(Greater of [(25 ns or 2 TPB)/N] + 50 ns	_	ns	VDD < 2.7V	
TB20	TCKEXTMRL	_	External TxCK to Timer Increment	_	1	Трв	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 33-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS

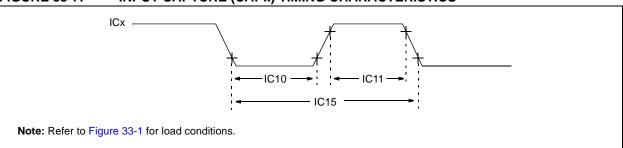


TABLE 33-26: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)						
AC CHARACTERISTICS	Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						

Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Con	ditions
IC10	TccL	ICx Input Low Time	[(12.5 ns or 1 TPB)/N] + 25 ns	_	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	[(12.5 ns or 1 TPB)/N] + 25 ns	_	ns	Must also meet parameter IC15.	
IC15	TccP	ICx Input Period	[(25 ns or 2 TPB)/N] + 50 ns	_	ns	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 33-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS

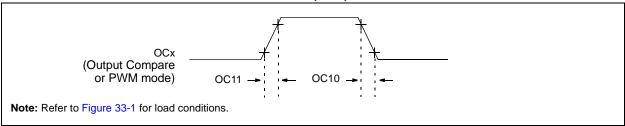


TABLE 33-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions		
OC10	TCCF	OCx Output Fall Time	_	_	_	ns	See parameter DO32		
OC11	TCCR	OCx Output Rise Time	ns See parameter						

- **Note 1:** These parameters are characterized, but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 33-9: OCx/PWM MODULE TIMING CHARACTERISTICS

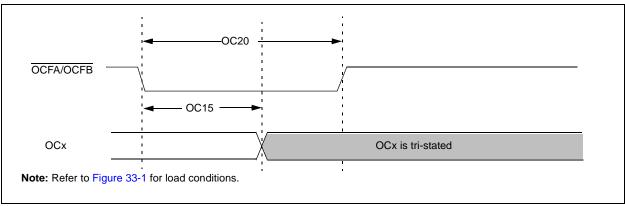


TABLE 33-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHAI	AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param No.	Symbol	Characteristics ⁽¹⁾	Min	Typical ⁽²⁾	Max	Units	Conditions		
OC15	TFD	Fault Input to PWM I/O Change	_	_	50	ns	_		
OC20	TFLT	Fault Input Pulse Width	50	_	_	ns	_		

- **Note 1:** These parameters are characterized, but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 33-10: SPIX MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

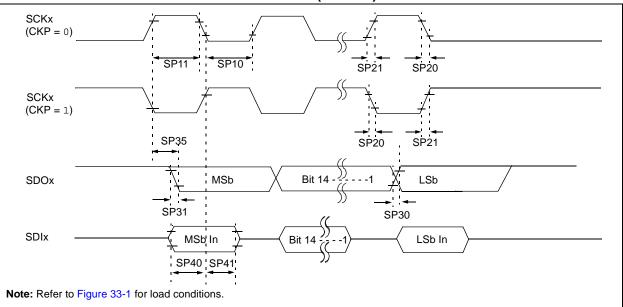


TABLE 33-29: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHA	ARACTERIST	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. ⁽²⁾ Max.			Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	_	_	ns	_
SP11	TscH	SCKx Output High Time (Note 3)	Tsck/2	_	_	ns	_
SP15	TscK	SPI Clock Speed	_	_	25	MHz	_
SP20	TscF	SCKx Output Fall Time (Note 4)	_	_	_	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)	_	_	_	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_	_	_	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	_	_	ns	See parameter DO31
SP35	TscH2DoV,	SDOx Data Output Valid after	_	_	15	ns	VDD > 2.7V
	TscL2doV	SCKx Edge	_	_	20	ns	VDD < 2.7V
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	_	_	ns	_
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	10	_	_	ns	_

- **Note 1:** These parameters are characterized, but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 33-11: SPIX MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

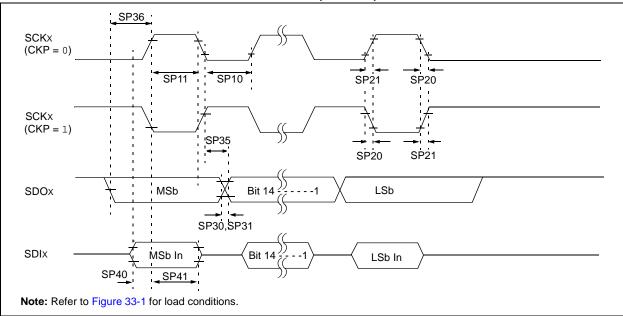


TABLE 33-30: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	_	_	ns	_	
SP11	TscH	SCKx Output High Time (Note 3)	Tsck/2	_	_	ns	_	
SP15	TscK	SPI Clock Speed	_	_	25	MHz	_	
SP20	TscF	SCKx Output Fall Time (Note 4)	_	_	_	ns	See parameter DO32	
SP21	TscR	SCKx Output Rise Time (Note 4)	_	_	_	ns	See parameter DO31	
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_	_	_	ns	See parameter DO32	
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	_	_	ns	See parameter DO31	
SP35	TSCH2DOV, TSCL2DOV	• 1	_	_	15	ns	VDD > 2.7V	
				_	20	ns	VDD < 2.7V	
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	15	_	_	ns	_	
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	15	_	-	ns	VDD > 2.7V	
			20	_	_	ns	VDD < 2.7V	
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	15	_	_	ns	VDD > 2.7V	
			20	_	_	ns	VDD < 2.7V	

- Note 1: These parameters are characterized, but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - **3:** The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 33-12: SPIX MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

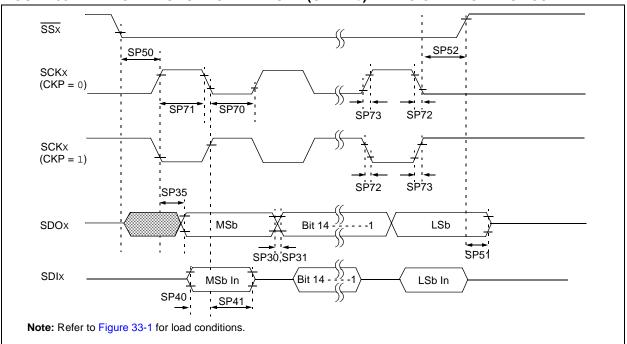


TABLE 33-31: SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature- 40° C \leq TA \leq +85 $^{\circ}$ C for Industrial -40° C \leq TA \leq +105 $^{\circ}$ C for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2	_	_	ns	_	
SP71	TscH	SCKx Input High Time (Note 3)	Tsck/2	_	_	ns	_	
SP72	TscF	SCKx Input Fall Time	_	_	1	ns	See parameter DO32	
SP73	TscR	SCKx Input Rise Time		_		ns	See parameter DO31	
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_	_		ns	See parameter DO32	
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	_		ns	See parameter DO31	
SP35	TscH2doV,	SDOx Data Output Valid after			15	ns	VDD > 2.7V	
	TscL2doV	SCKx Edge	_	_	20	ns	VDD < 2.7V	
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	10			ns	_	
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	10	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx Input	175	_	_	ns	_	
SP51	TssH2DoZ	SSx ↑ to SDOx Output High-Impedance (Note 3)	5	_	25	ns	_	
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	Tsck + 20	_	_	ns	_	

- Note 1: These parameters are characterized, but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 3: The minimum clock period for SCKx is 50 ns.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 33-13: SPIX MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

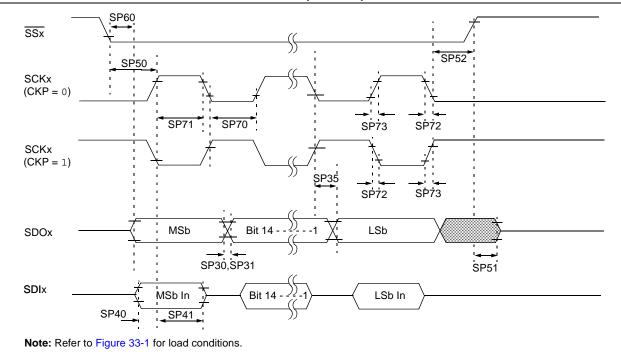


TABLE 33-32: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C \leq TA \leq +85°C for Industrial -40°C \leq TA \leq +105°C for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions	
SP70	TscL	SCKx Input Low Time (Note 3)	Tsck/2	_	_	ns	_	
SP71	TscH	SCKx Input High Time (Note 3)	Tsck/2	_	_	ns	_	
SP72	TscF	SCKx Input Fall Time	_	5	10	ns	_	
SP73	TscR	SCKx Input Rise Time	_	5	10	ns	_	
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_	_	_	ns	See parameter DO32	
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	_	_	ns	See parameter DO31	
SP35	TSCH2DOV, TSCL2DOV	·	_	_	20	ns	VDD > 2.7V	
			_	_	30	ns	VDD < 2.7V	
SP40	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	_	_	ns	_	
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	10	_	_	ns	_	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↓ or SCKx ↑ Input	175	_	_	ns	_	

- Note 1: These parameters are characterized, but not tested in manufacturing.
 - 2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 3: The minimum clock period for SCKx is 50 ns.
 - 4: Assumes 50 pF load on all SPIx pins.

TABLE 33-32: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature -40°C \leq TA \leq +85°C for Industrial -40°C \leq TA \leq +105°C for V-temp					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typical ⁽²⁾ Max. Units Conditions						
SP51	TssH2DoZ	SSx ↑ to SDOx Output High-Impedance (Note 4)	5	_	25	ns	_		
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	Тscк + 20	_	_	ns	_		
SP60	TssL2DoV	SDOx Data Output Valid after SSx Edge	_	_	25	ns	_		

- Note 1: These parameters are characterized, but not tested in manufacturing.
 - **2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
 - 3: The minimum clock period for SCKx is 50 ns.
 - 4: Assumes 50 pF load on all SPIx pins.

FIGURE 33-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

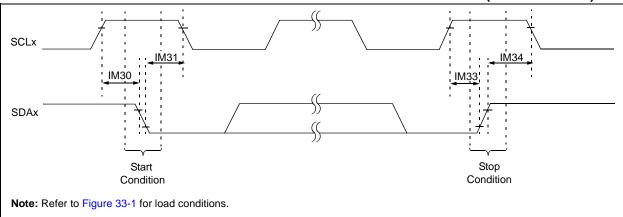


FIGURE 33-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

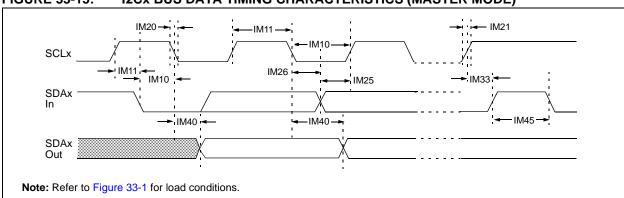


TABLE 33-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHA	RACTER	ISTICS		Standard Operation (unless otherwise Operating temperation)	e stated) ture -40	O°C ≤ TA ≤	5V to 3.6V £+85°C for Industrial £+105°C for V-temp
Param. No.	Symbol	Charact	eristics	Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)	_	μS	_
			400 kHz mode	Трв * (BRG + 2)	_	μS	_
			1 MHz mode (Note 2)	Трв * (BRG + 2)	_	μS	_
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	_	μS	_
			400 kHz mode	Трв * (BRG + 2)	_	μS	_
			1 MHz mode (Note 2)	Трв * (BRG + 2)	_	μS	_
IM20	TF:SCL		100 kHz mode	_	300	ns	CB is specified to be
l		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF
			1 MHz mode (Note 2)	_	100	ns	
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	_	1000	ns	CB is specified to be
		Rise Time	400 kHz mode	20 + 0.1 CB	300	ns	from 10 to 400 pF
			1 MHz mode (Note 2)	_	300	ns	
IM25	TSU:DAT	Data Input	100 kHz mode	250	_	ns	_
		Setup Time	400 kHz mode	100	_	ns	
			1 MHz mode (Note 2)	100		ns	
IM26	THD:DAT	Data Input	100 kHz mode	0	_	μS	_
		Hold Time	400 kHz mode	0	0.9	μS	
			1 MHz mode (Note 2)	0	0.3	μS	
IM30	TSU:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)	_	μS	Only relevant for
		Setup Time	400 kHz mode	Трв * (BRG + 2)	_	μS	Repeated Start condition
			1 MHz mode (Note 2)	Трв * (BRG + 2)	_	μS	Condition
IM31	THD:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)	_	μS	After this period, the
		Hold Time	400 kHz mode	Трв * (BRG + 2)	_	μS	first clock pulse is
			1 MHz mode (Note 2)	Трв * (BRG + 2)	_	μS	generated
IM33	Tsu:sto	Stop Condition	100 kHz mode	Трв * (BRG + 2)	_	μS	
		Setup Time	400 kHz mode	Трв * (BRG + 2)	_	μS]
			1 MHz mode (Note 2)	Трв * (BRG + 2)	_	μS	
IM34	THD:STO	Stop Condition	100 kHz mode	TPB * (BRG + 2)	_	ns	_
		Hold Time	400 kHz mode	TPB * (BRG + 2)	_	ns	
			1 MHz mode (Note 2)	Трв * (BRG + 2)		ns	

Note 1: BRG is the value of the I²C Baud Rate Generator.

^{2:} Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

^{3:} The typical value for this parameter is 104 ns.

TABLE 33-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHA	RACTER	ISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp				
Param. No. Symbol Characteristics Min. ⁽¹⁾ Max. Uni							Conditions	
IM40	TAA:SCL	Output Valid	100 kHz mode	_	3500	ns	_	
		from Clock	400 kHz mode	_	1000	ns	_	
			1 MHz mode (Note 2)	_	350	ns	_	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μS	The amount of time the	
			400 kHz mode	1.3	_	μS	bus must be free	
			1 MHz mode (Note 2)	0.5	_	μS	before a new transmission can start	
IM50	Св	Bus Capacitive L	oading	_	400	pF	_	
IM51	TPGD	Pulse Gobbler D	elay	52	312	ns	See Note 3	

Note 1: BRG is the value of the I²C Baud Rate Generator.

^{2:} Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

^{3:} The typical value for this parameter is 104 ns.

FIGURE 33-16: 12Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

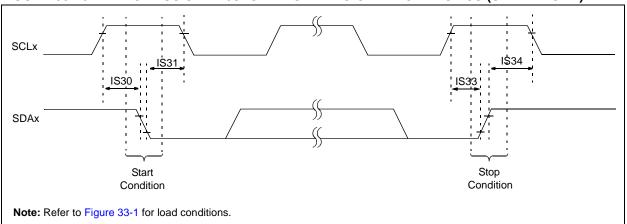


FIGURE 33-17: **12Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

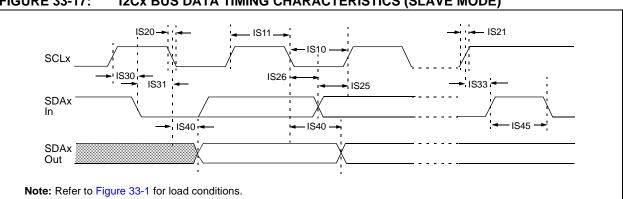


TABLE 33-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHA	RACTERIS	STICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Charact	eristics	Min.	Max.	Units	Conditions		
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	_	μS	PBCLK must operate at a minimum of 800 kHz		
			400 kHz mode	1.3	_	μS	PBCLK must operate at a minimum of 3.2 MHz		
			1 MHz mode (Note 1)	0.5	_	μS	_		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	_	μS	PBCLK must operate at a minimum of 800 kHz		
			400 kHz mode	0.6	_	μS	PBCLK must operate at a minimum of 3.2 MHz		
			1 MHz mode (Note 1)	0.5	_	μS	_		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode		300	ns	CB is specified to be from		
		Fall Time	400 kHz mode	20 + 0.1 CB	300	ns	10 to 400 pF		
			1 MHz mode (Note 1)	_	100	ns			
IS21	TR:SCL	SDAx and SCLx	100 kHz mode		1000	ns	CB is specified to be from		
		Rise Time	400 kHz mode	20 + 0.1 CB	300	ns	10 to 400 pF		
			1 MHz mode (Note 1)	_	300	ns			
IS25	TSU:DAT	Data Input	100 kHz mode	250	_	ns	_		
		Setup Time	400 kHz mode	100		ns			
			1 MHz mode (Note 1)	100	_	ns			
IS26	THD:DAT	Data Input	100 kHz mode	0		ns	_		
		Hold Time	400 kHz mode	0	0.9	μS			
			1 MHz mode (Note 1)	0	0.3	μS			
IS30	Tsu:sta	Start Condition	100 kHz mode	4700		ns	Only relevant for Repeated		
		Setup Time	400 kHz mode	600		ns	Start condition		
			1 MHz mode (Note 1)	250	_	ns			
IS31	THD:STA	Start Condition	100 kHz mode	4000	_	ns	After this period, the first		
		Hold Time	400 kHz mode	600		ns	clock pulse is generated		
			1 MHz mode (Note 1)	250	_	ns			
IS33	Tsu:sto	Stop Condition	100 kHz mode	4000	_	ns			
		Setup Time	400 kHz mode	600	_	ns			
			1 MHz mode (Note 1)	600	_	ns			

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 33-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHA	RACTERIS	STICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Charact	eristics	Min.	Max.	Units	Conditions	
IS34	THD:STO	Stop Condition	100 kHz mode	4000	_	ns	_	
		Hold Time	400 kHz mode	600	_	ns		
			1 MHz mode (Note 1)	250		ns		
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	_	
			400 kHz mode	0	1000	ns		
			1 MHz mode (Note 1)	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	_	μS	The amount of time the bus	
			400 kHz mode	1.3	_	μS	must be free before a new	
			1 MHz mode (Note 1)	0.5	_	μS	transmission can start	
IS50	Св	Bus Capacitive Lo	ading	_	400	pF	_	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

TABLE 33-35: ADC MODULE SPECIFICATIONS

	AC CHAR	RACTERISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions		
Device	Supply								
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5		Lesser of VDD + 0.3 or 3.6	V	_		
AD02	AVss	Module Vss Supply	Vss		AVDD	V	(Note 1)		
Referen	ce Inputs								
AD05 AD05a	VREFH	Reference Voltage High	AVss + 2.0 2.5	1 1	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)		
AD06	VREFL	Reference Voltage Low	AVss		VREFH - 2.0	V	(Note 1)		
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	1	AVDD	V	(Note 3)		
AD08 AD08a	IREF	Current Drain	_	250 —	400 3	μA μA	ADC operating ADC off		
Analog	Input				•				
AD12	VINH-VINL	Full-Scale Input Span	VREFL	_	VREFH	V	_		
AD13	VINL	Absolute VINL Input Voltage	AVss - 0.3	_	AVDD/2	V	_		
AD14	VIN	Absolute Input Voltage	AVss - 0.3	_	AVDD + 0.3	V	_		
AD15	_	Leakage Current	_	±0.001	±0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = $3.3V$ Source Impedance = $10 \text{ k}\Omega$		
AD17	RIN	Recommended Impedance of Analog Voltage Source		l	5k	Ω	(Note 1)		
ADC Ac	curacy – N	leasurements with Exte	rnal VREF+/V	REF-					
AD20c	Nr	Resolution		10 data bit	s	bits	_		
AD21c	INL	Integral Non-linearity	> -1		< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V		
AD22c	DNL	Differential Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)		
AD23c	GERR	Gain Error	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V		
AD24c	EOFF	Offset Error	> -1	_	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V		
AD25c	_	Monotonicity	_	_	_	_	Guaranteed		

- Note 1: These parameters are not characterized or tested in manufacturing.
 - 2: With no missing codes.
 - **3:** These parameters are characterized, but not tested in manufacturing.
 - **4:** Characterized with a 1 kHz sine wave.
 - **5:** The ADC module is functional at VBORMIN < VDD < 2.0V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 33-35: ADC MODULE SPECIFICATIONS (CONTINUED)

	AC CHAR	RACTERISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp								
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions				
ADC Accuracy – Measurements with Internal VREF+/VREF-											
AD20d	Nr	Resolution		10 data bits	3	bits	(Note 3)				
AD21d	INL	Integral Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Note 3)				
AD22d	DNL	Differential Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Notes 2,3)				
AD23d	GERR	Gain Error	> -4	_	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Note 3)				
AD24d	EOFF	Offset Error	> -2	_	< 2	LSb	VINL = AVSS = 0V, AVDD = 2.0V to 3.6V (Note 3)				
AD25d	_	Monotonicity	_	_	_	_	Guaranteed				
Dynami	c Performa	ance									
AD32b	SINAD	Signal to Noise and Distortion	55	58.5		dB	(Notes 3,4)				
AD34b	ENOB	Effective Number of bits	9.0	9.5		bits	(Notes 3,4)				

Note 1: These parameters are not characterized or tested in manufacturing.

- 2: With no missing codes.
- 3: These parameters are characterized, but not tested in manufacturing.
- 4: Characterized with a 1 kHz sine wave.
- **5:** The ADC module is functional at VBORMIN < VDD < 2.0V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 33-36: 10-BIT CONVERSION RATE PARAMETERS

AC CHARA	CTERISTIC	S ⁽²⁾	(unless o	therwise st	Conditions: 2.5V to 3.6V tated) e $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp
ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	VDD	ADC Channels Configuration
1 Msps to 400 ksps ⁽¹⁾	65 ns	132 ns	500Ω	3.0V to 3.6V	ANX CHX ADC
Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.0V to 3.6V	ANX SHA ADC ANX OF VREF-

- **Note 1:** External VREF+ pins must be used for correct operation.
 - 2: These parameters are characterized, but not tested in manufacturing.
 - **3:** The ADC module is functional at VBORMIN < VDD < 2.0V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 33-37: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHA	ARACTER	ISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions	
Clock P	arameter	s						
AD50	TAD	ADC Clock Period ⁽²⁾	65	_	_	ns	See Table 33-36	
Convers	sion Rate							
AD55	TCONV	Conversion Time	_	12 TAD	_	_	_	
AD56	FCNV	Throughput Rate	_	_	1000	ksps	AVDD = 3.0V to 3.6V	
		(Sampling Speed)	_		400	ksps	AVDD = 2.0V to 3.6V	
AD57	TSAMP	Sample Time	1 TAD	_	_	_	TSAMP must be ≥ 132 ns	
Timing	Paramete	rs						
AD60	TPCS	Conversion Start from Sample Trigger ⁽³⁾	_	1.0 TAD		_	Auto-Convert Trigger (SSRC<2:0> = 111) not selected	
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD		1.5 TAD	_	_	
AD62	TCSS	Conversion Completion to Sample Start $(ASAM = 1)^{(3)}$		0.5 TAD	_	_	_	
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ⁽³⁾	_		2	μS	_	

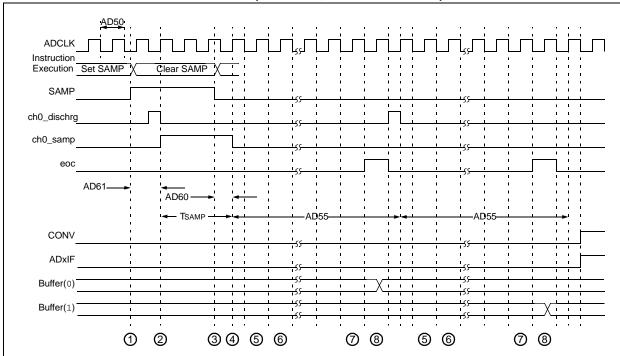
Note 1: These parameters are characterized, but not tested in manufacturing.

^{2:} Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

^{3:} Characterized by design but not tested.

^{4:} The ADC module is functional at VBORMIN < VDD < 2.0V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 33-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)



- 1 Software sets ADxCON. SAMP to start sampling.
- ② Sampling starts after discharge period. TSAMP is described in Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104) in the "PIC32 Family Reference Manual".
- 3 Software clears ADxCON. SAMP to start conversion.
- (4) Sampling ends, conversion sequence starts.
- (5) Convert bit 9.
- 6 Convert bit 8.
- (7) Convert bit 0.
- (8) One TAD for end of conversion.

FIGURE 33-19: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)

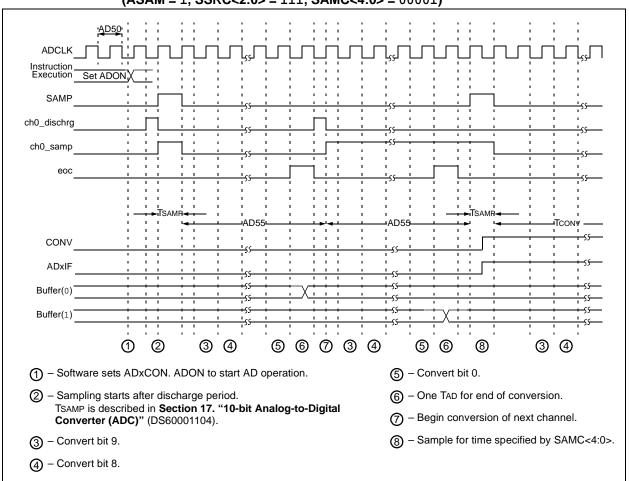


FIGURE 33-20: PARALLEL SLAVE PORT TIMING

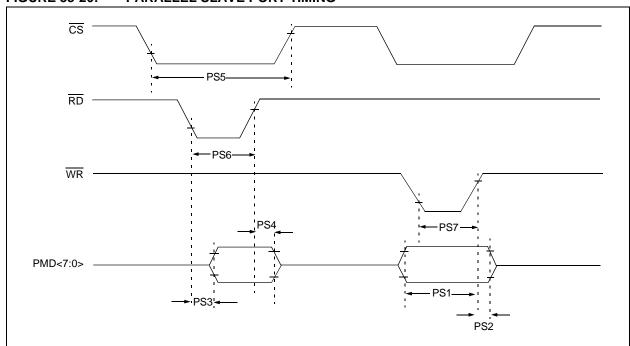


TABLE 33-38: PARALLEL SLAVE PORT REQUIREMENTS

AC CH	ARACTE	RISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Para m.No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions						
PS1	TdtV2wr H	Data In Valid before WR or CS Inactive (setup time)	20			ns	_		
PS2	TwrH2dt I	WR or CS Inactive to Data-In Invalid (hold time)	40			ns			
PS3	TrdL2dt V	RD and CS Active to Data-Out Valid	_	l	60	ns	1		
PS4	TrdH2dtl	RD Active or CS Inactive to Data-Out Invalid	0		10	ns			
PS5	Tcs	CS Active Time	TpB + 40			ns			
PS6	Twr	WR Active Time	TPB + 25 — ns —						
PS7	TRD	RD Active Time	TpB + 25	_	_	ns			

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 33-21: PARALLEL MASTER PORT READ TIMING DIAGRAM

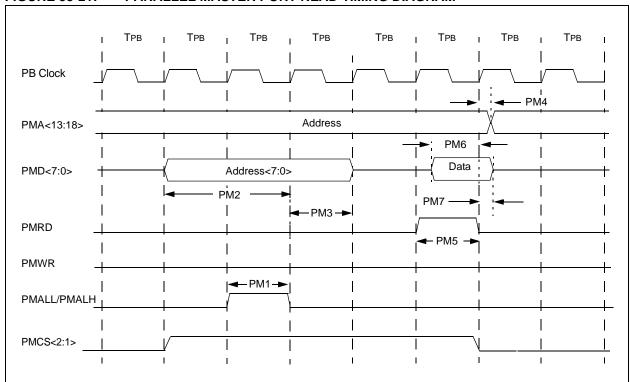


TABLE 33-39: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHA	ARACTER	ISTICS	Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions						
PM1	TLAT	PMALL/PMALH Pulse Width	_	1 Трв		_	_		
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	_	2 Трв	_	_	_		
РМ3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	_	1 Трв	_	_	_		
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	_	_	ns	_		
PM5	TRD	PMRD Pulse Width	_	1 Трв		_	_		
PM6	Tosu	PMRD or PMENB Active to Data In Valid (data setup time)	15	_	_	ns	_		
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	_	80	_	ns	_		

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 33-22: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

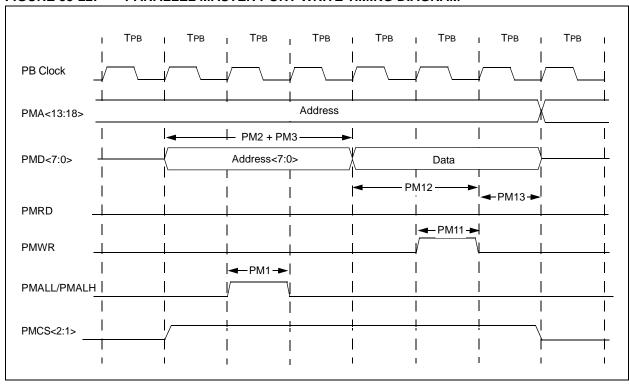


TABLE 33-40: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated)					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min. Typ. Max. Units Conditions					
PM11	Twr	PMWR Pulse Width	_	1 Трв	_	_	_	
PM12	Tovsu	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	_	2 ТРВ	_	_	_	
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	_	1 Трв	_	_	_	

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 33-41: OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0		3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
USB315	VILUSB	Input Low Voltage for USB Buffer	_		0.8	V	_
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	_	_	V	_
USB318	VDIFS	Differential Input Sensitivity	_	_	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	_	2.5	V	_
USB320	Zout	Driver Output Impedance	28.0	_	44.0	Ω	_
USB321	Vol	Voltage Output Low	0.0	_	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	Voн	Voltage Output High	2.8	_	3.6	V	1.425 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 33-42: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for V-temp					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
CTMU CUR	CTMU CURRENT SOURCE						
CTMUI1	IOUT1	Base Range ⁽¹⁾	_	0.55	_	μA	CTMUCON<9:8> = 01
CTMUI2	IOUT2	10x Range ⁽¹⁾	_	5.5	_	μA	CTMUCON<9:8> = 10
CTMUI3	Іоит3	100x Range ⁽¹⁾	_	55	_	μA	CTMUCON<9:8> = 11
CTMUI4	IOUT4	1000x Range ⁽¹⁾	_	550	_	μΑ	CTMUCON<9:8> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage ^(1,2)	_	0.598	_	V	TA = +25°C, CTMUCON<9:8> = 01
			_	0.658	_	V	TA = $+25^{\circ}$ C, CTMUCON<9:8> = 10
			_	0.721	_	V	TA = +25°C, CTMUCON<9:8> = 11
CTMUFV2	VFVR	Temperature Diode Rate of	_	-1.92	_	mV/ºC	CTMUCON<9:8> = 01
		Change ^(1,2)	_	-1.74	_	mV/ºC	CTMUCON<9:8> = 10
				-1.56		mV/ºC	CTMUCON<9:8> = 11

- **Note 1:** Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).
 - 2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:
 - VREF+ = AVDD = 3.3V
 - ADC module configured for conversion speed of 500 ksps
 - All PMD bits are cleared (PMDx = 0)
 - Executing a while(1) statement
 - Device operating from the FRC with no PLL
 - **3:** The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 33-23: EJTAG TIMING CHARACTERISTICS

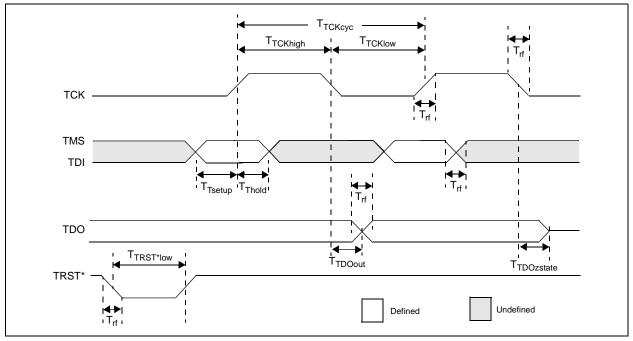


TABLE 33-43: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for I $-40^{\circ}\text{C} \le \text{TA} \le +105^{\circ}\text{C}$ for			
Param. No.	Symbol	Description ⁽¹⁾	Min.	Max.	Units	Conditions
EJ1	Ттсксүс	TCK Cycle Time	25	_	ns	_
EJ2	Ттскнідн	TCK High Time	10	_	ns	_
EJ3	TTCKLOW	TCK Low Time	10	_	ns	_
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	_	ns	_
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	_	ns	_
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	_	5	ns	_
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	_	5	ns	_
EJ8	TTRSTLOW	TRST Low Time	25	_	ns	_
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	_	_	ns	_

Note 1: These parameters are characterized, but not tested in manufacturing.

34.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 34-1: I/O OUTPUT VOLTAGE HIGH (VOH)

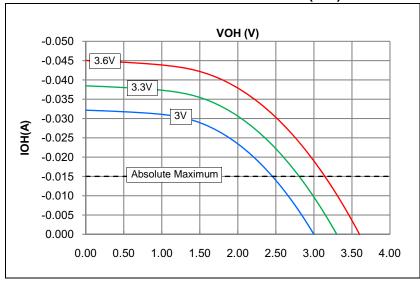
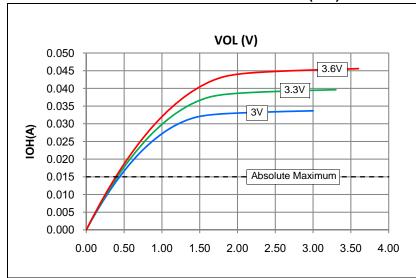
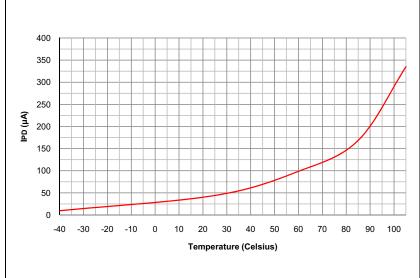


FIGURE 34-2: I/O OUTPUT VOLTAGE LOW (Vol)









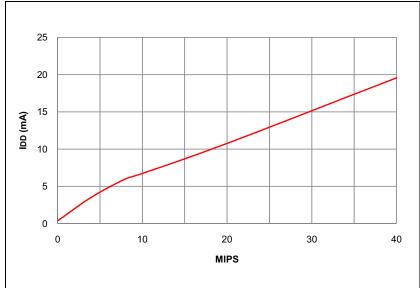
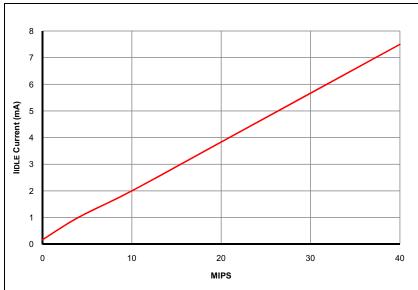
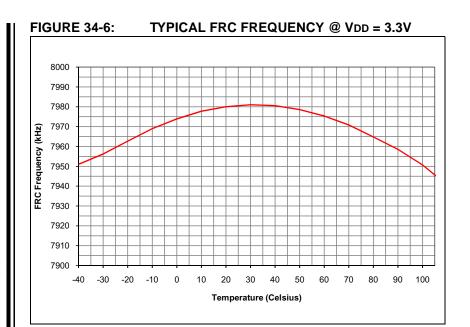
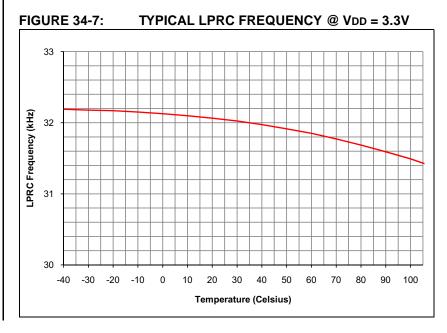
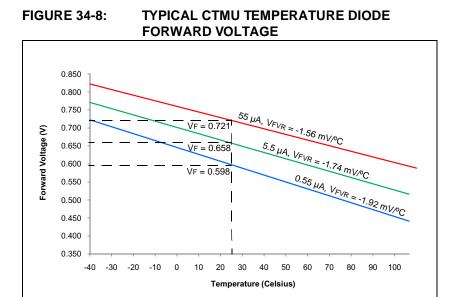


FIGURE 34-5: TYPICAL IIDLE CURRENT @ VDD = 3.3V









NOTES:

35.0 PACKAGING INFORMATION

35.1 Package Marking Information

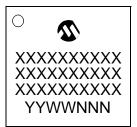
28-Lead SOIC



28-Lead QFN



44-Lead QFN



44-Lead TQFP



Example



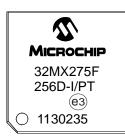
Example



Example



Example



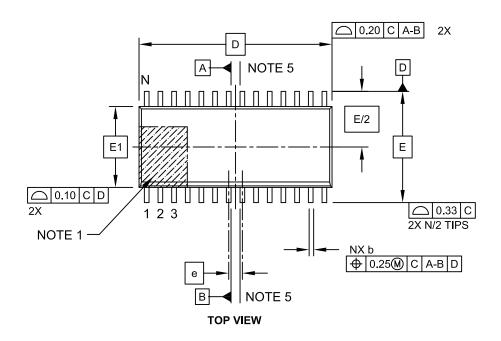
Legend: XX...X Customer-specific information Year code (last digit of calendar year) Υ YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) (e3) This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package. Note:

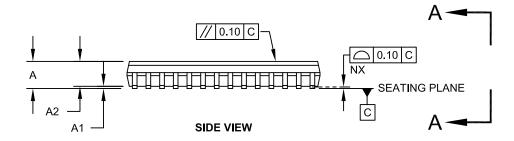
35.2 Package Details

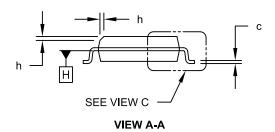
This section provides the technical details of the packages.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



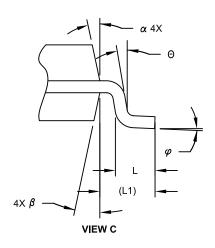


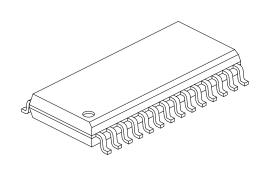


Microchip Technology Drawing C04-052C Sheet 1 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS				
Dimension Lim		MIN	NOM	MAX	
Number of Pins	N		28		
Pitch	е		1.27 BSC		
Overall Height	Α	-	-	2.65	
Molded Package Thickness	A2	2.05	-	-	
Standoff §	A1	0.10	-	0.30	
Overall Width	E	10.30 BSC			
Molded Package Width	E1	7.50 BSC			
Overall Length	D	17.90 BSC			
Chamfer (Optional)	h	0.25	-	0.75	
Foot Length	L	0.40	-	1.27	
Footprint	L1		1.40 REF		
Lead Angle	Θ	0°	-	-	
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.18	-	0.33	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M

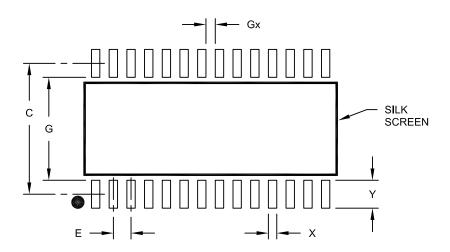
BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	II LLIMETER	S	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Υ			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

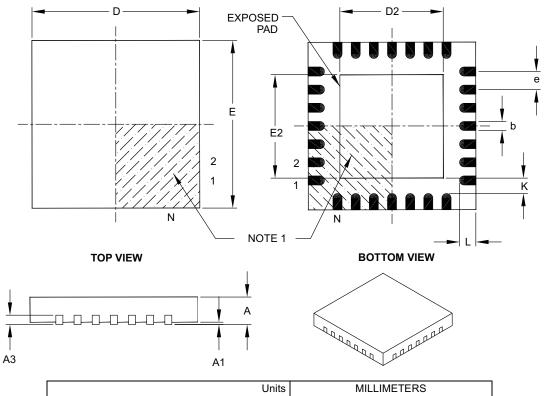
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3
Dimer	nsion Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	е		0.65 BSC	
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

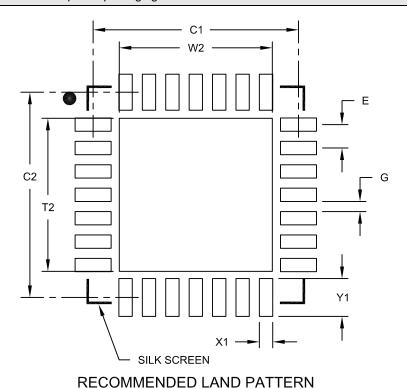
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units			MILLIM	ETERS
Dimension Limit		MIN	NOM	MAX
Contact Pitch	E 0.65 BSC			
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

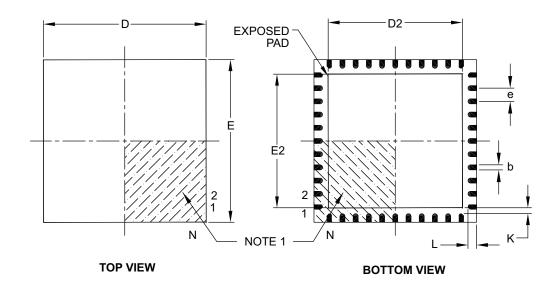
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

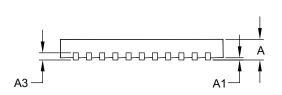
Microchip Technology Drawing No. C04-2105A

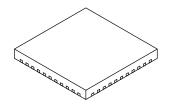
^{1.} Dimensioning and tolerancing per ASME Y14.5M

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Units		MILLIMETERS	3
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		44	
Pitch	е		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

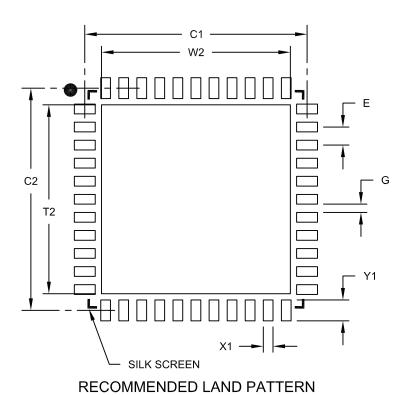
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

te: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



MILLIMETERS Units **Dimension Limits** MIN MOM MAX Contact Pitch Ε 0.65 BSC Optional Center Pad Width W2 6.80 Optional Center Pad Length T2 6.80 Contact Pad Spacing C1 8.00 Contact Pad Spacing C2 8.00 Contact Pad Width (X44) X1 0.35 Contact Pad Length (X44) <u>Y1</u> 0.80 0.25 Distance Between Pads G

Notes:

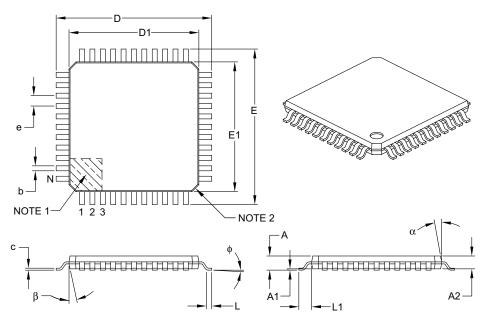
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			3
	Dimension Limits	MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	е	0.80 BSC		
Overall Height	A	_	_	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	_	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ф	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D		12.00 BSC	
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	С	0.09	_	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

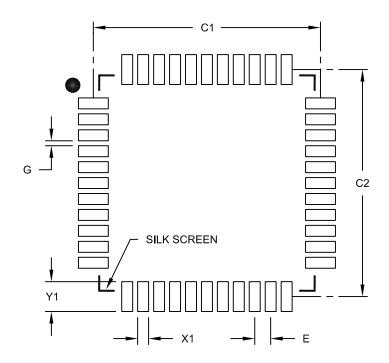
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Chamfers at corners are optional; size may vary.
- 3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units			S
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	Е	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

APPENDIX A: REVISION HISTORY

Revision A (May 2016)

This is the initial released version of this document.

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NOTES:

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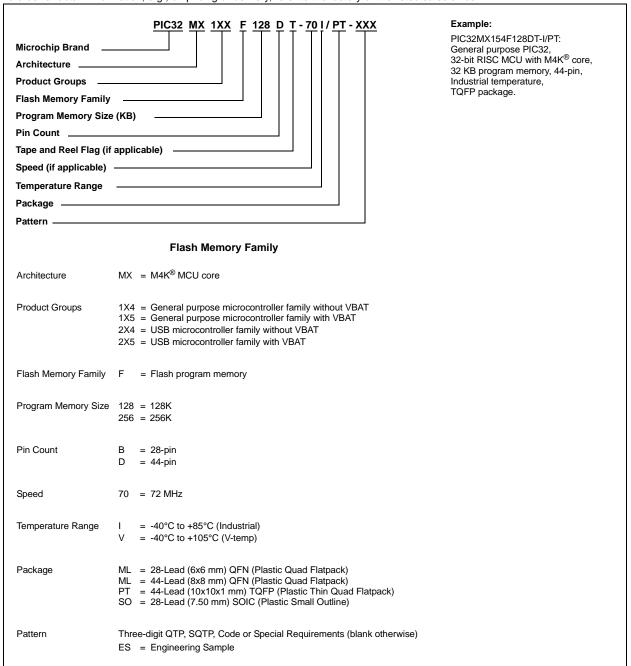
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