



LC75813E, 75813T

1/3, 1/4 Duty General-Purpose LCD Driver



An ON Semiconductor Company

Overview

The LC75813E and LC75813T are 1/3 duty and 1/4 duty general-purpose LCD drivers that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75813E and LC75813T can drive an LCD with up to 344 segments directly. The LC75813E and LC75813T can also control up to 8 general-purpose output ports. Since the LC75813E and LC75813T use separate power supply systems for the LCD drive block and the logic block, the LCD driver block power-supply voltage can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.

Features

- Switching between 1/3 duty and 1/4 duty drive techniques under serial data control.
- Switching between 1/2 bias and 1/3 bias drive techniques under serial data control.
- Up to 261 segments for 1/3 duty drive and 344 segments for 1/4 duty drive can be displayed.
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function.
- Serial data control of switching between the segment output port and the general-purpose output port functions.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD max}	V _{DD}	-0.3 to +7.0	V
	V _{LCD max}	V _{LCD}	-0.3 to +7.0	
Input voltage	V _{IN1}	CE, CL, DI, INH	-0.3 to +7.0	V
	V _{IN2}	OSC	-0.3 to V _{DD} + 0.3	
	V _{IN3}	V _{LCD1} , V _{LCD2}	-0.3 to V _{LCD} + 0.3	
Output voltage	V _{OUT1}	OSC	-0.3 to V _{DD} + 0.3	V
	V _{OUT2}	S1 to S87, COM1 to COM4, P1 to P8	-0.3 to V _{LCD} + 0.3	
Output current	I _{OUT1}	S1 to S87	300	μA
	I _{OUT2}	COM1 to COM4	3	mA
	I _{OUT3}	P1 to P8	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	T _{opr}		-40 to +85	°C
Storage temperature	T _{stg}		-55 to +125	°C

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- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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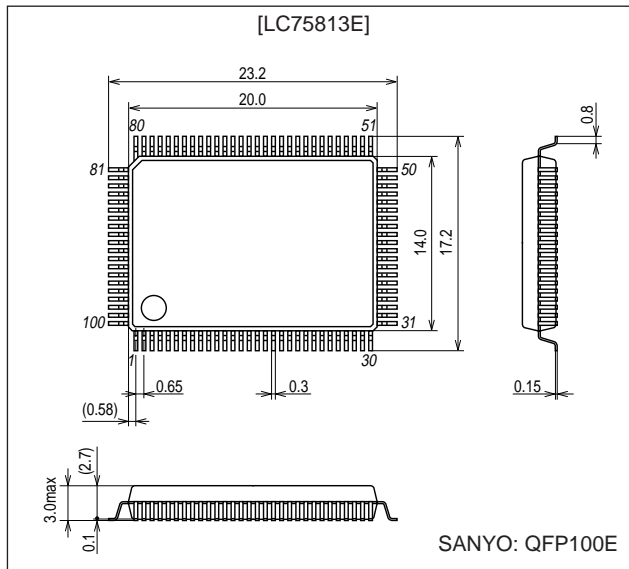
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- Serial data control of frame frequency for common and segment output waveforms.
- High generality, since display data is displayed directly without decoder intervention.
- Independent V_{LCD} for the LCD driver block (V_{LCD} can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.)
- The \overline{INH} pin can force the display to the off state.
- RC oscillator circuit

Package Dimensions

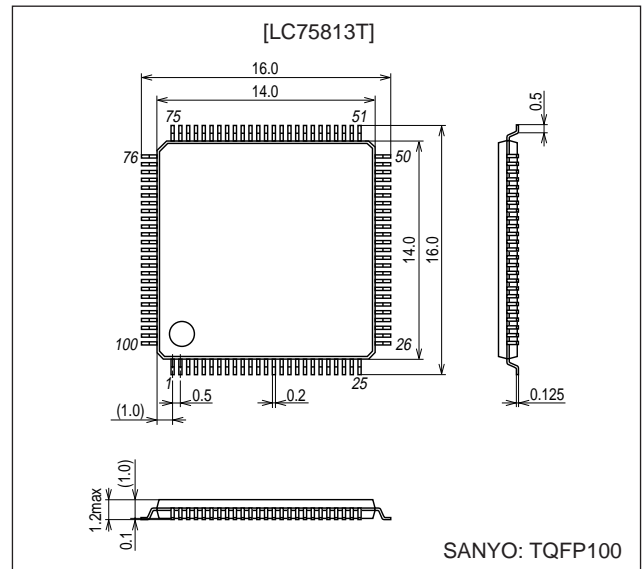
unit: mm

3151A-QFP100E



unit: mm

3274-TQFP100 (14×14)



Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}	2.7		6.0	
Input voltage	V_{LCD1}	V_{LCD1}		$2/3 V_{LCD}$	V_{LCD}	V
	V_{LCD2}	V_{LCD2}		$1/3 V_{LCD}$	V_{LCD}	
Input high level voltage	V_{IH}	CE, CL, DI, \overline{INH}	$0.8 V_{DD}$		6.0	V
Input low level voltage	V_{IL}	CE, CL, DI, \overline{INH}	0		$0.2 V_{DD}$	V
Recommended external resistance	R_{OSC}	OSC		39		k Ω
Recommended external capacitance	C_{OSC}	OSC		1000		pF
Guaranteed oscillation range	f_{OSC}	OSC	19	38	76	kHz
Data setup time	t_{ds}	CL, DI: Figure 2	160			ns
Data hold time	t_{dh}	CL, DI: Figure 2	160			ns
CE wait time	t_{cp}	CE, CL: Figure 2	160			ns
CE setup time	t_{cs}	CE, CL: Figure 2	160			ns
CE hold time	t_{ch}	CE, CL: Figure 2	160			ns
High level clock pulse width	$t_{\phi H}$	CL: Figure 2	160			ns
Low level clock pulse width	$t_{\phi L}$	CL: Figure 2	160			ns
Rise time	t_r	CE, CL, DI: Figure 2		160		ns
Fall time	t_f	CE, CL, DI: Figure 2		160		ns
\overline{INH} switching time	t_c	\overline{INH} , CE: Figure 3	10			μs

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Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{\text{INH}}$		$0.1 V_{DD}$		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{\text{INH}}$: $V_I = 6.0 \text{ V}$			5.0	μA
Input low level current	I_{IL}	CE, CL, DI, $\overline{\text{INH}}$: $V_I = 0 \text{ V}$	-5.0			μA
Output high level voltage	V_{OH1}	S1 to S87: $I_O = -20 \mu\text{A}$	$V_{LCD} - 0.9$			V
	V_{OH2}	COM1 to COM4: $I_O = -100 \mu\text{A}$	$V_{LCD} - 0.9$			
	V_{OH3}	P1 to P8: $I_O = -1 \text{ mA}$	$V_{LCD} - 0.9$			
Output low level voltage	V_{OL1}	S1 to S87: $I_O = 20 \mu\text{A}$			0.9	V
	V_{OL2}	COM1 to COM4: $I_O = 100 \mu\text{A}$			0.9	
	V_{OL3}	P1 to P8: $I_O = 1 \text{ mA}$			0.9	
Output middle level voltage*1	V_{MID1}	COM1 to COM4: 1/2 bias, $I_O = \pm 100 \mu\text{A}$	$1/2 V_{LCD} - 0.9$		$1/2 V_{LCD} + 0.9$	V
	V_{MID2}	S1 to S87: 1/3 bias, $I_O = \pm 20 \mu\text{A}$	$2/3 V_{LCD} - 0.9$		$2/3 V_{LCD} + 0.9$	
	V_{MID3}	S1 to S87: 1/3 bias, $I_O = \pm 20 \mu\text{A}$	$1/3 V_{LCD} - 0.9$		$1/3 V_{LCD} + 0.9$	
	V_{MID4}	COM1 to COM4: 1/3 bias, $I_O = \pm 100 \mu\text{A}$	$2/3 V_{LCD} - 0.9$		$2/3 V_{LCD} + 0.9$	
	V_{MID5}	COM1 to COM4: 1/3 bias, $I_O = \pm 100 \mu\text{A}$	$1/3 V_{LCD} - 0.9$		$1/3 V_{LCD} + 0.9$	
Oscillator frequency	f_{OSC}	OSC: $R_{OSC} = 39 \text{ k}\Omega$, $C_{OSC} = 1000 \text{ pF}$	30.4	38	45.6	kHz
Current drain	I_{DD1}	V_{DD} : Power-saving mode			5	μA
	I_{DD2}	V_{DD} : $V_{DD} = 6.0 \text{ V}$, output open, $f_{OSC} = 38 \text{ kHz}$		250	500	
	I_{LCD1}	V_{LCD} : Power-saving mode			5	
	I_{LCD2}	V_{LCD} : $V_{LCD} = 6.0 \text{ V}$, output open, 1/2 bias, $f_{OSC} = 38 \text{ kHz}$		200	400	
	I_{LCD3}	V_{LCD} : $V_{LCD} = 6.0 \text{ V}$, output open, 1/3 bias, $f_{OSC} = 38 \text{ kHz}$		120	240	

Note: *1 Excluding the bias voltage generation divider resistors built in the V_{LCD1} and V_{LCD2} . (See Figure 1.)

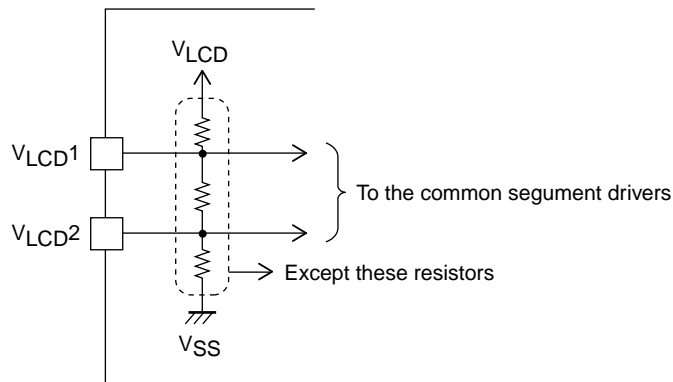
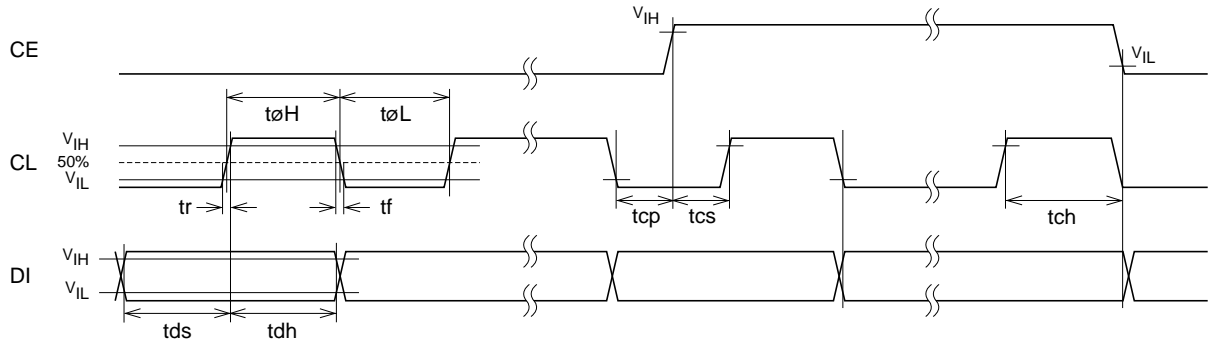


Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

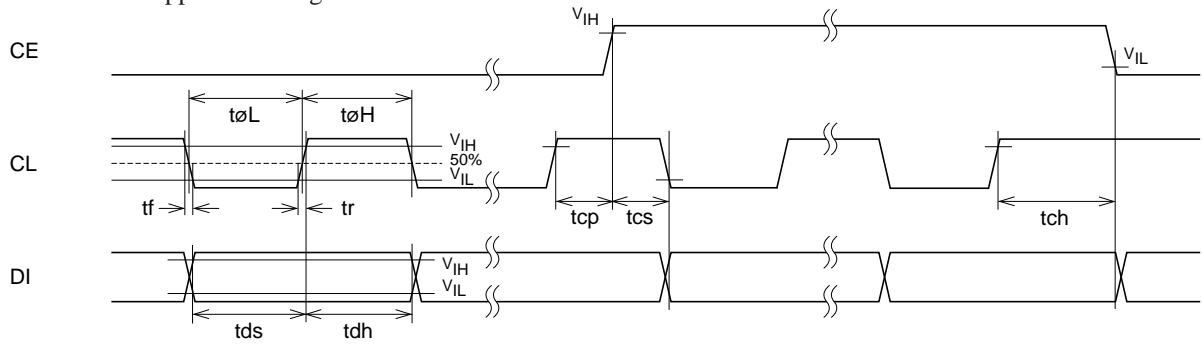
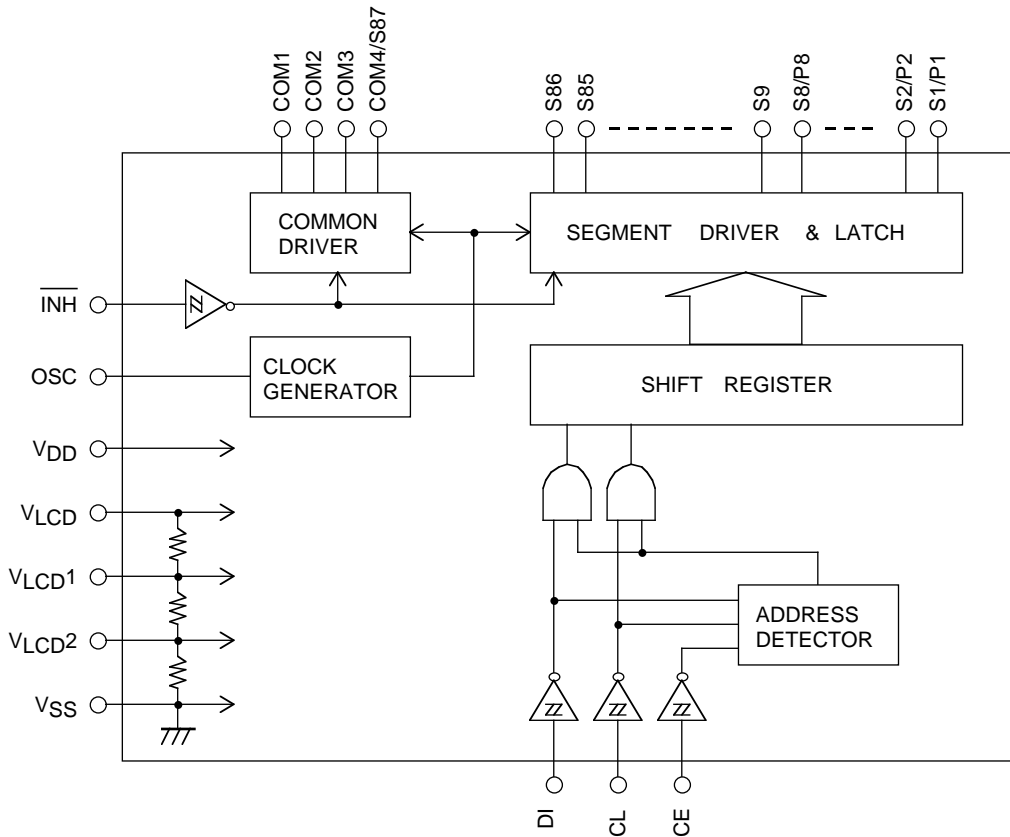


Figure 2

Block Diagram

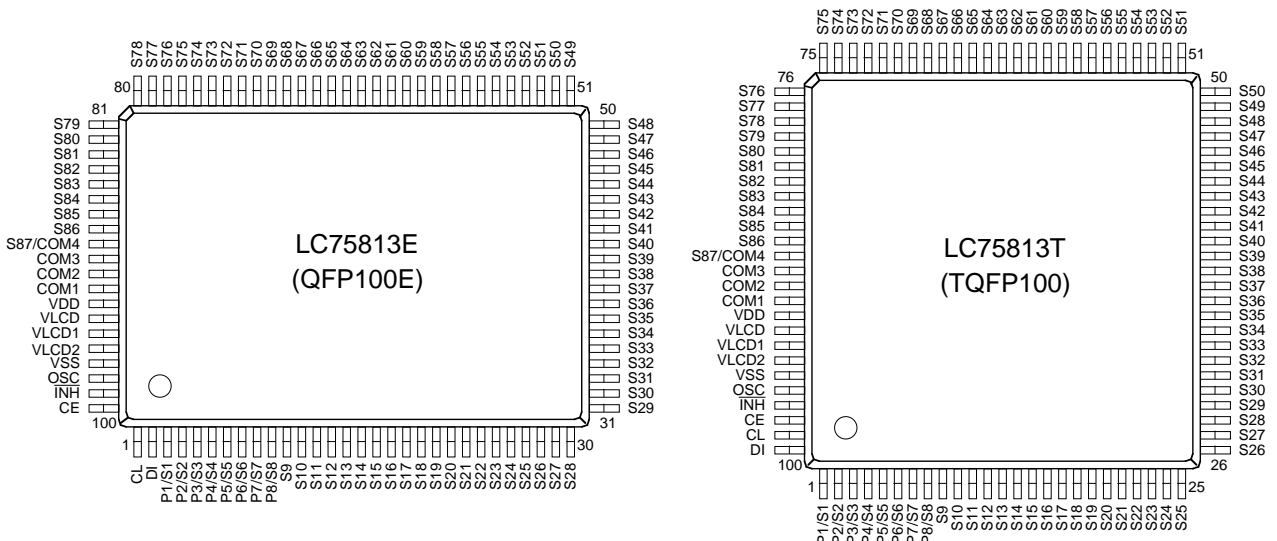


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Pin Functions

Symbol	Pin No.		Function	Active	I/O	Handling when unused
	LC75813E	LC75813T				
S1/P1 to S8/P8 S9 to S86	3 to 10 11 to 88	1 to 8 9 to 86	Segment outputs for displaying the display data transferred by serial data input. The pins S1/P1 to S8/P8 can be used as general-purpose output ports when so set up by the control data.	—	O	Open
COM1 to COM3 COM4/S87	92 to 90 89	90 to 88 87	Common driver outputs. The frame frequency is f_0 Hz. The COM4/S87 pin can be used as a segment output in 1/3 duty.	—	O	Open
OSC	98	96	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.	—	I/O	V_{DD}
CE CL DI	100 1 2	98 99 100	Serial data transfer inputs. These pins are connected to the control microprocessor. CE: Chip enable CL: Synchronization clock DI: Transfer data	H — —	I I I	GND
$\overline{\text{INH}}$	99	97	Display off control input • $\overline{\text{INH}} = \text{low} (V_{SS}) \dots \text{Off}$ S1/P1 to S8/P8 = low (V_{SS}) (These pins are forcibly set to the segment output port function and fixed at the V_{SS} level.) S9 to S86 = low (V_{SS}) COM1 to COM3 = low (V_{SS}) COM4/S87 = low (V_{SS}) • $\overline{\text{INH}} = \text{high} (V_{DD}) \dots \text{On}$ Note that serial data transfers can be performed when the display is forced off by this pin.	L	I	GND
V_{LCD1}	95	93	Used to apply the LCD drive 2/3 bias voltage externally. This pin must be connected to V_{LCD2} when 1/2 bias drive is used.	—	I	Open
V_{LCD2}	96	94	Used to apply the LCD drive 1/3 bias voltage externally. This pin must be connected to V_{LCD1} when 1/2 bias drive is used.	—	I	Open
V_{DD}	93	91	Logic block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—
V_{LCD}	94	92	LCD driver block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—
V_{SS}	97	95	Ground pin. Connect to ground.	—	—	—

Pin Assignments

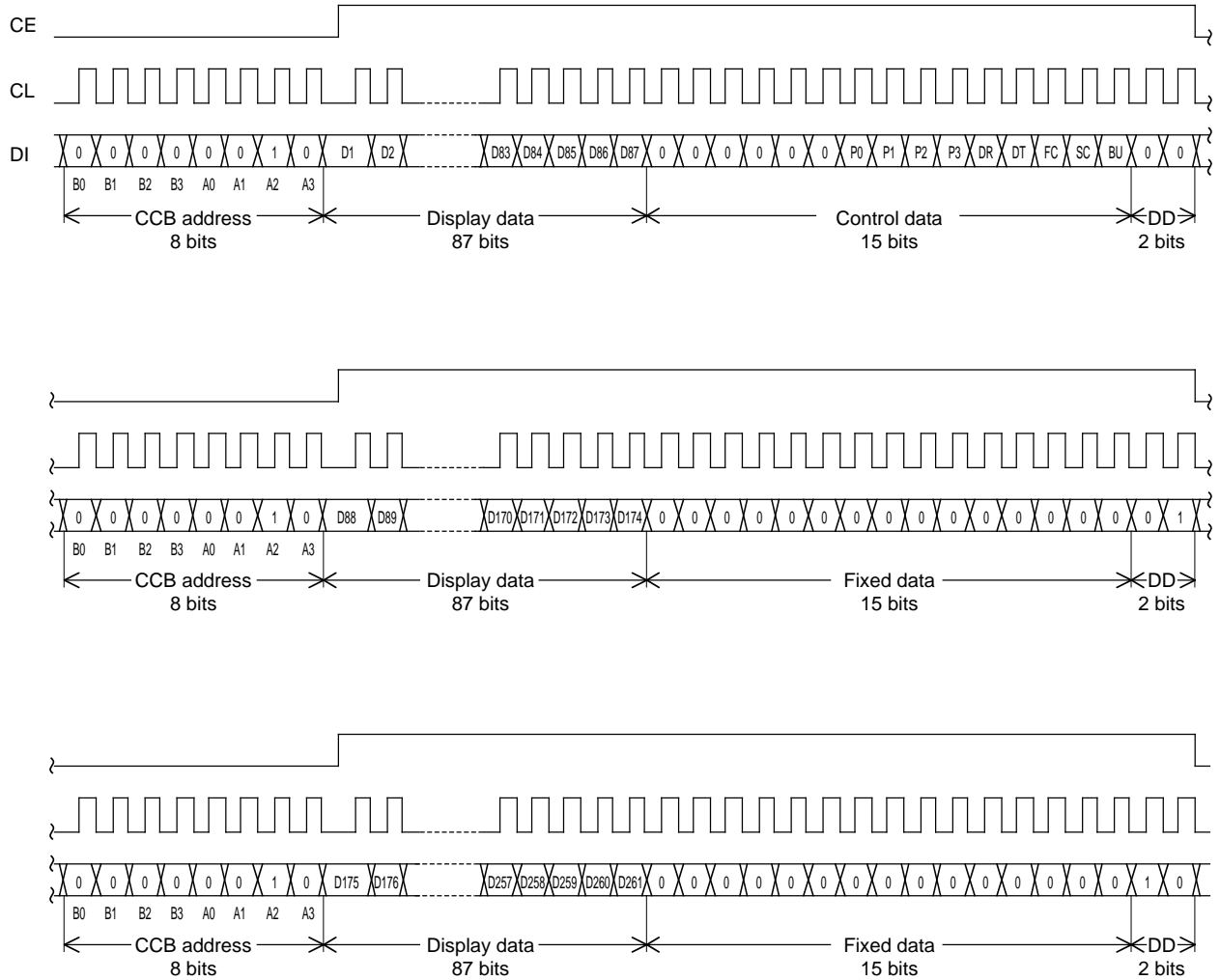


Top view

Serial Data Transfer Format

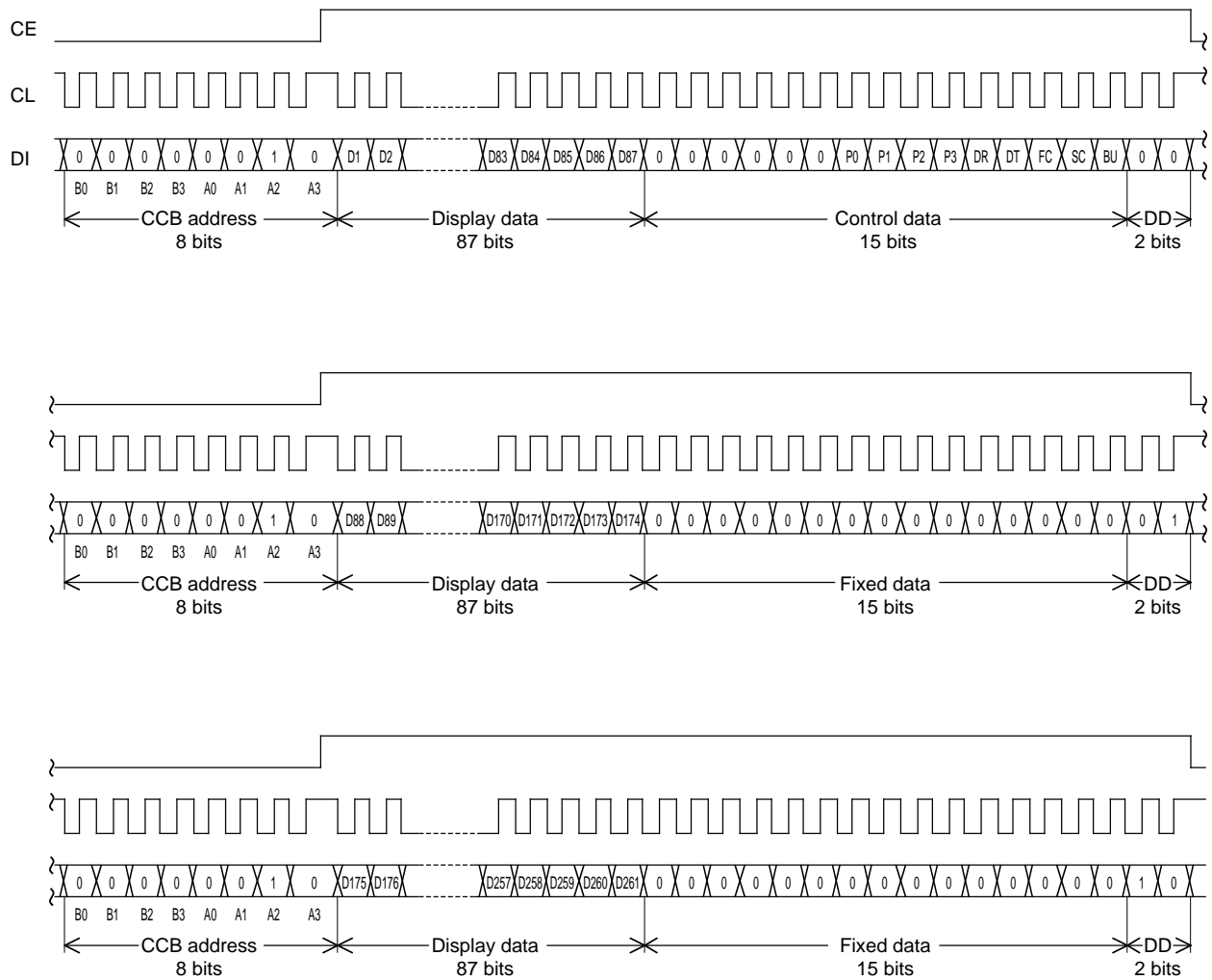
1. 1/3 duty

① When CL is stopped at the low level



Note: DD---Direction data.

② When CL is stopped at the high level



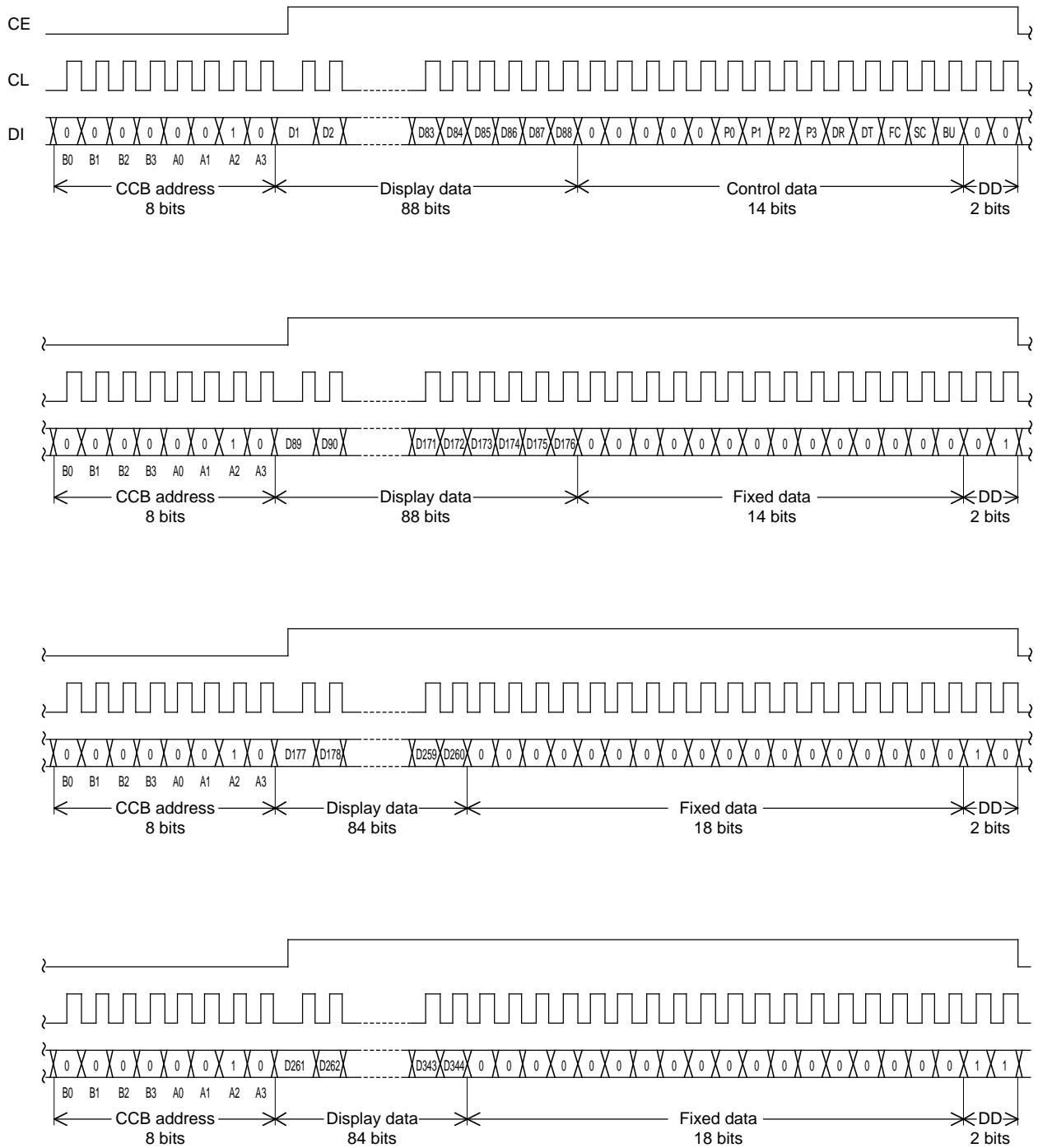
Note: DD...Direction data.

- CCB address.....40H
- D1 to D261.....Display data
- P0 to P3Segment output port/general-purpose output port switching control data
- DR1/2 bias drive or 1/3 bias drive switching control data
- DT1/3 duty drive or 1/4 duty drive switching control data
- FC.....Common and segment output waveforms frame frequency setting control data
- SC.....Segments on/off control data
- BUNormal mode/power-saving mode control data

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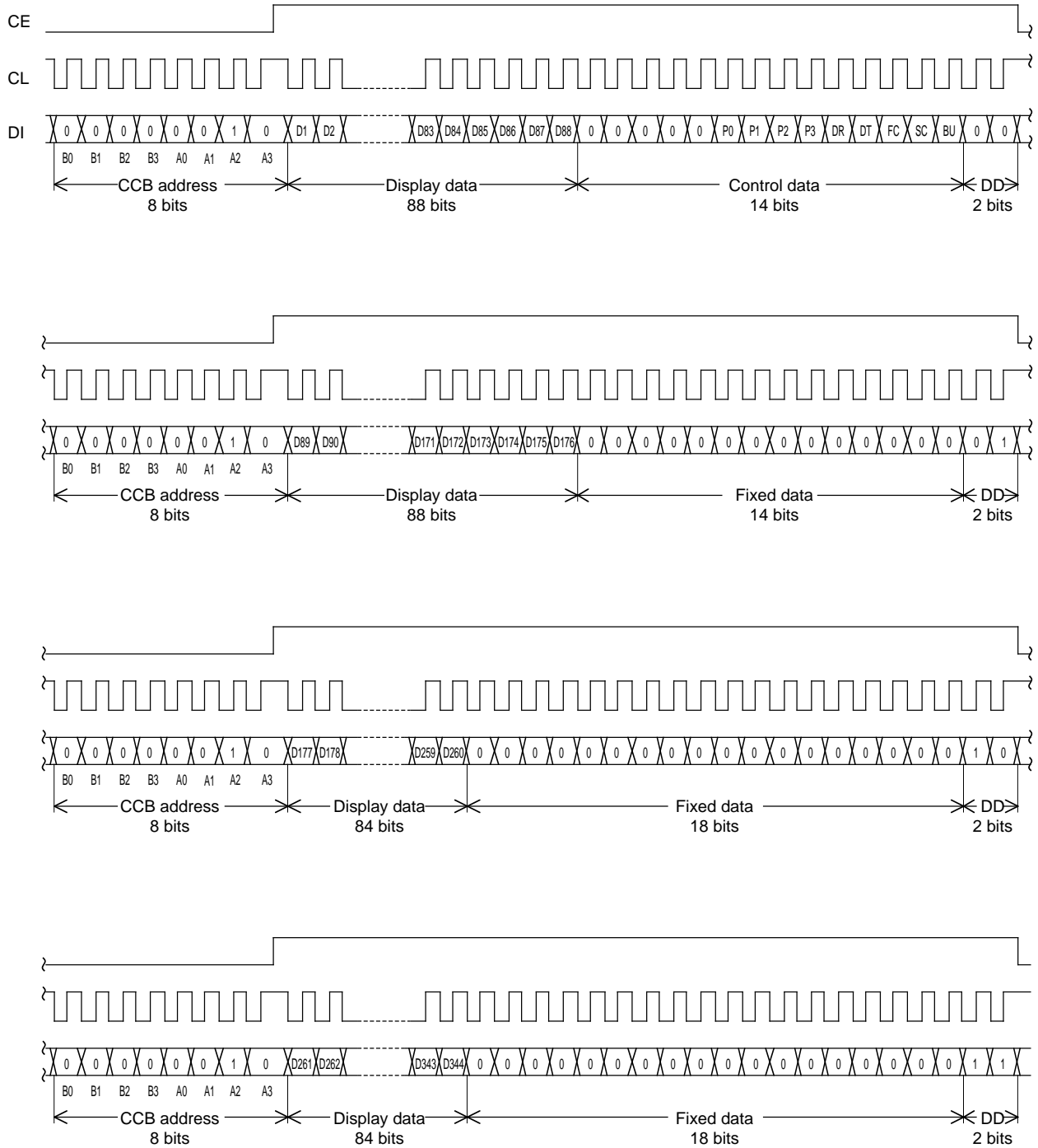
2. 1/4 duty

① When CL is stopped at the low level



Note: DD---Direction data.

② When CL is stopped at the high level



Note: DD...Direction data.

- CCB address.....40H
- D1 to D344.....Display data
- P0 to P3Segment output port/general-purpose output port switching control data
- DR1/2 bias drive or 1/3 bias drive switching control data
- DT1/3 duty drive or 1/4 duty drive switching control data
- FC.....Common and segment output waveforms frame frequency setting control data
- SC.....Segments on/off control data
- BUNormal mode/power-saving mode control data

Control Data Functions

1. P0 to P3: Segment output port/general-purpose output port switching control data.

These control data bits switch the S1/P1 to S8/P8 output pins between their segment output port and general-purpose output port functions.

Control data				Output pin state								
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8	
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8	
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8	
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8	
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8	
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8	
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8	
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8	
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8	

Note: Sn (n = 1 to 8): Segment output ports
Pn (n = 1 to 8): General-purpose output ports

Also note that when the general-purpose output port function is selected, the output pins and the display data will have the correspondences listed in the tables below.

Output pin	Corresponding display data	
	1/3 duty	1/4 duty
S1/P1	D1	D1
S2/P2	D4	D5
S3/P3	D7	D9
S4/P4	D10	D13
S5/P5	D13	D17
S6/P6	D16	D21
S7/P7	D19	D25
S8/P8	D22	D29

For example, when 1/4 duty drive scheme is used, if the general-purpose output port function is selected for the S4/P4 output pin, that output pin will output a high level (V_{LCD}) when the display data D13 is 1, and a low level (V_{SS}) when the D13 is 0.

2. DR: 1/2 bias drive or 1/3 bias drive switching control data

This control data bit selects either 1/2 bias drive or 1/3 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

3. DT: 1/3 duty drive or 1/4 duty drive switching control data

This control data bit selects either 1/3 duty drive or 1/4 duty drive.

DT	Duty drive scheme	Output pin state (COM4/S87)
0	1/4 duty drive	COM4
1	1/3 duty drive	S87

Note: COM4: common output
S87: segment output

4. FC: Common and segment output waveforms frame frequency setting control data

This control data bit sets the frame frequency for common and segment output waveforms.

FC	Frame frequency f0 [Hz]
0	$\frac{f_{osc}}{384}$
1	$\frac{f_{osc}}{192}$

5. SC: Segments on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

6. BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode (The OSC pin oscillator is stopped, and the common and segment output pins go to the V _{SS} level. However, the S1/P1 to S8/P8 output pins that are set to be general-purpose output ports by the control data P0 to P3 can be used as general-purpose output ports.)

Display Data to Segment Output Pin Correspondence

1. 1/3 duty

Segment Output pin	COM1	COM2	COM3	Segment Output pin	COM1	COM2	COM3	Segment Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3	S30	D88	D89	D90	S59	D175	D176	D177
S2/P2	D4	D5	D6	S31	D91	D92	D93	S60	D178	D179	D180
S3/P3	D7	D8	D9	S32	D94	D95	D96	S61	D181	D182	D183
S4/P4	D10	D11	D12	S33	D97	D98	D99	S62	D184	D185	D186
S5/P5	D13	D14	D15	S34	D100	D101	D102	S63	D187	D188	D189
S6/P6	D16	D17	D18	S35	D103	D104	D105	S64	D190	D191	D192
S7/P7	D19	D20	D21	S36	D106	D107	D108	S65	D193	D194	D195
S8/P8	D22	D23	D24	S37	D109	D110	D111	S66	D196	D197	D198
S9	D25	D26	D27	S38	D112	D113	D114	S67	D199	D200	D201
S10	D28	D29	D30	S39	D115	D116	D117	S68	D202	D203	D204
S11	D31	D32	D33	S40	D118	D119	D120	S69	D205	D206	D207
S12	D34	D35	D36	S41	D121	D122	D123	S70	D208	D209	D210
S13	D37	D38	D39	S42	D124	D125	D126	S71	D211	D212	D213
S14	D40	D41	D42	S43	D127	D128	D129	S72	D214	D215	D216
S15	D43	D44	D45	S44	D130	D131	D132	S73	D217	D218	D219
S16	D46	D47	D48	S45	D133	D134	D135	S74	D220	D221	D222
S17	D49	D50	D51	S46	D136	D137	D138	S75	D223	D224	D225
S18	D52	D53	D54	S47	D139	D140	D141	S76	D226	D227	D228
S19	D55	D56	D57	S48	D142	D143	D144	S77	D229	D230	D231
S20	D58	D59	D60	S49	D145	D146	D147	S78	D232	D233	D234
S21	D61	D62	D63	S50	D148	D149	D150	S79	D235	D236	D237
S22	D64	D65	D66	S51	D151	D152	D153	S80	D238	D239	D240
S23	D67	D68	D69	S52	D154	D155	D156	S81	D241	D242	D243
S24	D70	D71	D72	S53	D157	D158	D159	S82	D244	D245	D246
S25	D73	D74	D75	S54	D160	D161	D162	S83	D247	D248	D249
S26	D76	D77	D78	S55	D163	D164	D165	S84	D250	D251	D252
S27	D79	D80	D81	S56	D166	D167	D168	S85	D253	D254	D255
S28	D82	D83	D84	S57	D169	D170	D171	S86	D256	D257	D258
S29	D85	D86	D87	S58	D172	D173	D174	COM4/S87	D259	D260	D261

Note: This applies to the case where the S1/P1 to S8/P8, and COM4/S87 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data			Segment output pin (S11) state
D31	D32	D33	
0	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are off.
0	0	1	The LCD segment corresponding to COM3 is on.
0	1	0	The LCD segment corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM2 and COM3 are on.
1	0	0	The LCD segment corresponding to COM1 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1, COM2, and COM3 are on.

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2. 1/4 duty

Segment Output pin	COM1	COM2	COM3	COM4	Segment Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4	S44	D173	D174	D175	D176
S2/P2	D5	D6	D7	D8	S45	D177	D178	D179	D180
S3/P3	D9	D10	D11	D12	S46	D181	D182	D183	D184
S4/P4	D13	D14	D15	D16	S47	D185	D186	D187	D188
S5/P5	D17	D18	D19	D20	S48	D189	D190	D191	D192
S6/P6	D21	D22	D23	D24	S49	D193	D194	D195	D196
S7/P7	D25	D26	D27	D28	S50	D197	D198	D199	D200
S8/P8	D29	D30	D31	D32	S51	D201	D202	D203	D204
S9	D33	D34	D35	D36	S52	D205	D206	D207	D208
S10	D37	D38	D39	D40	S53	D209	D210	D211	D212
S11	D41	D42	D43	D44	S54	D213	D214	D215	D216
S12	D45	D46	D47	D48	S55	D217	D218	D219	D220
S13	D49	D50	D51	D52	S56	D221	D222	D223	D224
S14	D53	D54	D55	D56	S57	D225	D226	D227	D228
S15	D57	D58	D59	D60	S58	D229	D230	D231	D232
S16	D61	D62	D63	D64	S59	D233	D234	D235	D236
S17	D65	D66	D67	D68	S60	D237	D238	D239	D240
S18	D69	D70	D71	D72	S61	D241	D242	D243	D244
S19	D73	D74	D75	D76	S62	D245	D246	D247	D248
S20	D77	D78	D79	D80	S63	D249	D250	D251	D252
S21	D81	D82	D83	D84	S64	D253	D254	D255	D256
S22	D85	D86	D87	D88	S65	D257	D258	D259	D260
S23	D89	D90	D91	D92	S66	D261	D262	D263	D264
S24	D93	D94	D95	D96	S67	D265	D266	S267	D268
S25	D97	D98	D99	D100	S68	D269	D270	D271	D272
S26	D101	D102	D103	D104	S69	D273	D274	D275	D276
S27	D105	D106	D107	D108	S70	D277	D278	D279	D280
S28	D109	D110	D111	D112	S71	D281	D282	D283	D284
S29	D113	D114	D115	D116	S72	D285	D286	D287	D288
S30	D117	D118	D119	D120	S73	D289	D290	D291	D292
S31	D121	D122	D123	D124	S74	D293	D294	D295	D296
S32	D125	D126	D127	D128	S75	D297	D298	D299	D300
S33	D129	D130	D131	D132	S76	D301	D302	D303	D304
S34	D133	D134	D135	D136	S77	D305	D306	D307	D308
S35	D137	D138	D139	D140	S78	D309	D310	D311	D312
S36	D141	D142	D143	D144	S79	D313	D314	D315	D316
S37	D145	D146	D147	D148	S80	D317	D318	D319	D320
S38	D149	D150	D151	D152	S81	D321	D322	D323	D324
S39	D153	D154	D155	D156	S82	D325	D326	D327	D328
S40	D157	D158	D159	D160	S83	D329	D330	D331	D332
S41	D161	D162	D163	D164	S84	D333	D334	D335	D336
S42	D165	D166	D167	D168	S85	D337	D338	D339	D340
S43	D169	D170	D171	D172	S86	D341	D342	D343	D344

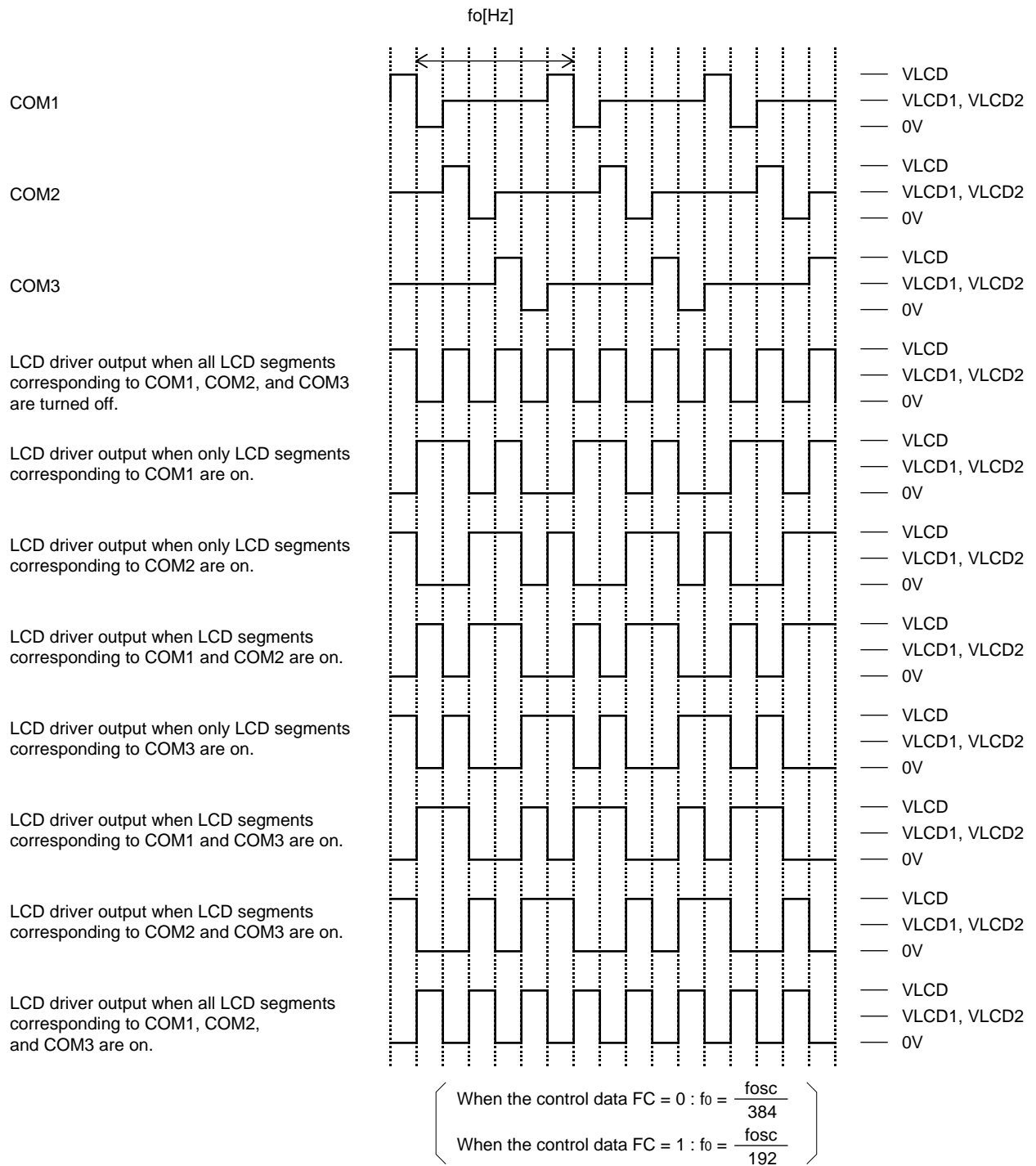
Note: This applies to the case where the S1/P1 to S8/P8 output pins are set to be segment output ports.

LC75813E, 75813T

For example, the table below lists the segment output states for the S11 output pin.

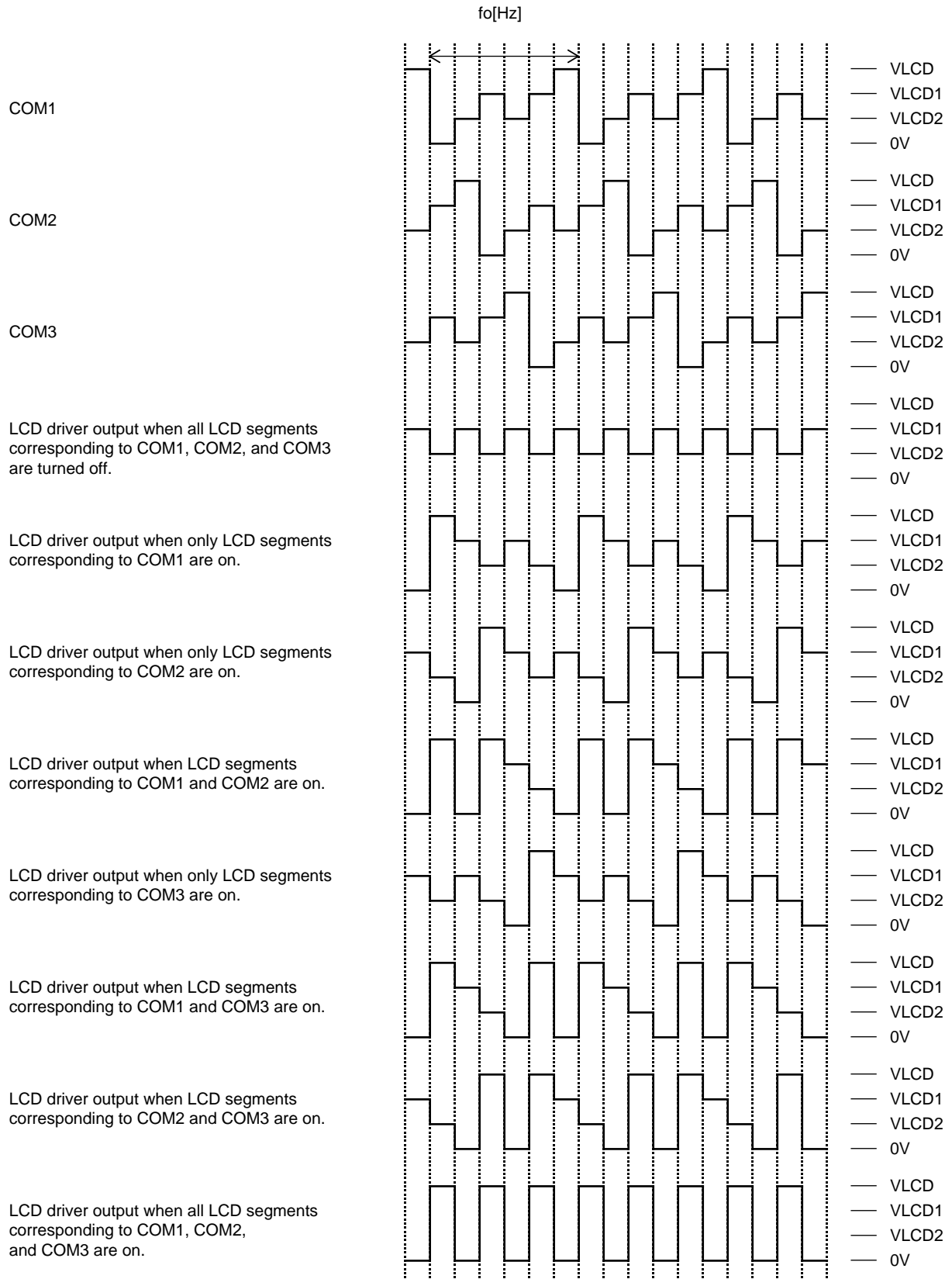
Display data				Segment output pin (S11) state
D41	D42	D43	D44	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

1/3 Duty, 1/2 Bias Drive Technique



1/3 Duty, 1/2 Bias Waveforms

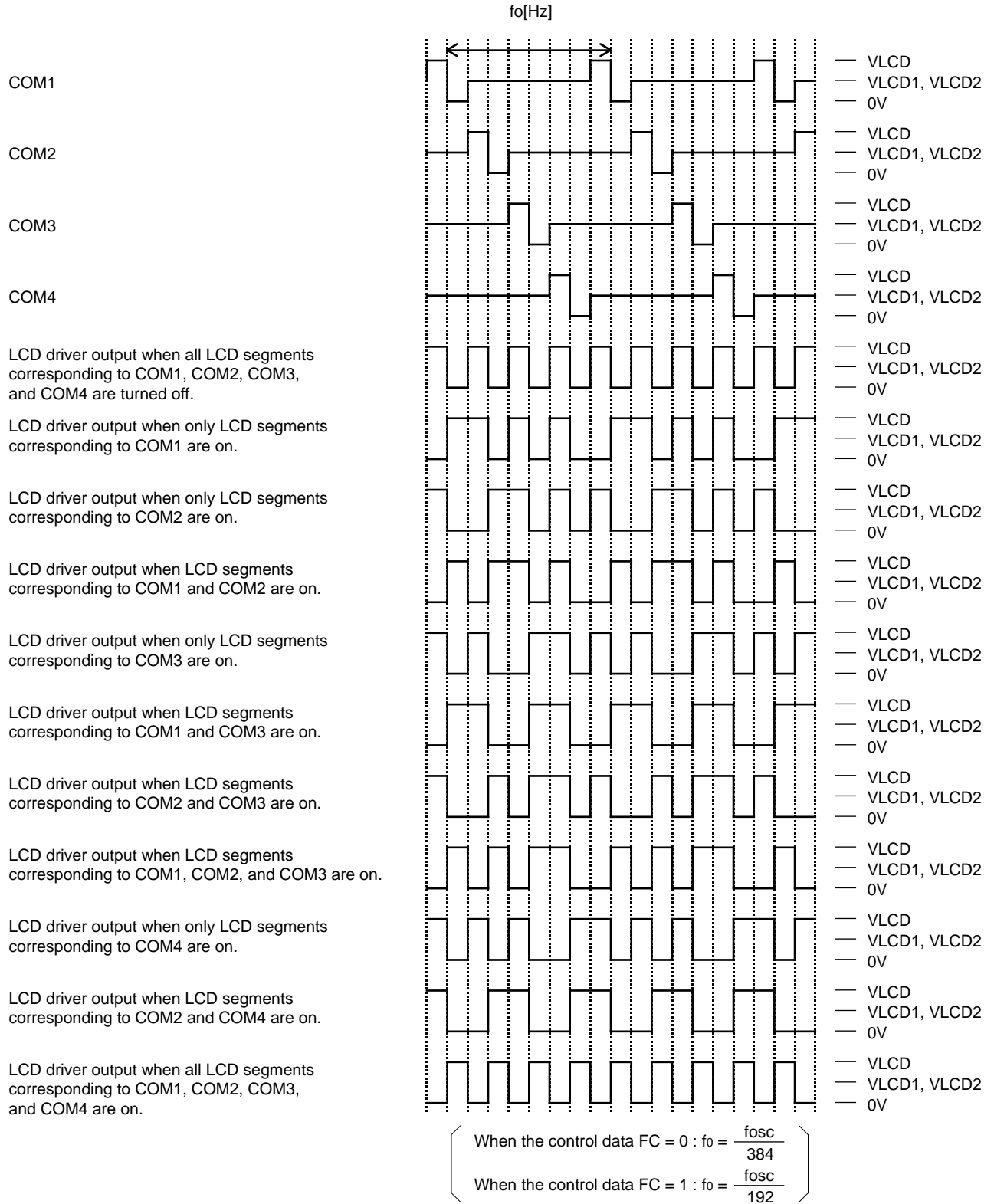
1/3 Duty, 1/3 Bias Drive Technique



$$\left(\begin{array}{l} \text{When the control data FC} = 0 : f_o = \frac{f_{osc}}{384} \\ \text{When the control data FC} = 1 : f_o = \frac{f_{osc}}{192} \end{array} \right)$$

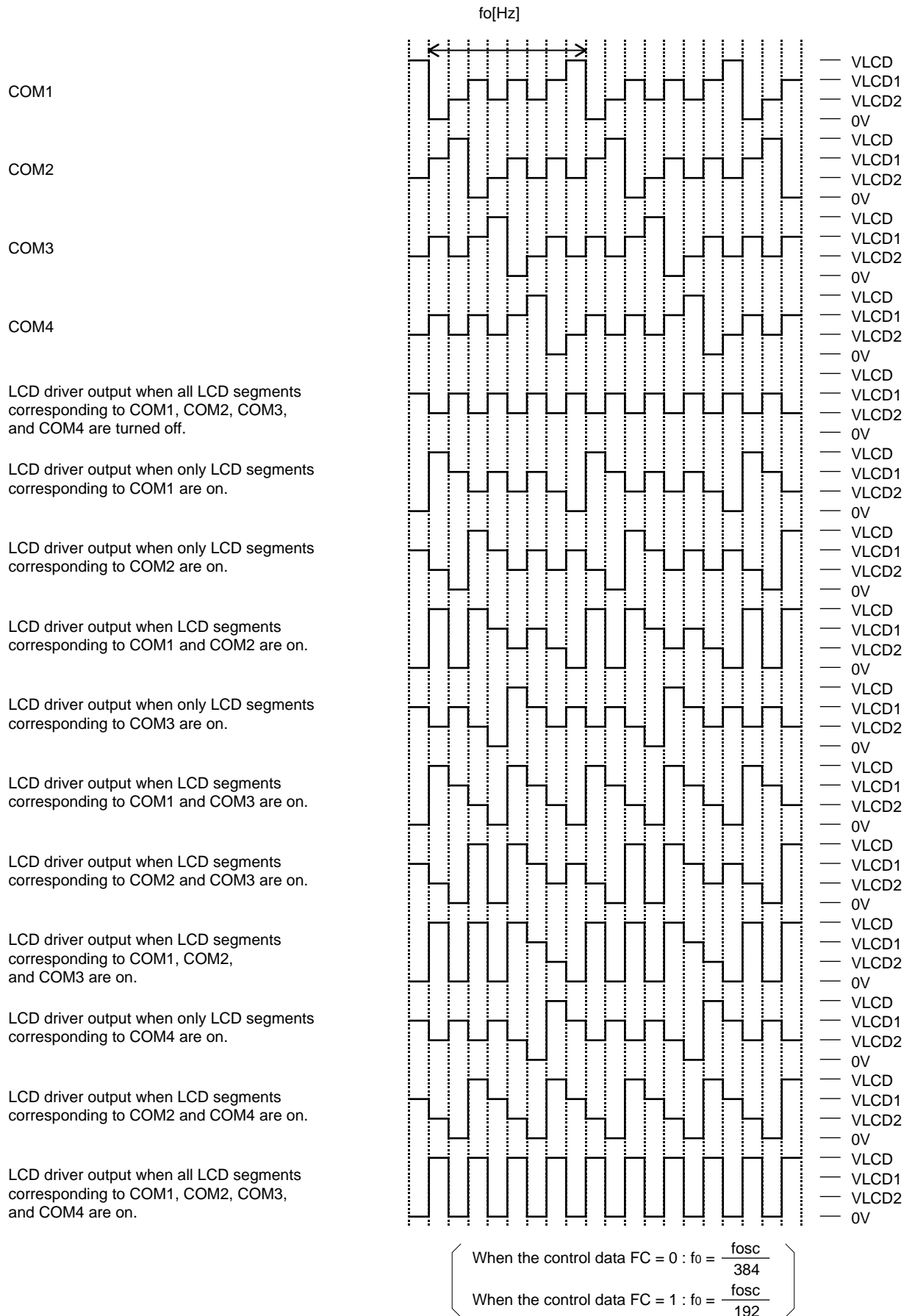
1/3 Duty, 1/3 Bias Waveforms

1/4 Duty, 1/2 Bias Drive Technique



1/4 Duty, 1/2 Bias Waveforms

1/4 Duty, 1/3 Bias Drive Technique



1/4 Duty, 1/3 Bias Waveforms

The $\overline{\text{INH}}$ pin and Display Control

Since the IC internal data (1/3 duty: the display data D1 to D261 and the control data, 1/4 duty: the display data D1 to D344 and the control data) is undefined when power is first applied, applications should set the $\overline{\text{INH}}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S8/P8, S9 to S86, COM1 to COM3, and COM4/S87 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{\text{INH}}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figures 3 and 4.)

Notes on the Power On/Off Sequences

Applications should observe the following sequences when turning the LC75813E and LC75813T power on and off.

- At power on: Logic block power supply (V_{DD}) on → LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off → Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

1. 1/3 duty

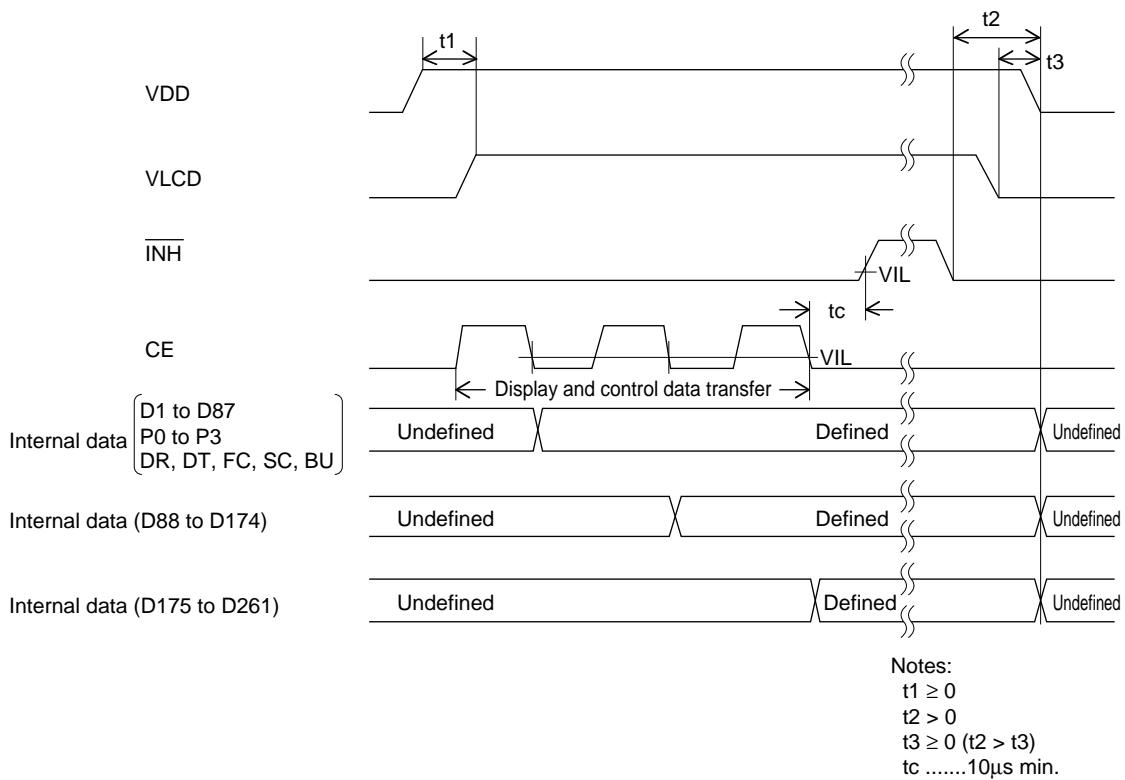


Figure 3

2. 1/4 duty

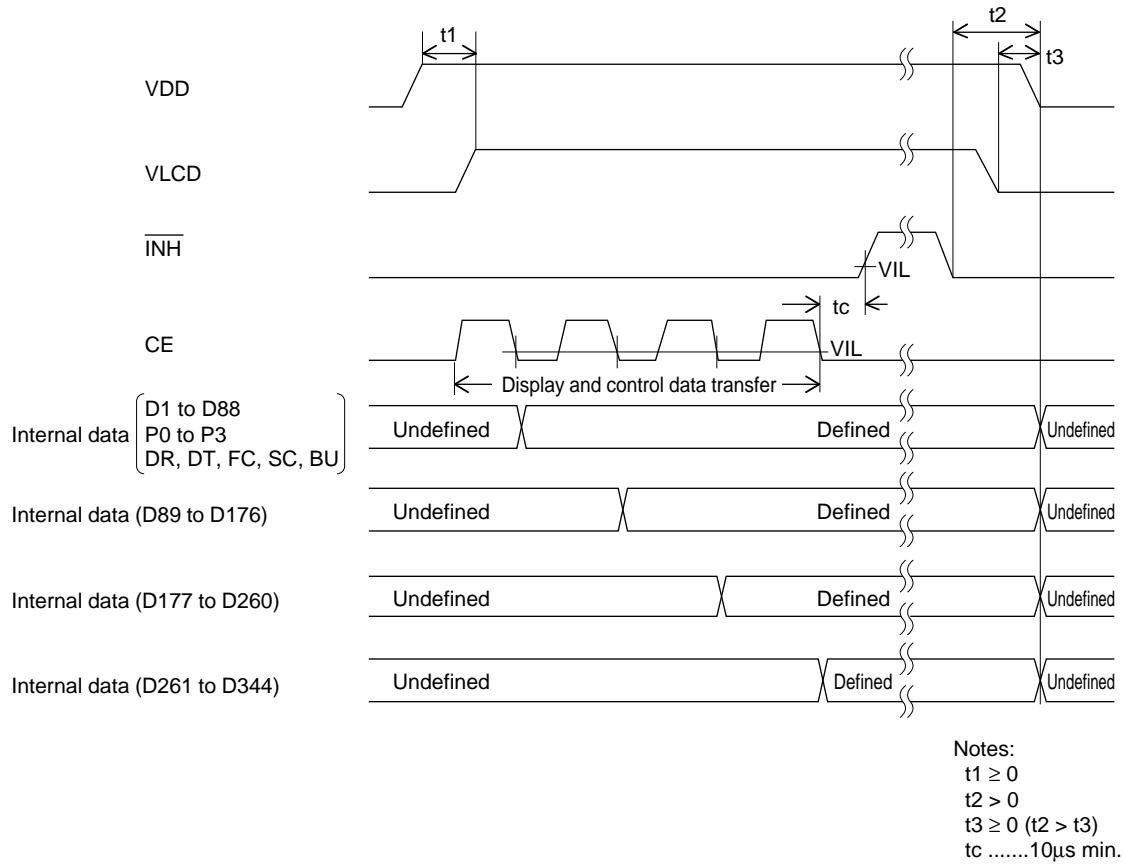


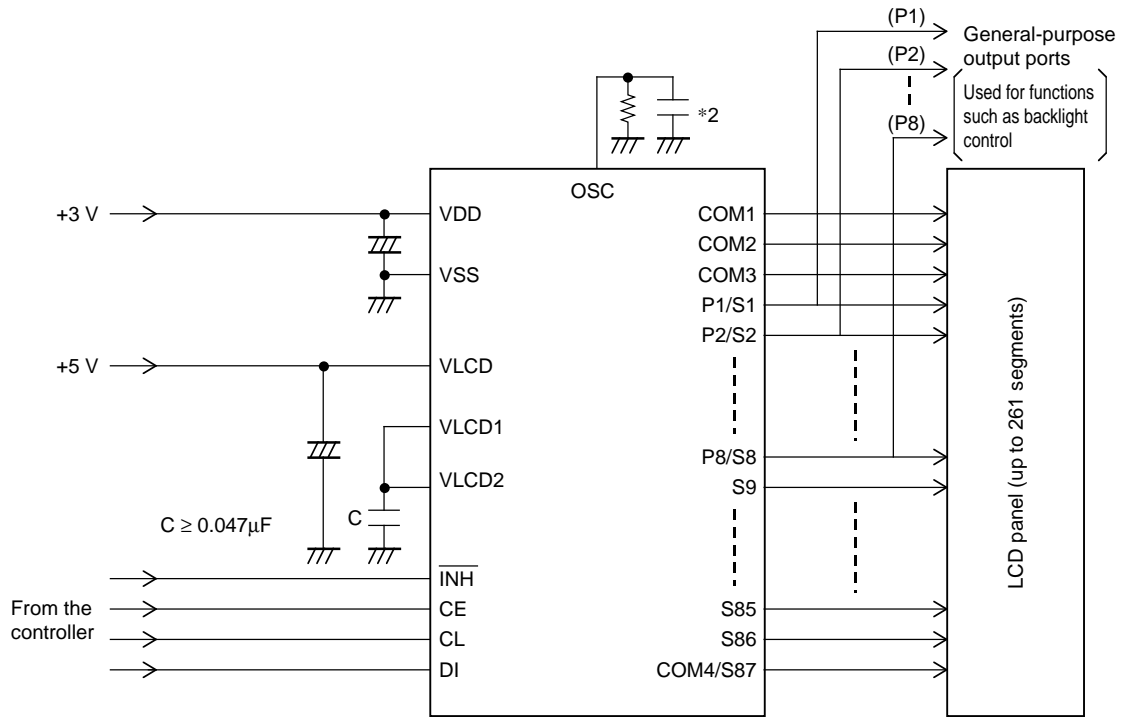
Figure 4

Notes on Controller Transfer of Display Data

Since the LC75813E and LC75813T accept the display data (D1 to D261) divided into three separate transfer operations when using 1/3 duty drive scheme and the data (D1 to D344) divided into four separate transfer operations when 1/4 duty drive, we recommend that applications transfer all of the display data within a period of less than 30 ms to prevent observable degradation of display quality.

Sample Application Circuit 1

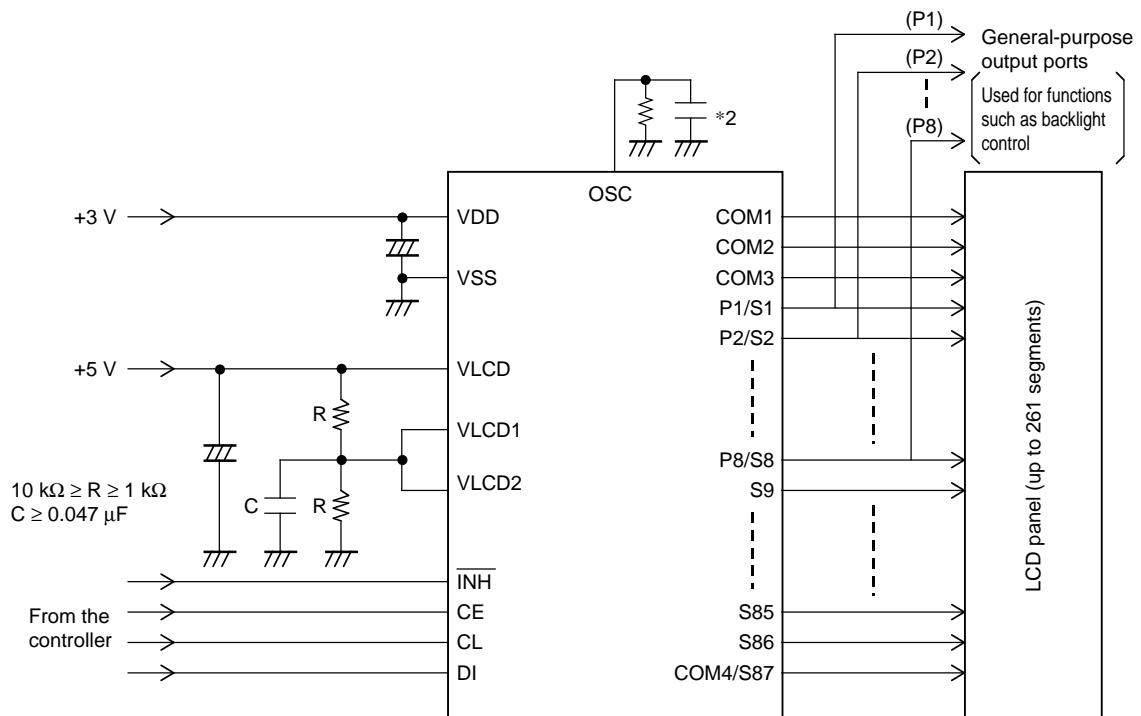
1/3 Duty, 1/2 Bias (for use with normal panels)



Note: *2 When a capacitor except the recommended external capacitance ($C_{osc} = 1000\text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 2

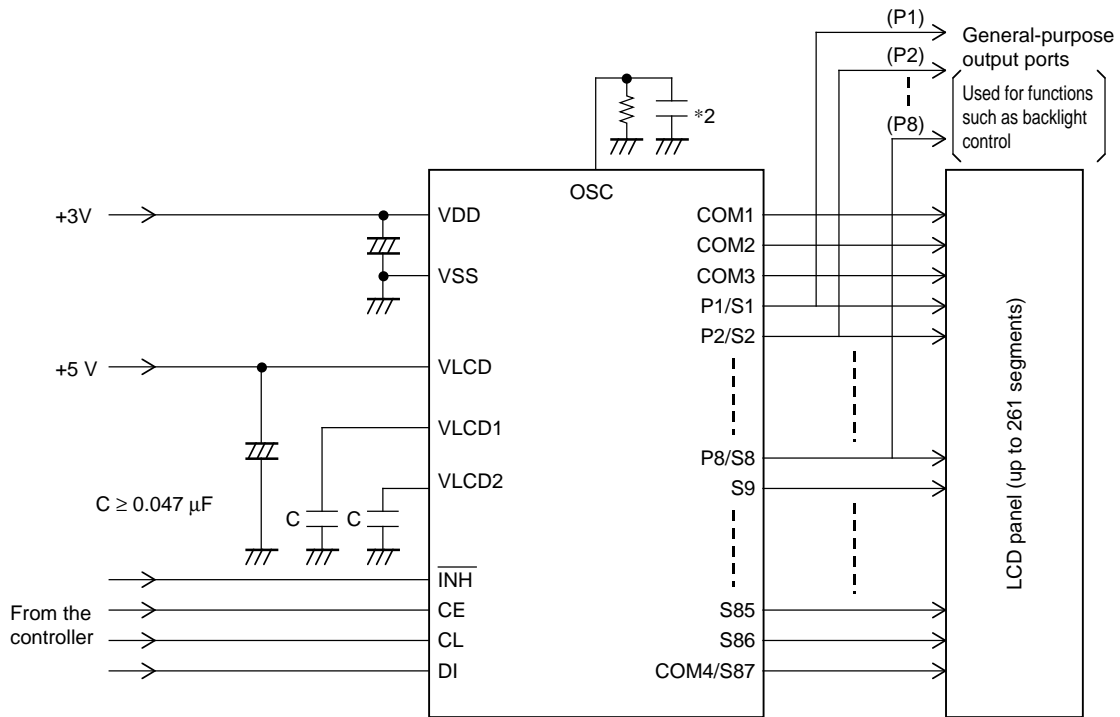
1/3 Duty, 1/2 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance ($C_{osc} = 1000\text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 3

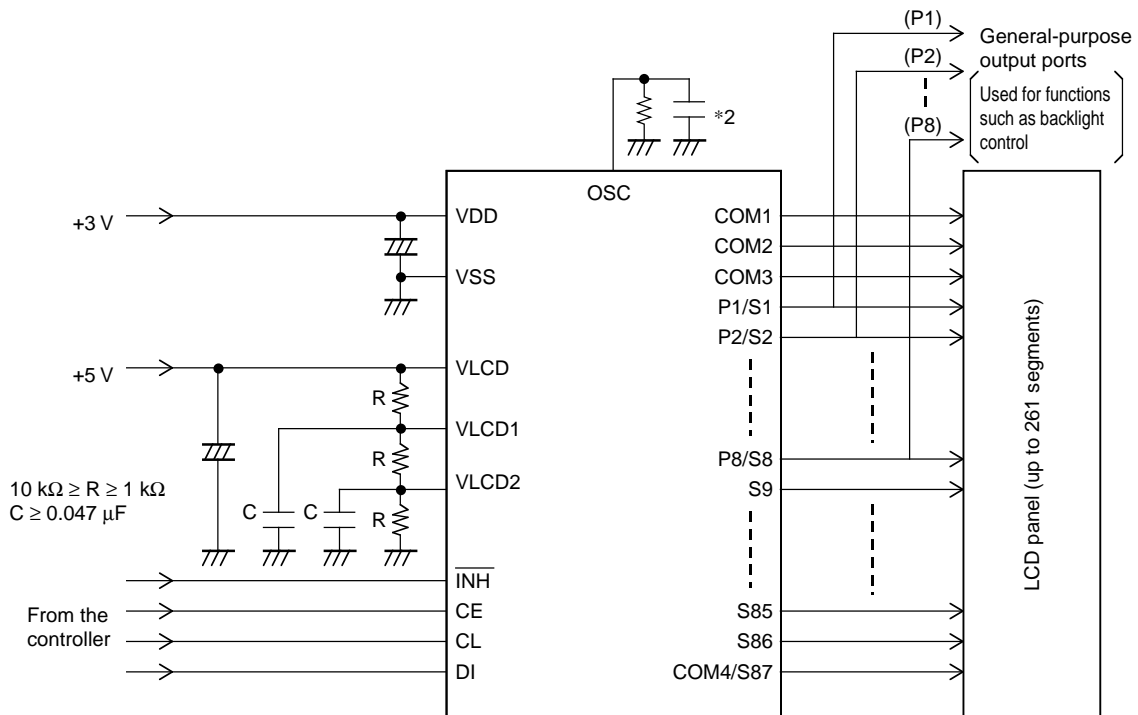
1/3 Duty, 1/3 Bias (for use with normal panels)



Note: *2 When a capacitor except the recommended external capacitance ($C_{osc} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 4

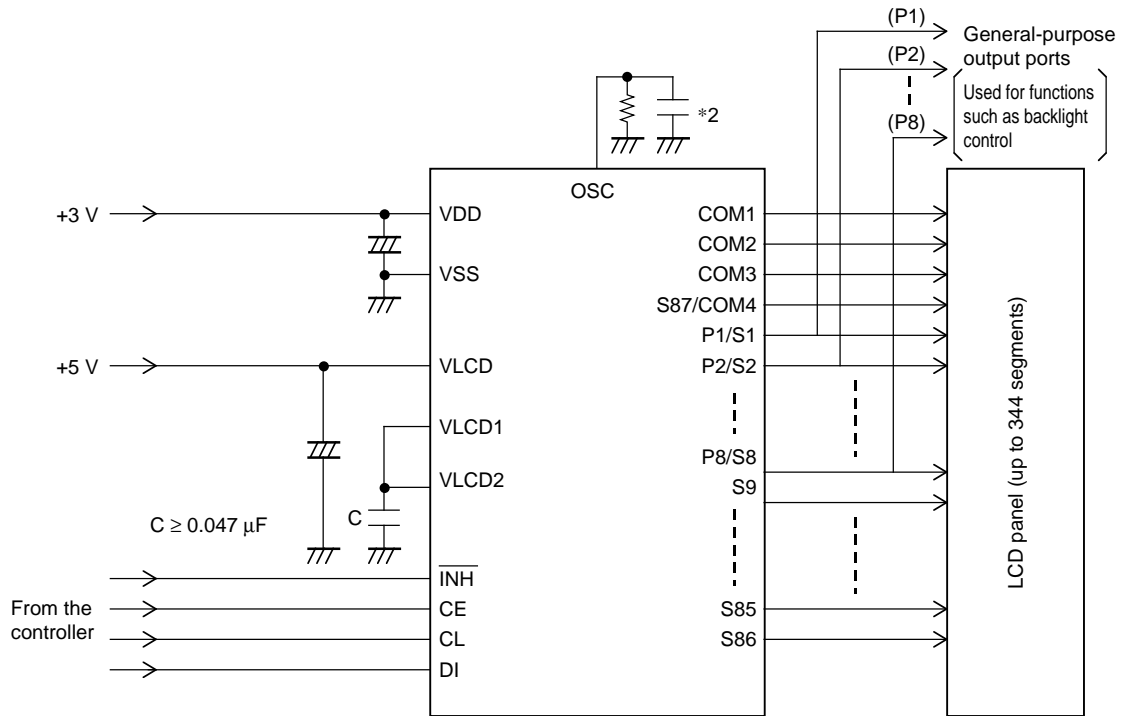
1/3 Duty, 1/3 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance ($C_{osc} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 5

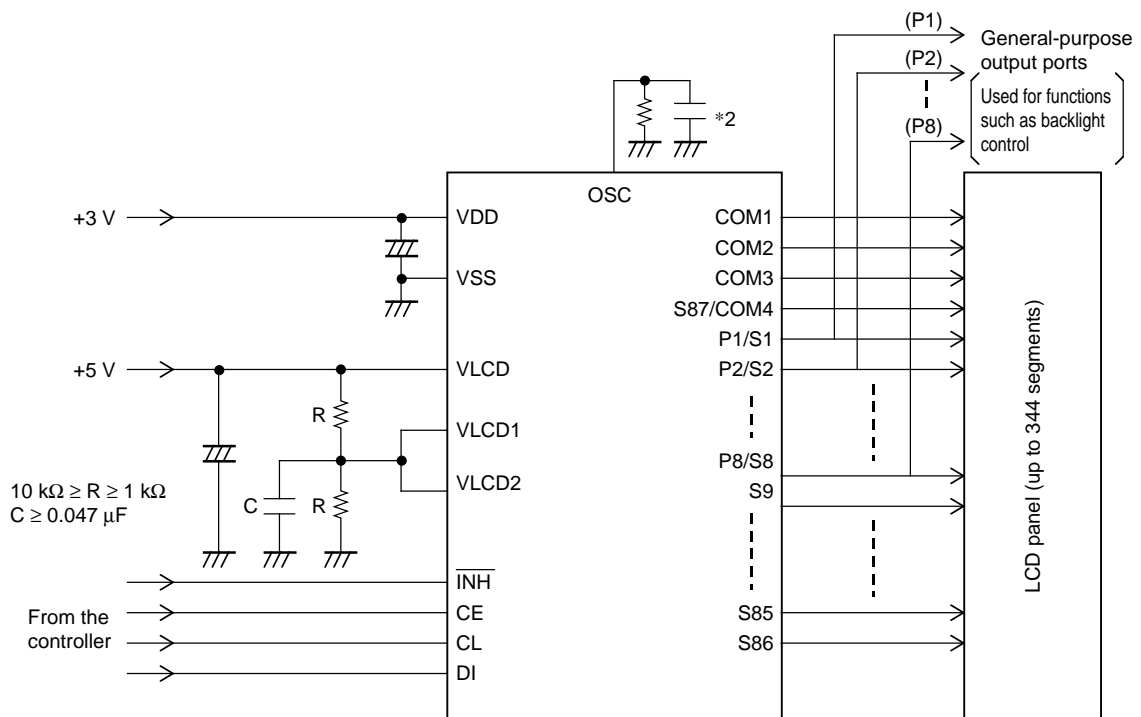
1/4 Duty, 1/2 Bias (for use with normal panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 6

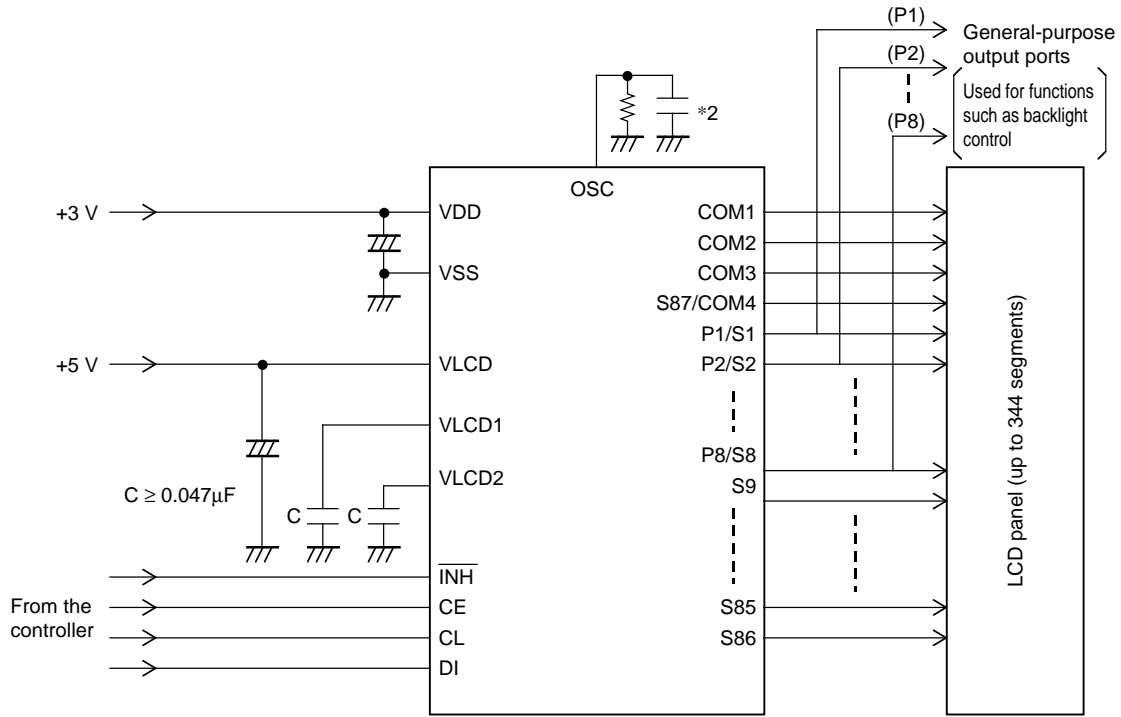
1/4 Duty, 1/2 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance (Cosc = 1000 pF) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 7

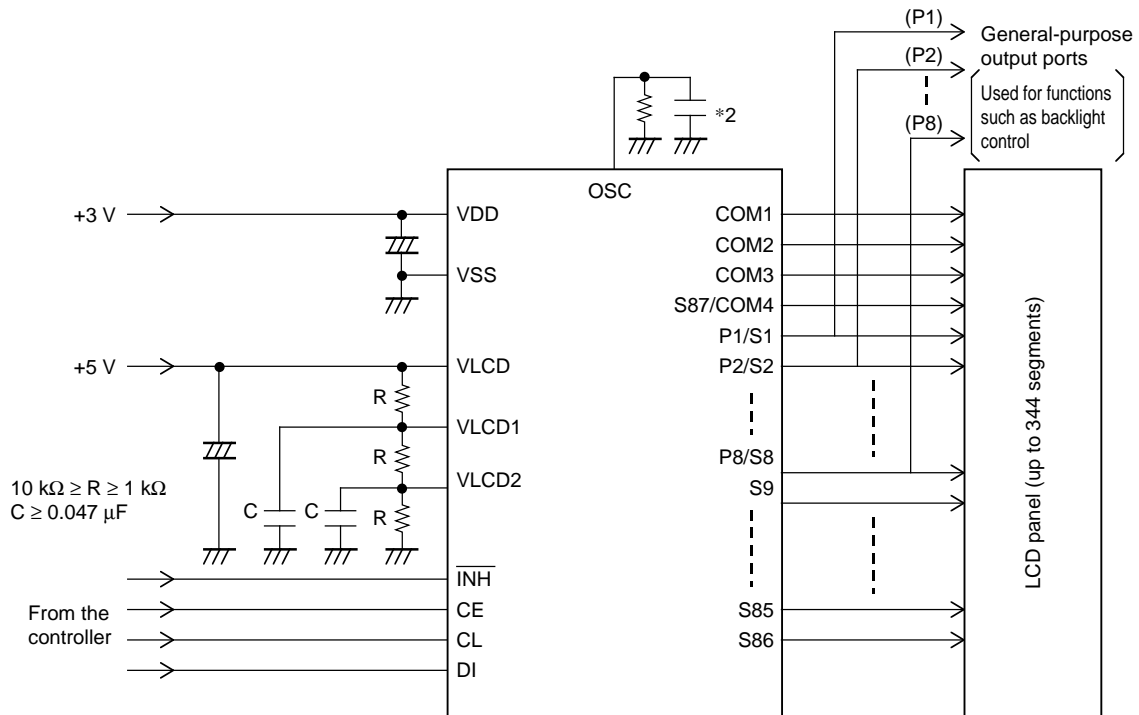
1/4 Duty, 1/3 Bias (for use with normal panels)



Note: *2 When a capacitor except the recommended external capacitance ($C_{osc} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

Sample Application Circuit 8

1/4 Duty, 1/3 Bias (for use with large panels)



Note: *2 When a capacitor except the recommended external capacitance ($C_{osc} = 1000 \text{ pF}$) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200 pF.

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