

FJ4B01120L

Single P-channel MOS FET

■ Features

- Drain-source On-state Resistance : $R_{DS(on)}$ typ. = $40 \text{ m}\Omega$ ($V_{GS} = -2.5 \text{ V}$)
- CSP(Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL : Level 1)

■ Marking Symbol : 1F

■ Packaging

Embossed type (Thermo-compression sealing) : 20 000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

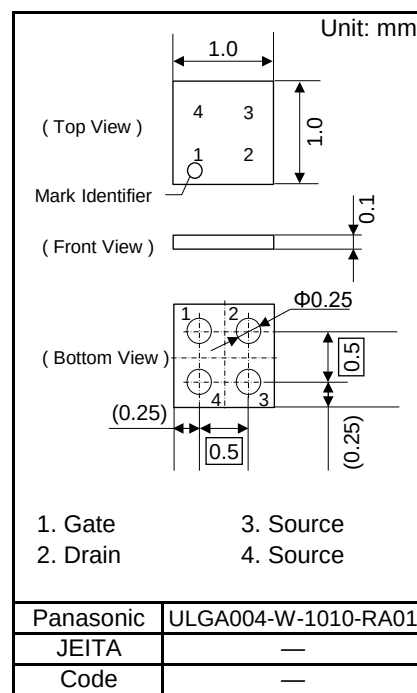
Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	-12	V
Gate-source Voltage		VGS	±8	V
Drain Current	DC	ID1 ^{*1}	-2.6	A
		ID2 ^{*2}	-4.2	A
		ID3 ^{*3}	-5.4	A
	Pulsed ^{*4}	IDp1	-20	A
		IDp2	-33	A
		IDp3	-43	A
Total Power Dissipation		PD1 ^{*1}	0.37	W
		PD2 ^{*2}	0.94	W
		PD3 ^{*3}	1.5	W
Channel Temperature		Tch	150	°C
Operating Ambient Temperature		Topr	-40 to +85	°C
Storage Temperature Range		Tstg	-55 to +150	°C

Note *1 FR4 board (25.4mm×25.4mm×t1.0mm)、Min Cu 36mm² Copper.

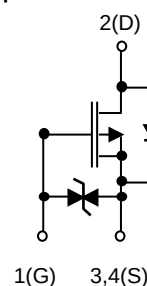
*2 FR4 board (25.4mm×25.4mm×t1.0mm)、Full Cu.

*3 Ceramic substrate (70mm×70mm×t1.0mm).

*4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$



Equivalent circuit



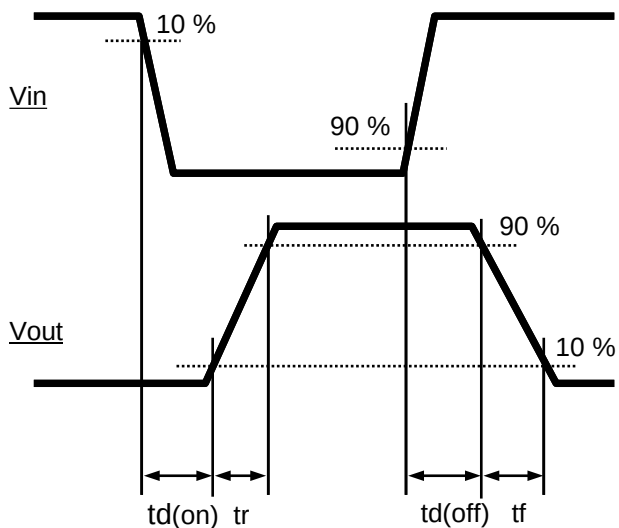
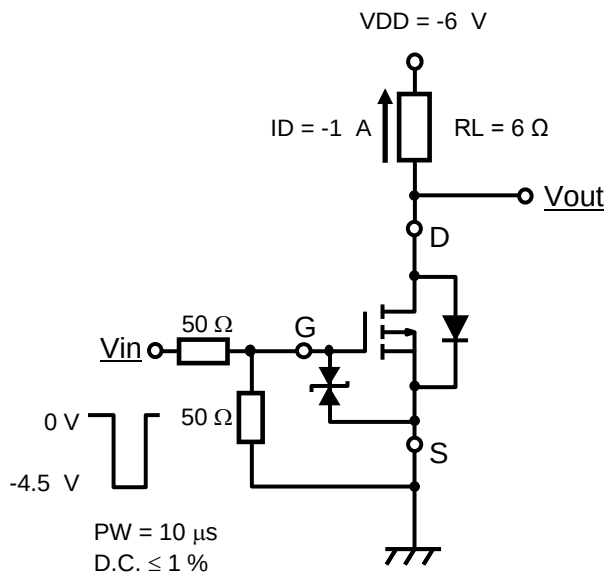
■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0	-12			V
Zero Gate Voltage Drain Current	IDSS	VDS = -12 V, VGS = 0			-1	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = -2 mA, VDS = -10 V	-0.3		-1.0	V
Drain-source On-state Resistance	RDS(on)1	ID = -2 A, VGS = -4.5 V		34	51	mΩ
	RDS(on)2	ID = -2 A, VGS = -2.5 V		40	61	
	RDS(on)3	ID = -0.2 A, VGS = -1.8 V		48	85	
	RDS(on)4	ID = -0.1 A, VGS = -1.5 V		57	170	
Body Diode Forward Voltage	VF(s-d)	IF = -0.2 A, VGS = 0 V		-0.7	-1.2	V
Input Capacitance ^{*1}	Ciss	VDS = -10 V, VGS = 0 V f = 1 MHz		814		pF
Output Capacitance ^{*1}	Coss			201		
Reverse Transfer Capacitance ^{*1}	Crss			187		
Turn-on Delay Time ^{*1,*2}	td(on)	VDD = -6 V, VGS = 0 to -4.5 V		6		ns
Rise Time ^{*1,*2}	tr	ID = -1 A		4		
Turn-off Delay Time ^{*1,*2}	td(off)	VDD = -6 V, VGS = -4.5 to 0 V		63		
Fall Time ^{*1,*2}	tf	ID = -1 A		46		
Total Gate Charge ^{*1}	Qg	VDD = -6 V, VGS = -4.5 V ID = -1 A		10.7		nC
Gate-source Charge ^{*1}	Qgs			1.4		
Gate-drain Charge ^{*1}	Qgd			2.1		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

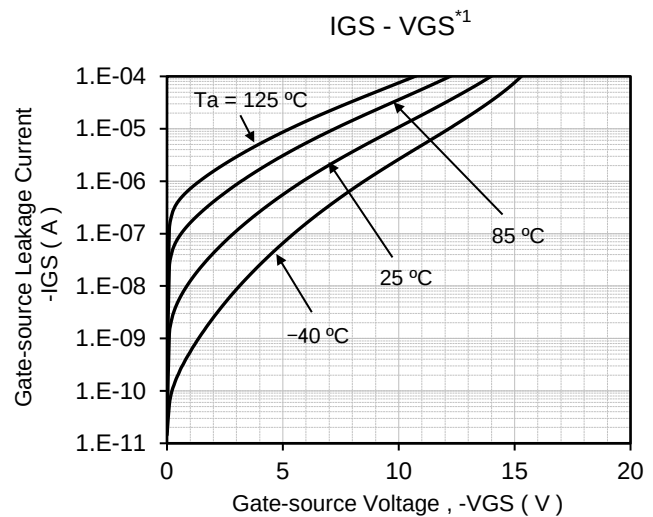
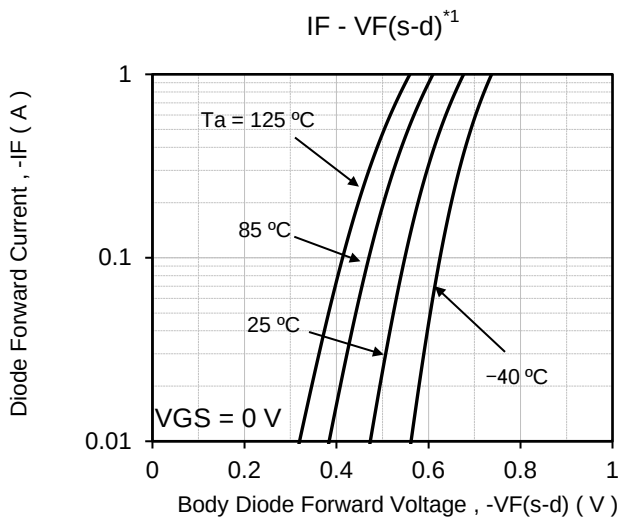
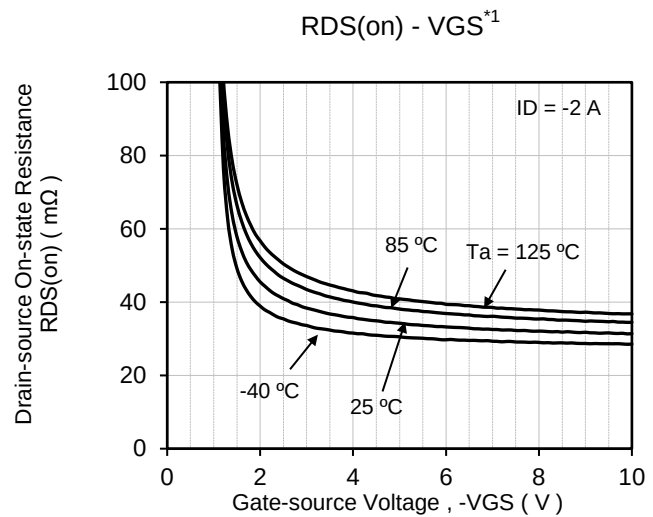
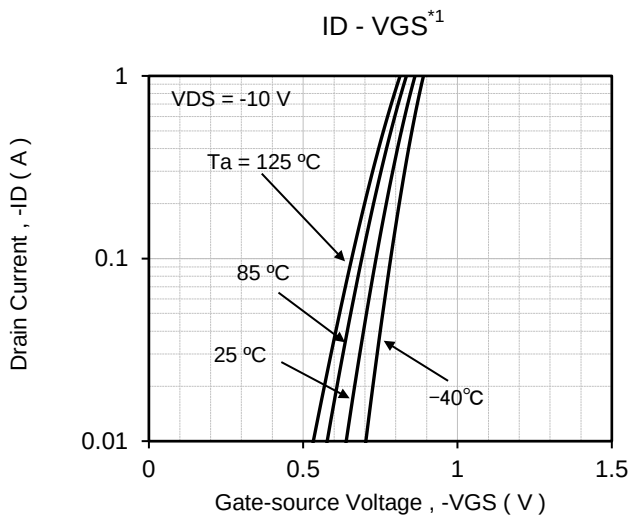
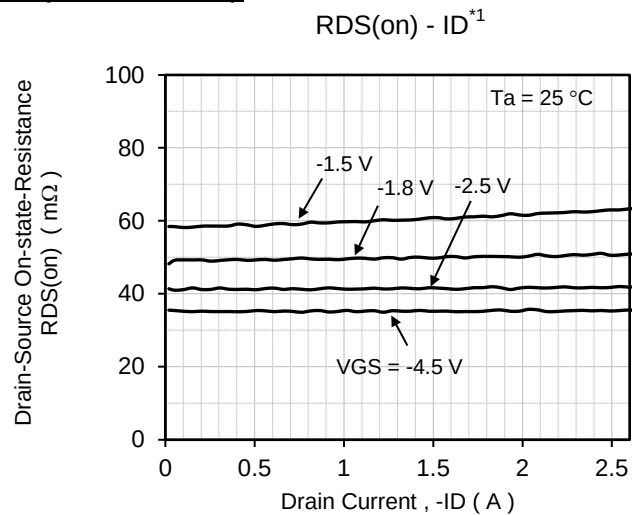
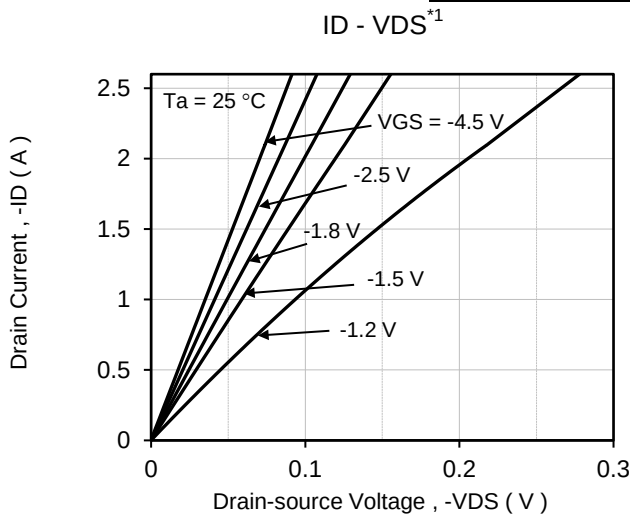
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



■ Electrical State Discharge Characteristics

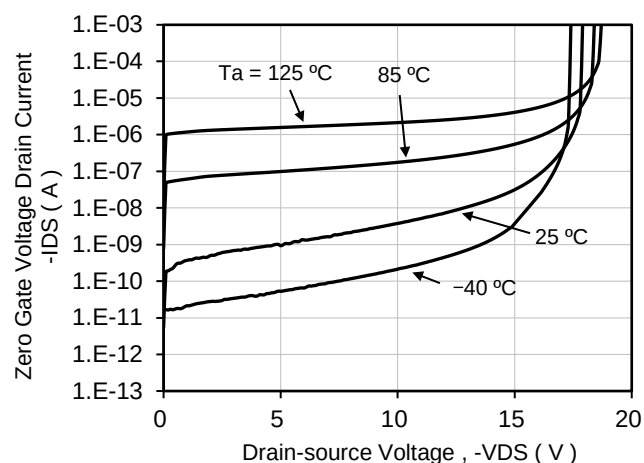
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H1C	> 1k to ≤ 2k	V
	Machine Model	MM	C = 200 pF, R = 0 Ω	M2	> 100 to ≤ 200	V

Technical Data (reference)

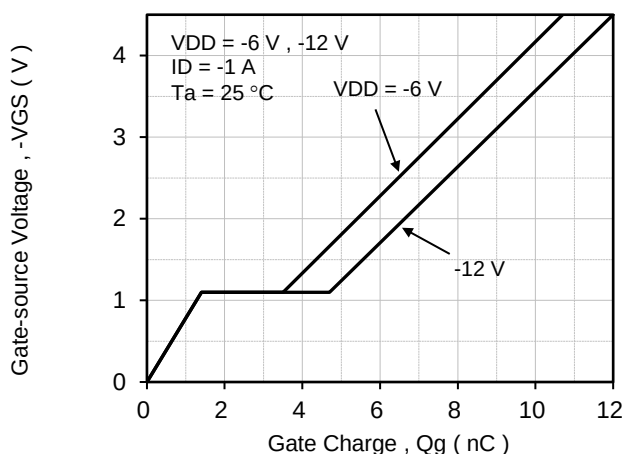


Technical Data (reference)

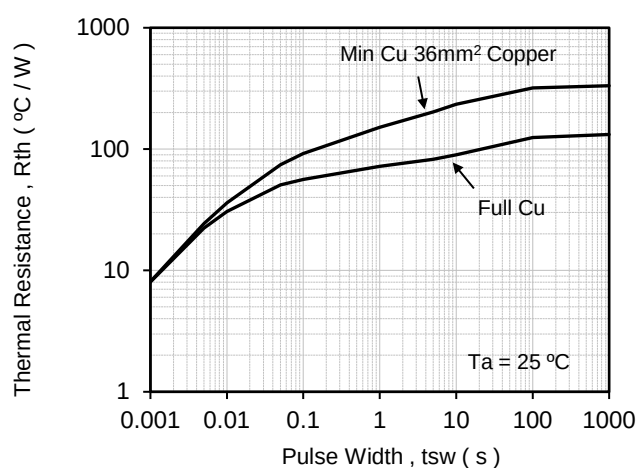
$I_{DS} - V_{DS}^{*1}$



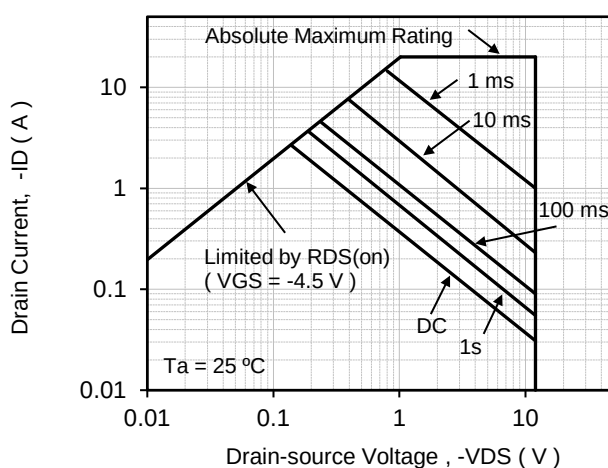
Dynamic Input / Output Characteristics



$R_{th} - t_{sw}^{*2*3}$



Safe Operating Area^{*2}



Note

*1 Pulse measurement

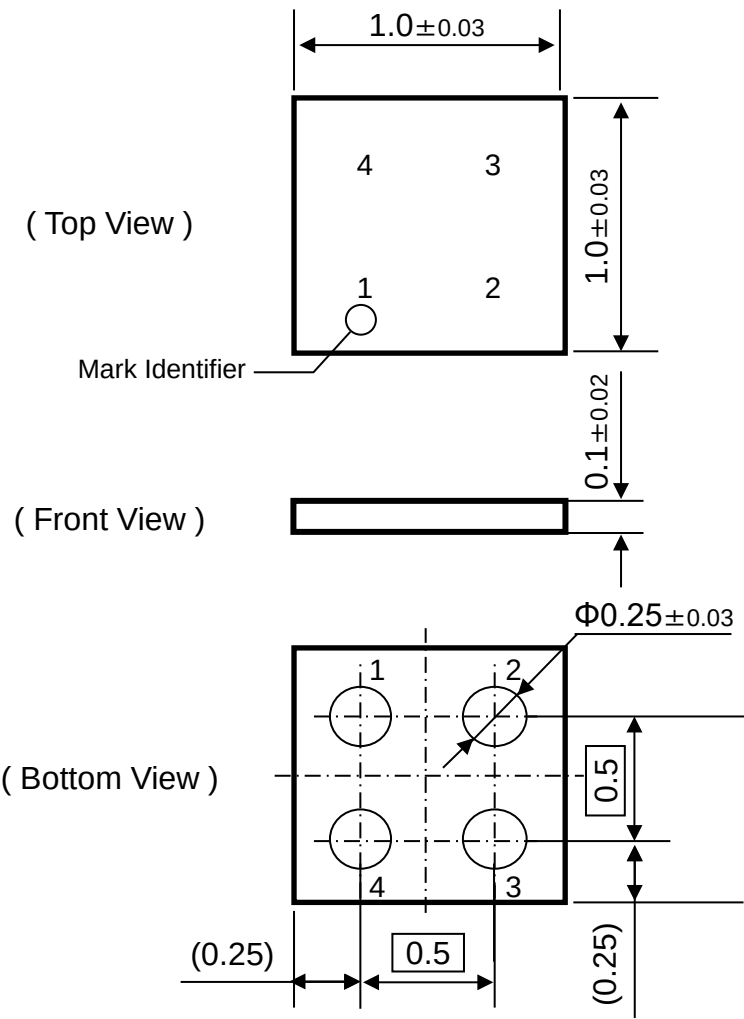
*2 FR4 board (25.4mm×25.4mm×t1.0mm), Min Cu 36mm² Copper.

*3 FR4 board (25.4mm×25.4mm×t1.0mm), Full Cu.



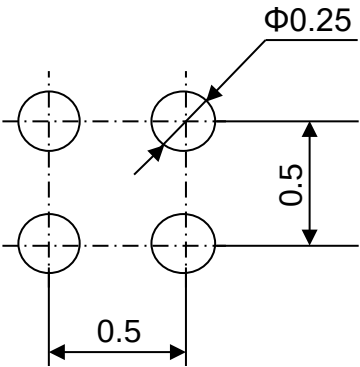
■ Outline

Unit: mm



■ Land & Stencil Pattern (Reference)

Unit: mm



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