

FEATURES

EEMBC ULPMark™-CP score: 245.5
Ultra low power active and hibernate mode
Active mode dynamic current: 30 μ A/MHz (typical)
Flexi mode: 300 μ A (typical)
Hibernate mode: 750 nA (typical)
Shutdown mode: 60 nA (typical)
ARM Cortex-M3 processor with MPU
Up to 26 MHz with serial wire debug interface
Power management
 Single-supply operation (V_{BAT}): 1.74 V to 3.6 V
 Optional buck converter for improved efficiency
Memory options
 128 kB/256 kB of embedded flash memory with ECC
 4 kB of cache memory to reduce active power
 64 kB of configurable system SRAM with parity up to 32 kB of SRAM retained in hibernate mode
Safety
 Watchdog with dedicated on-chip oscillator
 Hardware CRC with programmable polynomial
 Multiparity bit protected SRAM
 ECC protected embedded flash
Security
 TRNG
 User code protection
 Hardware cryptographic accelerator supporting AES-128, AES-256, and SHA-256

Digital peripherals

3 SPI interfaces to enable glueless interface to sensors, radios, and converters
 I²C and UART interfaces
 SPORT for natively interfacing with converters and radios
 Programmable GPIOs (44 in LFCSP and 34 in WLCSP)
 3 general-purpose timers with PWM support
 RTC and FLEX_RTC with SensorStrobe and time stamping
 Programmable beeper
 25-channel DMA controller
Clocking features
 26 MHz clock: on-chip oscillator, external crystal oscillator
 32 kHz clock: on-chip oscillator, low power crystal oscillator
 Integrated PLL with programmable divider

Analog peripherals

12-bit SAR ADC, 1.8 MSPS, 8 channels, and digital comparator

APPLICATIONS

Internet of Things (IoT)
 Electronic shelf label (ESL) and signage
 Smart infrastructure
 Smart lock
 Asset tracking
 Smart machine, smart metering, smart building, smart city, and smart agriculture
 Wearables
 Fitness and clinical
 Machine learning and neural network

FUNCTIONAL BLOCK DIAGRAM

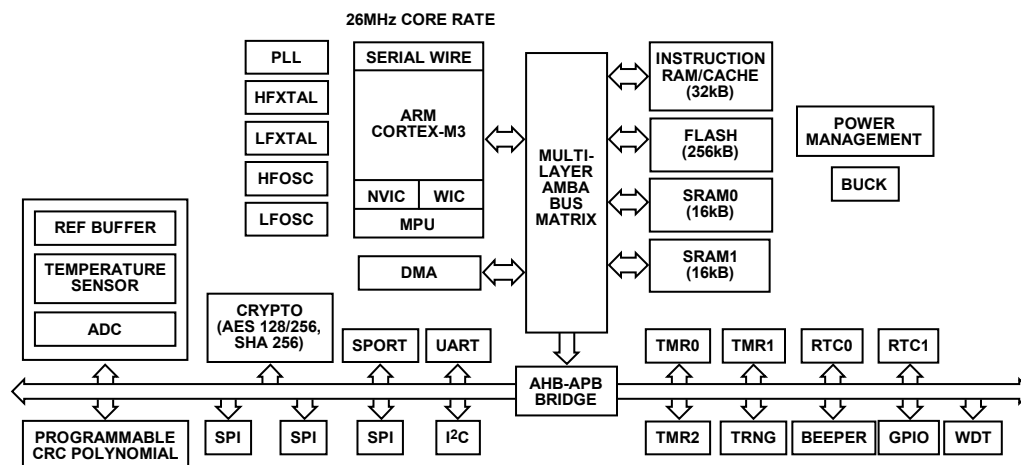


Figure 1.

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Rev. B

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| REVISION HISTORY | | | |
| 5/2019—Rev. A to Rev. B | | | |
| Change to Features Section | 1 | Change to MMRs (Peripheral Control and Status) Section | 23 |
| Changes to General Description Section | 3 | Changes to Cache Controller Section and Booting Section | 24 |
| Change to VBAT_ADC Current (I_{VBAT_ADC}) Parameter, Table 7 | 7 | Changes to Programmable GPIOs Section | 26 |
| Added Crystal Equivalent Series Resistance Parameter, Table 8 | 8 | Changes to I ² C Section | 28 |
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| Changes to Figure 5 and Figure 6 | 10 | Changes to Figure 26 | 33 |
| Changed Timer PWM_OUT Cycle Timing Section to Timer Pulse-Width Modulation (PWM) Output Cycle Timing Section | 14 | Changes to Figure 27 | 34 |
| Change to Figure 13 Caption | 14 | Changes to Figure 28 | 35 |
| Change to Table 19 | 15 | Added About ADuCM3027/ADuCM3029 Silicon Anomalies Section, Table 30, Table 31, and Table 32; Renumbered Sequentially | 36 |
| Changes to Figure 14 and Table 20 | 16 | Added Table 33 | 37 |
| Changes to Figure 15 and Table 21 | 18 | Changes to Ordering Guide | 39 |
| Changes to Figure 16 to Figure 19 | 20 | | |
| Changes to Figure 20 and Figure 21 | 21 | | |
| | | 12/2018—Revision A: Initial Version | |

GENERAL DESCRIPTION

The ADuCM3027/ADuCM3029 microcontroller units (MCUs) are ultra low power microcontroller systems with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM® Cortex®-M3 processor, a collection of digital peripherals, embedded SRAM and flash memory, and an analog subsystem which provides clocking, reset, and power management capability in addition to an analog-to-digital converter (ADC) subsystem. For a feature comparison across the ADuCM3027/ADuCM3029 product offerings, see Table 1.

Table 1. Product Flash Memory Options

| Device | Embedded Flash Memory Size |
|-----------|----------------------------|
| ADuCM3029 | 256 kB |
| ADuCM3027 | 128 kB |

System features that are common across the ADuCM3027/ADuCM3029/ADuCM3029-1/ADuCM3029-2 MCUs include the following:

- Up to 26 MHz ARM Cortex-M3 processor
- Up to 256 kB of embedded flash memory with error correction code (ECC)
- Optional 4 kB cache for lower active power
- 64 kB system SRAM with parity
- Power management unit (PMU)
- Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
- Central direct memory access (DMA) controller
- Beeper interface
- Serial port (SPORT), serial peripheral interface (SPI), inter-integrated circuit (I²C), and universal asynchronous receiver/transmitter (UART) peripheral interfaces
- Cryptographic hardware support with advanced encryption standard (AES) and secure hash algorithm (SHA)-256
- Real-time clock (RTC)
- General-purpose and watchdog timers
- Programmable general-purpose input/output (GPIO) pins
- Hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial
- Power-on reset (POR) and power supply monitor (PSM)
- 12-bit successive approximation register (SAR) ADC
- True random number generator (TRNG)

To support low dynamic and hibernate power management, the ADuCM3027/ADuCM3029 MCUs provide a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

The ADuCM3029-1 and ADuCM3029-2 MCU models share the same features and functionality as that of the ADuCM3029 MCU. All specifications pertaining to the ADuCM3027 and ADuCM3029 are also applicable to the ADuCM3029-1 and ADuCM3029-2.

For full details on the ADuCM3027/ADuCM3029 MCUs, refer to the [ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference Manual](#).

PRODUCT HIGHLIGHTS

1. Industry leading ultralow power consumption.
2. Robust operation, including full voltage monitoring in deep sleep modes, ECC support on flash, and parity error detection on SRAM memory.
3. Leading edge security. Fast encryption provides read protection to customer algorithms. Write protection prevents device reprogramming by unauthorized code.
4. Failure detection of 32 kHz LFXTAL via interrupt.
5. SensorStrobe™ for precise time synchronized sampling of external sensors. Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the [ADXL363](#) accelerometer. Software intervention is not required after setup. No pulse drift due to software execution.

SPECIFICATIONS

OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|----------------------|------|------|------|------|--|
| EXTERNAL BATTERY SUPPLY VOLTAGE ^{1,2} | V _{BAT} | 1.74 | 3.0 | 3.6 | V | |
| INPUT VOLTAGE | | | | | | |
| High Level | V _{IH} | 2.5 | | | V | V _{BAT} = 3.6 V |
| Low Level | V _{IL} | | | 0.45 | V | V _{BAT} = 1.74 V |
| ADC SUPPLY VOLTAGE | V _{BAT_ADC} | 1.74 | 3.0 | 3.6 | V | |
| OUTPUT VOLTAGE ³ | | | | | | |
| High Level | V _{OH} | 1.4 | | | V | V _{BAT} = 1.74 V, I _{OH} = -1.0 mA |
| Low Level | V _{OL} | | | 0.4 | V | V _{BAT} = 1.74 V, I _{OL} = 1.0 mA |
| INPUT CURRENT PULL-UP ⁴ | | | | | | |
| High Level | I _{IHPU} | | 0.01 | 0.2 | μA | V _{BAT} = 3.6 V, V _{IN} = 3.6 V |
| Low Level | I _{ILPU} | | | 100 | μA | V _{BAT} = 3.6 V, V _{IN} = 0 V |
| THREE-STATE LEAKAGE CURRENT | | | | | | |
| High Level ⁵ | I _{OZH} | | 0.01 | 0.15 | μA | V _{BAT} = 3.6 V, V _{IN} = 3.6 V |
| Pull-Up ⁶ | I _{OZHPU} | | | 0.30 | μA | V _{BAT} = 3.6 V, V _{IN} = 3.6 V |
| Pull-Down ⁷ | I _{OZHDP} | | | 100 | μA | V _{BAT} = 3.6 V, V _{IN} = 3.6 V |
| Low Level ⁵ | I _{OZL} | | 0.01 | 0.15 | μA | V _{BAT} = 3.6 V, V _{IN} = 0 V |
| Pull-Up ⁶ | I _{OZLPU} | | | 100 | μA | V _{BAT} = 3.6 V, V _{IN} = 0 V |
| Pull-Down ⁷ | I _{OZLPD} | | | 0.15 | μA | V _{BAT} = 3.6 V, V _{IN} = 0 V |
| INPUT CAPACITANCE | C _{IN} | | 10 | | pF | T _J = 25°C |
| JUNCTION TEMPERATURE | T _J | -40 | | +85 | °C | T _{AMBIENT} = -40°C to +85°C |

¹ Value applies to VBAT_ANA1, VBAT_ANA2, VBAT_DIG1, and VBAT_DIG2 pins.

² Must remain powered (even if the associated function is not used).

³ Applies to the output and bidirectional pins: P0_00 to P0_15, P1_00 to P1_15, and P2_00 to P2_11.

⁴ Applies to the SYS_HWRST input pin with pull-up.

⁵ Applies to the three-state pins: P0_00 to P0_05, P0_08 to P0_15, P1_00 to P1_15, and P2_00 to P2_11.

⁶ Applies to the three-state pins with pull-ups: P0_00 to P0_05, P0_07 to P0_15, and P1_00 to P1_11.

⁷ Applies to the P0_06 three-state pin with pull-down.

EMBEDDED FLASH SPECIFICATIONS

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------|--------|--------|-----|-----|--------|--------------------------|
| FLASH | | | | | | |
| Endurance | | 10,000 | | | Cycles | |
| Data Retention | | | 10 | | Years | |

POWER SUPPLY CURRENT SPECIFICATIONS**Active Mode**

Table 4.

| Parameter | Min | Typ ¹ | Max ² | Unit | Test Conditions/Comments |
|--------------------------|------|------------------|------------------|---|---|
| ACTIVE MODE ³ | | | | | Current consumption when V _{BAT} = 3.0 V |
| Buck Enabled | 0.40 | 2.71 | | mA | Code executing from flash, cache enabled, peripheral clocks off, HCLK = 6.5 MHz |
| | 0.98 | 1.29 | | mA | Code executing from flash, cache enabled, peripheral clocks off, HCLK = 26 MHz |
| Dynamic Current | 1.28 | 1.64 | | mA | Code executing from flash, cache disabled, peripheral clocks off, HCLK = 26 MHz |
| | 0.95 | 1.36 | | mA | Code executing from SRAM, peripheral clocks off, HCLK = 26 MHz |
| | 1.08 | 1.43 | | mA | Code executing from flash, cache enabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz |
| | 1.37 | 1.78 | | mA | Code executing from flash, cache disabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz |
| | 1.08 | 1.49 | | mA | Code executing from SRAM, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz |
| | 30 | | | μA/MHz | Code executing from flash, cache enabled |
| | 1.75 | 8.05 | | mA | Code executing from flash, cache enabled, peripheral clocks off, HCLK = 26 MHz |
| | 2.34 | 3.0 | | mA | Code executing from flash, cache disabled, peripheral clocks off, HCLK = 26 MHz |
| | 1.78 | 2.48 | | mA | Code executing from SRAM, peripheral clocks off, HCLK = 26 MHz |
| | 1.99 | 2.67 | | mA | Code executing from flash, cache enabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz |
| 2.55 | 3.29 | | mA | Code executing from flash, cache disabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | |
| 2.03 | 2.74 | | mA | Code executing from SRAM, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | |
| 60 | | | μA/MHz | Code executing from flash, cache enabled | |

¹ T_J = 25°C.² T_J = 85°C.³ The code being executed is a prime number generation in a continuous loop, with HFOSC as the system clock source.**Flexi Mode**

Table 5.

| Parameter | Min | Typ ¹ | Max ² | Unit | Test Conditions/Comments |
|---------------|------|------------------|------------------|------|---|
| FLEXI™ MODE | | | | | Current consumption when V _{BAT} = 3.0 V |
| Buck Enabled | 0.3 | 0.67 | | mA | Peripheral clocks off |
| | 0.39 | 0.80 | | mA | Peripheral clocks on, PCLK = 26 MHz |
| Buck Disabled | 0.52 | 1.11 | | mA | Peripheral clocks off |
| | 0.7 | 1.38 | | mA | Peripheral clocks on, PCLK = 26 MHz |

¹ T_J = 25°C.² T_J = 85°C.

Deep Sleep Modes— $V_{BAT} = 3.0\text{ V}$

Table 6.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------------------|-----|-------|-------|---------------|--|
| HIBERNATE MODE | | | | | $V_{BAT} = 3.0\text{V}$ |
| $T_J = 25^\circ\text{C}$ | | 0.75 | | μA | RTC1 and RTC0 disabled, 8 kB SRAM retained, LFX TAL off |
| | | 0.77 | | μA | RTC1 and RTC0 disabled, 16 kB SRAM retained, LFX TAL off |
| | | 0.79 | | μA | RTC1 and RTC0 disabled, 24 kB SRAM retained, LFX TAL off |
| | | 0.81 | | μA | RTC1 and RTC0 disabled, 32 kB SRAM retained, LFX TAL off |
| | | 0.78 | | μA | RTC1 enabled, 8 kB SRAM retained, LFO SC as source for RTC1 |
| | | 0.83 | | μA | RTC1 enabled, 8 kB SRAM retained, LFX TAL as source for RTC1 |
| | | 0.93 | | μA | RTC1 and RTC0 enabled, 8 kB SRAM retained, LFX TAL as source for RTC1 and RTC0 |
| $T_J = 85^\circ\text{C}$ | | 2.0 | 6.05 | μA | RTC1 and RTC0 disabled, 8 kB SRAM retained, LFX TAL off |
| | | 2.4 | 6.4 | μA | RTC1 and RTC0 disabled, 16 kB SRAM retained, LFX TAL off |
| | | 2.6 | 6.75 | μA | RTC1 and RTC0 disabled, 24 kB SRAM retained, LFX TAL off |
| | | 3.0 | 7.1 | μA | RTC1 and RTC0 disabled, 32 kB SRAM retained, LFX TAL off |
| | | 2.05 | 6.1 | μA | RTC1 enabled, 8 kB SRAM retained, LFO SC as source for RTC1 |
| | | 2.1 | 6.15 | μA | RTC1 enabled, 8 kB SRAM retained, LFX TAL as source for RTC1 |
| | | 2.25 | 6.3 | μA | RTC1 and RTC0 enabled, 8 kB SRAM retained, LFX TAL as source for RTC1 and RTC0 |
| SHUTDOWN MODE ¹ | | | | | $V_{BAT} = 3.0\text{ V}$ |
| $T_J = 25^\circ\text{C}$ | | 0.31 | | μA | RTC0 enabled, LFX TAL as source for RTC0 |
| | | 0.056 | | μA | RTC0 disabled |
| $T_J = 85^\circ\text{C}$ | | 0.49 | 1.180 | μA | RTC0 enabled, LFX TAL as source for RTC0 |
| | | 0.26 | 0.95 | μA | RTC0 disabled |

¹ Buck enable/disable does not affect power consumption.

ADC SPECIFICATIONS

Table 7.

| Parameter ^{1, 2} | Min | Typ ³ | Max | Unit | Test Conditions/Comments |
|--|------|------------------|-------|------|---|
| INTEGRAL NONLINEARITY ERROR | | | | | |
| 64-Lead LFCSP | | ±1.6 | | LSB | 1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴ |
| 64-Lead LFCSP | | ±1.4 | | LSB | 3.0 V (V _{BAT})/2.5 V (internal/external V _{REF}) ⁴ |
| 54-Ball WLCSP | | ±1.8 | | LSB | 1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴ |
| DIFFERENTIAL NONLINEARITY ERROR | | | | | |
| 64-Lead LFCSP | | -0.7 to +1.15 | | LSB | 1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴ |
| 64-Lead LFCSP | | -0.7 to +1.1 | | LSB | 3.0 V (V _{BAT})/2.5 V (internal/external V _{REF}) ⁴ |
| 54-Ball WLCSP | | -0.75 to +1.2 | | LSB | 1.8 V (V _{BAT})/1.25 V (internal/external V _{REF}) ⁴ |
| OFFSET ERROR | | | | | |
| 64-Lead LFCSP | | ±0.5 | | LSB | 1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴ |
| 64-Lead LFCSP | | ±0.5 | | LSB | 3.0 V (V _{BAT})/2.5 V (external V _{REF}) ⁴ |
| 54-Ball WLCSP | | ±0.5 | | LSB | 1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴ |
| GAIN ERROR | | | | | |
| 64-Lead LFCSP | | ±2.5 | | LSB | 1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴ |
| 64-Lead LFCSP | | ±0.5 | | LSB | 3.0 V (V _{BAT})/2.5 V (external V _{REF}) ⁴ |
| 54-Ball WLCSP | | ±3.0 | | LSB | 1.8 V (V _{BAT})/1.25 V (external V _{REF}) ⁴ |
| VBAT_ADC CURRENT (I _{VBAT_ADC}) ⁵ | | | | | |
| 64-Lead LFCSP | | 104 | | µA | 1.8 V (V _{BAT})/1.25 V (internal V _{REF}) ⁶ |
| 64-Lead LFCSP | | 131 | | µA | 3.0 V (V _{BAT})/2.5 V (internal V _{REF}) ⁶ |
| 54-Ball WLCSP | | 108 | | µA | 1.8 V (V _{BAT})/1.25 V (internal V _{REF}) ⁶ |
| INTERNAL REFERENCE VOLTAGE | | | | | |
| | | 1.25 | | V | Internal reference, 1.25 V selected |
| | | 2.50 | | V | Internal reference, 2.5 V selected |
| INTEGRAL NONLINEARITY ERROR | | | | | |
| 64-Lead LFCSP | 1.22 | 1.25 | 1.275 | V | 1.25 V (internal) ⁷ |
| 64-Lead LFCSP | 2.45 | 2.5 | 2.545 | V | 2.5 V (internal) |
| 54-Ball WLCSP | 1.22 | 1.25 | 1.275 | V | 1.25 V (internal) |
| 54-Ball WLCSP | 2.45 | 2.5 | 2.545 | V | 2.5 V (internal) |
| ADC SAMPLING FREQUENCY (f _s) ⁸ | 0.01 | | 1.8 | MSPS | |

¹ The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.

² The specifications are characterized after performing internal ADC offset calibration.

³ T_J = 25°C.

⁴ f_{IN} = 1068 Hz, f_s = 100 kSPS, internal reference in low power mode, 400,000 samples end point method used.

⁵ Current consumption from VBAT_ADC supply when ADC is performing the conversion.

⁶ f_{IN} = 1068 Hz, f_s = 100 kSPS, internal reference in low power mode.

⁷ No load current, C_L = 0.1 µF and 4.7 µF, reference buffer low power mode is enabled.

⁸ Effects of analog source impedance must be considered when selecting ADC sampling frequency.

SYSTEM CLOCKS

External Crystal Oscillator Specifications

Table 8.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|----------------|-----|--------|-----|------------|--|
| LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL) | | | | | | |
| Frequency | f_{LFXTAL} | | 32,768 | | Hz | External capacitors on SYS_LFXTAL_IN and SYS_LFXTAL_OUT pins must be selected considering the printed circuit board (PCB) trace capacitance due to routing |
| External Capacitance from SYS_LFXTAL_IN Pin to Ground and from SYS_LFXTAL_OUT Pin to Ground | C_{LFXTAL} | 6 | | 10 | pF | |
| Crystal Equivalent Series Resistance | ESR_{LFXTAL} | | | 30 | k Ω | |
| HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL) | | | | | | |
| Frequency | f_{HFXTAL} | | 26 | | MHz | External capacitors on SYS_HFXTAL_IN and SYS_HFXTAL_OUT pins must be selected considering the PCB trace capacitance due to routing |
| External Capacitance from SYS_HFXTAL_IN Pin to Ground and from SYS_HFXTAL_OUT Pin to Ground | C_{HFXTAL} | | | 20 | pF | |
| Crystal Equivalent Series Resistance | ESR_{HFXTAL} | | | 50 | Ω | |

On-Chip RC Oscillator Specifications

Table 9.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|-------------|--------|--------|--------|------|
| LOW FREQUENCY RC OSCILLATOR (LFOSC) | | | | | |
| Frequency | f_{LFOSC} | 30,800 | 32,768 | 34,407 | Hz |
| HIGH FREQUENCY RC OSCILLATOR (HFOSC) | | | | | |
| Frequency | f_{HFOSC} | 25.09 | 26 | 26.728 | MHz |

System Clocks and PLL Specifications

Table 10.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|--------|-----|-----|------|
| PLL SPECIFICATIONS | | | | | |
| PLL Input Clock Frequency ¹ | f_{PLLIN} | 16 | | 26 | MHz |
| PLL Output Clock Frequency ^{2,3} | f_{PLLOUT} | 16 | | 60 | MHz |
| System Peripheral Clock (PCLK) Frequency | f_{PCLK} | 0.8125 | | 26 | MHz |
| Advanced High Performance Bus Clock (HCLK) Frequency | f_{HCLK} | 0.8125 | | 26 | MHz |

¹ The input to the PLL can come from either the high frequency external crystal (HFXTAL), SYS_CLKIN pin or from the high frequency internal RC oscillator (HFOSC).

² For the maximum value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16, PLL_DIV2 = 1 for PLL input clock = 26 MHz; and PLL_MSEL = 13, PLL_NSEL = 26, PLL_DIV2 = 1 for PLL input clock = 16 MHz.

³ For the minimum value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 30, PLL_DIV2 = 0 for PLL input clock = 26 MHz; and PLL_MSEL = 8, PLL_NSEL = 30, PLL_DIV2 = 0 for 16 MHz.

TIMING SPECIFICATIONS

Reset Timing

Table 11.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-------------------|-----|-----|-----|------|
| RESET TIMING REQUIREMENTS | | | | | |
| SYS_HWRST Asserted Pulse Width ¹ | t _{WRST} | 4 | | | μs |

¹ Applies after power-up sequence is complete.

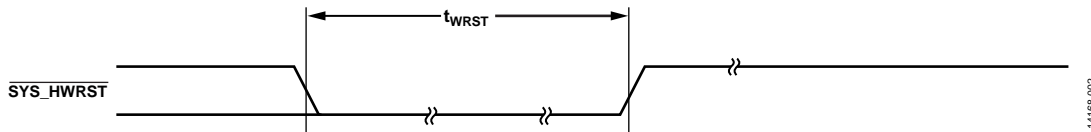


Figure 2. Reset Timing

Serial Ports Timing

Table 12.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|---------------------|------------------------------|-----|-----|------|---|
| EXTERNAL CLOCK SERIAL PORTS | | | | | | |
| Timing Requirements | | | | | | |
| Frame Sync Setup Before SPT_CLK ¹ | t _{SFSE} | 5 | | | ns | Externally generated frame sync in transmit or receive mode |
| Frame Sync Hold After SPT_CLK ¹ | t _{HFSE} | 5 | | | ns | Externally generated frame sync in transmit or receive mode |
| Receive Data Setup Before Receive SPT_CLK ¹ | t _{SDRE} | 5 | | | ns | |
| Receive Data Hold After SPT_CLK ¹ | t _{HDRE} | 8 | | | ns | |
| SPT_CLK Width ² | t _{SCLKW} | 38.5 | | | ns | |
| SPT_CLK Period ² | t _{SPTCLK} | 77 | | | ns | |
| Switching Characteristics ³ | | | | | | |
| Frame Sync Delay After SPT_CLK | t _{DFSE} | | | 20 | ns | Internally generated frame sync in transmit or receive mode |
| Frame Sync Hold After SPT_CLK | t _{HOFSE} | 2 | | | ns | Internally generated frame sync in transmit or receive mode |
| Transmit Data Delay After Transmit SPT_CLK | t _{DDTE} | | | 20 | ns | |
| Transmit Data Hold After Transmit SPT_CLK | t _{HDTE} | 1 | | | ns | |
| INTERNAL CLOCK SERIAL PORTS | | | | | | |
| Timing Requirements ¹ | | | | | | |
| Receive Data Setup Before SPT_CLK | t _{SDRI} | 25 | | | ns | |
| Receive Data Hold After SPT_CLK | t _{HDRI} | 0 | | | ns | |
| Switching Characteristics | | | | | | |
| Frame Sync Delay After SPT_CLK ³ | t _{DFSI} | | | 20 | ns | Internally generated frame sync in transmit or receive mode |
| Frame Sync Hold After SPT_CLK ³ | t _{HOFSI} | -8 | | | ns | Internally generated frame sync in transmit or receive mode |
| Transmit Data Delay After SPT_CLK ³ | t _{DDTI} | | | 20 | ns | |
| Transmit Data Hold After SPT_CLK ³ | t _{HDTI} | -7 | | | ns | |
| SPT_CLK Width | t _{SCLKIW} | t _{PCLK} - 1.5 | | | ns | |
| SPT_CLK Period | t _{SPTCLK} | (2 × t _{PCLK}) - 1 | | | ns | Not shown in Figure 3 to Figure 7 |
| ENABLE AND THREE-STATE SERIAL PORTS | | | | | | |
| Switching Characteristics | | | | | | |
| Data Enable from Internal Transmit SPT_CLK ³ | t _{DDTIN} | 5 | | | ns | |
| Data Disable from Internal Transmit SPT_CLK ³ | t _{DDTTI} | | | 160 | ns | |

¹ This specification is referenced to the sample edge.

² This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.

³ These specifications are referenced to the drive edge.

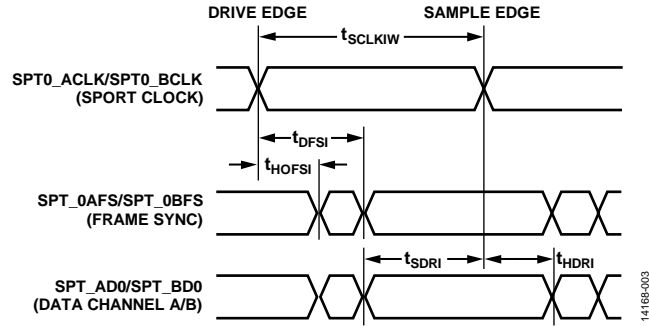


Figure 3. Serial Ports (Data Receive Mode through Internal Clock)

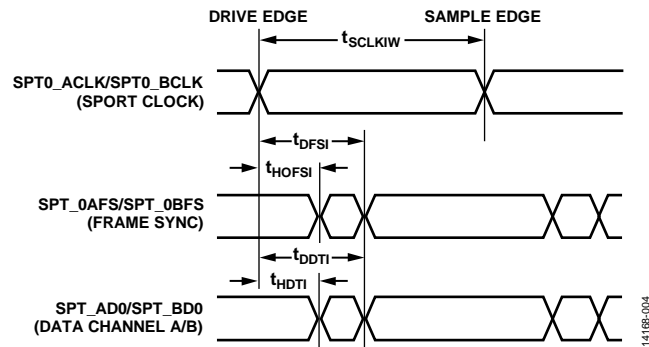


Figure 4. Serial Ports (Data Transmit Mode through Internal Clock)

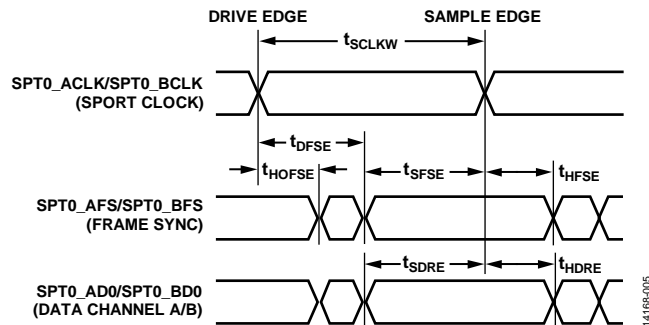


Figure 5. Serial Ports (Data Receive Mode through External Clock)

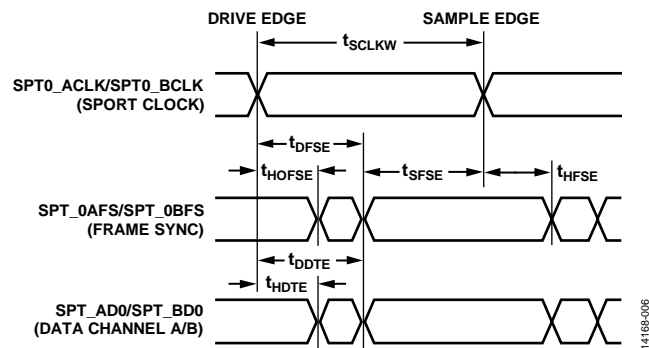


Figure 6. Serial Ports (Data Transmit Mode through External Clock)

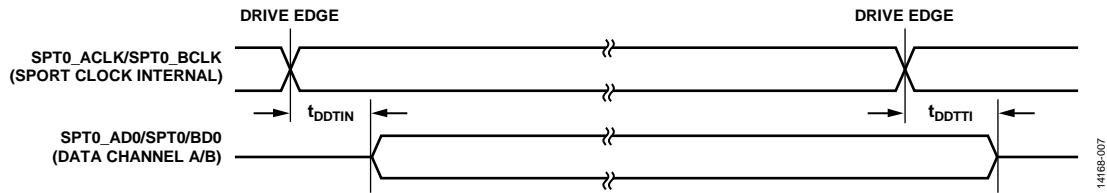


Figure 7. Enable and Three-State Serial Ports

14168E-007

SPI Timing

Table 13.

| Parameter ¹ | Symbol | Min | Typ | Max | Unit |
|---|------------|-----------------------------|-----|-----|------|
| SPI MASTER MODE TIMING | | | | | |
| Timing Requirements | | | | | |
| Chip Select (\overline{CS}) to Serial Clock (SCLK) Edge | t_{CS} | $(0.5 \times t_{PCLK}) - 3$ | | | ns |
| SCLK Low Pulse Width | t_{SL} | $t_{PCLK} - 3.5$ | | | ns |
| SCLK High Pulse Width | t_{SH} | $t_{PCLK} - 3.5$ | | | ns |
| Data Input Setup Time Before SCLK Edge | t_{DSU} | 5 | | | ns |
| Data Input Hold Time After SCLK Edge | t_{DHD} | 20 | | | ns |
| Switching Characteristics | | | | | |
| Data Output Valid After SCLK Edge | t_{DAV} | | | 25 | ns |
| Data Output Setup Before SCLK Edge | t_{DOSU} | $t_{PCLK} - 2.2$ | | | ns |
| \overline{CS} High After SCLK Edge | t_{SFS} | $(0.5 \times t_{PCLK}) - 3$ | | | ns |
| SPI SLAVE MODE TIMING | | | | | |
| Timing Requirements | | | | | |
| \overline{CS} to SCLK Edge | t_{CS} | 38.5 | | | ns |
| SCLK Low Pulse Width | t_{SL} | 38.5 | | | ns |
| SCLK High Pulse Width | t_{SH} | 38.5 | | | ns |
| Data Input Setup Time Before SCLK Edge | t_{DSU} | 6 | | | ns |
| Data Input Hold Time After SCLK Edge | t_{DHD} | 8 | | | ns |
| Switching Characteristics | | | | | |
| Data Output Valid After SCLK Edge | t_{DAV} | | | 20 | ns |
| Data Output Valid After \overline{CS} Edge | t_{DOCS} | | | 20 | ns |
| \overline{CS} High After SCLK Edge | t_{SFS} | 38.5 | | | ns |

¹ These specifications are characterized with respect to double drive strength.

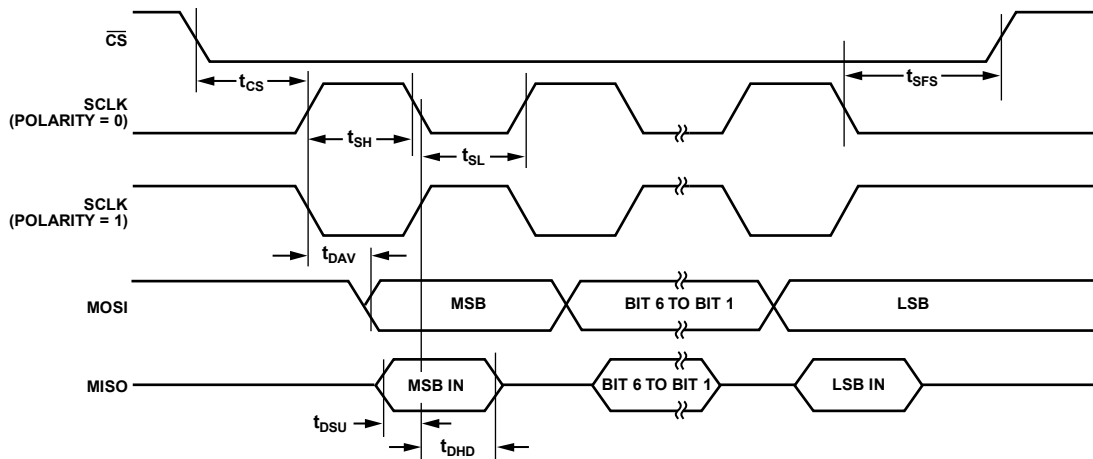


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

14168-008

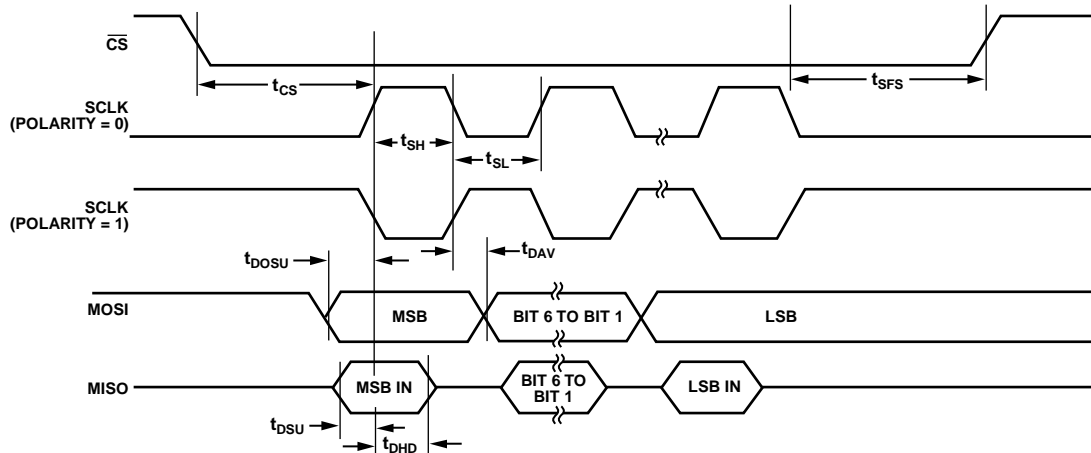


Figure 9. SPI Master Mode Timing (Phase = 0)

14168-009

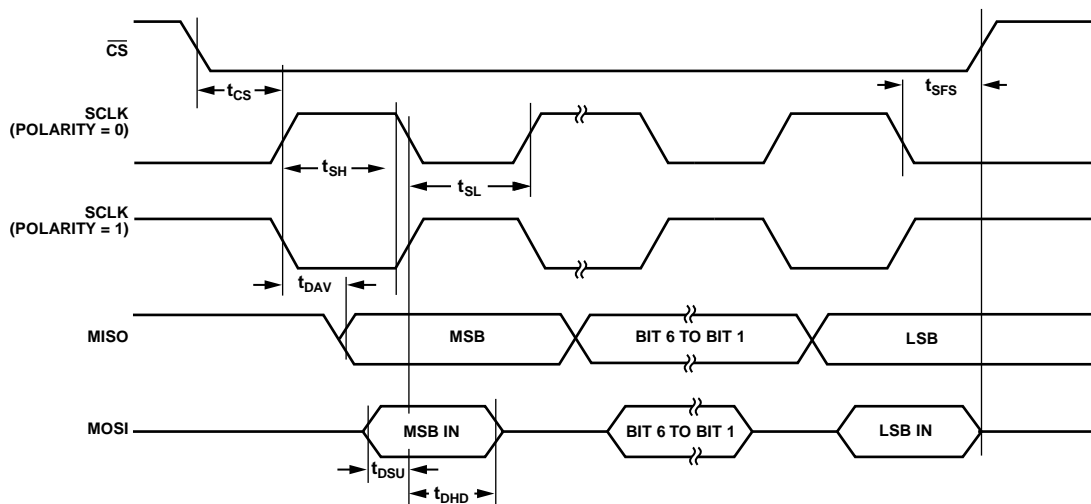


Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

14168-010

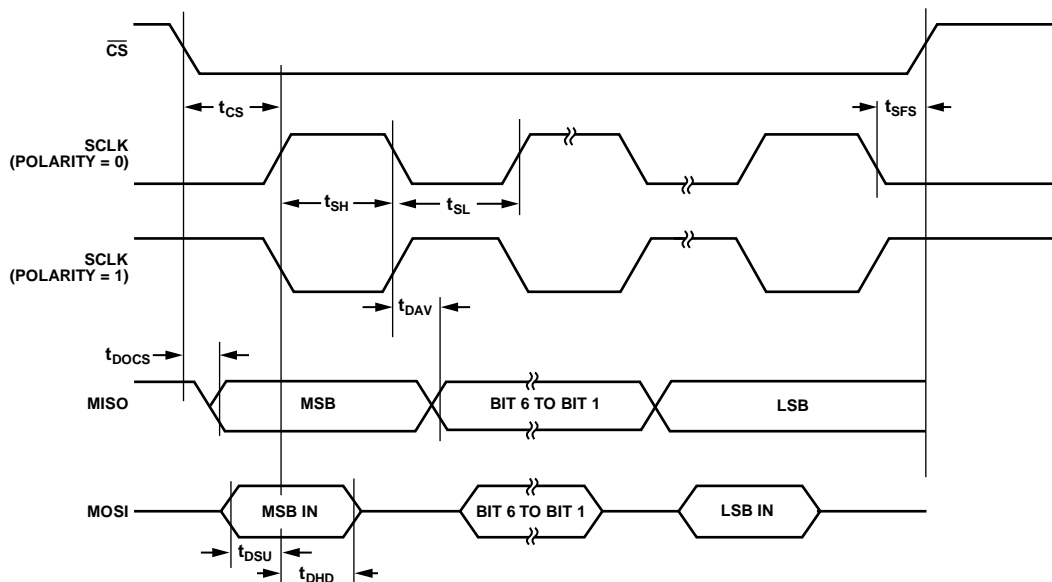


Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

14168-011

I²C Specifications

Table 14.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|--------|-----|-----|-----|------|
| I ² C SCLK FREQUENCY | | | | | |
| Standard Mode | | | 100 | | kHz |
| Fast Mode | | | 400 | | kHz |

General-Purpose Port Timing

Table 15.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|------------------|-----------------------|-----|-----|------|
| TIMING REQUIREMENTS | | | | | |
| General-Purpose Port Pin Input Pulse Width | t _{WFI} | 4 × t _{PCLK} | | | ns |

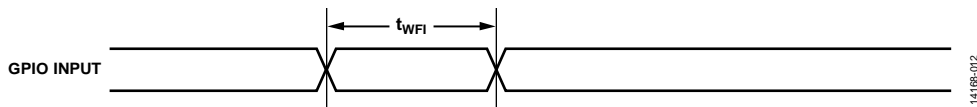


Figure 12. General-Purpose Timing

RTC1 (FLEX_RTC) Specifications

Table 16.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------|--------|-----|--------|-----|------|
| SENSORSTROBE | | | | | |
| Minimum Output Frequency | | | 0.5 | | Hz |
| Maximum Output Frequency | | | 16.384 | | kHz |
| RTC1 ALARM | | | | | |
| Minimum Time Resolution | | | 30.52 | | μs |

Timer Pulse-Width Modulation (PWM) Output Cycle Timing

Table 17.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------|-------------------|------------------------------|-----|-----------------|------|
| SWITCHING REQUIREMENTS | | | | | |
| Timer Pulse Width Output | t _{PWMO} | (4 × t _{PCLK}) – 6 | | 256 × (216 – 1) | ns |

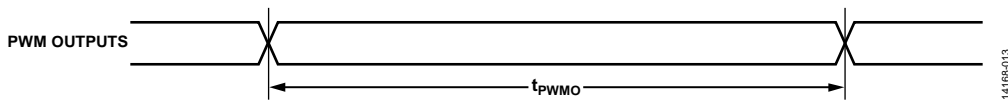


Figure 13. Timer PWM Output Cycle Timing

ABSOLUTE MAXIMUM RATINGS

Table 18.

| Parameter | Rating |
|--|-------------------|
| Supply VBAT_ANA1, VBAT_ANA2, VBAT_ADC, VBAT_DIG1, VBAT_DIG2, and VREF_ADC | –0.3 V to +3.6 V |
| Analog VDCDC_CAP1N, VDCDC_CAP1P, VDCDC_OUT, VDCDC_CAP2N, and VDCDC_CAP2P | –0.3 V to +3.6 V |
| VLDO_OUT, SYS_HFXTAL_IN, SYS_ HFXTAL_OUT, SYS_LFXTAL_IN, and SYS_LFXTAL_OUT | –0.3 V to +1.32 V |
| Digital Input/Output P0_xx, P1_xx, P2_xx, and SYS_HWRST | –0.3 V to +3.6 V |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_J is junction temperature (°C).

T_A is ambient temperature (°C).

P_D is power dissipation (to calculate power dissipation).

Table 19. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|--------------|---------------|---------------|------|
| CP-64-16 | 26.3 | 1.0 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

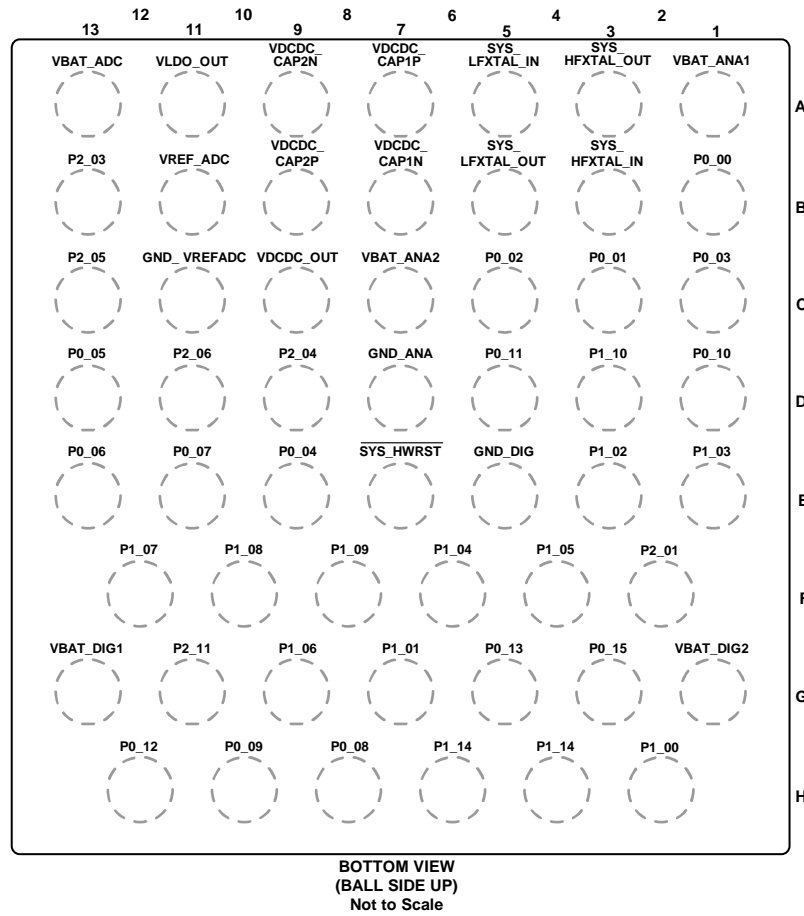
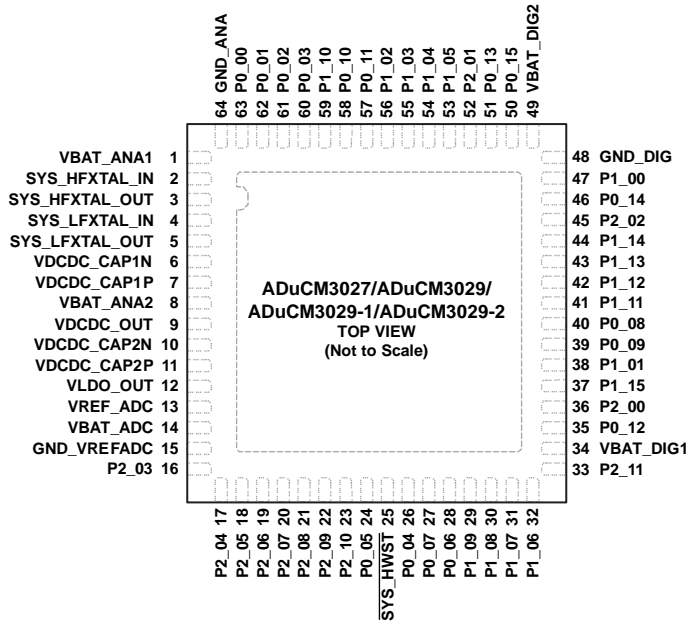


Figure 14. ADuCM3027/ADuCM3029 54-Ball WLCSP Configuration

Table 20. ADuCM3027/ADuCM3029 54-Ball WLCSP Pin Function Descriptions

| Pin No. | Mnemonic | Signal Name | Description |
|---------|----------------|--|--|
| A1 | VBAT_ANA1 | Not Applicable | External Supply for Analog Circuits in the MCU. |
| A3 | SYS_HFXTAL_OUT | Not Applicable | High Frequency Crystal Output. |
| A5 | SYS_LFXTAL_IN | Not Applicable | High Frequency Crystal Input. |
| A7 | VDCDC_CAP1P | Not Applicable | Buck Converter Capacitor 1 Positive Terminal. |
| A9 | VDCDC_CAP2N | Not Applicable | Buck Converter Capacitor 2 Negative Terminal. |
| A11 | VLDO_OUT | Not Applicable | Low Drop Out Regulator Output. This pin is only for connecting the decoupling capacitor. Do not connect this pin to the external load. |
| A13 | VBAT_ADC | Not Applicable | External Supply for Internal ADC. |
| B1 | P0_00 | SPIO_CLK/SPT0_BCLK/GPIO00 | GPIO. See the GPIO Multiplexing section for more information. |
| B3 | SYS_HFXTAL_IN | Not Applicable | High Frequency Crystal Input. |
| B5 | SYS_LFXTAL_OUT | Not Applicable | Low Frequency Crystal Output. |
| B7 | VDCDC_CAP1N | Not Applicable | Buck Converter Capacitor 1 Negative Terminal. |
| B9 | VDCDC_CAP2P | Not Applicable | Buck Converter Capacitor 2 Positive Terminal. |
| B11 | VREF_ADC | Not Applicable | External Reference Voltage for Internal ADC. |
| B13 | P2_03 | ADC0_VIN0/GPIO35 | GPIO. See the GPIO Multiplexing section for more information. |
| C1 | P0_03 | SPIO_CS0/SPT0_BCNV/ SPI2_RDY/GPIO03 | GPIO. See the GPIO Multiplexing section for more information. |
| C3 | P0_01 | SPIO_MOSI/SPT0_BFS/GPIO01 | GPIO. See the GPIO Multiplexing section for more information. |
| C5 | P0_02 | SPIO_MISO/SPT0_BD0/GPIO02 | GPIO. See the GPIO Multiplexing section for more information. |
| C7 | VBAT_ANA2 | Not Applicable | External Supply for Analog Circuits in the MCU. |

| Pin No. | Mnemonic | Signal Name | Description |
|---------|-------------|---|--|
| C9 | VDCDC_OUT | Not Applicable | Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect this pin to the external load. |
| C11 | GND_VREFADC | Not Applicable | Ground for Internal ADC. |
| C13 | P2_05 | ADC0_VIN2/GPIO37 | GPIO. See the GPIO Multiplexing section for more information. |
| D1 | P0_10 | UART0_TX/GPIO10 | GPIO. See the GPIO Multiplexing section for more information. |
| D3 | P1_10 | SPI0_CS1/SYS_CLKIN/ SPI1_CS3/GPIO26 | GPIO. See the GPIO Multiplexing section for more information. |
| D5 | P0_11 | UART0_RX/GPIO11 | GPIO. See the GPIO Multiplexing section for more information. |
| D7 | GND_ANA | Not Applicable | Ground Reference for Analog Circuits in the MCU. |
| D9 | P2_04 | ADC0_VIN1/GPIO36 | GPIO. See the GPIO Multiplexing section for more information. |
| D11 | P2_06 | ADC0_VIN3/GPIO38 | GPIO. See the GPIO Multiplexing section for more information. |
| D13 | P0_05 | I2C0_SDA/GPIO05 | GPIO. See the GPIO Multiplexing section for more information. |
| E1 | P1_03 | SPI2_MOSI/GPIO19 | GPIO. See the GPIO Multiplexing section for more information. |
| E3 | P1_02 | SPI2_CLK/GPIO18 | GPIO. See the GPIO Multiplexing section for more information. |
| E5 | GND_DIG | Not Applicable | Ground Reference for Digital Circuits in the MCU. |
| E7 | SYS_HWRST | Not Applicable | Hardware Reset Pin. |
| E9 | P0_04 | I2C0_SCL/GPIO04 | GPIO. See the GPIO Multiplexing section for more information. |
| E11 | P0_07 | GPIO07/SWD0_DATA | GPIO. See the GPIO Multiplexing section for more information. |
| E13 | P0_06 | GPIO06/SWD0_CLK | GPIO. See the GPIO Multiplexing section for more information. |
| F2 | P2_01 | XINT0_WAKE3/TMR2_OUT/GPIO33 | GPIO. See the GPIO Multiplexing section for more information. |
| F4 | P1_05 | SPI2_CS0/GPIO21 | GPIO. See the GPIO Multiplexing section for more information. |
| F6 | P1_04 | SPI2_MISO/GPIO20 | GPIO. See the GPIO Multiplexing section for more information. |
| F8 | P1_09 | SPI1_CS0/GPIO25 | GPIO. See the GPIO Multiplexing section for more information. |
| F10 | P1_08 | SPI1_MISO/GPIO24 | GPIO. See the GPIO Multiplexing section for more information. |
| F12 | P1_07 | SPI1_MOSI/GPIO23 | GPIO. See the GPIO Multiplexing section for more information. |
| G1 | VBAT_DIG2 | Not Applicable | External Supply for Digital Circuits in the MCU. |
| G3 | P0_15 | XINT0_WAKE0/GPIO15 | GPIO. See the GPIO Multiplexing section for more information. |
| G5 | P0_13 | XINT0_WAKE2/GPIO13 | GPIO. See the GPIO Multiplexing section for more information. |
| G7 | P1_01 | GPIO17/SYS_BMODE0 | GPIO. See the GPIO Multiplexing section for more information. |
| G9 | P1_06 | SPI1_CLK/GPIO22 | GPIO. See the GPIO Multiplexing section for more information. |
| G11 | P2_11 | SPI1_CS1/SYS_CLKOUT/GPIO43/ RTC1_SS1 | GPIO. See the GPIO Multiplexing section for more information. |
| G13 | VBAT_DIG1 | Not Applicable | External Supply for Digital Circuits in the MCU. |
| H2 | P1_00 | XINT0_WAKE1/GPIO16 | GPIO. See the GPIO Multiplexing section for more information. |
| H4 | P0_14 | TMR0_OUT/SPI1_RDY/GPIO14 | GPIO. See the GPIO Multiplexing section for more information. |
| H6 | P1_14 | SPI0_RDY/GPIO30 | GPIO. See the GPIO Multiplexing section for more information. |
| H8 | P0_08 | BPR0_TONE_N/GPIO08 | GPIO. See the GPIO Multiplexing section for more information. |
| H10 | P0_09 | BPR0_TONE_P/SPI2_CS1/GPIO09 | GPIO. See the GPIO Multiplexing section for more information. |
| H12 | P0_12 | SPT0_AD0/GPIO12/ UART0_SOUT_EN | GPIO. See the GPIO Multiplexing section for more information. |



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE GROUNDED.

14168-015

Figure 15. ADuCM3027/ADuCM3029/ADuCM3029-1/ADuCM3029-2 64-Lead LFCSP Configuration

Table 21. ADuCM3027/ADuCM3029/ADuCM3029-1/ADuCM3029-2, 64-Lead LFCSP Pin Function Descriptions

| Pin No. | Mnemonic | Signal Name | Description |
|---------|----------------|---------------------------|--|
| 1 | VBAT_ANA1 | Not applicable | External Supply for Analog Circuits in the MCU. |
| 2 | SYS_HFXTAL_IN | Not applicable | High Frequency Crystal Input. |
| 3 | SYS_HFXTAL_OUT | Not applicable | High Frequency Crystal Output. |
| 4 | SYS_LFXTAL_IN | Not applicable | Low Frequency Crystal Input. |
| 5 | SYS_LFXTAL_OUT | Not applicable | Low Frequency Crystal Output. |
| 6 | VDCDC_CAP1N | Not applicable | Buck Converter Capacitor 1 Negative Terminal. |
| 7 | VDCDC_CAP1P | Not applicable | Buck Converter Capacitor 1 Positive Terminal. |
| 8 | VBAT_ANA2 | Not applicable | External Supply for Analog Circuits in the MCU |
| 9 | VDCDC_OUT | Not applicable | Buck Converter Output. This pin is only for connecting the decoupling capacitor. Do not connect this pin to the external load. |
| 10 | VDCDC_CAP2N | Not applicable | Buck Converter Capacitor 2 Negative Terminal. |
| 11 | VDCDC_CAP2P | Not applicable | Buck Converter Capacitor 2 Positive Terminal. |
| 12 | VLD0_OUT | Not applicable | Low Drop Out Regulator Output. This pin is only for connecting the decoupling capacitor. Do not connect this pin to the external load. |
| 13 | VREF_ADC | Not applicable | External Reference Voltage for Internal ADC. |
| 14 | VBAT_ADC | Not applicable | External Supply for Internal ADC. |
| 15 | GND_VREFADC | Not applicable | Ground for Internal ADC. |
| 16 | P2_03 | ADC0_VIN0/GPIO35 | GPIO. See the GPIO Multiplexing section. |
| 17 | P2_04 | ADC0_VIN1/GPIO36 | GPIO. See the GPIO Multiplexing section. |
| 18 | P2_05 | ADC0_VIN2/GPIO37 | GPIO. See the GPIO Multiplexing section. |
| 19 | P2_06 | ADC0_VIN3/GPIO38 | GPIO. See the GPIO Multiplexing section. |
| 20 | P2_07 | ADC0_VIN4/SPI2_CS3/GPIO39 | GPIO. See the GPIO Multiplexing section. |
| 21 | P2_08 | ADC0_VIN5/SPI0_CS2/GPIO40 | GPIO. See the GPIO Multiplexing section. |
| 22 | P2_09 | ADC0_VIN6/SPI0_CS3/GPIO41 | GPIO. See the GPIO Multiplexing section. |
| 23 | P2_10 | ADC0_VIN7/SPI2_CS2/GPIO42 | GPIO. See the GPIO Multiplexing section. |
| 24 | P0_05 | I2C0_SDA/GPIO05 | GPIO. See the GPIO Multiplexing section. |
| 25 | SYS_HWRST | Not applicable | Hardware Reset Pin. |
| 26 | P0_04 | I2C0_SCL/GPIO04 | GPIO. See the GPIO Multiplexing section. |
| 27 | P0_07 | GPIO07/SWD0_DATA | GPIO. See the GPIO Multiplexing section. |
| 28 | P0_06 | GPIO06/SWD0_CLK | GPIO. See the GPIO Multiplexing section. |

| Pin No. | Mnemonic | Signal Name | Description |
|---------|-----------------|---|--|
| 29 | P1_09 | SPI1_CS0/GPIO25 | GPIO. See the GPIO Multiplexing section. |
| 30 | P1_08 | SPI1_MISO/GPIO24 | GPIO. See the GPIO Multiplexing section. |
| 31 | P1_07 | SPI1_MOSI/GPIO23 | GPIO. See the GPIO Multiplexing section. |
| 32 | P1_06 | SPI1_CLK/GPIO22 | GPIO. See the GPIO Multiplexing section. |
| 33 | P2_11 | SPI1_CS1/SYS_CLKOUT/GPIO43/ RTC1_SS1 | GPIO. See the GPIO Multiplexing section. |
| 34 | VBAT_DIG1 | Not applicable | External Supply for Digital Circuits in the MCU. |
| 35 | P0_12 | SPT0_AD0/GPIO12 | GPIO. See the GPIO Multiplexing section. |
| 36 | P2_00 | SPT0_AFS/GPIO32 | GPIO. See the GPIO Multiplexing section. |
| 37 | P1_15 | SPT0_ACLK/GPIO31 | GPIO. See the GPIO Multiplexing section. |
| 38 | P1_01 | GPIO17/SYS_BMODE0 | GPIO. See the GPIO Multiplexing section. |
| 39 | P0_09 | BPR0_TONE_P/SPI2_CS1/GPIO09 | GPIO. See the GPIO Multiplexing section. |
| 40 | P0_08 | BPR0_TONE_N/GPIO08 | GPIO. See the GPIO Multiplexing section. |
| 41 | P1_11 | TMR1_OUT/GPIO27 | GPIO. See the GPIO Multiplexing section. |
| 42 | P1_12 | GPIO28 | GPIO. See the GPIO Multiplexing section. |
| 43 | P1_13 | GPIO29 | GPIO. See the GPIO Multiplexing section. |
| 44 | P1_14 | SPIO_RDY/GPIO30 | GPIO. See the GPIO Multiplexing section. |
| 45 | P2_02 | SPT0_ACNV/SPI1_CS2/GPIO34 | GPIO. See the GPIO Multiplexing section. |
| 46 | P0_14 | TMR0_OUT/SPI1_RDY/GPIO14 | GPIO. See the GPIO Multiplexing section. |
| 47 | P1_00 | XINT0_WAKE1/GPIO16 | GPIO. See the GPIO Multiplexing section. |
| 48 | GND_DIG | Not applicable | Ground Reference for Digital Circuits in the MCU. |
| 49 | VBAT_DIG2 | Not applicable | External Supply for Digital Circuits in the MCU. |
| 50 | P0_15 | XINT0_WAKE0/GPIO15 | GPIO. See the GPIO Multiplexing section. |
| 51 | P0_13 | XINT0_WAKE2/GPIO13 | GPIO. See the GPIO Multiplexing section. |
| 52 | P2_01 | XINT0_WAKE3/TMR2_OUT/GPIO33 | GPIO. See the GPIO Multiplexing section. |
| 53 | P1_05 | SPI2_CS0/GPIO21 | GPIO. See the GPIO Multiplexing section. |
| 54 | P1_04 | SPI2_MISO/GPIO20 | GPIO. See the GPIO Multiplexing section. |
| 55 | P1_03 | SPI2_MOSI/GPIO19 | GPIO. See the GPIO Multiplexing section. |
| 56 | P1_02 | SPI2_CLK/GPIO18 | GPIO. See the GPIO Multiplexing section. |
| 57 | P0_11 | UART0_RX/GPIO11 | GPIO. See the GPIO Multiplexing section. |
| 58 | P0_10 | UART0_TX/GPIO10 | GPIO. See the GPIO Multiplexing section. |
| 59 | P1_10 | SPIO_CS1/SYS_CLKIN/SPI1_CS3/ GPIO26 | GPIO. See the GPIO Multiplexing section. |
| 60 | P0_03 | SPIO_CS0/SPT0_BCNV/SPI2_RDY/ GPIO03 | GPIO. See the GPIO Multiplexing section. |
| 61 | P0_02 | SPIO_MISO/SPT0_BD0/GPIO02 | GPIO. See the GPIO Multiplexing section. |
| 62 | P0_01 | SPIO_MOSI/SPT0_BFS/GPIO01 | GPIO. See the GPIO Multiplexing section. |
| 63 | P0_00 | SPIO_CLK/SPT0_BCLK/GPIO00 | GPIO. See the GPIO Multiplexing section. |
| 64 | GND_ANA EPAD | Not applicable | Ground Reference for Analog Circuits in the MCU. Exposed Pad. The exposed pad must be grounded. |

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU. The curves represent the current drive capability of the output drivers as a function of output voltage.

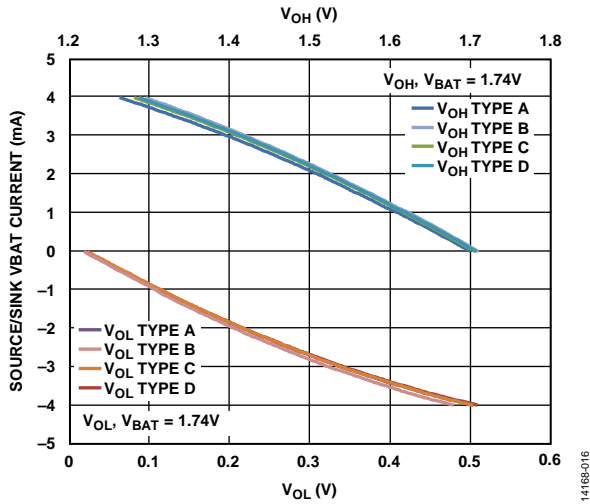


Figure 16. Output Double Drive Strength Characteristics ($V_{BAT} = 1.74 V$)

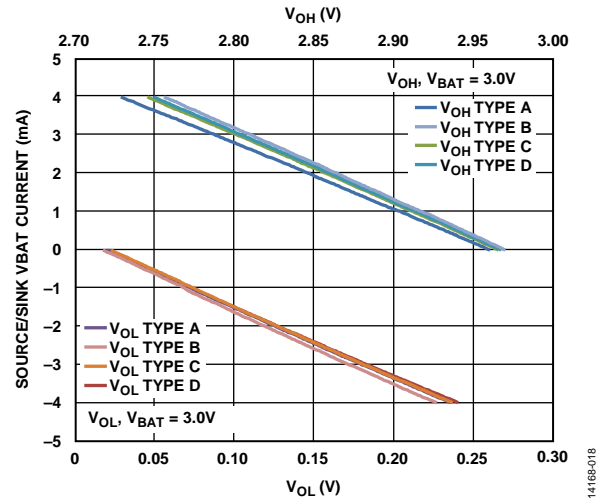


Figure 18. Output Double Drive Strength Characteristics ($V_{BAT} = 3.0 V$)

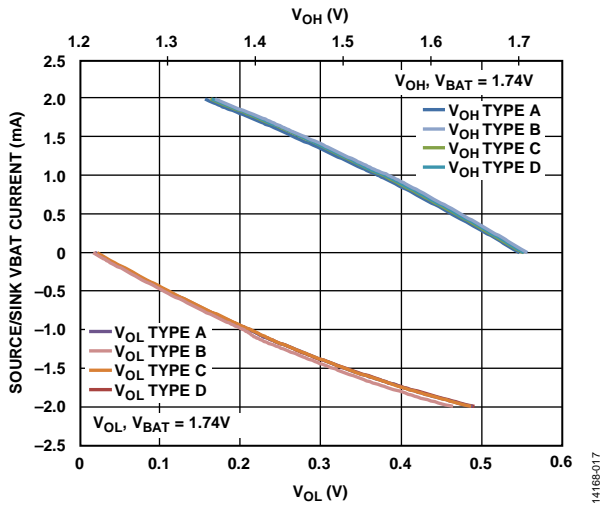


Figure 17. Output Single Drive Strength Characteristics ($V_{BAT} = 1.74 V$)

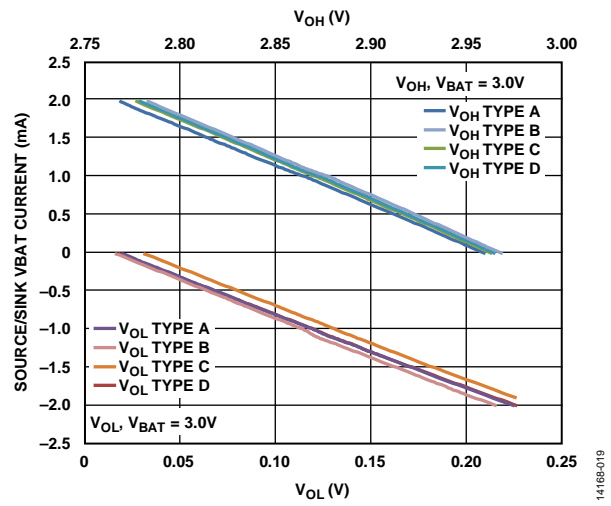


Figure 19. Output Single Drive Strength Characteristics ($V_{BAT} = 3.0 V$)

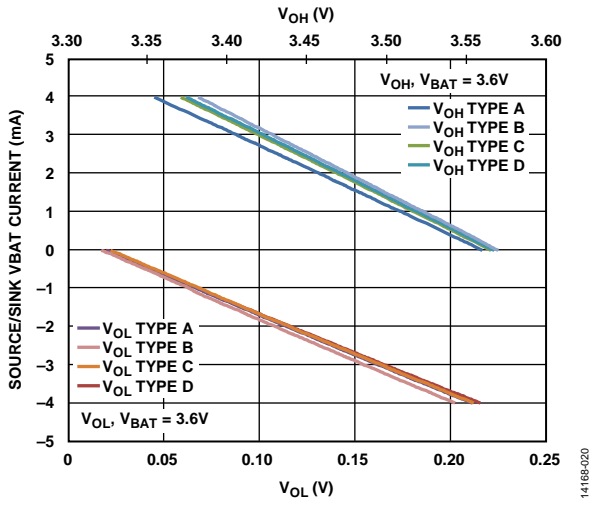


Figure 20. Output Double Drive Strength Characteristics ($V_{BAT} = 3.6 V$)

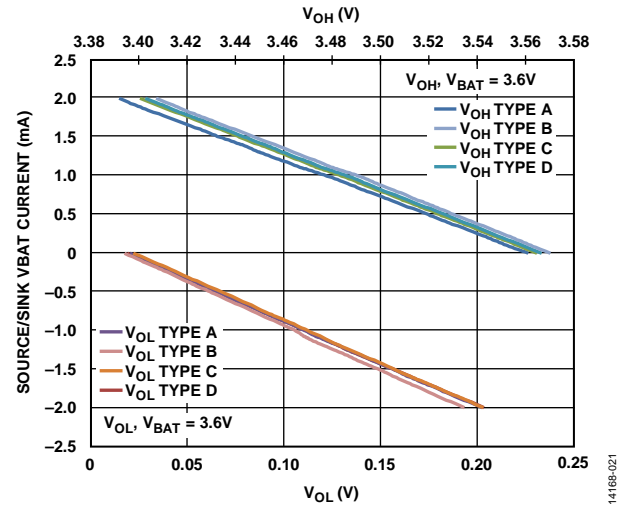


Figure 21. Output Single Drive Strength Characteristics ($V_{BAT} = 3.6 V$)

THEORY OF OPERATION

ARM CORTEX-M3 PROCESSOR

The ARM Cortex-M3 core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits.

The processor has the following features:

- Cortex-M3 architecture
 - Thumb-2 instruction set architecture (ISA) technology
 - Three-stage pipeline with branch speculation
 - Low latency interrupt processing with tail chaining
 - Single-cycle multiply
 - Hardware divide instructions
 - Nested vectored interrupt controller (NVIC) (64 interrupts and 8 priorities)
 - Two hardware breakpoints and one watchpoint (unlimited software breakpoints using Segger JLink)
- Memory protection unit (MPU)
 - Eight region MPU with subregions and background region
 - Programmable clock generator unit
- Configurable for ultra low power operation
 - Deep sleep mode, dynamic power management
 - Programmable clock generator unit

ARM Cortex-M3 Memory Subsystem

The memory map of the ADuCM3027/ADuCM3029 is based on the Cortex-M3 model from ARM. By retaining the standardized memory mapping, it is easier to port applications across M3 platforms.

The ADuCM3027/ADuCM3029 application development is based on memory blocks across code/SRAM regions. Internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in this region (0x0000 0000 to 0x0001 FC00 for the ADuCM3027 and 0x0000 0000 to 0x0003 FFFF for the ADuCM3029) are performed by the core and target the memory and cache resources.

SRAM Region

Accesses in this region (0x2000 0000 to 0x2004 7FFF) are performed by the ARM Cortex-M3 core. The SRAM region of the core can otherwise act as a data region for an application.

- Internal SRAM data region. This space can contain read/write data. Internal SRAM can be partitioned between code and data (SRAM region in M3 space) in 32 kB blocks. Access to this region occurs at core clock speed with no wait states.
- It also supports read/write access by the ARM Cortex-M3 core and read/write DMA access by system devices. It supports exclusive memory accesses via the global exclusive access monitor within the Cortex-M3 platform.
- System memory mapped registers (MMRs). Various system MMRs reside in this region.

System Region

Accesses in this region (0xE000 0000 to 0xF7FF FFFF) are performed by the ARM Cortex-M3 core and are handled within the Cortex-M3 platform.

- CoreSight™ ROM. The read-only memory (ROM) table entries point to the debug components of the processor.
- ARM APB Peripheral. This space is defined by ARM and occupies the bottom 256 kB/128 kB of the system (SYS) region (0xE000 0000 to 0xE004 0000) depending on the device used. The space supports read/write access by the M3 core to the internal peripherals of the ARM core (NVIC, system control space (SCS), wake-up interrupt controller (WIC)), and CoreSight ROM. It is not accessible by system DMA.

MEMORY ARCHITECTURE

The internal memory of the ADuCM3027/ADuCM3029 is shown in Figure 22. The internal memory incorporates up to 256 kB of embedded flash memory for program code and nonvolatile data storage, 32 kB of data SRAM, and 32 kB of SRAM (configured as instruction space or data space).

SRAM Region

This memory space contains the application instructions and literal (constant) data that must be accessed in real-time. It supports read/write access by the ARM Cortex-M3 core and read/write DMA access by system peripherals. Byte, half-word, and word accesses are supported.

SRAM is divided into 32 kB data SRAM and 32 kB instruction SRAM. If instruction SRAM is not enabled, then the associated 32 kB can be mapped as data SRAM, resulting in 64 kB of data SRAM.

Parity bit error detection (optional) is available on all SRAM memories. Two parity bits are associated with each 32-bit word.

When the cache controller is enabled, 4 kB of the instruction SRAM is reserved as cache memory.

Users can select the SRAM configuration modes depending on the instruction SRAM and cache needed.

In hibernate mode, 8 kB to 32 kB of the SRAM can be retained in increments of 8 kB. 8 kB of data SRAM is always retained.

Users can additionally retain

- 16 kB out of 32 kB of instruction SRAM
- 8 kB out of 32 kB of data SRAM

MMRs (Peripheral Control and Status)

For the address space containing MMRs, refer to Figure 22. These registers provide control and status for on-chip peripherals of the ADuCM3027/ADuCM3029. For more information about the MMRs, refer to the [ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference](#).

Flash Memory

The ADuCM3027/ADuCM3029 MCUs include 128 kB to 256 kB of embedded flash memory, which is accessed using a flash controller. For memory available on each product, see Table 1. The flash controller is coupled with a cache controller. A prefetch mechanism is implemented in the flash controller to optimize code performance.

Flash writes are supported by a key hole mechanism via advanced peripheral bus (APB) writes to MMRs. The flash controller provides support for DMA-based key hole writes.

With respect to flash integrity, the devices support the following:

- A fixed user key required for running protected commands, including mass erase and page erase.
- An optional and user definable user failure analysis key (FAA key). Analog Devices personnel need this key while performing failure analysis.
- An optional and user definable write protection for user accessible memory.
- 8-bit ECC.

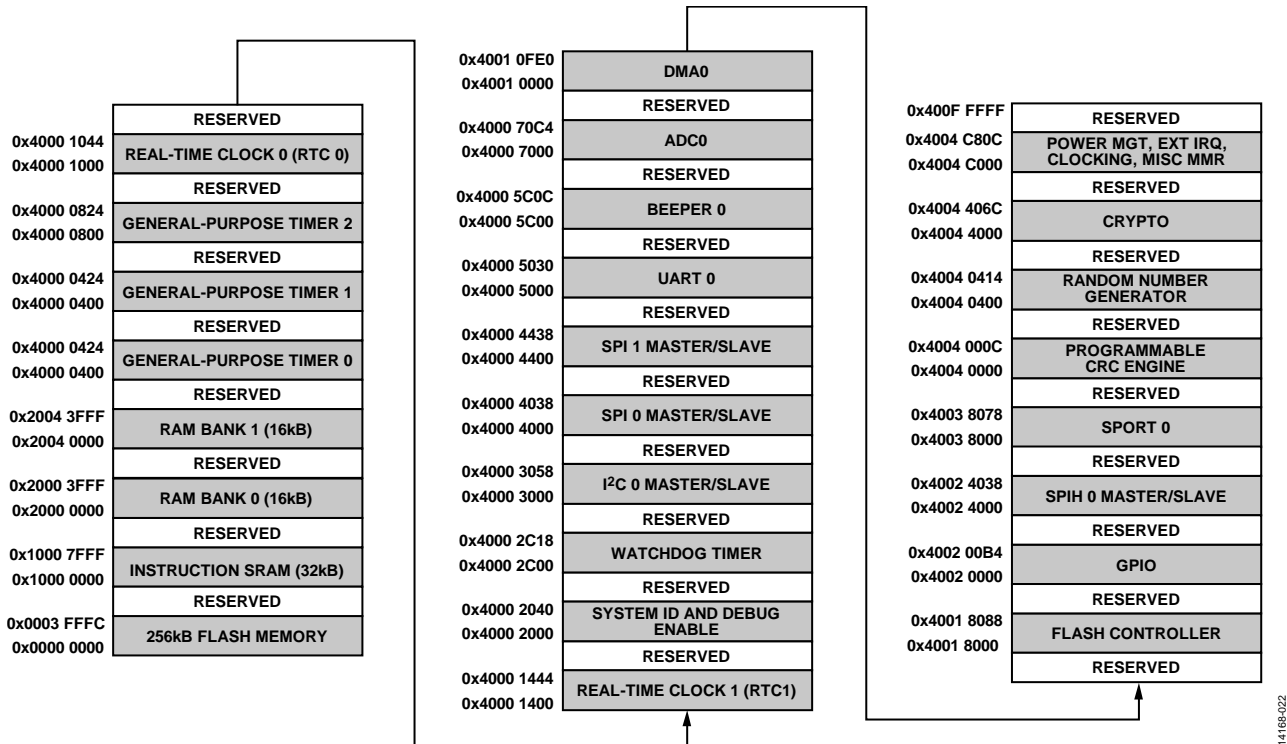


Figure 22. ADuCM3027/ADuCM3029 Memory Map—SRAM Mode 0

CACHE CONTROLLER

The ADuCM3027/ADuCM3029 MCUs have an optional 4 kB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption rather than operating directly from flash. When enabling the cache controller, 4 kB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

SYSTEM AND INTEGRATION FEATURES

The ADuCM3027/ADuCM3029 MCUs provide several features that ease system integration.

Reset

There are four types of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the ARM Cortex-M3 core.

The `SYS_HWRST` pin is toggled to perform a hardware reset.

Booting

The ADuCM3027/ADuCM3029 MCUs support two boot modes: booting from internal flash and upgrading software through UART download. If `SYS_BMODE0` (Pin P1_01) is pulled low during power-up or a hard reset, the MCU enters into serial download mode. In serial download mode, an on-chip routine initiates in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 22. Boot Modes

| Boot Mode | Description |
|-----------|--|
| 0 | UART download mode. |
| 1 | Flash boot. Boot from integrated flash memory. |

Power Management

The ADuCM3027/ADuCM3029 MCUs have an integrated power management system that optimizes performance and extends battery life of the devices.

The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes.

Additional power management features include the following:

- Customized clock gating for active and Flexi™ modes
- Power gating to reduce leakage in hibernate and shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency buck converter to reduce power
- Integrated low power oscillators

Power Modes

The PMU provides control of the ADuCM3027/ADuCM3029 power modes and allows the ARM Cortex-M3 to control the clocks and power gating to reduce the power consumption.

Several power modes are available. Each mode provides an additional low power benefit with a corresponding reduction in functionality.

Active Mode

In active mode, all peripherals can be enabled. Active power is managed by optimized clock management. See Table 4 for details on active mode power.

Flexi Mode

In Flexi mode, the ARM Cortex-M3 core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals and memory as well as memory to memory. See Table 5 for details on Flexi mode power.

Hibernate Mode

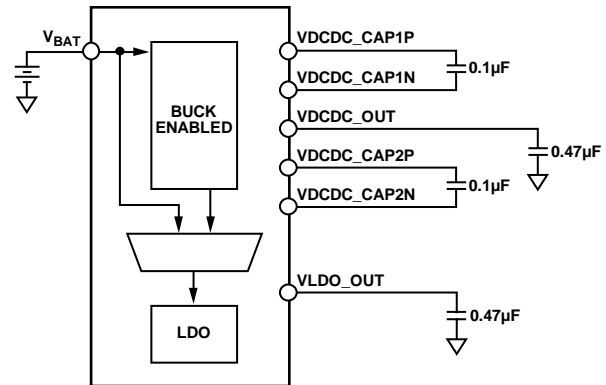
This mode provides state retention, configurable SRAM and port pin retention, a limited number of wake-up interrupts (XINT0_WAKEn and UART0_RX), and, optionally, two RTCs—RTC0 and RTC1 (FLEX_RTC).

Shutdown Mode

This mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from four possible wake-up sources: three external interrupts and RTC0. The RTC0 can be optionally enabled in this mode and the device can be periodically woken up by the RTC0 interrupt. See Table 6 for deep sleep (hibernate and shutdown) mode specifications.

The following features are available for power management and control:

- A voltage range of 1.74 V to 3.6 V using a single supply (such as the CR2032 coin cell battery).
- GPIOs are driven directly from the battery. The pin state is retained in hibernate and shutdown modes. The GPIO configuration is only retained in hibernate mode.
- Wake-up from external interrupt (via GPIOs), UART0_RX interrupt, and RTCs for hibernate mode.
- Wake-up from external interrupt (via GPIOs) and RTC0 for shutdown mode.
- Optional high power buck converter for 1.2 V full on support (for MCU use only). See Figure 23 for the suggested external circuitry.



NOTES

1. FOR DESIGNS IN WHICH THE OPTIONAL BUCK IS NOT USED, THE FOLLOWING PINS MUST BE LEFT UNCONNECTED: VDCDC_CAP1P, VDCDC_CAP1N, VDCDC_OUT, VDCDC_CAP2P, AND VDCDC_CAP2N

Figure 23. Buck Enabled Design

For designs in which the optional buck is not used, the following pins must be left unconnected: VDCDC_CAP1P, VDCDC_CAP1N, VDCDC_OUT, VDCDC_CAP2P, and VDCDC_CAP2N.

Security Features

The ADuCM3027/ADuCM3029 MCUs provide a combination of hardware and software protection mechanisms that lock out access to the devices in secure mode but grant access in open mode. These mechanisms include password protected slave boot mode (UART), as well as password protected serial wire debug (SWD) interfaces.

Mechanisms are provided to protect the device contents (flash, SRAM, CPU registers, and peripheral registers) from being read through an external interface by an unauthorized user, which is referred to as read protection.

It is possible to protect the device from being reprogrammed in circuit with unauthorized code. This is referred to as in circuit write protection.

The devices can be configured with no protection, read protection, or read and in circuit write protection. It is not necessary to provide in circuit write protection without read protection.

Cryptographic Accelerator

The cryptographic accelerator is a 32-bit APB DMA capable peripheral. There are two 32-bit buffers provided for data input/output operations. These buffers read in or read out 128 bits in four data accesses. Big endian and little endian data formats are supported, as are the following modes:

- Electronic code book (ECB) mode—AES mode
- Counter (CTR) mode
- Cipher block chaining (CBC) mode
- Message authentication code (MAC) mode
- Cipher block chaining-message authentication code (CCM/CCM*) mode
- SHA-256 modes

True Random Number Generator (TRNG)

The TRNG is used during operations where nondeterministic values are required. These operations can include generating challenges for secure communication or keys for an encrypted communication channel. The generator can run multiple times to generate a sufficient number of bits for the strength of the intended operation. The TRNG can seed a deterministic random bit generator.

Reliability and Robustness Features

The ADuCM3027/ADuCM3029 MCUs provide a number of features that can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness.

ECC Enabled Flash Memory

The entire flash array can be protected to either correct single-bit errors or detect two-bit errors per 64-bit flash data.

Multiparity Bit Protected SRAM

Each word of the SRAM and cache memory is protected by multiple parity bits to allow detection of random soft errors.

Software Watchdog

The on-chip watchdog timer can provide software-based supervision of the ADuCM3027/ADuCM3029.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator computes the CRC for a block of memory locations. The exact memory location can be in the SRAM, flash, or any combination of MMRs. The CRC accelerator generates a checksum that can be compared with an expected signature.

The main features of the CRC include the following:

- Generates a CRC signature for a block of data.
- Supports programmable polynomial length of up to 32 bits.
- Operates on 32 bits of data at a time.
- Supports MSB first and LSB first CRC implementations.
- Various data mirroring capabilities.
- Initial seed to be programmed by user.
- DMA controller (memory to memory transfer) used for data transfer to offload the MCU.

Programmable GPIOs

The ADuCM3027 and ADuCM3029 MCUs have 44 and 34 GPIO pins in the LFCSP and WLCSP packages, respectively. Note that the ADuCM3029-1 and ADuCM3029-2 models have 44 GPIO pins and are available in the LFCSP only. These GPIO pins have multiple, configurable functions defined by user code. They can be configured as an input/output and have programmable pull-up resistors. All GPIO pins are functional over the full supply range.

In deep sleep mode, the GPIO pins retain their state. On reset, the GPIO pins tristate.

Timers

The ADuCM3027/ADuCM3029 MCUs have three general-purpose timers and a watchdog timer.

General-Purpose Timers

The ADuCM3027/ADuCM3029 MCUs have three identical general-purpose timers, each with a 16-bit up and down counter. The up and down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

Watchdog Timer (WDT)

The WDT is a 16-bit count down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The WDT is clocked by the 32 kHz on-chip oscillator (LFOSC) and recovers from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt to the MCU.

Analog-to-Digital Converter (ADC) Subsystem

The ADuCM3027/ADuCM3029 MCUs integrate a 12-bit SAR ADC with up to eight external channels. Conversions can be performed in single or autcycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the channels. Autocycle mode is provided to reduce MCU overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using dedicated channels. Temperature sensing and battery monitoring cannot be included with external channels in autocycle mode.

A digital comparator triggers an interrupt if ADC input is above or below a programmable threshold. The ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 input channels can be used with the digital comparator.

Use the ADC in DMA mode to reduce MCU overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions has been completely logged to memory.

The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS.
- Integrated input multiplexer that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V and 2.5 V.
- Software selectable internal or external reference.
- Autocycle mode—ability to automatically select a sequence of input channels for conversion.
- Averaging function—converted data on single-channel or multiple channels can be averaged up to 256 samples.
- Alert function—internal digital comparator for ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold.
- Dedicated DMA channel support.

- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

Clocking

The ADuCM3027/ADuCM3029 MCUs have the following clocking options:

- 26 MHz
 - Internal oscillator—HFOSC (26 MHz)
 - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
 - GPIO clock in—SYS_CLKIN
- 32 kHz
 - Internal oscillator—LFOSC
 - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator.
- LFOSC cannot be disabled even if using LFXTAL.

Table 23. RTC Features

| Features | RTC0 | RTC1 (FLEX_RTC) |
|--------------------------------------|--|--|
| Resolution of Time Base (Prescaling) | Counts time at 1 Hz in units of seconds. Operationally, RTC0 always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds. | Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, ..., 16,384, or 32,768. |
| Source Clock | LFXTAL. | Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC. |
| Wake-Up Timer | Wake-up time is specified in units of seconds. | Supports alarm times down to a resolution of 30.52 μs, that is, where the time is specified down to a specific 32 kHz clock cycle. |
| Number of Alarms | One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec. | Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units. |
| SensorStrobe Mechanism | Not available. | SensorStrobe is an alarm mechanism in the RTC that sends an output pulse via GPIOs to an external device to instruct the device to take a measurement or perform some action at a specific time. SensorStrobe events are schedule data specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, Flexi, and hibernate modes. |
| Input Capture | Not available. | Input capture takes a snapshot of the RTC when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM3027/ADuCM3029. Typically, an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM3027/ADuCM3029 that the RTC must take a snapshot of time corresponding to the event. Taking the snapshot can wake up the ADuCM3027/ADuCM3029 and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred. |

Beeper Driver

The ADuCM3027/ADuCM3029 MCUs have an integrated audio driver for a beeper.

The beeper driver module in the ADuCM3027/ADuCM3029 MCUs generate a differential square wave of programmable frequency. It drives an external piezoelectric sound component with two terminals that connect to the differential square wave output.

The beeper driver consists of a module that can deliver frequencies ranging from 8 kHz to approximately 0.25 kHz; the minimum frequency is determined by the maximum value of a divide register that can be programmed to 127. This results in a beeper frequency of

$$32.768 \text{ kHz}/127 = 0.25802 \text{ kHz}$$

The beeper driver allows programmable tone durations in 4 ms increments. Pulse (single-tone) and sequence (multitone) modes provide versatile playback options.

In sequence mode, the beeper can be programmed to play any number of tone pairs from 1 to 254 (2 tones to 508 tones) or be programmed to play forever (until stopped by the user). Interrupts are available to indicate the start or end of any beep, the end of a sequence, or when the sequence is nearing completion.

Debug Capability

The ADuCM3027/ADuCM3029 MCUs support SWD. The ADuCM3027/ADuCM3029 MCUs have a reduced flash patch and breakpoint (FPB) unit with support for up to two hardware breakpoints.

ON-CHIP PERIPHERAL FEATURES

The ADuCM3027/ADuCM3029 MCUs have a rich set of peripherals connected to the core via several concurrent high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1).

The ADuCM3027/ADuCM3029 MCUs contain high speed serial ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the MCU and system to many application scenarios.

Serial Ports (SPORT)

The ADuCM3027/ADuCM3029 MCUs provide two single direction half SPORTs or one bidirectional full SPORT. The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices audio codecs, ADCs, and DACs. The serial ports contain two data lines, a clock, and a frame sync. The data lines can be programmed to either transmit or receive, and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory or external memory via dedicated DMA

channels. The frame sync and clock can be shared. Some of the ADCs and DACs require two control signals for their conversion process. To interface with such devices, the SPT0_ACNV and SPT0_BCNV signals are provided. To use these signals, enable the timer enable mode. In this mode, a PWM timer inside the module generates the programmable SPT0_ACNV and SPT0_BCNV signals.

Serial ports operate in two modes:

- Standard digital signal processor (DSP) serial mode
- Timer enable mode

SPI Ports

The ADuCM3027/ADuCM3029 MCUs provide three SPIs. SPI is an industry standard, full-duplex, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received. Each SPI incorporates two DMA channels that interface with the DMA controller. One DMA channel transmits and the other receives. The SPI on the MCU eases interfacing to external serial flash devices.

The SPI features include the following:

- Serial clock phase mode and serial clock polarity mode
- Loopback mode
- Continuous and repeated transfer mode
- Wired OR output mode
- Read command mode for half-duplex operation (transmit followed by receive)
- Flow control support in read command mode
- Support for 3-pin SPI in read command mode
- Multiple $\overline{\text{CS}}$ line support
- $\overline{\text{CS}}$ software override support

UART Port

The ADuCM3027/ADuCM3029 MCUs provide a full-duplex UART port, which is fully compatible with PC standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA, and asynchronous transfers of serial data. The UART port includes support for five to eight data bits, and none, even, or odd parity. A frame is terminated by one, one and a half, or two stop bits.

I²C

The ADuCM3027/ADuCM3029 MCUs provide an I²C bus peripheral that has two pins for data transfer. SCL (Pin P0_04) is a serial clock pin, and SDA (Pin P0_05) is a serial data pin. The pins are configured in a wired AND format that allows arbitration in a multimaster system. A master device can be configured to generate the serial clock. The frequency is programmed by the user in the serial clock divisor register. The master channel can operate in fast mode (400 kHz) or standard mode (100 kHz).

DEVELOPMENT SUPPORT

Development support for the ADuCM3027/ADuCM3029 MCU includes documentation, evaluation hardware, and development software tools.

Documentation

The [ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference](#) details the functionality of each block on the ADuCM3027/ADuCM3029 MCUs. It includes power management, clocking, memories, and peripherals.

Hardware

The [EV-COG-AD3029LZ](#) is available to prototype sensor configurations with the ADuCM3027/ADuCM3029 MCUs.

Software

The [EV-COG-AD3029LZ](#) includes a complete development and debug environment for the ADuCM3027/ADuCM3029 MCUs. The device family pack (DFP) for the ADuCM3027/ADuCM3029 is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The DFP also includes operating system (OS) aware drivers and example code for all the peripherals on the devices.

ADDITIONAL INFORMATION

The following documentation that describe the ADuCM3027/ADuCM3029 MCUs can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website:

- [ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.](#)

This data sheet describes the ARM Cortex-M3 core and memory architecture used on the ADuCM3027/ADuCM3029 MCUs but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M3 processor include the following:

- ARM Cortex-M3 Devices Generic User Guide
- ARM Cortex-M3 Technical Reference Manual

REFERENCE DESIGNS

The [Circuits from the Lab®](#) page provides the following for the ADuCM3027/ADuCM3029 reference design:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

MCU TEST CONDITIONS

The ac signal specifications (timing parameters) appearing in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the voltage threshold (V_{MEAS}) level as described in Figure 24. All delays (in nanoseconds or microseconds) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS} . The value of V_{MEAS} is set to $V_{BAT}/2$. The tester pin electronics is shown in Figure 25.

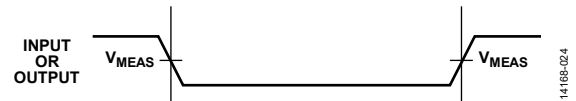
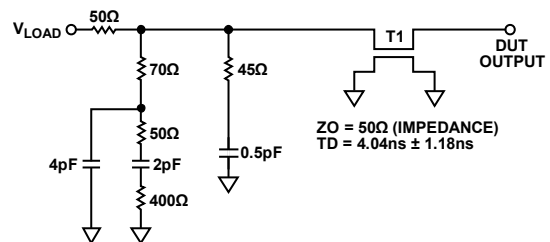


Figure 24. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES

1. THE WORST-CASE TRANSMISSION LINE DELAY (TD) IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. TRANSMISSION LINE IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.
2. ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 25. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

DRIVER TYPES

Table 24 shows the driver types.

Table 24. Driver Types

| Driver Type ^{1,2,3} | Associated Pins |
|------------------------------|---|
| Type A | P0_00 to P0_03, P0_07, P0_10 to P0_13, P0_15, P1_00 to P1_10, P1_15, P2_00, P2_01, P2_04 to P2_14, P3_00 to P3_03, and SYS_HWRST. |
| Type B | P0_08, P0_09, P0_14, P1_11 to P1_14, and P2_02 |
| Type C | P0_04 and P0_05 |
| Type D | P0_06 |

¹ In single drive mode, the maximum source/sink capacity is 2 mA.

² In double drive mode, the maximum source/sink capacity is 4 mA.

³ At maximum drive capacity, only 16 GPIOs are allowed to switch at any given point of time.

EEMBC ULPMARK™-CP SCORE

Using the software configuration and the profile configuration shown in the following tables, the EEMBC ULPMark-CP score is 245.5.

Table 25. EEMBC ULPMark™-CP Software Configuration

| Software Configuration | Value |
|--------------------------------|--|
| Compiler Name and Version | IAR EWARM 7.50.2.10505 |
| Compiler Flags | -Ohs -- endian=little -- cpu=Cortex-M3 -D __ADuCM3029__ |
| ULPBench Profile and Version | Core Profile v1.1 |
| EnergyMonitor Software Version | V1.1.3 |

Table 26. EEMBC ULPMark™-CP Profile Configuration

| Profile Configuration | Value |
|---------------------------------|----------------------------|
| Wakeup Timer Module | RTC1 |
| Wakeup Timer Clock Source | External crystal |
| Wakeup Timer Frequency | 32768 Hz |
| Wakeup Timer Accuracy | 20 PPM |
| Active Power Mode Name | Active mode |
| Active Mode Clock Configuration | 26 MHz (CPU), 32 kHz (RTC) |
| Active Mode Voltage Integrity | 1.74 V |
| Inactive Power Mode Name | Hibernate |
| Inactive Clock Configuration | Off (CPU), 32 kHz (RTC) |
| Inactive Mode Voltage Integrity | 1.74 V |

GPIO MULTIPLEXING

Table 27 through Table 29 show the signal multiplexing options for the GPIO pins.

Table 27. Signal Multiplexing for PORT 0

| Pin | Availability | | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function 3 |
|-------|--------------|-------|------------------------|------------------------|------------------------|------------------------|
| | WLCSP | LFCSP | | | | |
| P0_00 | Yes | Yes | GPIO00 | SPIO_CLK | SPT0_BCLK | Not available |
| P0_01 | Yes | Yes | GPIO01 | SPIO_MOSI | SPT0_BFS | Not available |
| P0_02 | Yes | Yes | GPIO02 | SPIO_MISO | SPT0_BD0 | Not available |
| P0_03 | Yes | Yes | GPIO03 | SPIO_CS0 | SPT0_BCNV | SPI2_RDY |
| P0_04 | Yes | Yes | GPIO04 | I2C0_SCL | Not available | Not available |
| P0_05 | Yes | Yes | GPIO05 | I2C0_SDA | Not available | Not available |
| P0_06 | Yes | Yes | SWD0_CLK | GPIO06 | Not available | Not available |
| P0_07 | Yes | Yes | SWD0_DATA | GPIO07 | Not available | Not available |
| P0_08 | Yes | Yes | GPIO08 | BPR0_TONE_N | Not available | Not available |
| P0_09 | Yes | Yes | GPIO09 | BPR0_TONE_P | SPI2_CS1 | Not available |
| P0_10 | Yes | Yes | GPIO10 | UART0_TX | Not available | Not available |
| P0_11 | Yes | Yes | GPIO11 | UART0_RX | Not available | Not available |
| P0_12 | Yes | Yes | GPIO12 | SPT0_AD0 | Not available | UART0_SOUT_EN |
| P0_13 | Yes | Yes | GPIO13/XINT0_WAKE2 | Not available | Not available | Not available |
| P0_14 | Yes | Yes | GPIO14 | TMRO_OUT | SPI1_RDY | Not available |
| P0_15 | Yes | Yes | GPIO15/XINT0_WAKE0 | Not available | Not available | Not available |

Table 28. Signal Multiplexing for PORT 1

| Pin | Availability | | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function 3 |
|-------|--------------|-------|------------------------|------------------------|------------------------|------------------------|
| | WLCSP | LFCSP | | | | |
| P1_00 | Yes | Yes | GPIO16/XINT0_WAKE1 | Not available | Not available | Not available |
| P1_01 | Yes | Yes | SYS_BMODE0 | GPIO17 | Not available | Not available |
| P1_02 | Yes | Yes | GPIO18 | SPI2_CLK | Not available | Not available |
| P1_03 | Yes | Yes | GPIO19 | SPI2_MOSI | Not available | Not available |
| P1_04 | Yes | Yes | GPIO20 | SPI2_MISO | Not available | Not available |
| P1_05 | Yes | Yes | GPIO21 | SPI2_CS0 | Not available | Not available |
| P1_06 | Yes | Yes | GPIO22 | SPI1_CLK | Not available | Not available |
| P1_07 | Yes | Yes | GPIO23 | SPI1_MOSI | Not available | Not available |
| P1_08 | Yes | Yes | GPIO24 | SPI1_MISO | Not available | Not available |
| P1_09 | Yes | Yes | GPIO25 | SPI1_CS0 | Not available | Not available |
| P1_10 | Yes | Yes | GPIO26 | SPIO_CS1 | SYS_CLKIN | SPI1_CS3 |
| P1_11 | No | Yes | GPIO27 | Not available | TMR1_OUT | Not available |
| P1_12 | No | Yes | GPIO28 | Not available | Not available | Not available |
| P1_13 | No | Yes | GPIO29 | Not available | Not available | Not available |
| P1_14 | Yes | Yes | GPIO30 | Not available | SPIO_RDY | Not available |
| P1_15 | No | Yes | GPIO31 | SPT0_ACLK | Not available | Not available |

Table 29. Signal Multiplexing for PORT 2

| Pin | Availability | | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function 3 |
|-------|--------------|------|------------------------|------------------------|------------------------|------------------------|
| | WLCSP | LFCS | | | | |
| P2_00 | No | Yes | GPIO32 | SPT0_AFS | Not available | Not available |
| P2_01 | Yes | Yes | GPIO33/XINT0_WAKE3 | Not available | TMR2_OUT | Not available |
| P2_02 | No | Yes | GPIO34 | SPT0_ACNV | SPI1_CS2 | Not available |
| P2_03 | Yes | Yes | GPIO35 | ADC0_VIN0 | Not available | Not available |
| P2_04 | Yes | Yes | GPIO36 | ADC0_VIN1 | Not available | Not available |
| P2_05 | Yes | Yes | GPIO37 | ADC0_VIN2 | Not available | Not available |
| P2_06 | Yes | Yes | GPIO38 | ADC0_VIN3 | Not available | Not available |
| P2_07 | No | Yes | GPIO39 | ADC0_VIN4 | SPI2_CS3 | Not available |
| P2_08 | No | Yes | GPIO40 | ADC0_VIN5 | SPI0_CS2 | Not available |
| P2_09 | No | Yes | GPIO41 | ADC0_VIN6 | SPI0_CS3 | Not available |
| P2_10 | No | Yes | GPIO42 | ADC0_VIN7 | SPI2_CS2 | Not available |
| P2_11 | Yes | Yes | GPIO43 | SPI1_CS1 | SYS_CLKOUT | RTC1_SS1 |

APPLICATIONS INFORMATION

This section contains circuit diagrams that show the recommended external components for proper operation of the ADuCM3027/ADuCM3029 in example application scenarios.

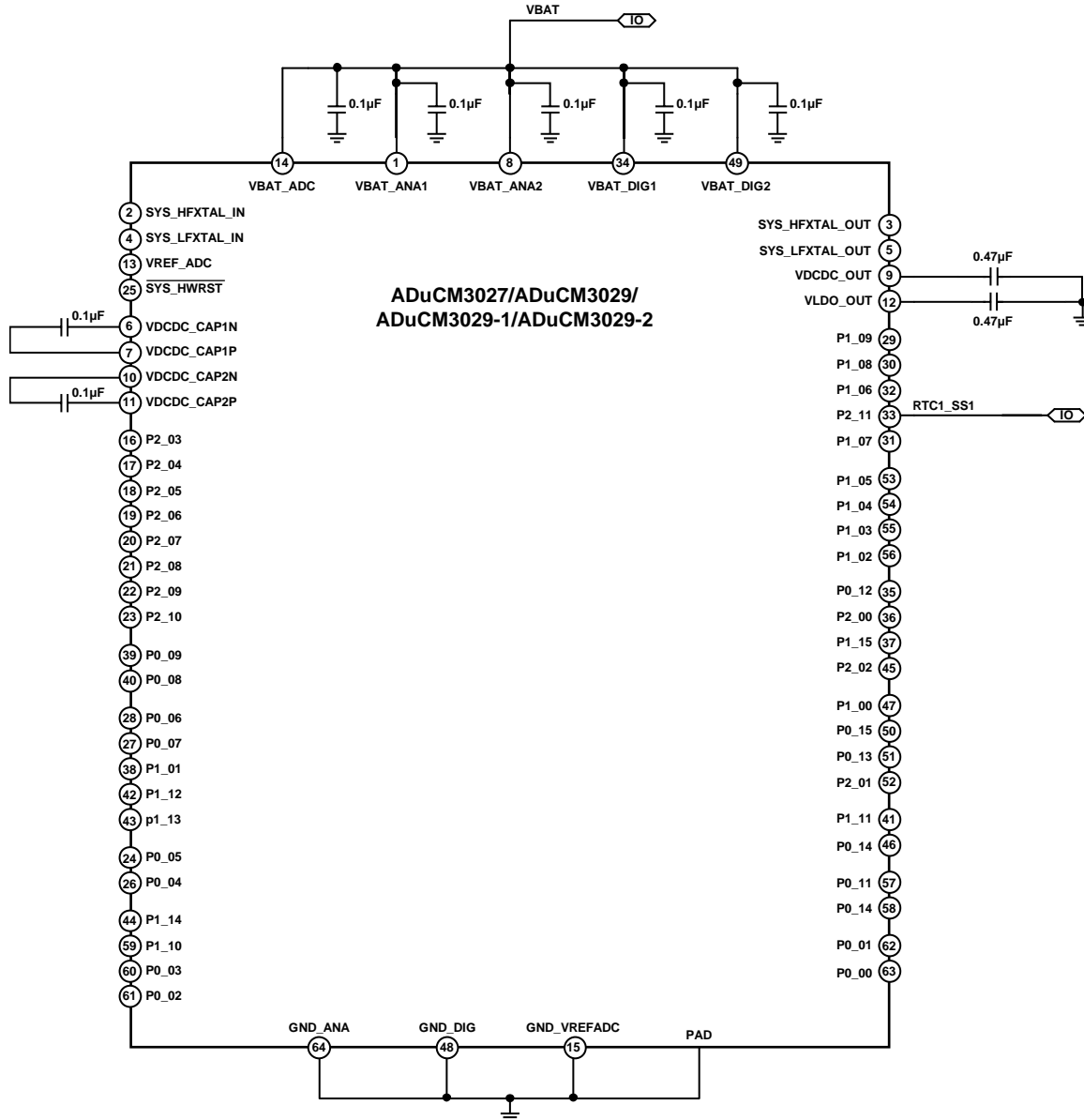


Figure 26. Recommended External Components when Using the Internal Buck Converter

141659-026

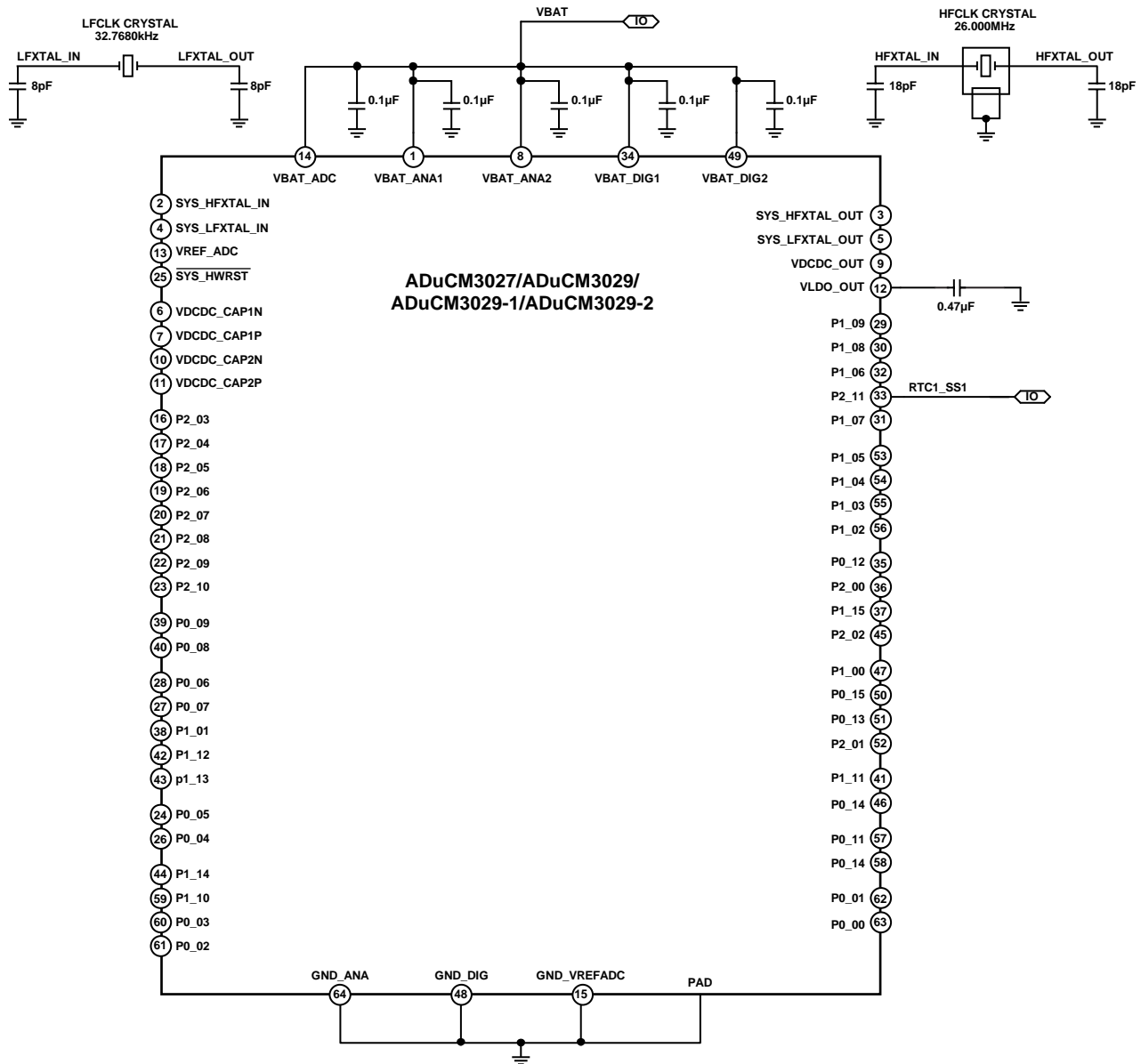


Figure 27. Recommended External Components when Using LFXTAL and HFXTAL

14188-027

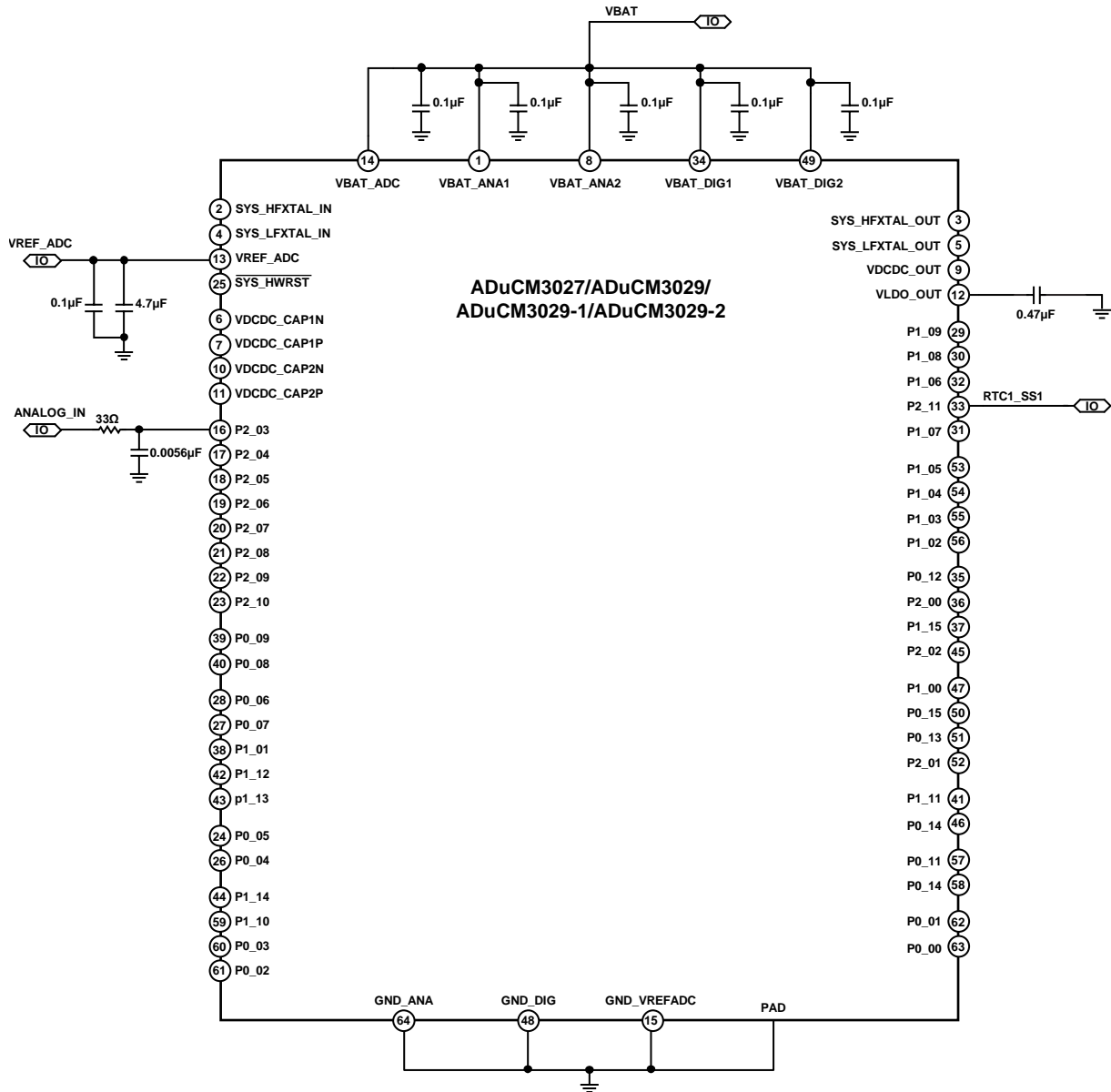


Figure 28. Recommended External Components on VREF_ADC Pin and ADC Input Channel (ADC0_VIN0 Used as Example) when Using the Internal ADC

14165-028

ABOUT ADuCM3027/ADuCM3029 SILICON ANOMALIES

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuCM3027/ADuCM3029. These anomalies represent the currently known differences between revisions of the ADuCM3027/ADuCM3029 product(s) and the functionality specified in the ADuCM3027/ADuCM3029 data sheet(s) and the [Hardware Reference](#) manual.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined in this section.

ADuCM3027/ADuCM3029 FUNCTIONALITY ISSUES

| Silicon Revision Identifier | Silicon Status | No. of Reported Anomalies |
|-----------------------------|----------------|--|
| 1.2 | Released | 4 (21000011, 21000015, 21000016, 21000017) |

A silicon revision number with the form x.y is branded on all devices. The silicon revision can be electronically determined by reading Bits[3:0] of the SYS_CHIPID register. SYS_CHIPID = 0x4 indicates Silicon Revision 1.2.

FUNCTIONALITY ISSUES

Table 30 through Table 33 detail all known silicon anomalies for the ADuCM3027/ADuCM3029 including a description, workaround, and identification of applicable silicon revisions.

Table 30. 21000011—I²C Master Mode Fails to Generate Clock

| | |
|-----------------------|---|
| Background | When the I ² C clock dividers are configured in master mode such that the sum of the LOW bit in the I2C_DIV register and the HIGH bit in the I2C_DIV register is less than 16, the I ² C fails to generate a clock. |
| Issue | The I ² C master mode fails to generate clock when clock dividers are too small. |
| Workaround | Program the I ² C clock dividers such that I2C_DIV.LOW + I2C_DIV.HIGH ≥ 16. |
| Related Issues | None. |

Table 31. 21000015—Pin P2_11 Not Retained

| | |
|-----------------------|--|
| Background | The state of the P2_11 pin is not retained after waking up from shutdown mode. |
| Issue | Pin P2_11 is not retained after shutdown wake up. |
| Workaround | None. To retain the pin state through shutdown, use any other GPIO pin instead of P2_11. |
| Related Issues | None. |

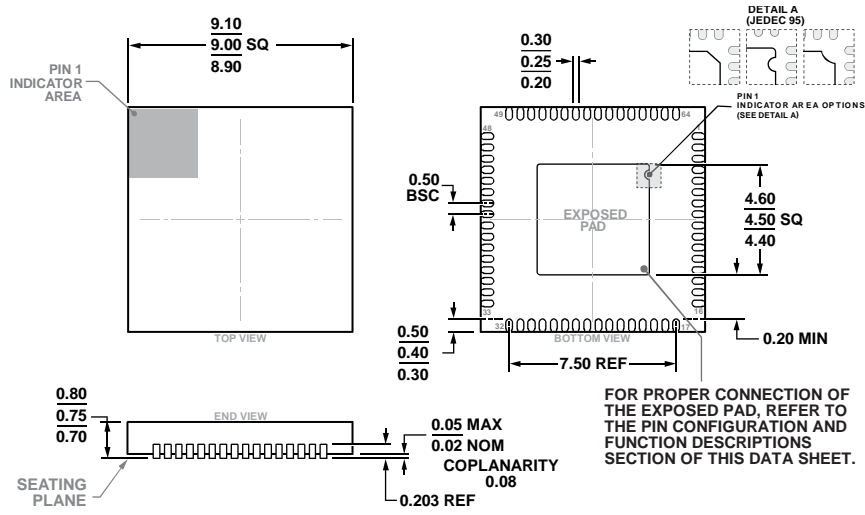
Table 32. 21000016—Data Loss with I²C Automatic Clock Stretching

| | |
|-----------------------|--|
| Background | When the I ² C Rx FIFO is full and new I ² C data is received, a data overflow occurs. When automatic clock stretching is enabled, the transaction is paused by holding the SCL line low. This pause function works as expected when the next read happens after the clock is stretched (for example, after the overflow is detected). However, if the read occurs after the last bit of the I ² C data is received but before the clock is stretched, the received data is not written to the Rx FIFO and is lost. |
| Issue | Possible receive data loss with I ² C automatic clock stretching. |
| Workaround | After I ² C automatic clock stretching is enabled, read the FIFO only after the overflow flag is set in the status register to ensure the Rx FIFO is never read at the same time the overflow is asserted. |
| Related Issues | None. |

Table 33. 21000017—SPI Read Command Mode Does Not Work

| | |
|-----------------------|--|
| Background | When the SPI master is enabled and uses the DMA mode with SPI_CNT = 1, the read command mode may not function properly. Consider the following configurations: SPI_RD_CTL = 0x07, SPI_CNT = 1, and the Tx and Rx DMA channels configured for one half-word. In this configuration, the read command sent in the first byte on the MOSI output is repeated in the second byte (in the address slot); thus, the slave device responds on the MISO line with whatever content is at the address equivalent to the read command value (for example, if the read command is 0xB, the response is the data read from Slave Address 0xB). |
| Issue | SPI read command mode does not work properly when SPI_CNT is 1 and DMA is enabled. |
| Workaround | Use the overlap mode to align the transmit/receive SPI operations and discard the junk bytes, as follows: Set the OVERLAP bit in the SPI_RD_CTL register = 1 to enable overlap mode. Set the TXBYTES bit in the SPI_RD_CTL register = 1 to configure a single transmit byte (8-bit address register). Set SPI_CNT.VALUE = 3 to configure the transfer count: one byte for the address register, one byte for the command, and one dummy byte to obtain the read value, and on the receive side, discard the first two bytes received during the transfer of the address and command bytes before processing the actual read value in the third byte. Do not use Tx DMA operation on the SPI transmit side, as follows: enable only the SPI Rx DMA requests, fill the SPI Tx FIFO by using core accesses to write to the SPI_TX register, and perform a dummy read of the SPI_RX register to start the SPI transfers. |
| Related Issues | None. |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WMMD

Figure 29. 64-Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm Body and 0.75 mm Package Height
(CP-64-16)

Dimensions shown in millimeters

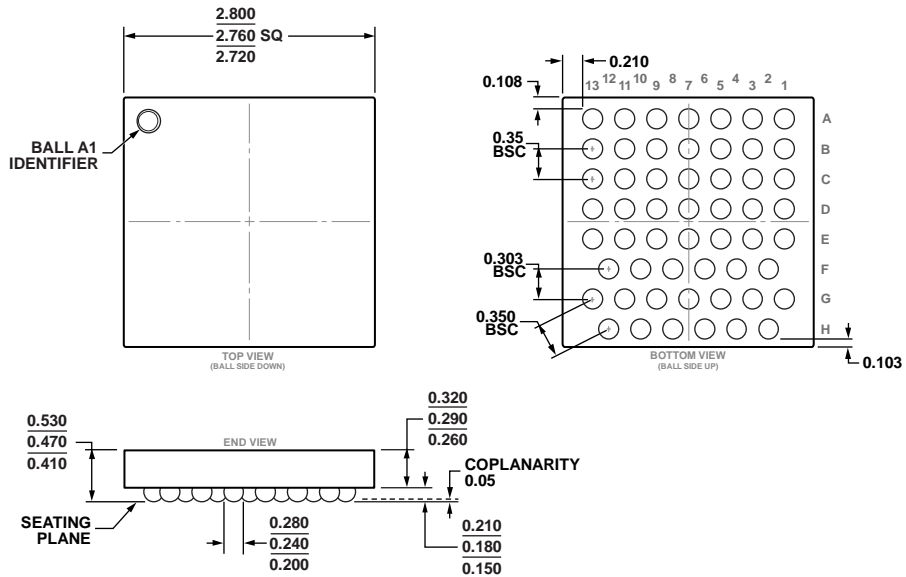


Figure 30. 54-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-54-1)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Description | Temperature ² | Package Description | Package Option |
|--------------------|--|--------------------------|-------------------------|----------------|
| ADuCM3027BCBZ-RL | ULP ARM Cortex-M3 with 128 kB Embedded Flash | –40°C to +85°C | 54-Ball WLCSP, 13" Reel | CB-54-1 |
| ADuCM3027BCBZ-R7 | ULP ARM Cortex-M3 with 128 kB Embedded Flash | –40°C to +85°C | 54-Ball WLCSP, 7" Reel | CB-54-1 |
| ADuCM3027BCPZ | ULP ARM Cortex-M3 with 128 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADuCM3027BCPZ-RL | ULP ARM Cortex-M3 with 128 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP, 13" Reel | CP-64-16 |
| ADuCM3027BCPZ-R7 | ULP ARM Cortex-M3 with 128 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP, 7" Reel | CP-64-16 |
| ADuCM3029BCBZ-RL | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 54-Ball WLCSP, 13" Reel | CB-54-1 |
| ADuCM3029BCBZ-R7 | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 54-Ball WLCSP, 7" Reel | CB-54-1 |
| ADuCM3029BCPZ | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADuCM3029BCPZ-RL | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP, 13" Reel | CP-64-16 |
| ADuCM3029BCPZ-R7 | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP, 7" Reel | CP-64-16 |
| ADuCM3029-1BCPZ | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADuCM3029-1BCPZ-R7 | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP, 7" Reel | CP-64-16 |
| ADuCM3029-2BCPZ | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADuCM3029-2BCPZ-R7 | ULP ARM Cortex-M3 with 256 kB Embedded Flash | –40°C to +85°C | 64-Lead LFCSP, 7" Reel | CP-64-16 |
| EV-COG-AD3029LZ | ADuCM3029 LFCSP Development Board | | | |
| EV-COG-AD3029WZ | ADuCM3029 WLCSP Development Board | | | |

¹ Z = RoHS Compliant Part.

² Referenced temperature is ambient temperature. The ambient temperature is not a specification. See the Absolute Maximum Ratings section for junction temperature (T_J) specification which is the only temperature specification.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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