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2N7002PW

60 V, 310 mA N-channel Trench MOSFET Rev. 02 — 29 July 2010

Product data sheet

Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- AEC-Q101 qualified
- Logic-level compatible

- Trench MOSFET technology
- Very fast switching

1.3 Applications

- High-speed line driver
- Low-side loadswitch

- Relay driver
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _{amb} = 25 °C		-	-	60	V
V_{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V_{GS} = 10 V; T_{amb} = 25 °C	[1]	-	-	310	mA
Static char	racteristics						
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA; T_j = 25 °C; t_p ≤ 300 µs; pulsed; δ ≤ 0.01		-	1	1.6	Ω

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



60 V, 310 mA N-channel Trench MOSFET

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source	3	D
3	D	drain	1	mbb076 S

3. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
2N7002PW	SC-70	plastic surface-mounted package; 3 leads	SOT323			

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
2N7002PW	X8%

^[1] % = -: made in Hong Kong; % = p: made in Hong Kong; % = t: made in Malaysia; % = W: made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _{amb} = 25 °C		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	V_{GS} = 10 V; T_{amb} = 25 °C	<u>[1]</u>	-	310	mΑ
		V _{GS} = 10 V; T _{amb} = 100 °C	<u>[1]</u>	-	240	mΑ
I_{DM}	peak drain current	$T_{amb} = 25 ^{\circ}C$; single pulse; $t_p \le 10 \mu s$		-	1.2	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	260	mW
			[1]	-	310	mW
		T _{sp} = 25 °C		-	830	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-dra	nin diode					
Is	source current	T _{amb} = 25 °C	[1]	-	310	mA

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

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60 V, 310 mA N-channel Trench MOSFET

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

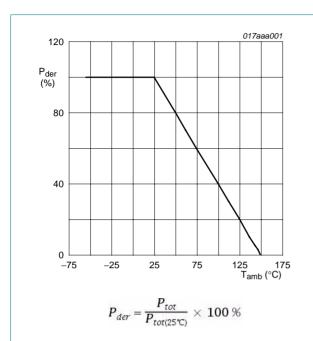


Fig 1. Normalized total power dissipation as a function of ambient temperature

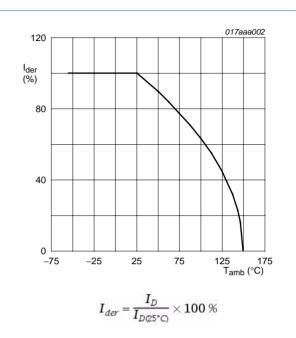
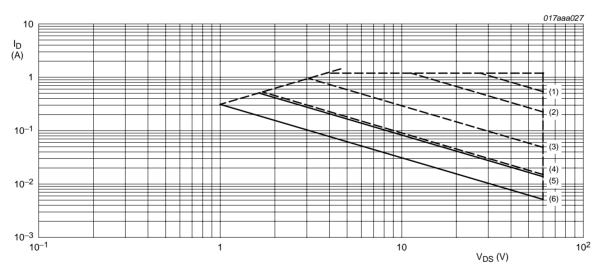


Fig 2. Normalized continuous drain current as a function of ambient temperature



I_{DM} = single pulse

(1) $t_p = 100 \mu s$

(2) $t_p = 1 \text{ ms}$

(3) $t_p = 10 \text{ ms}$

(4) $t_p = 100 \text{ ms}$

(5) DC; $T_{sp} = 25 \, ^{\circ}\text{C}$

(6) DC; $T_{amb} = 25$ °C; drain mounting pad 1 cm²

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

2N7002PW **NXP Semiconductors**

60 V, 310 mA N-channel Trench MOSFET

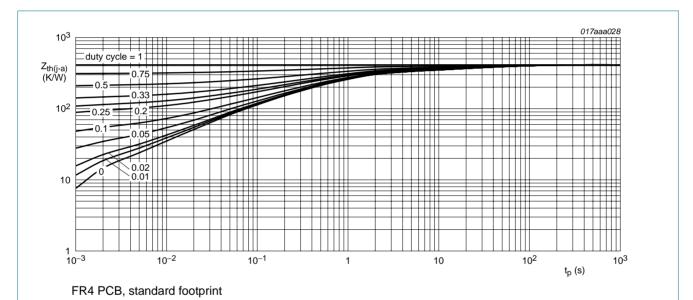
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Thermal characteristics

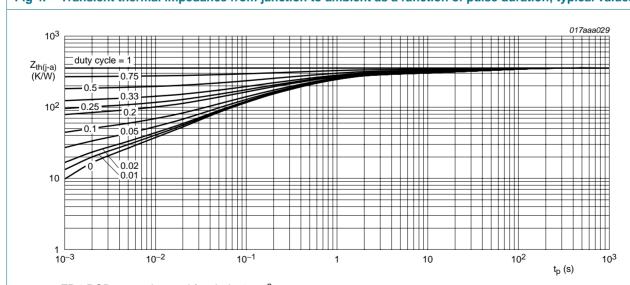
Thermal characteristics Table 6.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air [1]	<u>[1]</u>	-	415	480	K/W
			[2]	-	350	400	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	150	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

60 V, 310 mA N-channel Trench MOSFET

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1.1	1.75	2.4	V
I _{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	10	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 50 \text{ mA}; \text{ pulsed};$ $t_p \le 300 \mu\text{s}; \delta \le 0.01 ; T_j = 25 ^{\circ}\text{C}$	-	1.3	2	Ω
		V_{GS} = 10 V; I_{D} = 500 mA; pulsed; $t_{p} \le$ 300 µs; $\delta \le$ 0.01 ; T_{j} = 25 °C	-	1	1.6	Ω
9 _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 200 \text{ mA}; \text{ pulsed};$ $t_p \le 300 \mu\text{s}; \delta \le 0.01 ; T_j = 25 ^{\circ}\text{C}$	-	400	-	mS
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	$I_D = 300 \text{ mA}; V_{DS} = 30 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	0.6	8.0	nC
Q_{GS}	gate-source charge	$T_j = 25 ^{\circ}\text{C}$	-	0.2	-	nC
Q_{GD}	gate-drain charge		-	0.2	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 10 \text{ V}; f = 1 \text{ MHz};$	-	30	50	pF
C _{oss}	output capacitance	$T_j = 25 ^{\circ}\text{C}$	-	7	-	pF
C _{rss}	reverse transfer capacitance		-	4	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 250 \Omega; V_{GS} = 10 \text{ V};$	-	3	6	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	4	-	ns
t _{d(off)}	turn-off delay time		-	10	20	ns
t _f	fall time		-	5	-	ns
Source-drai	n diode					
V_{SD}	source-drain voltage	$I_S = 115 \text{ mA}; V_{GS} = 0 \text{ V}; T_i = 25 \text{ °C}$	0.47	0.75	1.1	V

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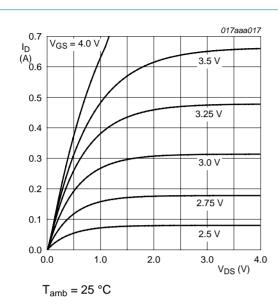
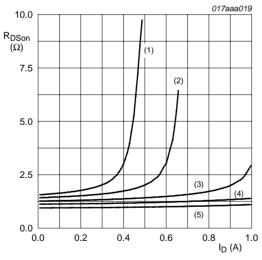


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_{amb} = 25 \, ^{\circ}C$

(1) $V_{GS} = 3.25 \text{ V}$

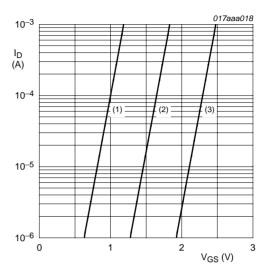
(2) $V_{GS} = 3.5 \text{ V}$

(3) $V_{GS} = 4 V$

(4) $V_{GS} = 5 \text{ V}$

 $(5) V_{GS} = 10 V$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



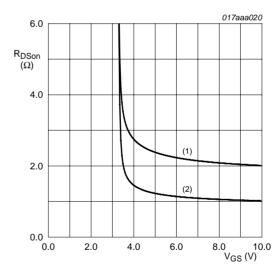
 $T_{amb} = 25 \, ^{\circ}C; \, V_{DS} = 5 \, V$

(1) minimum values

(2) typical values

(3) maximum values

Fig 7. Sub-threshold drain current as a function of gate-source voltage



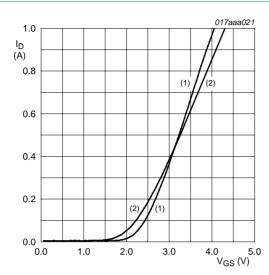
 $I_D = 500 \text{ mA}$

(1) $T_{amb} = 150 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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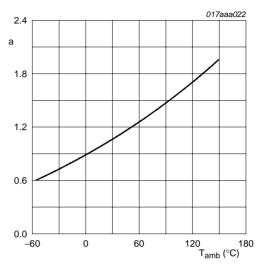


 $V_{DS} > I_D \times R_{DSon}$

(1) $T_{amb} = 25 \, ^{\circ}C$

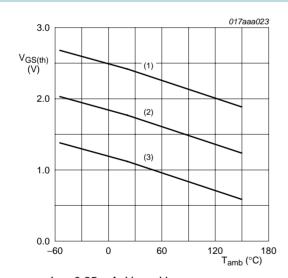
(2) $T_{amb} = 150 \, ^{\circ}C$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$

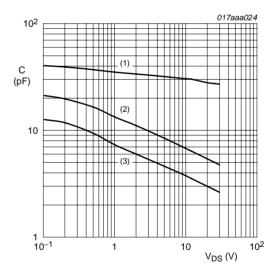
Fig 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values



 I_D = 0.25 mA; V_{DS} = V_{GS}

- (1) maximum values
- (2) typical values
- (3) minimum values

Fig 12. Gate-source threshold voltage as a function of ambient temperature



 $f = 1 MHz; V_{GS} = 0 V$

- (1) C_{iss}
- (2) Coss
- (3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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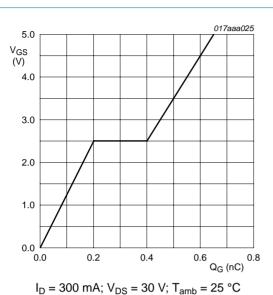


Fig 14. Gate-source voltage as a function of gate charge; typical values

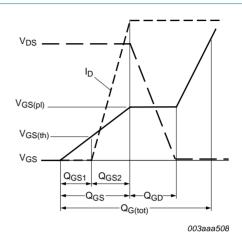
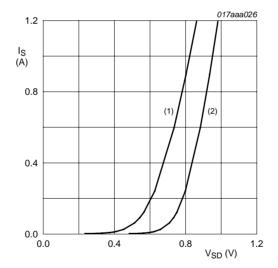


Fig 15. Gate charge waveform definitions



 $V_{GS} = 0 V$

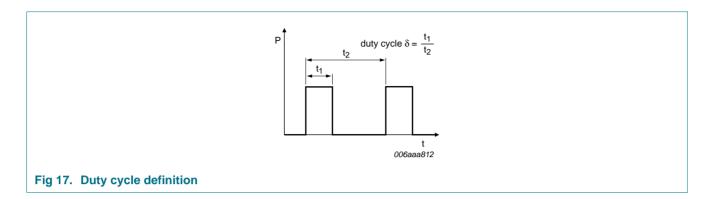
(1) $T_{amb} = 150 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

Fig 16. Source current as a function of source-drain voltage; typical values

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8. Test information



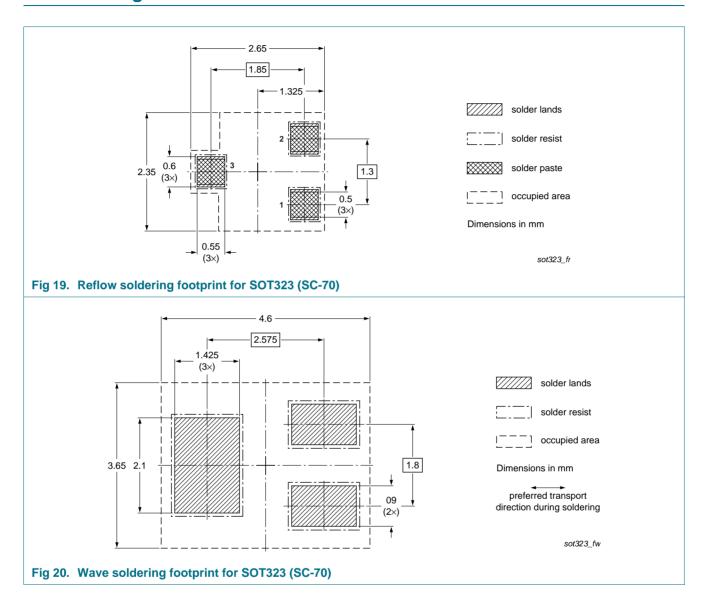
9. Package outline

Plastic surface-mounted package; 3 leads **SOT323** В Α Х = v M A Q **←** | w (M) B е detail X 2 mm scale **DIMENSIONS (mm are the original dimensions)** UNIT D Ε Q С bp е ΗE Lp w max 0.4 1.1 0.25 2.2 1.35 0.45 0.23 0.2 mm 1.3 0.65 0.2 8.0 0.10 1.15 REFERENCES EUROPEAN OUTLINE **ISSUE DATE** PROJECTION **VERSION** IEC **JEDEC** JEITA 04-11-04 SOT323 SC-70 06-03-16

Fig 18. Package outline SOT323 (SC-70)

60 V, 310 mA N-channel Trench MOSFET

10. Soldering



60 V, 310 mA N-channel Trench MOSFET

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
2N7002PW v.2	20100729	Product data sheet	-	2N7002PW_1
Modifications:	 Correction of t 	hermal values.		
	 Correction of v 	arious characteristics values	s including related grap	hs.
2N7002PW_1	20100422	Product data sheet	-	-

60 V, 310 mA N-channel Trench MOSFET

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Product data sheet

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14. Contents

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Date of release: 29 July 2010 Document identifier: 2N7002PW

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