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**November 2013** 

## FQU4N50TU\_WS

### N-Channel QFET® MOSFET

500 V, 2.6 A, 2.7 Ω

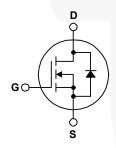
#### **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

#### **Features**

- 2.6 A, 500 V,  $R_{DS(on)}$  = 2.7  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 1.3 A
- Low Gate Charge (Typ. 10 nC)
- · Low Crss (Typ. 6.0 pF)
- 100% Avalanche Tested





#### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQU4N50TU_WS	Unit
V <sub>DSS</sub>	Drain-Source Voltage		500	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		2.6	Α
	- Continuous (T <sub>C</sub> = 100°C)		1.64	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	10.4	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		260	mJ
I <sub>AR</sub>	Avalanche Current (Note 1		2.6	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		4.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *		2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C)		45	W
	- Derate above 25°C		0.36	W/°C
$T_J$ , $T_{STG}$	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FQU4N50TU_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.78	
Ъ	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU4N50TU WS	FQU4N50S	IPAK	Tube	N/A	N/A	75 units

#### Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V, } I_D = 250  \mu\text{A}$	500			V
ΔBV <sub>DSS</sub> / ΔT	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.38		V/°C
I <sub>DSS</sub>	7 0 1 1/1 5 1 0 1	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			1	μΑ
Zero Gate Voltage Dr	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I = 1.3 A		2.0	2.7	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.3 A		2.6		S
Dynam	ic Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		350	460	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		55	70	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			6	8	pF
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 3.4 A,		12	30	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25 \Omega$		45	100	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	- 1.6 = 3 = 1		20	50	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		30	70	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 3.4 A,		10	13	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.5		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)	/	4.7		nC
Drain-S	ource Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2.6	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				10.4	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.6 A	-		1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.4 A,		210		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dl <sub>F</sub> / dt = 100 A/μs		1.15	//	μС

**Notes:** 1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 68 mH,  $I_{AS}$  = 2.6 A,  $V_{DD}$  = 50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C. 3.  $I_{SD} \le 3.4$  A, di/dt  $\le 200$  A/ $\mu$ s ,  $V_{DD} \le BV_{DSS}$ , starting  $T_{J}$  = 25°C. 4. Essentially independent of operating temperature.

### **Typical Characteristics**

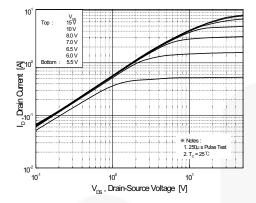


Figure 1. On-Region Characteristics

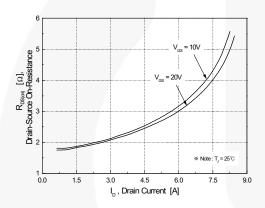


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

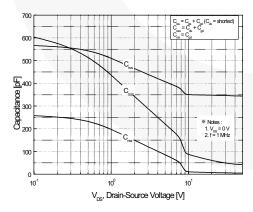


Figure 5. Capacitance Characteristics

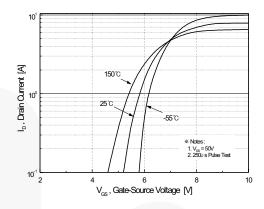


Figure 2. Transfer Characteristics

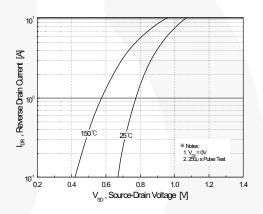


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

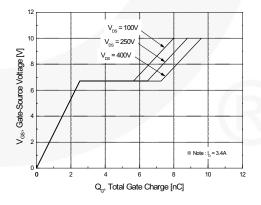


Figure 6. Gate Charge Characteristics

### Typical Characteristics (Continued)

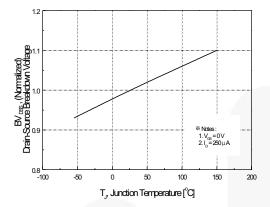


Figure 7. Breakdown Voltage Variation vs. Temperature

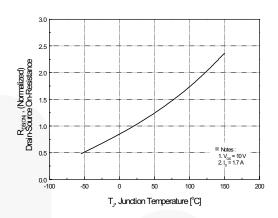


Figure 8. On-Resistance Variation vs. Temperature

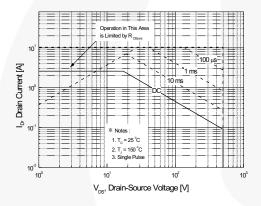


Figure 9. Maximum Safe Operating Area

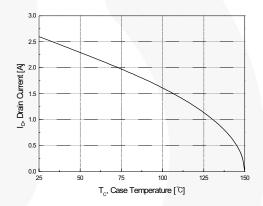


Figure 10. Maximum Drain Current vs. Case Temperature

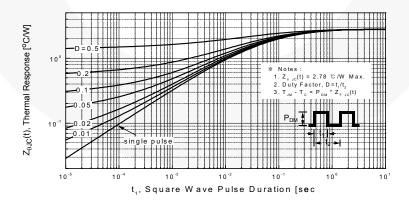


Figure 11. Transient Thermal Response Curve

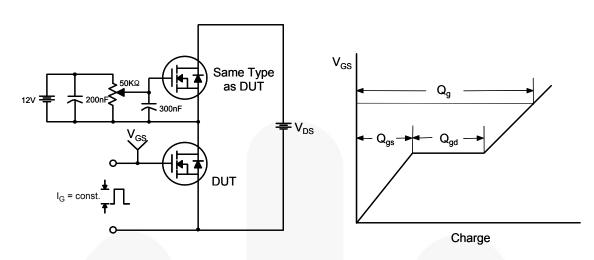


Figure 12. Gate Charge Test Circuit & Waveform

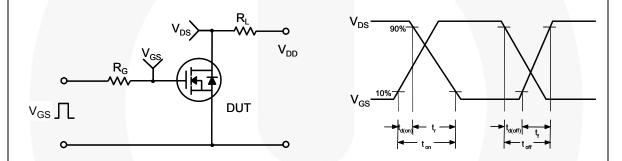


Figure 13. Resistive Switching Test Circuit & Waveforms

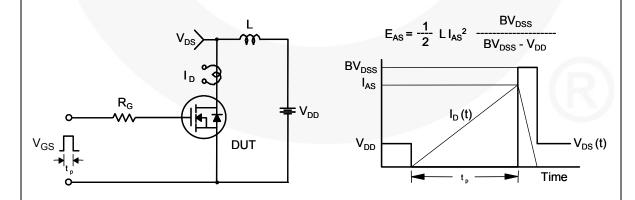


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

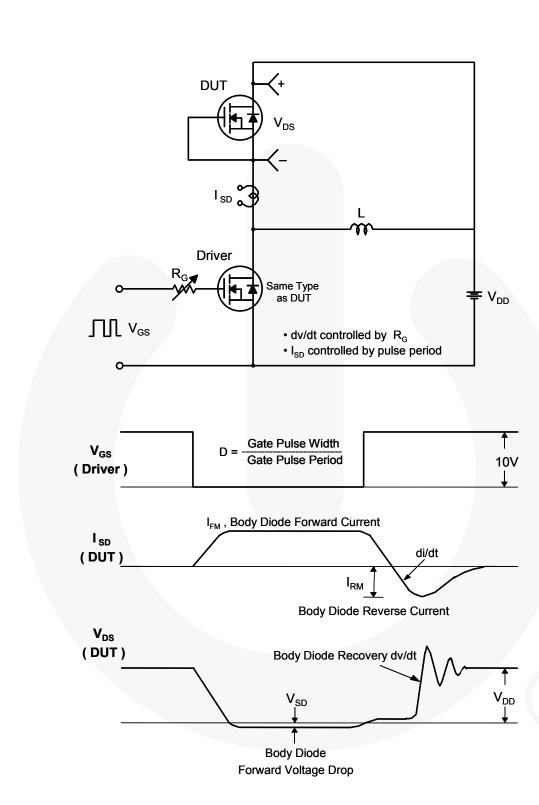


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

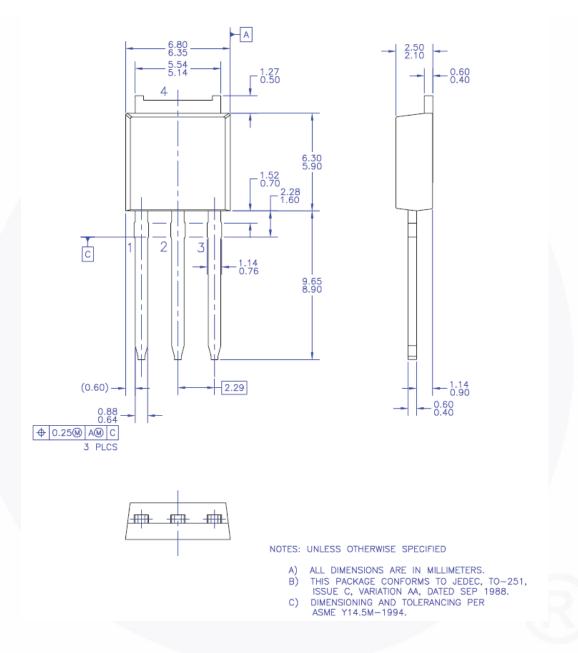


Figure 16. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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