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March 2015

FDMS5672

N-Channel UltraFET Trench $^{\mbox{\scriptsize 0}}$ MOSFET 60V, 22A, 11.5m $_{\mbox{\scriptsize Ω}}$

Features

- Max $r_{DS(on)}$ = 11.5m Ω at V_{GS} = 10V, I_D = 10.6A
- Max $r_{DS(on)}$ = 16.5m Ω at V_{GS} = 6V, I_D = 8A
- Typ Qg = 32nC at $V_{GS} = 10V$
- Low Miller Charge
- Optimized Efficiency at High Frequencies
- RoHS Compliant

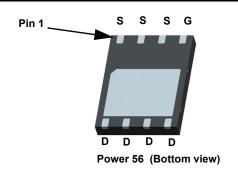


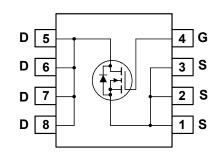
General Description

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Application

■ DC - DC Conversion





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted.

Symbol	Param		Ratings	Units	
V _{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25°C	(Note 5)	65	
	-Continuous	T _C = 100°C	(Note 5)	39	^
ID	-Continuous	T _A = 25°C	(Note 1a)	10.6	Α
	-Pulsed	(Note 4		176	
E _{AS} Single Pulse Avalanche Energy			(Note 3)	337	mJ
Б	Power Dissipation	T _C = 25°C		78	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.6	°C/W
R _{e.IA}	Thermal Resistance, Junction to Ambient (Note 1a		50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS5672	FDMS5672	Power 56	13"	12mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Characteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		59		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48V, V _{GS} = 0V			1	μА
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20V, V _{DS} = 0V			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25°C		-11		mV/°C
	Drain to Source On Resistance	V _{GS} = 10V, I _D = 10.6A		9.4	11.5	- mΩ
rno()		$V_{GS} = 6V$, $I_D = 8A$		13.0	16.5	
r _{DS(on)}		$V_{GS} = 10V$, $I_D = 10.6A$, $T_J = 125$ °C		15.0	18.0	
g _{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 10.6A$		26		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 20V V - 0V	2100	2800	pF
C _{oss}	Output Capacitance	V _{DS} = 30V, V _{GS} = 0V, f = 1MHz	375	500	рF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112	120	180	pF
R_g	Gate Resistance	f = 1MHz	1.2		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		1	6 2	9 r	ns
t _r	Rise Time	V _{DD} = 30V, I _D = 10.6A	1	7 3	1 r	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GEN} = 6\Omega$	2:	2 3	5 r	ns
t _f	Fall Time		8	1	6 r	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$ $V_{DD} = 30V$	3:	2 4	5 r	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 30V$ $I_{D} = 10.6A$	1)	r	nC
Q_{gd}	Gate to Drain "Miller" Charge	ID = 10.0A	8.	3	r	nC

Drain-Source Diode Characteristics

	V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 10.6A$ (Note 2)		0.80	1.20	V
-	t _{rr}	Reverse Recovery Time	$I_F = 10.6A$, di/dt = $100A/\mu s$ 35 53 42 63		ns		
	Q _{rr}	Reverse Recovery Charge			42	63	nC

1. $R_{\theta JC}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in² pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < $300\mu s$, Duty cycle < 2.0%. 3. Starting T $_J$ = 25° C, L = 3mH, I $_{AS}$ = 15A, V $_{DD}$ = 60V, V $_{GS}$ = 10V. 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_{.1} = 25°C unless otherwise noted.

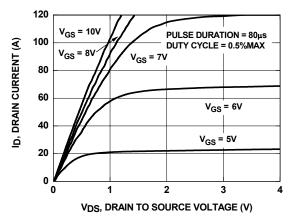


Figure 1. On Region Characteristics

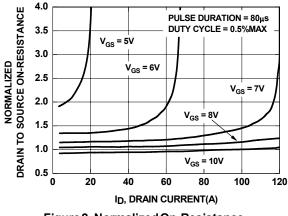


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

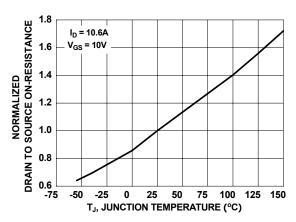


Figure 3. Normalized On Resistance vs. Junction Temperature

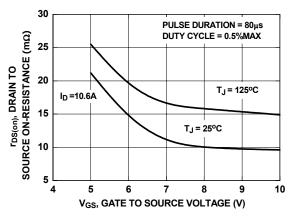


Figure 4. On-Resistance vs. Gate to Source Voltage

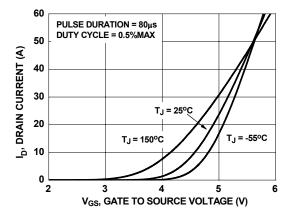


Figure 5. Transfer Characteristics

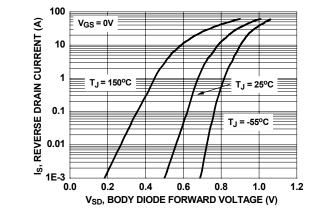


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

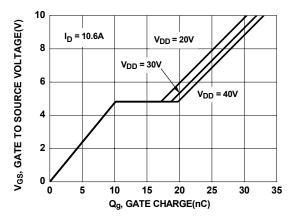


Figure 7. Gate Charge Characteristics

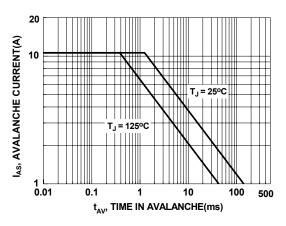


Figure 9. Unclamped Inductive Switching Capability

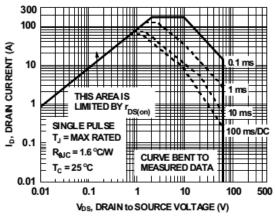


Figure 11. Forward Bias Safe Operating Area

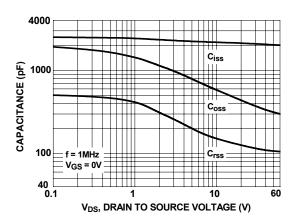


Figure 8. Capacitance vs. Drain to Source Voltage

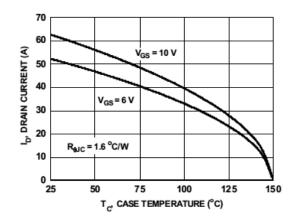


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

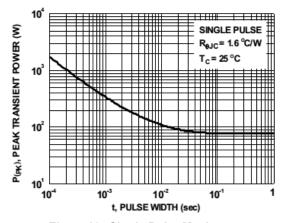


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

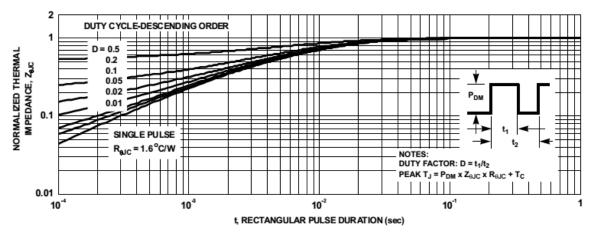
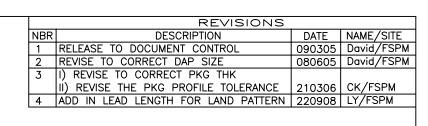
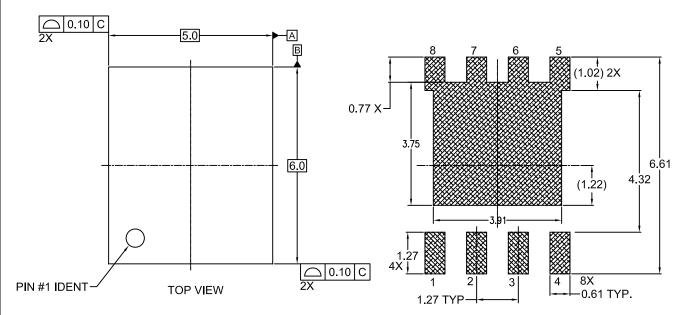
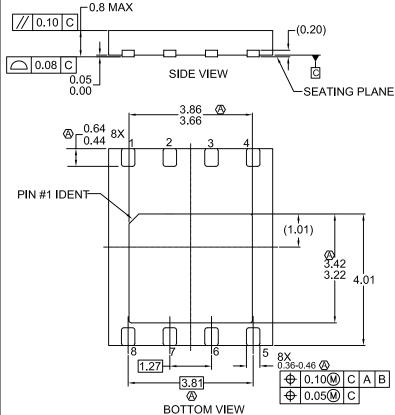


Figure 13. Transient Thermal Response Curve







RECOMMENDED LAND PATTERN

NOTES:

- $\begin{tabular}{ll} \textcircled{A} DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229. \end{tabular}$
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE
- E. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- F. DRAWING FILENAME: MKT-MLP08Grev4

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