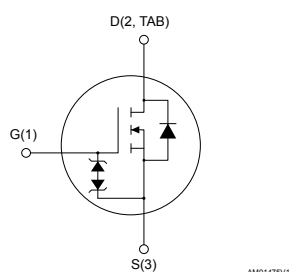


N-channel 500 V, 0.45 Ω typ., 8 A MDmesh™ M2 Power MOSFETs in DPAK and TO-220FP packages



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)max.}$	I_D	Package
STD11N50M2	550 V	0.53 Ω	8 A	DPAK
STF11N50M2				TO-220FP

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.



Product status

STD11N50M2

STF11N50M2

Product summary

Order code	STD11N50M2
Marking	11N50M2
Package	DPAK
Packing	Tape and reel
Order code	STF11N50M2
Marking	11N50M2
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	8		A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	5		A
$I_{DM}^{(1)}$	Drain current (pulsed)	32		A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	85	25	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15		V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)		2.5	kV
T_j	Operating junction temperature range	-55 to 150		$^{\circ}\text{C}$
T_{stg}	Storage temperature range			

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case	1.47	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50		$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	2	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	190	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	500			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 500 V, V _{GS} = 0 V			1	μA
		V _{DS} = 500 V, V _{GS} = 0 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 4 A		0.45	0.53	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	395	-	pF
C _{oss}	Output capacitance			26		
C _{rss}	Reverse transfer capacitance			1		
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 to 400 V	-	108	-	pF
R _g	Gate input resistance	f = 1 MHz open drain	-	6.3	-	Ω
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 8 A, V _{GS} = 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)	-	12	-	nC
Q _{gs}	Gate-source charge			2		
Q _{gd}	Gate-drain charge			6.4		

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 250 V, I _D = 4 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	11	-	ns
t _r	Rise time			9		
t _{d(off)}	Turn-off delay time			8		
t _f	Fall time			28.5		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				32	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	258		ns
Q_{rr}	Reverse recovery charge			1.84		μC
I_{RRM}	Reverse recovery current			14.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	370		ns
Q_{rr}	Reverse recovery charge			2.87		μC
I_{RRM}	Reverse recovery current			15.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

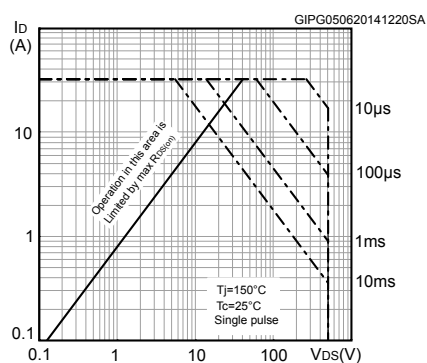
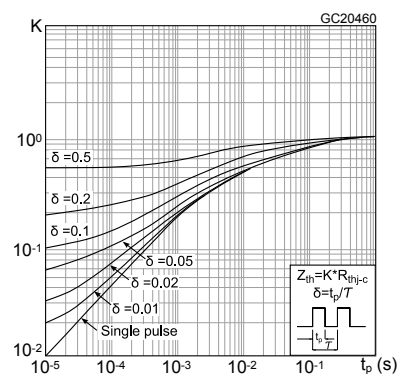
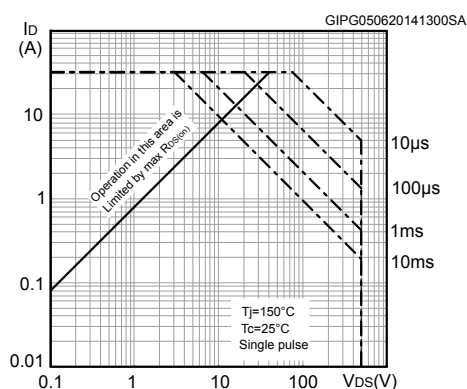
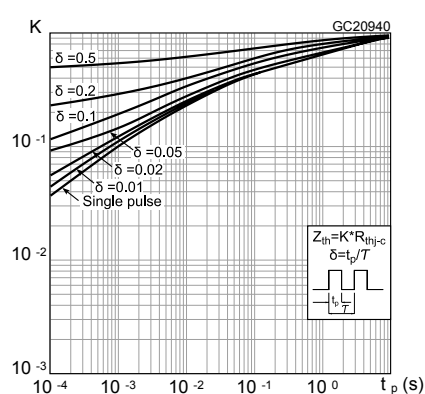
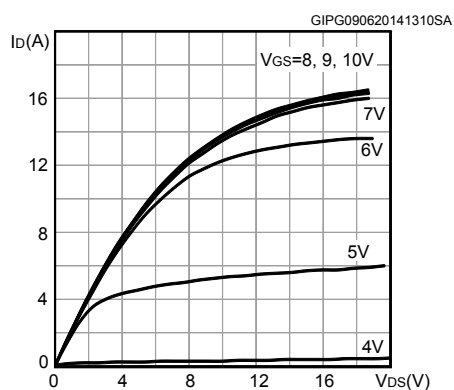
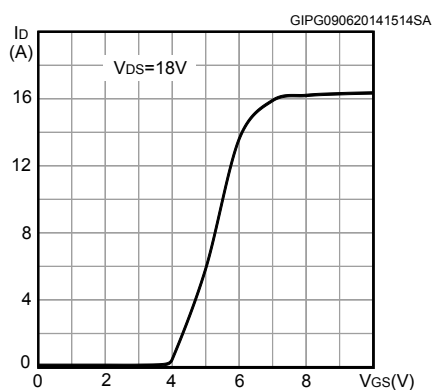
Figure 1. Safe operating area for DPAK

Figure 2. Thermal impedance for DPAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Output characteristics

Figure 6. Transfer characteristics


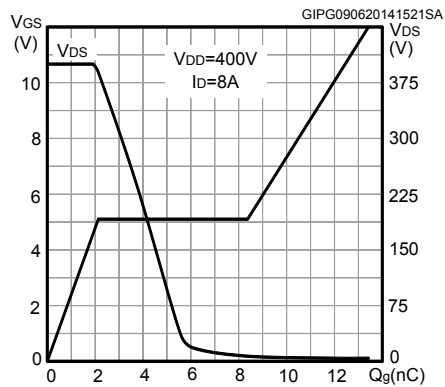
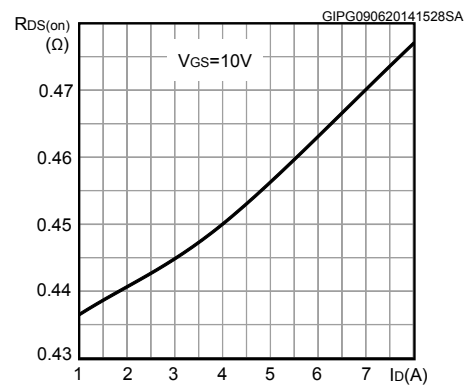
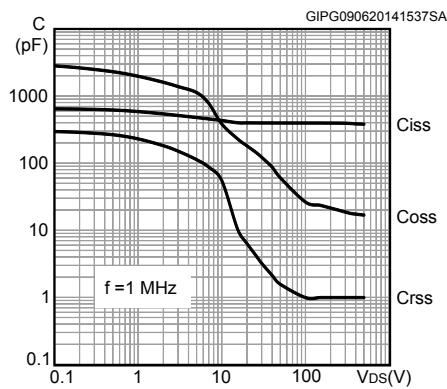
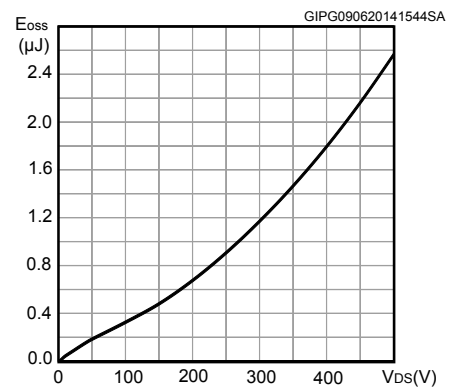
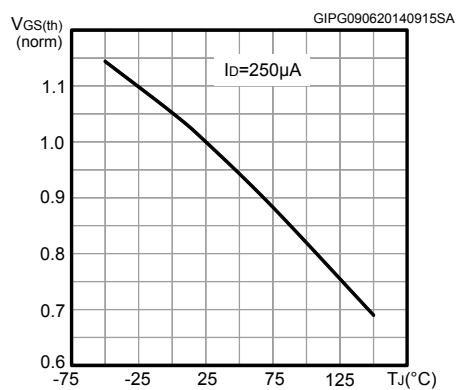
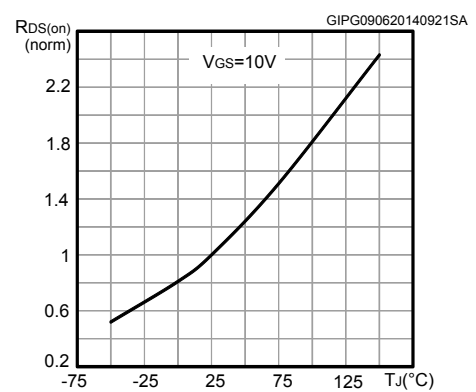
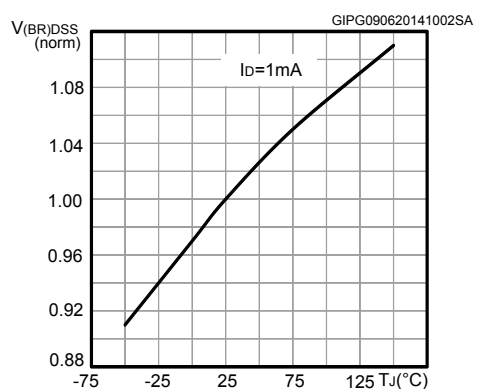
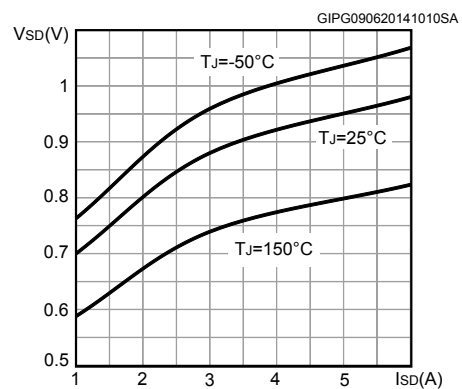
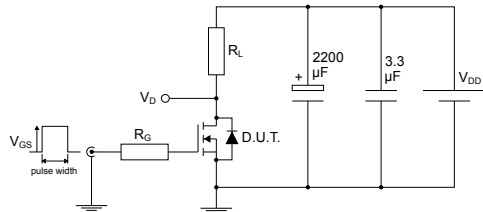
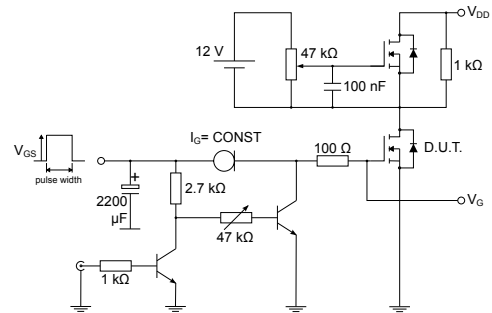
Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance

Figure 9. Capacitance variations

Figure 10. Output capacitance stored energy

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

Figure 14. Source-drain diode forward characteristics


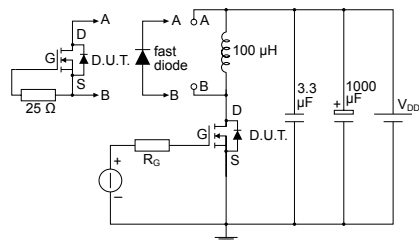
3 Test circuits

Figure 15. Test circuit for resistive load switching times


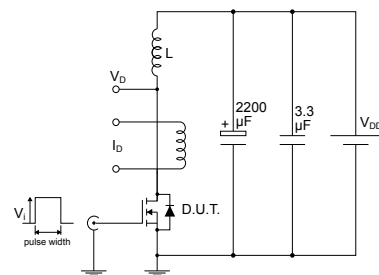
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Figure 16. Test circuit for gate charge behavior


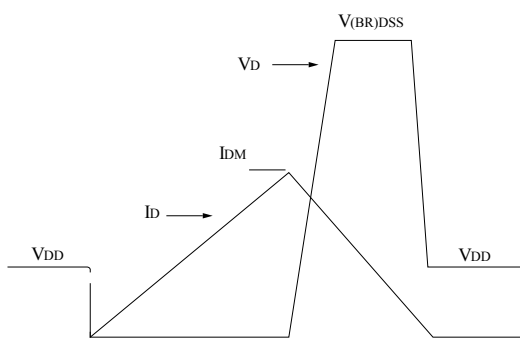
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Figure 17. Test circuit for inductive load switching and diode recovery times


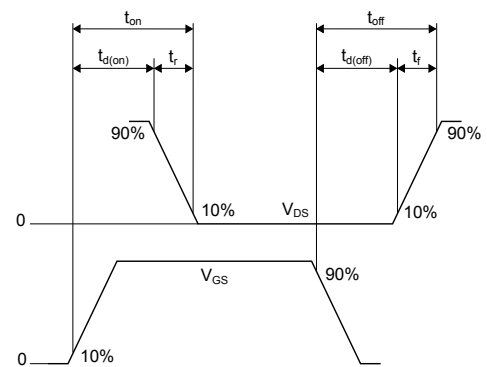
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Figure 18. Unclamped inductive load test circuit


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Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


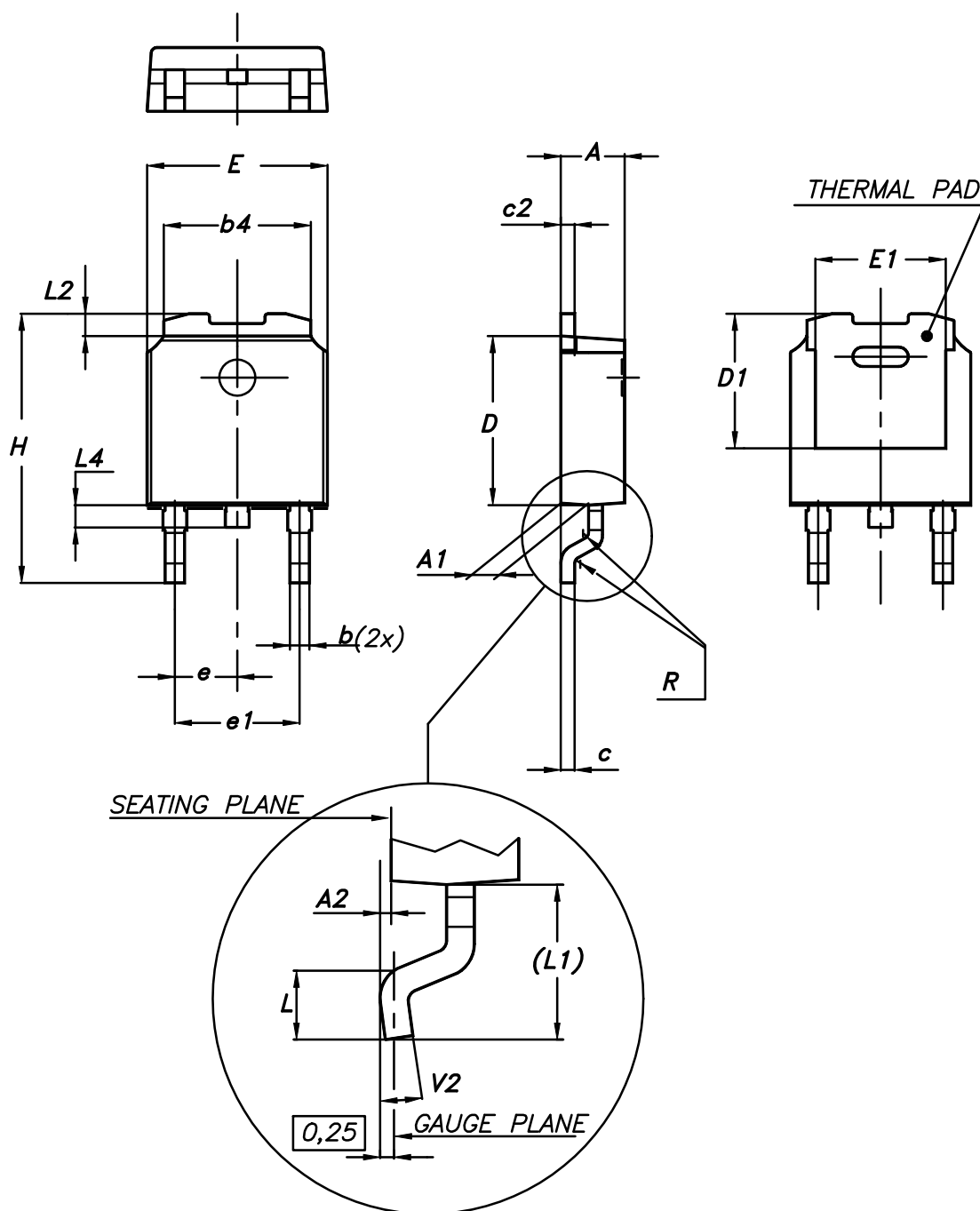
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 21. DPAK (TO-252) type A package outline



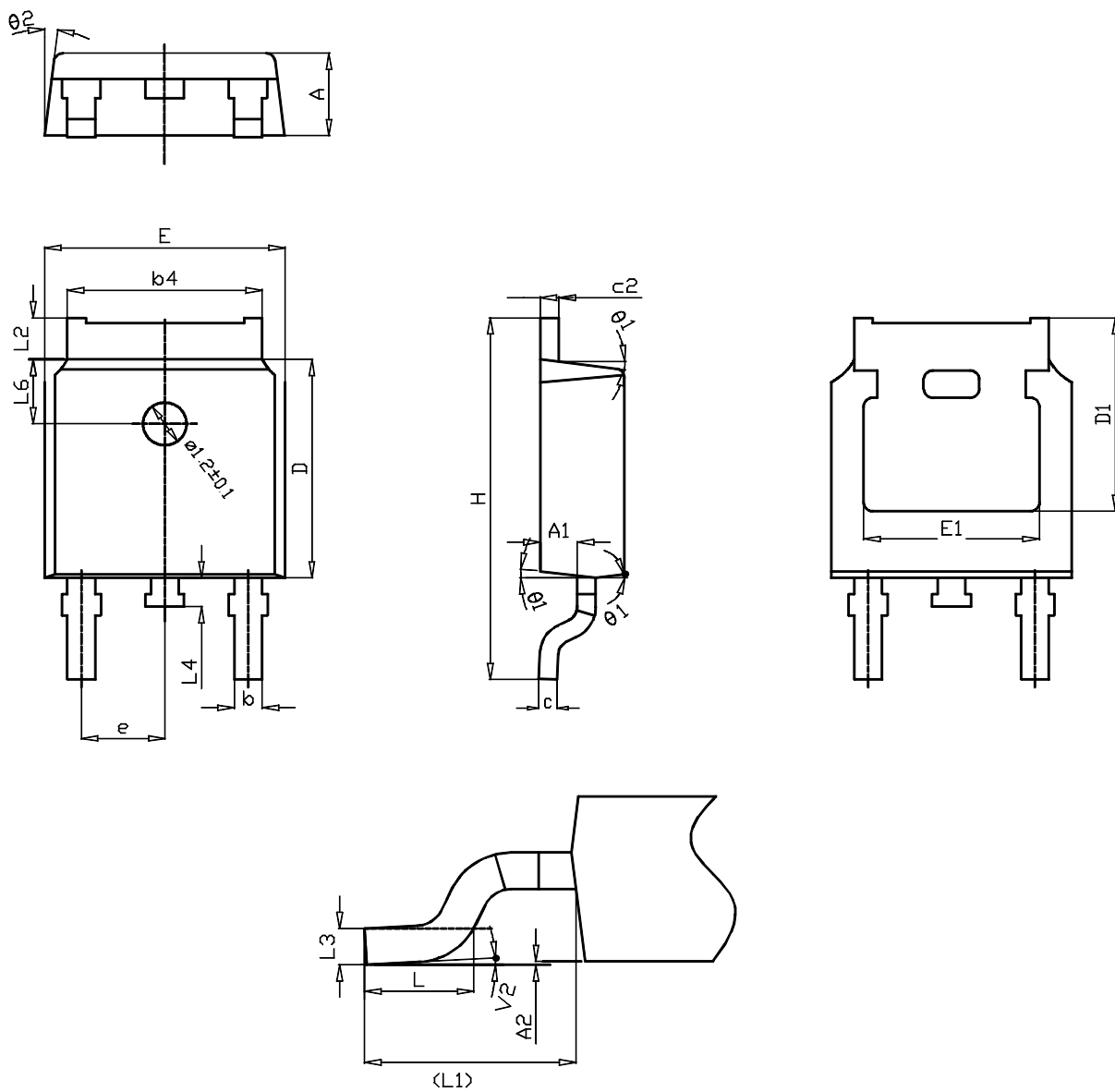
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Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 22. DPAK (TO-252) type C package outline



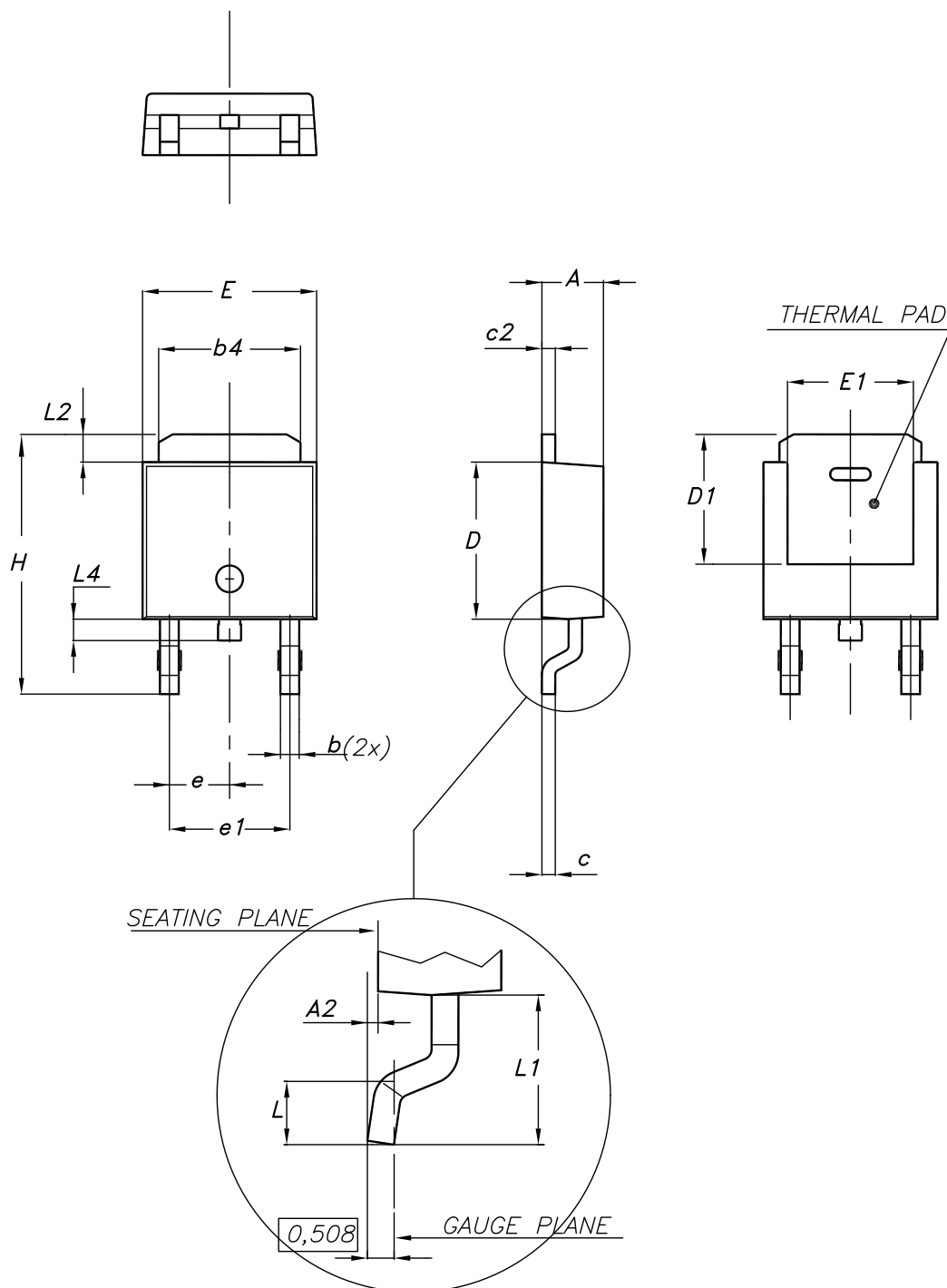
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Table 9. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.3 DPAK (TO-252) type E package information

Figure 23. DPAK (TO-252) type E package outline

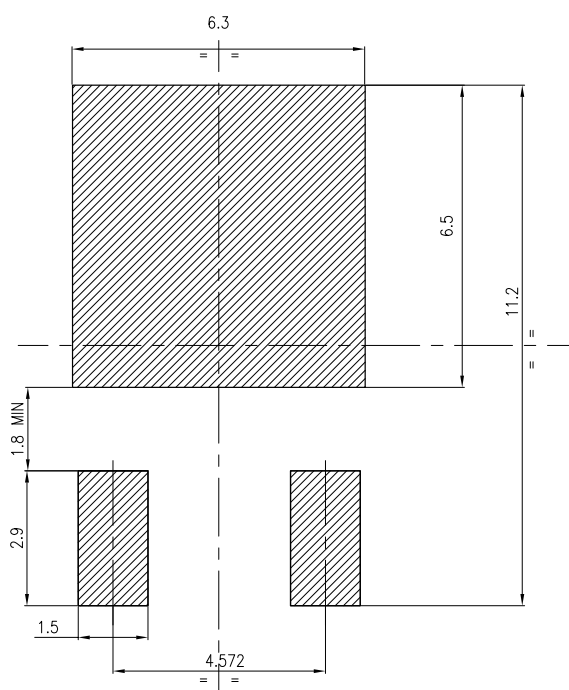


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Table 10. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



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4.4 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline

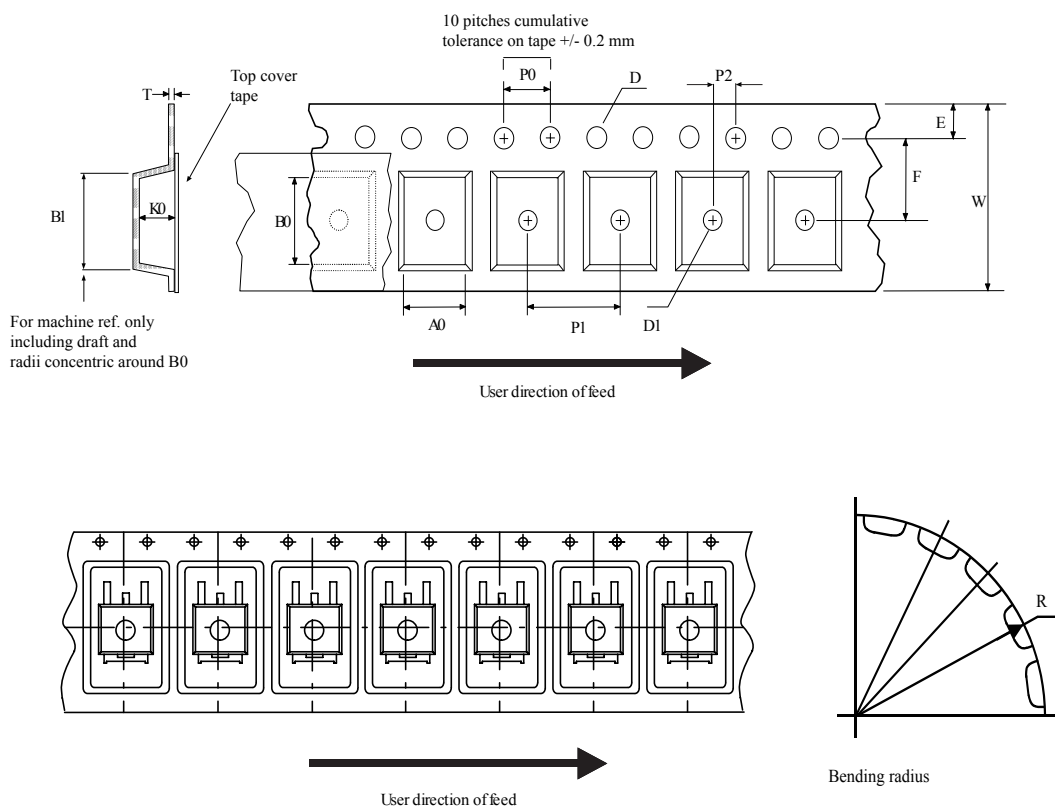
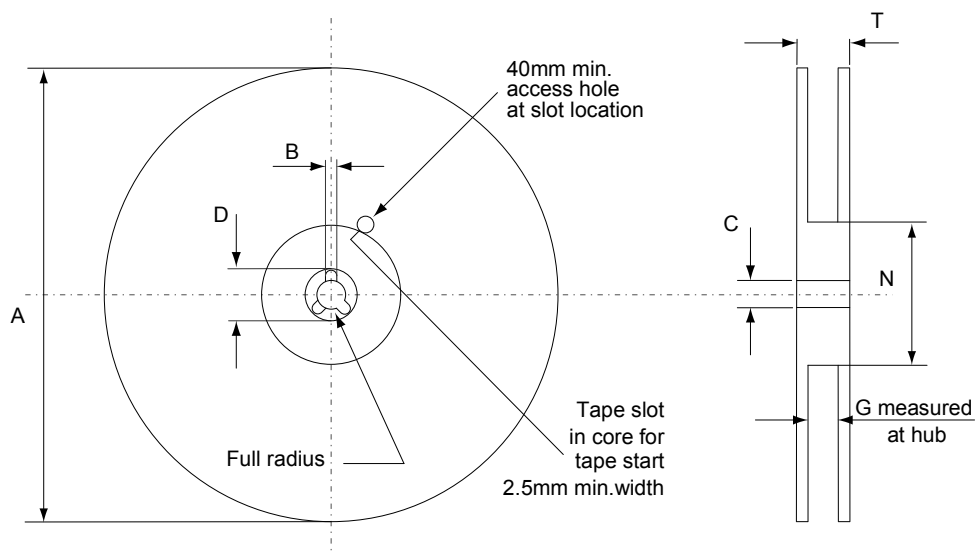


Figure 26. DPAK (TO-252) reel outline


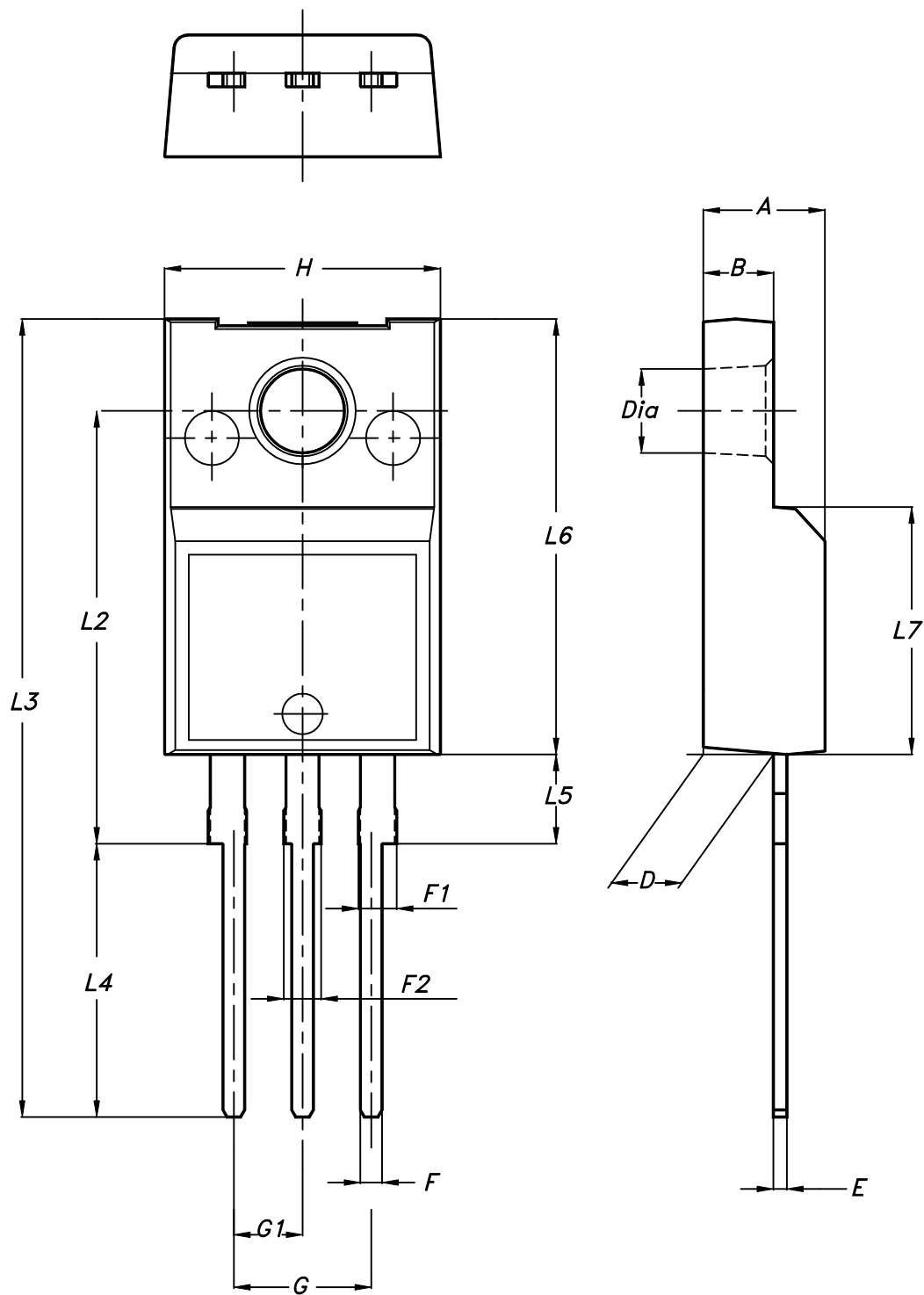
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Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.5 TO-220FP package information

Figure 27. TO-220FP package outline



7012510_Rev_12_B

Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 13. Document revision history

Date	Version	Changes
12-Mar-2014	1	First release.
17-Jun-2014	2	– Modified: title – Modified: dv/dt values in <i>Table 2</i> – Modified: values in <i>Table 4</i> – Modified: $R_{DS(on)}$ value in <i>Table 5</i> – Modified: the entire typical values in <i>Table 6</i>, <i>7</i> and <i>8</i> – Added: <i>Section 2.1: Electrical characteristics (curves)</i> – Updated: <i>Section 4: Package mechanical data</i> – Minor text changes
26-Oct-2018	3	Removed maturity status indication from cover page. The document status is production data. Modified title, features and description on cover page. Updated Section 4 Package information. Minor text changes.

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4.4	DPAK (TO-252) packing information.....	15
4.5	TO-220FP package information	17
	Revision history	20

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