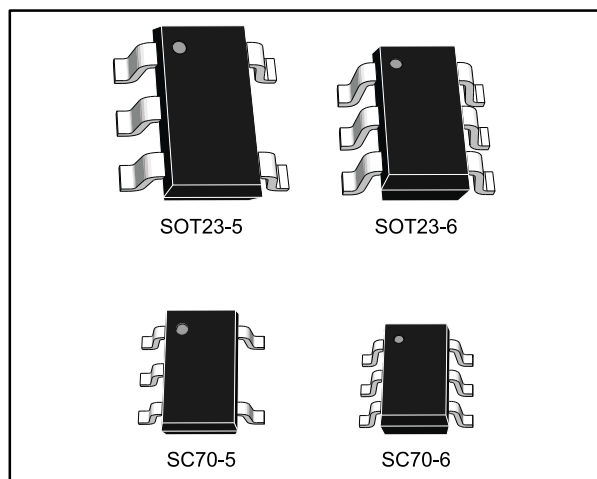


## Micropower with high merit factor CMOS operational amplifiers

Datasheet - production data



### Features

- Low supply voltage: 1.5 V – 5.5 V
- Rail-to-rail input and output
- Low input offset voltage: 800  $\mu$ V max (A version)
- Low power consumption: 29  $\mu$ A typical
- Gain bandwidth product: 1.3 MHz typical
- Stable when used in gain configuration
- Micropackages: SOT23-5/6, SC70-5/6
- Low input bias current: 1 pA typical
- Extended temperature range: -40 to 125 °C
- 4 kV human body model

### Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

### Description

The TSV6290 and the TSV6291 are single operational amplifiers with a high bandwidth which consume only 29  $\mu$ A. They must be used in a gain configuration ( $G < -3$ ,  $G > 4$ ).

With a very low input bias current and low offset voltage (800  $\mu$ V maximum for the A version), the TSV629x family of devices is ideal for applications requiring precision. The devices can operate at a power supply ranging from 1.5 to 5.5 V, and therefore suit battery-powered devices, extending battery life.

The TSV6290 comes with a shutdown function.

The TSV6290 and TSV6291 present a high tolerance to ESD, sustaining 4 kV for the human body model.

The TSV6290 and TSV6291 are offered in SOT23-5/6 and SC70-5/6 micropackages, with extended temperature ranges from -40 °C to 125 °C.

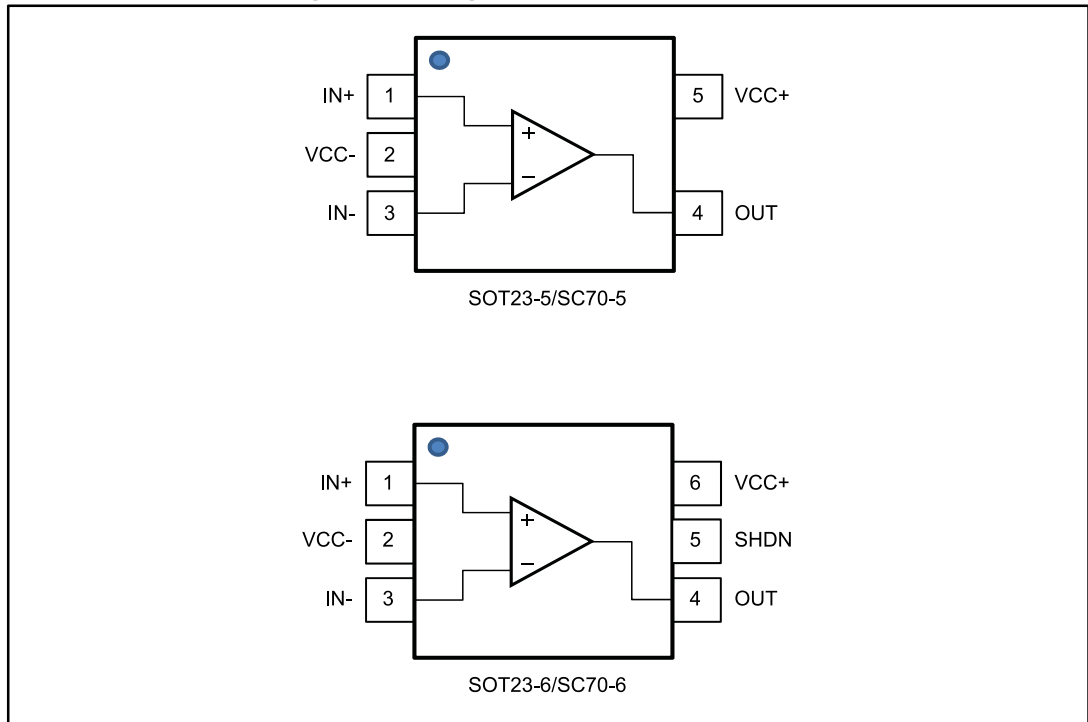
All these features make the TSV629x ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

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# 1 Package pin connections

Figure 1: Package pin connections (top view)



## 2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>	6	V	
V <sub>id</sub>	Differential input voltage <sup>(2)</sup>	±V <sub>CC</sub>		
V <sub>in</sub>	Input voltage <sup>(3)</sup>	(V <sub>CC-</sub> ) - 0.2 to (V <sub>CC+</sub> ) + 0.2		
I <sub>in</sub>	Input current <sup>(4)</sup>	10	mA	
$\overline{\text{SHDN}}$	Shutdown voltage <sup>(3)</sup>	(V <sub>CC-</sub> ) - 0.2 to (V <sub>CC+</sub> ) + 0.2	V	
T <sub>stg</sub>	Storage temperature	-65 to 150	°C	
T <sub>j</sub>	Maximum junction temperature	150		
R <sub>thja</sub>	Thermal resistance junction-to-ambient <sup>(5)/(6)</sup>	SOT23-5	250	°C/W
		SOT23-6	240	
		SC70-5	205	
		SC70-6	232	
ESD	HBM: human body model <sup>(7)</sup>	4	kV	
	MM: machine model <sup>(8)</sup>	300	V	
	CDM: charged device model <sup>(9)</sup>	1.5	kV	
	Latch-up immunity	200	mA	

**Notes:**

- <sup>(1)</sup>All voltage values, except differential voltage, are with respect to network ground terminal.
- <sup>(2)</sup>Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- <sup>(3)</sup>V<sub>CC</sub> - V<sub>in</sub> must not exceed 6 V, V<sub>in</sub> must not exceed 6 V.
- <sup>(4)</sup>Input current must be limited by a resistor in series with the inputs.
- <sup>(5)</sup>R<sub>th</sub> are typical values.
- <sup>(6)</sup>Short-circuits can cause excessive heating and destructive dissipation.
- <sup>(7)</sup>Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- <sup>(8)</sup>Machine mode: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
- <sup>(9)</sup>Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	1.5 to 5.5	V
V <sub>icm</sub>	Common mode input voltage range	(V <sub>CC-</sub> ) - 0.1 to (V <sub>CC+</sub> ) + 0.1	
T <sub>oper</sub>	Operating free air temperature range	-40 to 125	°C

### 3 Electrical characteristics

Table 3: Electrical characteristics at (VCC+) = 1.8 V with (VCC-) = 0 V, Vicm = VCC/2, Tamb = 25 °C, and RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV6290, TSV6291			4	mV
		TSV6290A, TSV6291A			0.8	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV6290, TSV6291			6	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV6290A, TSV6291A			2	
DV <sub>io</sub>	Input offset voltage drift		2		μV/°C	
I <sub>io</sub>	Input offset current, V <sub>out</sub> = V <sub>CC</sub> /2 <sup>(1)</sup>			1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current, V <sub>out</sub> = V <sub>CC</sub> /2 <sup>(1)</sup>			1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio, 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	0 V to 1.8 V, V <sub>out</sub> = 0.9 V	53	74		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	51			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 kΩ, V <sub>out</sub> = 0.5 V to 1.3 V	78	95		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	73			
V <sub>OH</sub>	High-level output voltage, V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub>	R <sub>L</sub> = 10 kΩ		5	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 kΩ		4	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	Isink	V <sub>out</sub> = 1.8 V	6	12		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	4			
	Isource	V <sub>out</sub> = 0 V	6	10		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	4			
I <sub>CC</sub>	Supply current (per operator)	No load, V <sub>out</sub> = V <sub>CC</sub> /2		25	31	μA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			33	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF		1.1		MHz
Gain	Minimum gain for stability	Phase margin = 60°, R <sub>f</sub> = 10 kΩ, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 20 pF		4		V/V
				-3		
SR	Slew rate	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF, V <sub>out</sub> = 0.5 V to 1.3 V		0.33		V/μs

**Notes:**

<sup>(1)</sup>Guaranteed by design.

Table 4: Shutdown characteristics VCC = 1.8 V (TSV6290)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
I <sub>CC</sub>	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = (V_{CC-})$		2.5	50	nA
		$T_{\min} < T_{\text{op}} < 85\text{ }^{\circ}\text{C}$			200	
		$T_{\min} < T_{\text{op}} < 125\text{ }^{\circ}\text{C}$			1.5	$\mu\text{A}$
t <sub>on</sub>	Amplifier turn-on time	R <sub>L</sub> = 5 k $\Omega$ , V <sub>out</sub> = (V <sub>CC-</sub> ) to (V <sub>CC-</sub> ) + 0.2 V		300		ns
t <sub>off</sub>	Amplifier turn-off time	R <sub>L</sub> = 5 k $\Omega$ , V <sub>out</sub> = (V <sub>CC+</sub> ) - 0.5 to (V <sub>CC+</sub> ) - 0.7 V		30		
V <sub>IH</sub>	$\overline{\text{SHDN}}$ logic high		1.3			V
V <sub>IL</sub>	$\overline{\text{SHDN}}$ logic low				0.5	
I <sub>IH</sub>	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = (V_{CC+})$		10		pA
I <sub>IL</sub>	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = (V_{CC-})$		10		
I <sub>OLeak</sub>	Output leakage in shutdown mode	$\overline{\text{SHDN}} = (V_{CC-})$		50		nA
		$T_{\min} < T_{\text{op}} < T_{\text{max}}$		1		

Table 5: (VCC+) = 3.3 V, (VCC-) = 0 V, Vicm = VCC/2, Tamb = 25 °C, RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV6290, TSV6291			4	mV
		TSV6290A, TSV6291A			0.8	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV6290, TSV6291			6	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV6290A, TSV6291A			2	
DV <sub>io</sub>	Input offset voltage drift		2			μV/°C
I <sub>io</sub>	Input offset current <sup>(1)</sup>			1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current <sup>(1)</sup>			1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio, 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	0 V to 3.3 V, V <sub>out</sub> = 1.65 V	57	79		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	53			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 kΩ, V <sub>out</sub> = 0.5 V to 2.8 V	81	98		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	76			
V <sub>OH</sub>	High-level output voltage, V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub>	R <sub>L</sub> = 10 kΩ		5	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 kΩ		4	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	Isink	V <sub>out</sub> = 5 V	23	45		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	20			
	Isource	V <sub>out</sub> = 0 V	23	38		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	20			
I <sub>cc</sub>	Supply current (per operator)	No load, V <sub>out</sub> = 2.5 V		26	33	μA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			35	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF		1.2		MHz
Gain	Minimum gain for stability	Phase margin = 60 °, R <sub>f</sub> = 10 kΩ, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 20 pF		4		V/V
					-3	
SR	Slew rate	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF, V <sub>out</sub> = 0.5 V to 2.8 V		0.4		V/μs

**Notes:**<sup>(1)</sup>Guaranteed by design.

Table 6: (VCC+) = 5 V, (VCC-) = 0 V, Vicm = VCC/2, Tamb = 25 °C, RL connected to VCC/2 (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV6290, TSV6291			4	mV
		TSV6290A, TSV6291A			0.8	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV6290, TSV6291			6	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> , TSV6290A, TSV6291A			2	
DV <sub>io</sub>	Input offset voltage drift		2			μV/°C
I <sub>io</sub>	Input offset current <sup>(1)</sup>			1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current <sup>(1)</sup>			1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio, 20 log (ΔV <sub>ic</sub> /ΔV <sub>io</sub> )	0 V to 5 V, V <sub>out</sub> = 2.5 V	60	80		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	55			
SVR	Supply voltage rejection ratio, 20 log (ΔV <sub>CC</sub> /ΔV <sub>io</sub> )	V <sub>CC</sub> = 1.8 to 5 V	75	102		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	73			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 kΩ, V <sub>out</sub> = 0.5 V to 4.5 V	85	98		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	80			
V <sub>OH</sub>	High-level output voltage, V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub>	R <sub>L</sub> = 10 kΩ		7	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 kΩ		6	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>out</sub> = 5 V	40	69		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	35			
	I <sub>source</sub>	V <sub>out</sub> = 0 V	40	74		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	35			
I <sub>CC</sub>	Supply current (per operator)	No load, V <sub>out</sub> = 2.5 V		30	36	μA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			38	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF		1.3		MHz
Gain	Minimum gain for stability	Phase margin = 60°, R <sub>f</sub> = 10 kΩ, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 20 pF		4		V/V
				-3		
SR	Slew rate	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 100 pF, V <sub>out</sub> = 0.5 V to 4.5 V		0.5		V/μs
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		70		nV/√Hz
THD	Total harmonic distortion	A <sub>v</sub> = -10, f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 100 kΩ, V <sub>icm</sub> = V <sub>CC</sub> /2, V <sub>in</sub> = 40 mV <sub>pp</sub>		0.15		%

**Notes:**<sup>(1)</sup>Guaranteed by design.



Table 7: Shutdown characteristics VCC = 5 V (TSV6290)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
I <sub>CC</sub>	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{\text{IL}}$		5	50	nA
		$T_{\text{min}} < T_{\text{op}} < 85\text{ }^{\circ}\text{C}$			200	
		$T_{\text{min}} < T_{\text{op}} < 125\text{ }^{\circ}\text{C}$			1.5	$\mu\text{A}$
t <sub>on</sub>	Amplifier turn-on time	R <sub>L</sub> = 5 k $\Omega$ , V <sub>out</sub> = (V <sub>CC-</sub> ) to (V <sub>CC-</sub> ) + 0.2 V		300		ns
t <sub>off</sub>	Amplifier turn-off time	R <sub>L</sub> = 5 k $\Omega$ , V <sub>out</sub> = (V <sub>CC+</sub> ) - 0.5 V to (V <sub>CC+</sub> ) - 0.7 V		30		
V <sub>IH</sub>	$\overline{\text{SHDN}}$ logic high		4.5			V
V <sub>IL</sub>	$\overline{\text{SHDN}}$ logic low				0.5	
I <sub>IH</sub>	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = (V_{\text{CC+}})$		10		pA
I <sub>IL</sub>	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = (V_{\text{CC-}})$		10		
I <sub>OLeak</sub>	Output leakage in shutdown mode	$\overline{\text{SHDN}} = (V_{\text{CC-}})$		50		
		$T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$		1		nA

### 4 Electrical characteristic curves

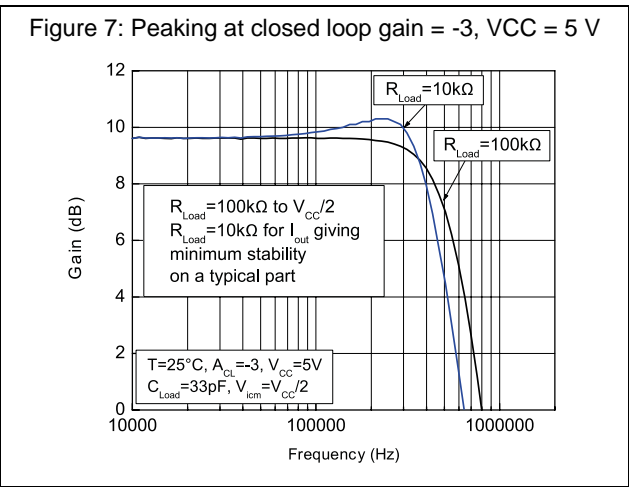
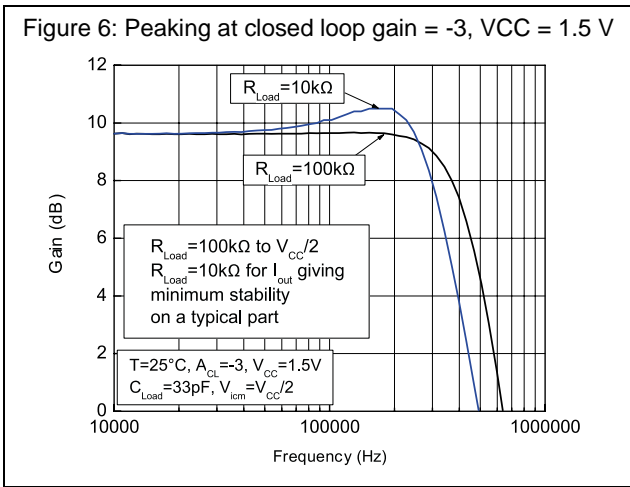
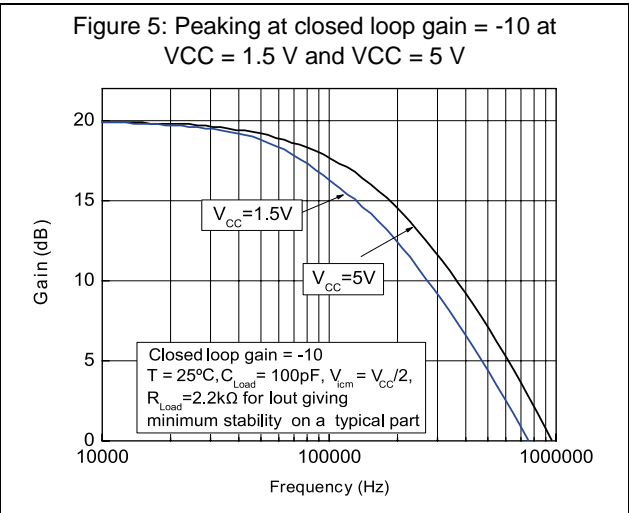
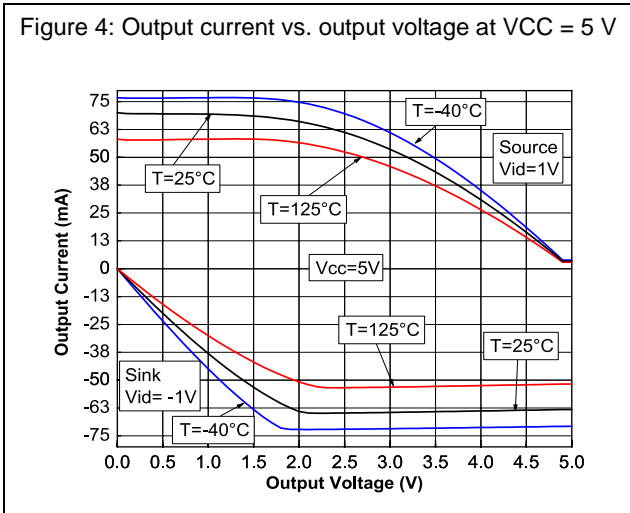
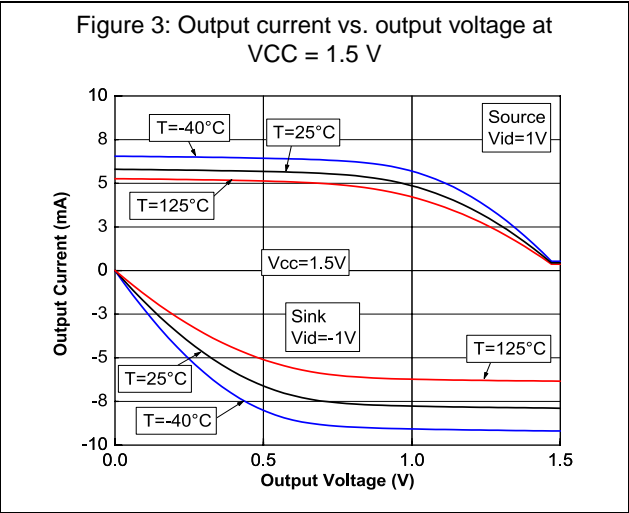
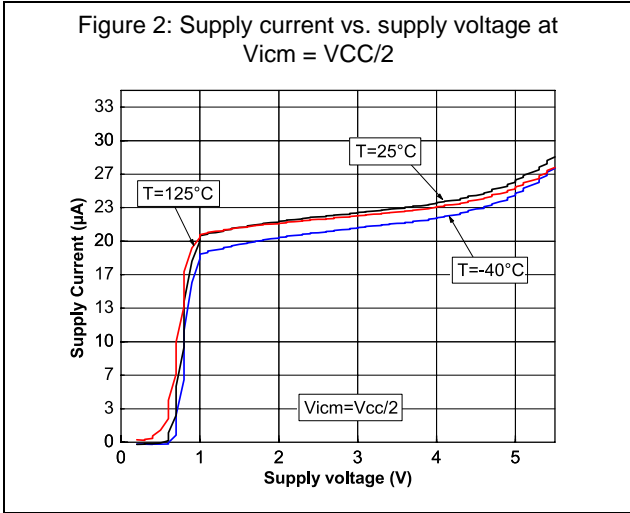


Figure 8: Positive slew rate vs. supply voltage in closed loop

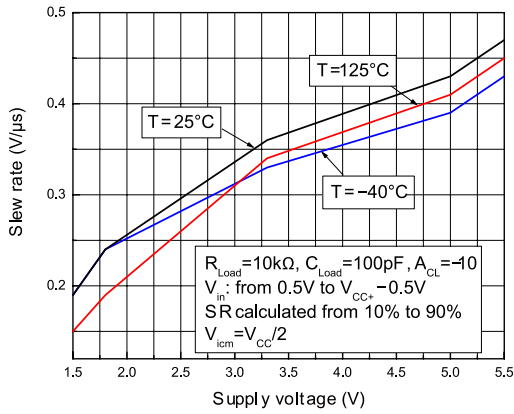


Figure 9: Negative slew rate vs. supply voltage in closed loop

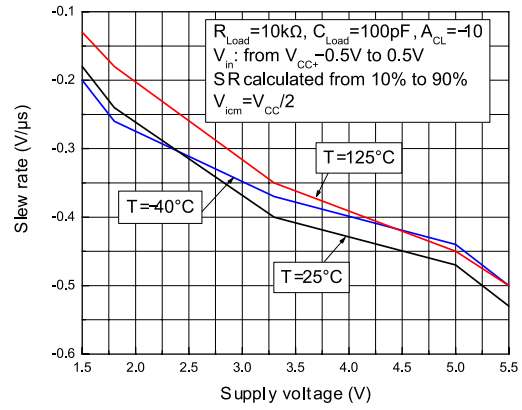


Figure 10: Slew rate vs. supply voltage in open loop

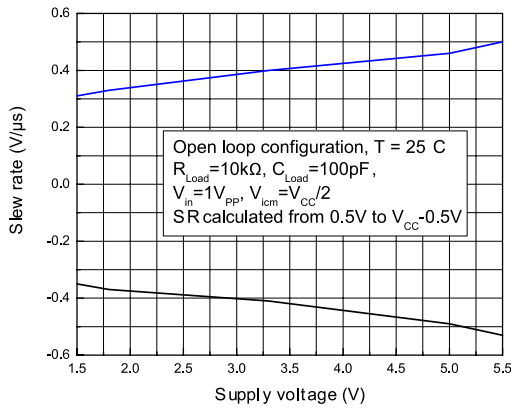


Figure 11: Slew rate timing in open loop

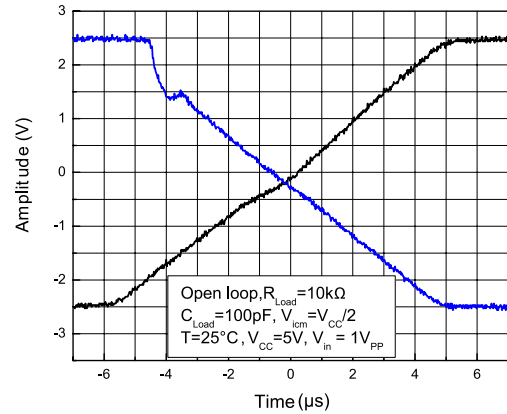


Figure 12: Slew rate timing in closed loop

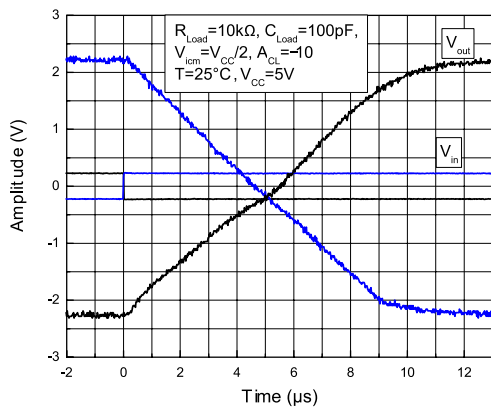
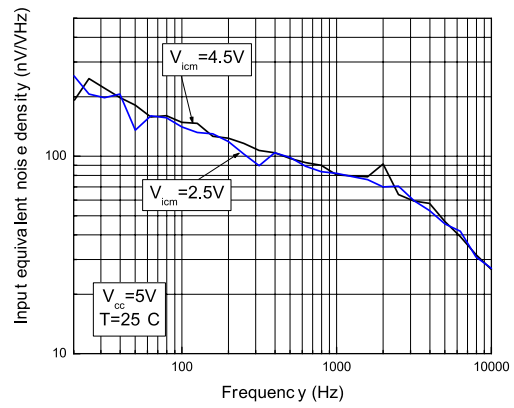


Figure 13: Noise at VCC = 5 V



Electrical characteristic curves

TSV6290, TSV6290A, TSV6291, TSV6291A

Figure 14: Distortion + noise vs. output voltage at VCC = 1.8 V

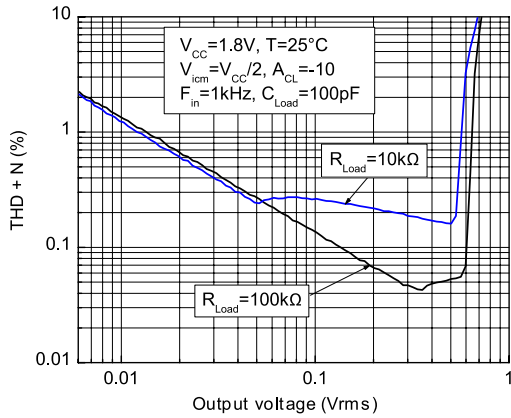


Figure 15: Distortion + noise vs. output voltage at VCC = 5 V

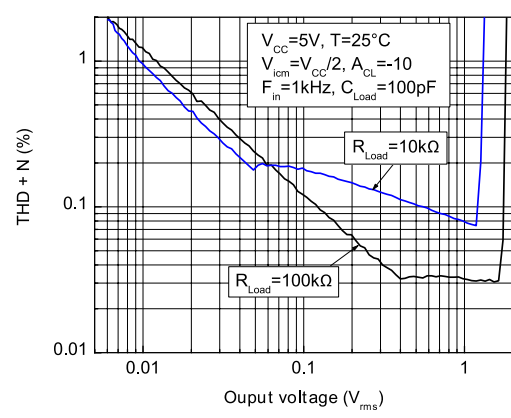


Figure 16: Distortion + noise vs. frequency at VCC = 1.8 V

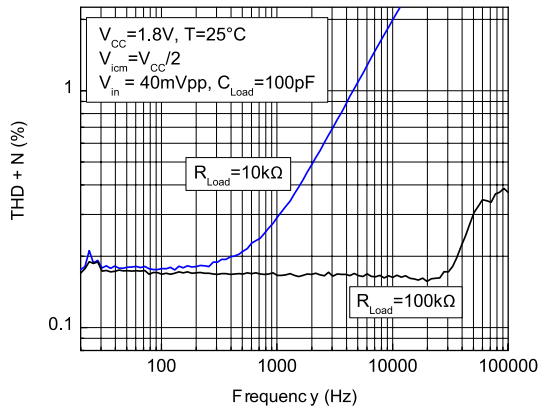
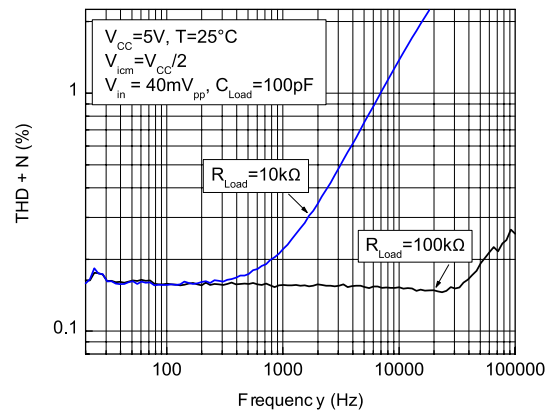


Figure 17: Distortion + noise vs. frequency at VCC = 5 V



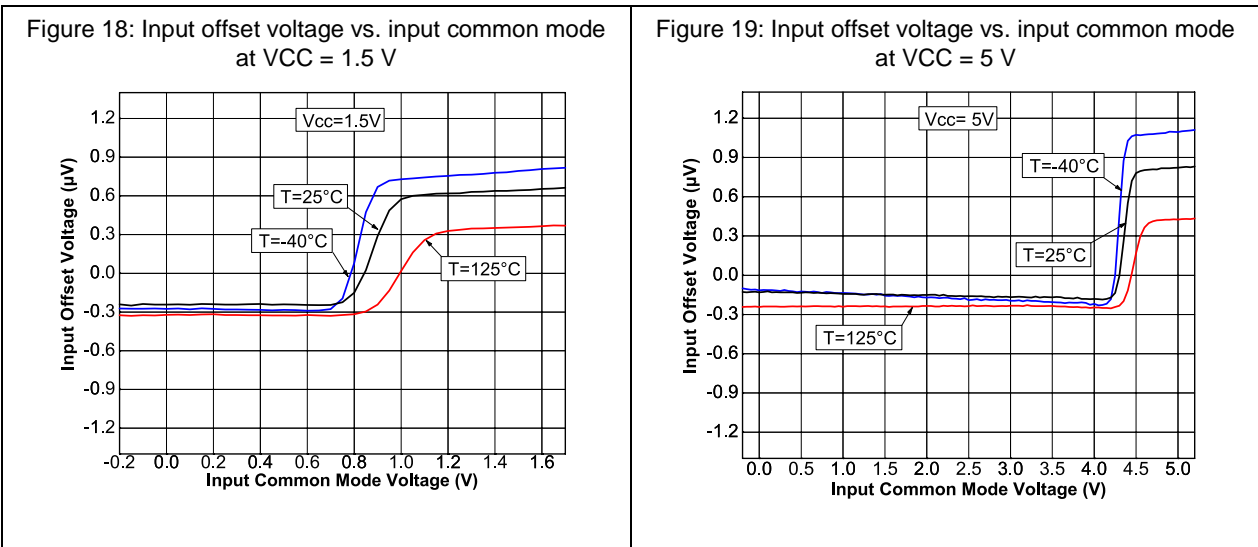
## 5 Application information

### 5.1 Operating voltages

The TSV6290 and TSV6291 can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8, 3.3 and 5 V power supplies. However, the parameters are very stable in the full  $V_{CC}$  range and several characterization curves show the TSV629x characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 °C to 125 °C.

### 5.2 Rail-to-rail input

The TSV6290 and TSV6291 are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common-mode range is extended from  $(V_{CC-}) - 0.1$  V to  $(V_{CC+}) + 0.1$  V. The transition between the two pairs appears at  $(V_{CC+}) - 0.7$  V. In the transition region, the performance of CMR, SVR,  $V_{io}$  and THD is slightly degraded (as shown in [Figure 18](#) and [Figure 19](#) for  $V_{io}$  vs.  $V_{icm}$ ).



The devices are guaranteed without phase reversal.

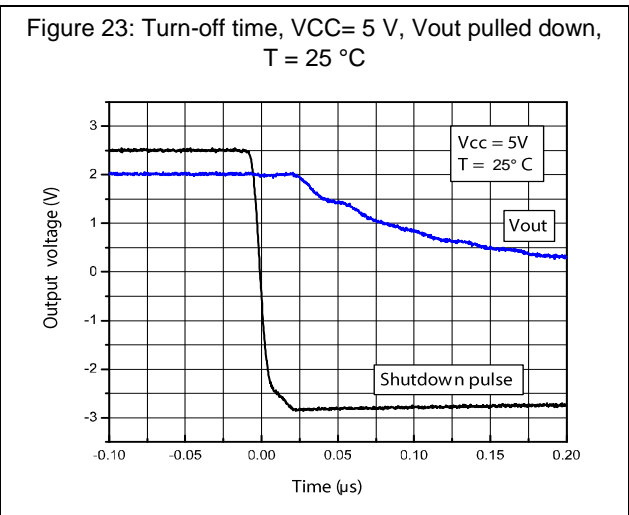
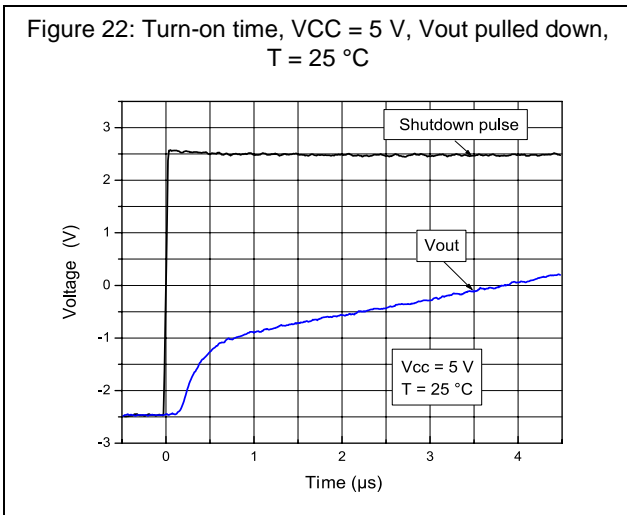
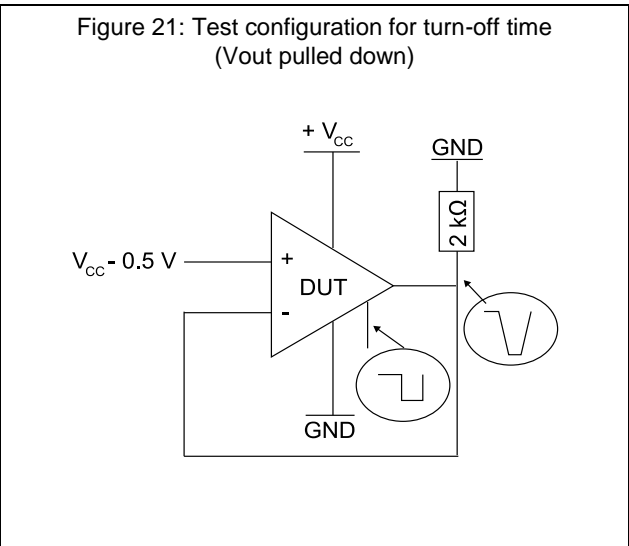
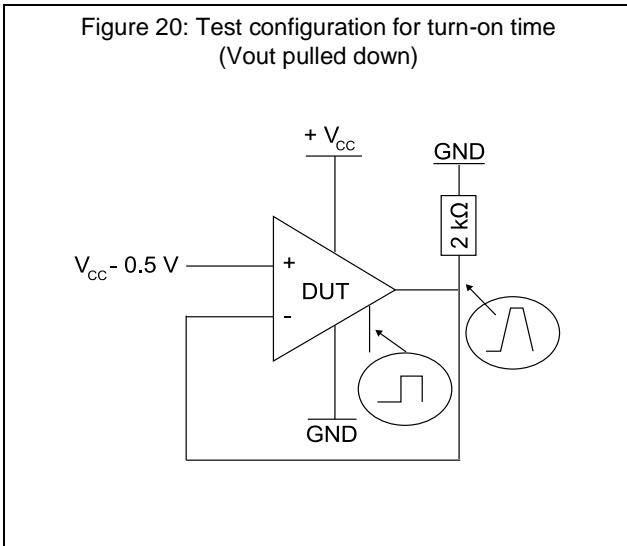
### 5.3 Rail-to-rail output

The operational amplifiers' output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 kΩ resistive load to  $V_{CC}/2$ .

### 5.4 Shutdown function (TSV6290)

The operational amplifier is enabled when the  $\overline{\text{SHDN}}$  pin is pulled high. To disable the amplifier, the  $\overline{\text{SHDN}}$  must be pulled down to  $V_{\text{CC-}}$ . When in shutdown mode, the amplifier's output is in a high impedance state. The  $\overline{\text{SHDN}}$  pin must never be left floating, but tied to ( $V_{\text{CC+}}$ ) or ( $V_{\text{CC-}}$ ).

The turn-on and turn-off times are calculated for an output variation of  $\pm 200$  mV (Figure 20 and Figure 21 show the test configurations).



### 5.5 Optimization of DC and AC parameters

These devices use an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of the current consumption (29  $\mu\text{A}$  typical, min/max at  $\pm 17$  %). Parameters linked to the current consumption value, such as GBP, SR and  $A_{\text{vd}}$ , benefit from this narrow dispersion.

## 5.6 Driving resistive and capacitive loads

These products are micropower, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 5 k $\Omega$ . For lower resistive loads, the THD level may significantly increase.

The amplifiers have a relatively low internal compensation capacitor, making them very fast while consuming very little. They are ideal when used in a non-inverting configuration or in an inverting configuration in the following conditions.

- $|Gain| \geq 3$  in an inverting configuration ( $C_L = 20$  pF,  $R_L = 100$  k $\Omega$ ) or  $|gain| \geq 10$  ( $C_L = 100$  pF,  $R_L = 100$  k $\Omega$ )
- $Gain \geq 4$  in a non-inverting configuration ( $C_L = 20$  pF,  $R_L = 100$  k $\Omega$ ) or  $gain \geq 11$  ( $C_L = 100$  pF,  $R_L = 100$  k $\Omega$ )

As these operational amplifiers are not unity gain stable, for a low closed-loop gain it is recommended to use the TSV62x (29  $\mu$ A, 420 kHz) or TSV63x (60  $\mu$ A, 880 kHz) which are unity gain stable.

Table 8: Related products

Part #	I <sub>cc</sub> ( $\mu$ A) at 5 V	GBP (MHz)	SR (V/ $\mu$ s)	Minimum gain for stability (C <sub>Load</sub> = 100 pF)
TSV620-1	29	0.42	0.14	1
TSV6290-1	29	1.3	0.5	11
TSV630-1	60	0.88	0.34	1
TSV6390-1	60	2.4	1.1	11

## 5.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

## 5.8 Macromodel

An accurate macromodel of the TSV6290 and TSV6291 is available on STMicroelectronics' web site at [www.st.com](http://www.st.com). This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV629x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



## 6.1 SOT23-5 package information

Figure 24: SOT23-5 package outline

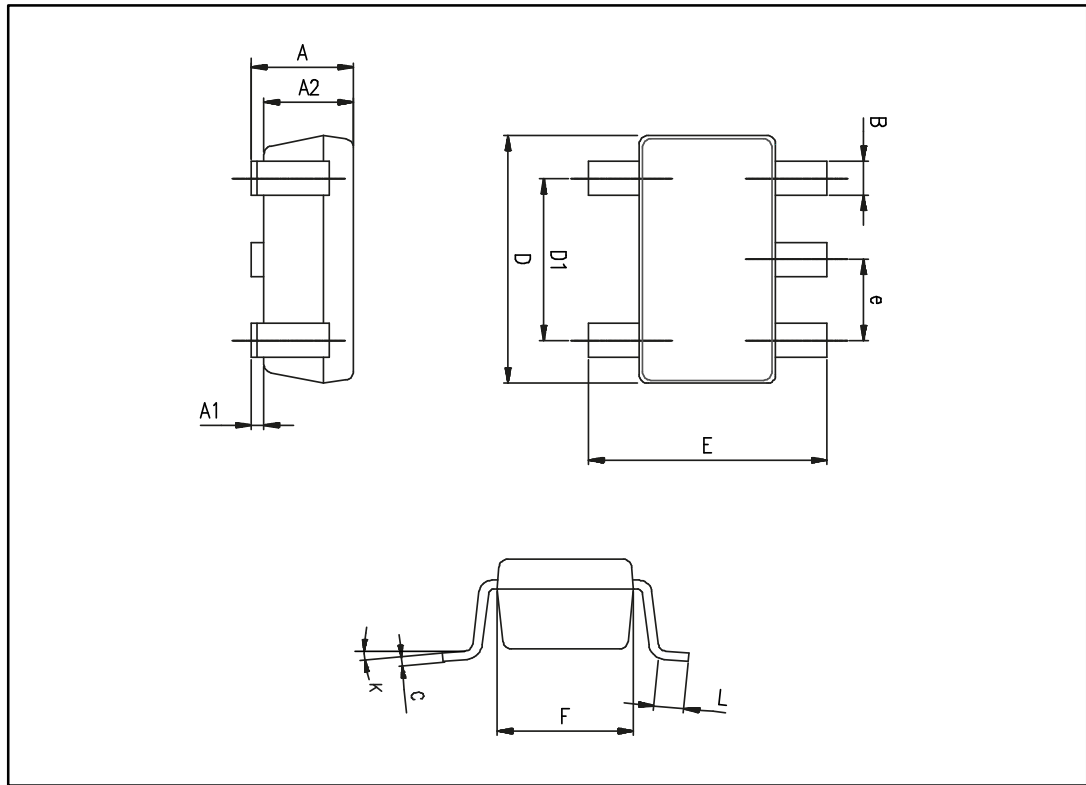


Table 9: SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

## 6.2 SOT23-6 package information

Figure 25: SOT23-6 package outline

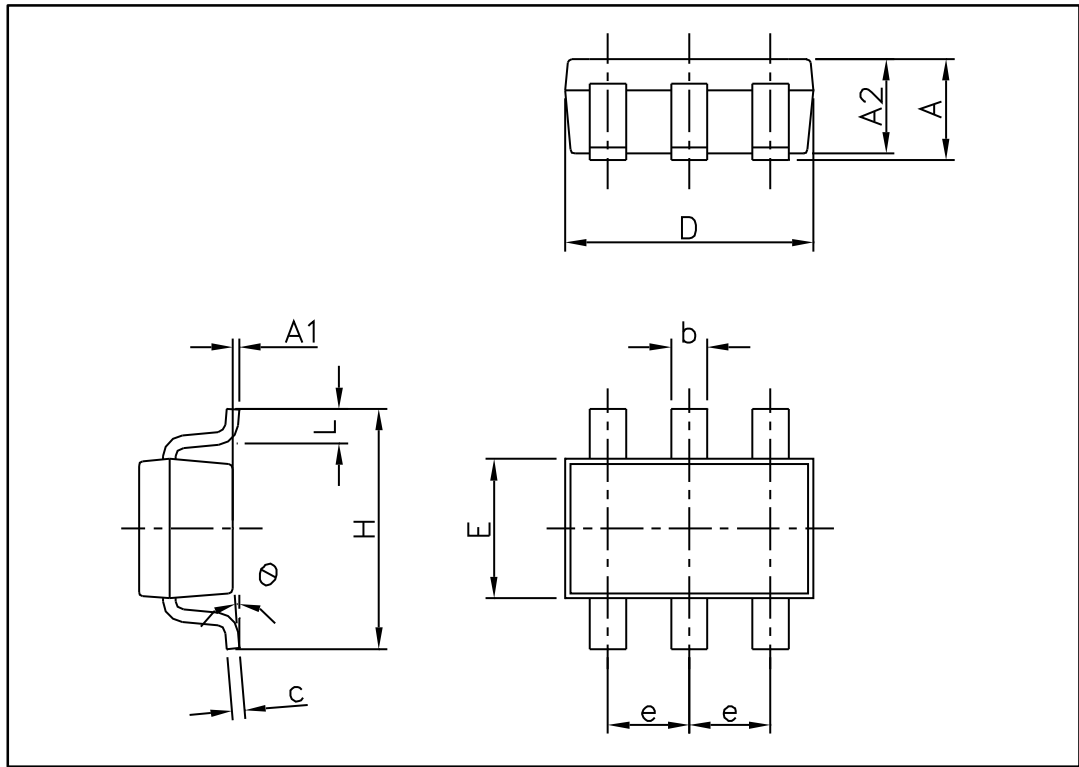


Table 10: SOT23-6 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1			0.10			0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.013		0.019
c	0.09		0.20	0.003		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.060		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
$\theta$	0°		10°	0°		10°

### 6.3 SC70-5 (or SOT323-5) package information

Figure 26: SC70-5 (or SOT323-5) package outline

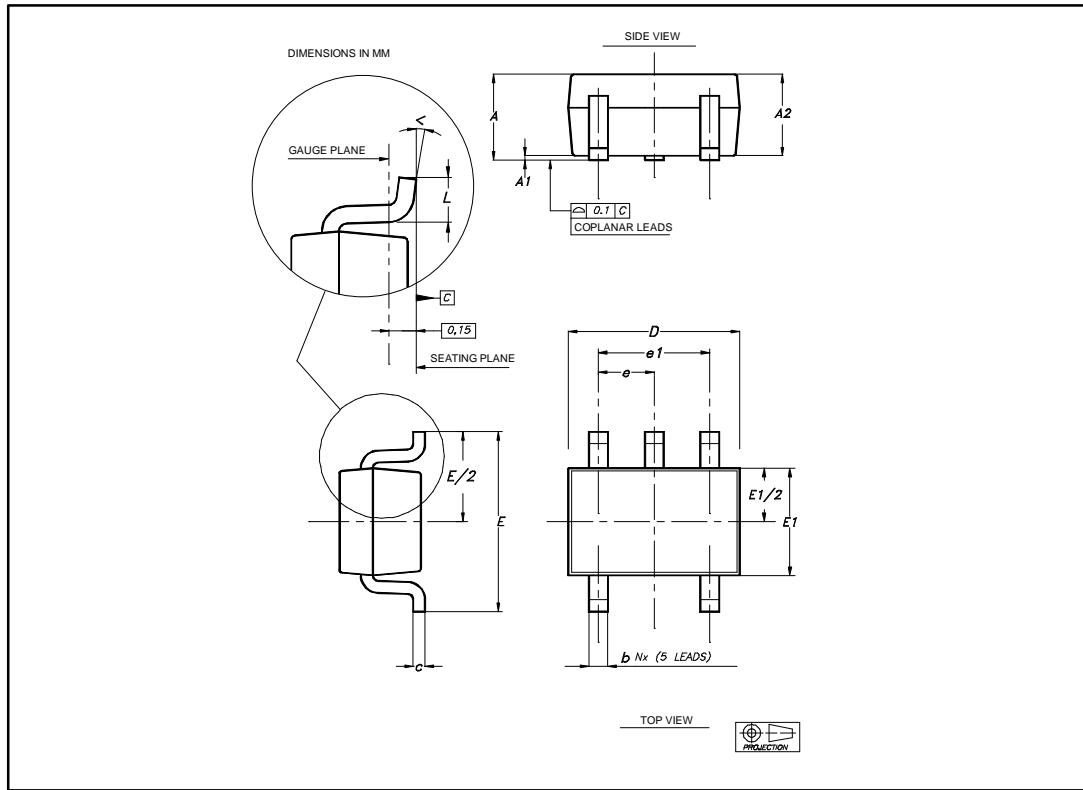


Table 11: SC70-5 (or SOT323-5) mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

### 6.4 SC70-6 (or SOT323-6) package information

Figure 27: SC70-6 (or SOT323-6) package outline

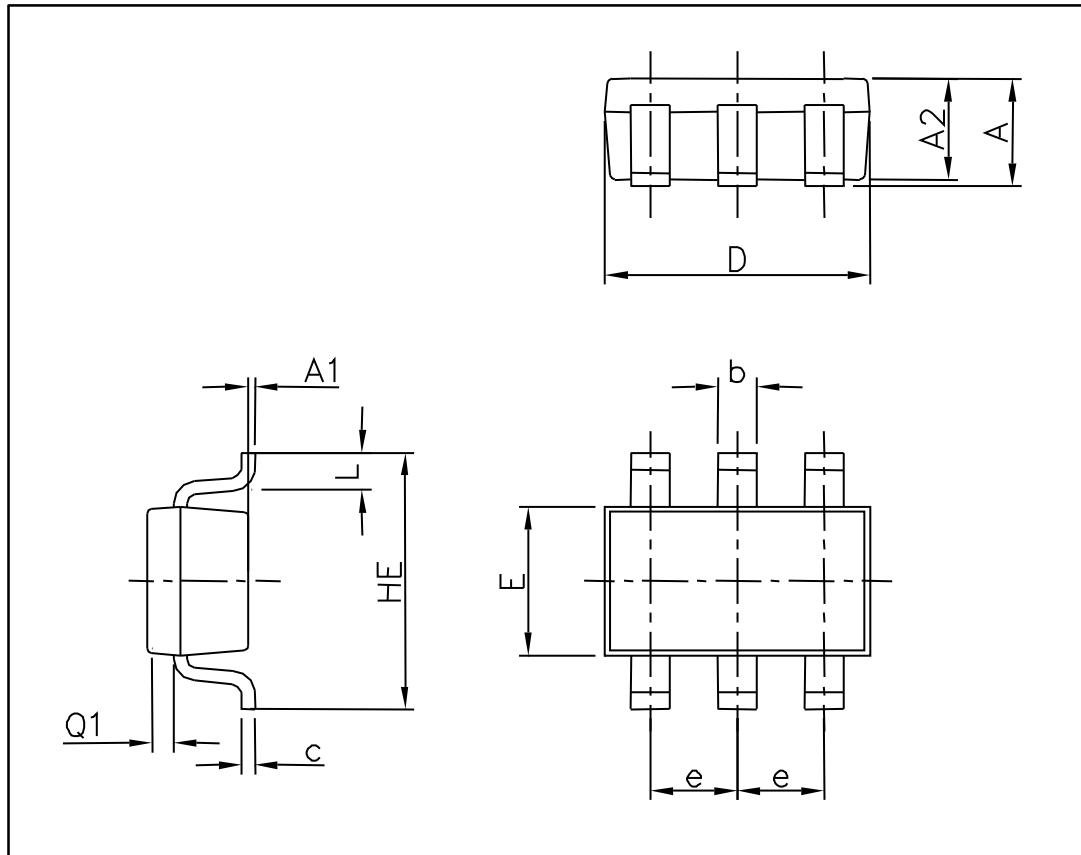
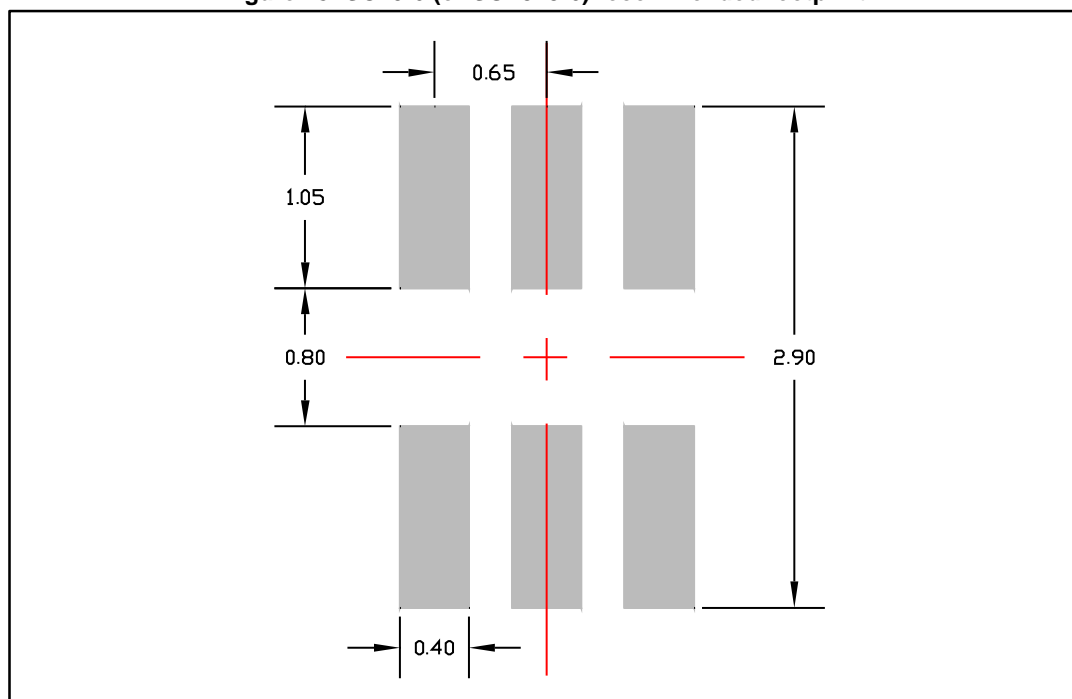


Table 12: SC70-6 (or SOT323-6) mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.031		0.043
A1			0.10			0.004
A2	0.80		1.00	0.031		0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.18	0.004		0.007
D	1.80		2.20	0.071		0.086
E	1.15		1.35	0.045		0.053
e		0.65			0.026	
HE	1.80		2.40	0.071		0.094
L	0.10		0.40	0.004		0.016
Q1	0.10		0.40	0.004		0.016

Figure 28: SC70-6 (or SOT323-6) recommended footprint



## 7 Ordering information

Table 13: Order codes

Part number	Temperature range	Package	Packing	Marking
TSV6290ILT	-40 °C to 125 °C	SOT23-6	Tape and reel	K106
TSV6290ICT		SC70-6		K16
TSV6290AILT		SOT23-6		K139
TSV6290AICT		SC70-6		K39
TSV6291ILT		SOT23-5		K107
TSV6291ICT		SC70-5		K14
TSV6291AILT		SOT23-5		K113
TSV6291AICT		SC70-5		K15

## 8 Revision history

**Table 14: Document revision history**

Date	Revision	Changes
04-Mar-2010	1	Initial release.
10-Aug-2016	2	Updated datasheet layout <i>Table 3, Table 5, and Table 6</i> : V <sub>OH</sub> "min." values changed to "max." values. <i>Figure 8, Figure 9, Figure 10</i> : updated Y-axes <i>Table 11</i> : updated A and A2 min. values in inches

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