

Monolithic 700mA Step-Down Regulator with
Power-On Reset and Watchdog Timer

DESCRIPTION

Demonstration circuit 1312 is a Monolithic 700mA Step-Down Regulator with Power-On Reset and Watchdog Timer featuring the LT3689. The board operates from inputs up to 36V and withstands transients up to 60V. Output is 3.3V, 700mA. When output current is low, the circuit operates in Burst Mode. Users can poplar R7 on the EN/UVLO pin to provide a programmable under voltage lockout. Fault protections are provided through power switch current limit, switching frequency fold back and thermal shutdown, etc.

The power-on reset and watchdog timer periods are independently adjustable using external capacitors. Tight accuracy specifications and glitch immunity ensure reliable operation of the circuit. Window mode or time out mode is selectable through JP1. Watchdog can be enabled or dis-

abled by JP2. Circuit can be synchronized to an external clock connected to SYNC turret. If SYNC function is used, the Rt resistor should be chosen to set the LT3689 internal switching frequency at least 20% below the lowest synchronization input frequency.

The LT3689 datasheet gives complete descriptions of the part, operation and application information. The datasheet must be read in conjunction with this quick start guide for working on or modifying the demo circuit 1327.

**Design files for this circuit board are available.
Call the LTC factory.**

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PERFORMANCE SUMMARY Specifications are at TA = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN}	Input Supply Range	V _{OUT} =3.3V	4.5		36	V
V _{OUT}	Output Voltage Range		3.2	3.3	3.4	V
I _{OUT}	Output Current		0		700	mA
I _Q	No Load Quiescent Current	No load		77		μA
EFF	Efficiency	V _{IN} = 12V, I _{OUT} = 700mA		82		%
T _{WDU}	Watchdog Upper Boundary Period	C3=10nF		182		ms
T _{WDL}	Watchdog Lower Boundary Period	C3=10nF		5.88		ms
T _{RST}	Programmed Reset Period	C4=10nF		23		ms

QUICK START PROCEDURE

Demonstration circuit 1312 is easy to set up to evaluate the performance of the LT3689. Refer to 0 for proper measurement equipment setup and follow the procedure below:

NOTE. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the terminals of the input or output capacitors. See Figure 2 for proper scope probe technique.

1. Place jumpers in the following positions:

JP1 T or W (bar)

JP2 ON or OFF (When OFF, watchdog disabled)

2. With power off, connect the input power supply to VIN and GND.
3. With power off, connect the load to VOUT and GND.

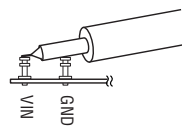
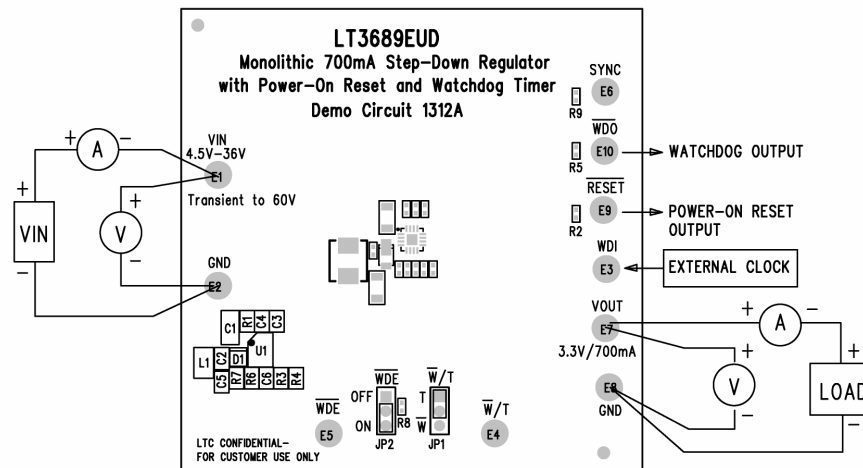
4. Turn on the power at the input.

NOTE. Make sure that the input voltage does not exceed 36V.

5. Check for the proper output voltages. VOUT=3.3V

NOTE. If there is no output, temporarily disconnect the load to make sure that the load is not set too high or is shorted.

6. Once the proper output voltage is established, adjust the loads within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.
7. To test watchdog timer, connect a clock input to the WDI terminal. Observe output at the WDO terminal while the clock parameters are adjusted.
8. To test Power-On reset, observe output at the RESET terminals.





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