

## N-channel 80 V, 4.2 mΩ typ., 110 A STripFET™ F7 Power MOSFET in an H<sup>2</sup>PAK-2 package

Datasheet - production data

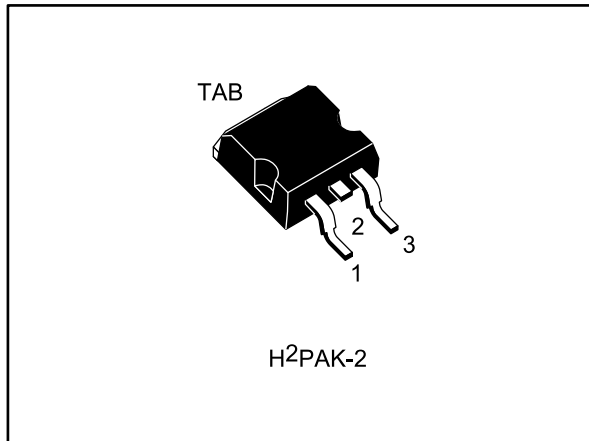


Figure 1: Internal schematic diagram

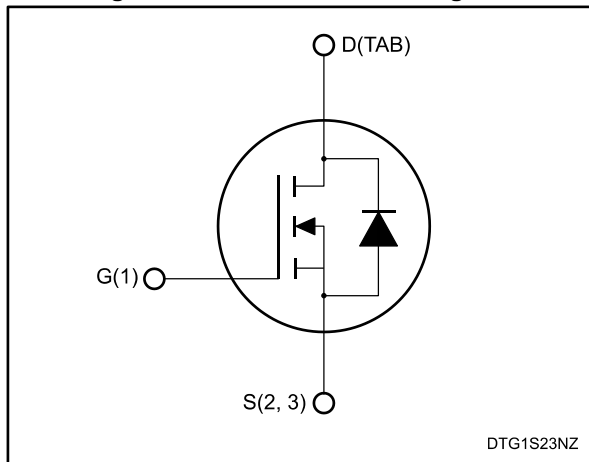


Table 1: Device summary

Order code	Marking	Package	Packaging
STH130N8F7-2	130N8F7	H <sup>2</sup> PAK-2	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)max.</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STH130N8F7-2	80 V	5.0 mΩ	110 A	205 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

---

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
	4.1 H <sup>2</sup> PAK-2 package information .....	10
	4.2 H <sup>2</sup> PAK-2 packing information .....	12
<b>5</b>	<b>Revision history .....</b>	<b>14</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	80	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_c = 25\text{ }^\circ\text{C}$	110	A
$I_D$	Drain current (continuous) at $T_c = 100\text{ }^\circ\text{C}$	100	A
$I_{DM}^{(1)}$	Drain current (pulsed)	440	A
$P_{TOT}$	Total dissipation at $T_c = 25\text{ }^\circ\text{C}$	205	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	320	mJ
$T_j$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area

<sup>(2)</sup>Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 55\text{ A}$ ,  $V_{DD} = 40\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.73	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1inch<sup>2</sup>, 2 oz Cu

## 2 Electrical characteristics

(T<sub>CASE</sub>= 25 °C unless otherwise specified)

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V, T <sub>J</sub> =125 °C <sup>(1)</sup>			100	μA
I <sub>GSS</sub>	Gate-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		4.5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 55 A		4.2	5.0	mΩ

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	4500	-	pF
C <sub>oss</sub>	Output capacitance		-	1100	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	110	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 110 A, V <sub>GS</sub> = 0 to 10 V <i>Figure 14: "Test circuit for gate charge behavior"</i>	-	60	-	nC
Q <sub>gs</sub>	Gate-source charge		-	25	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	15	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 55 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V <i>Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform"</i>	-	140	-	ns
t <sub>r</sub>	Rise time		-	210	-	ns
t <sub>d(off)</sub>	Turn-off-delay time		-	190	-	ns
t <sub>f</sub>	Fall time		-	120	-	ns

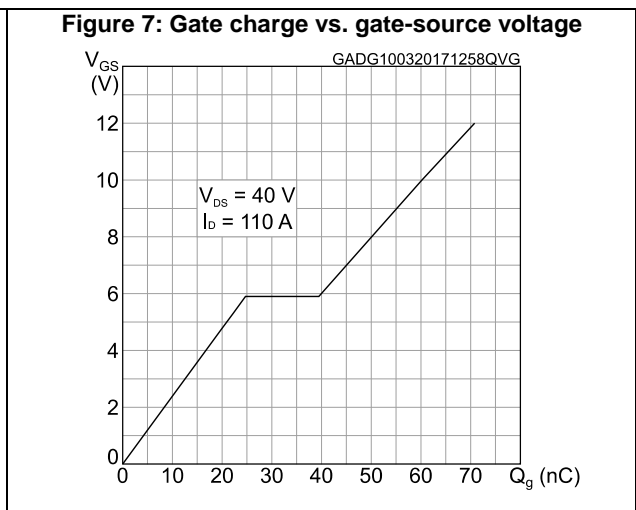
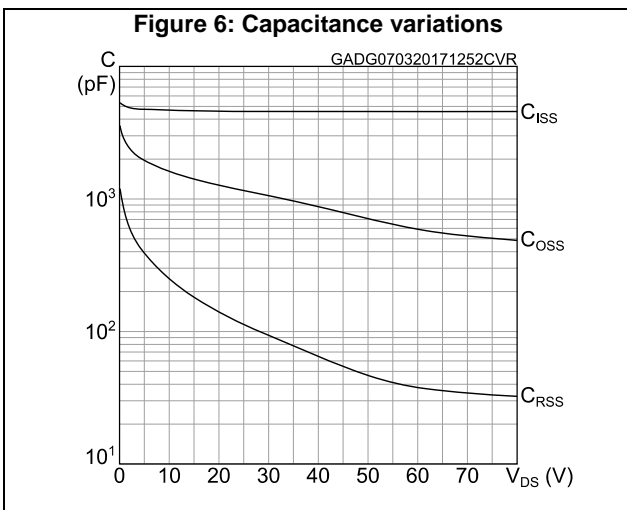
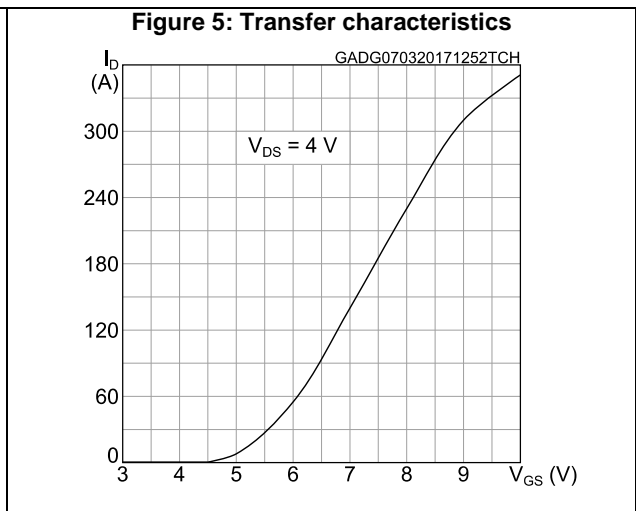
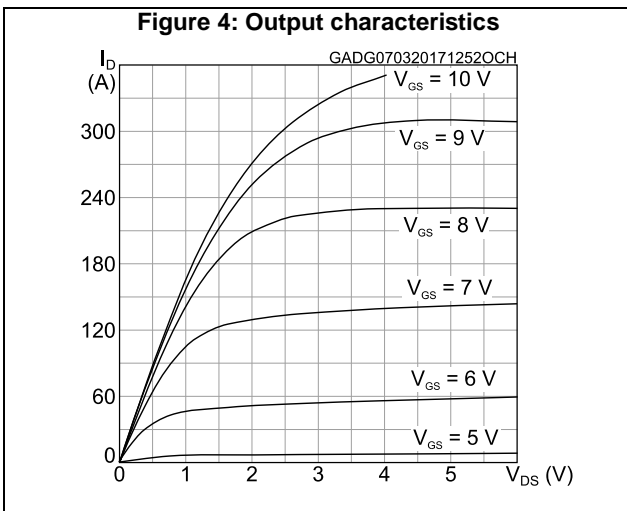
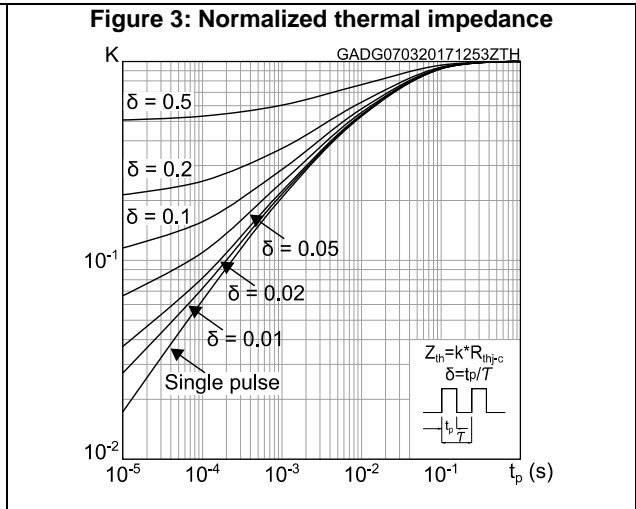
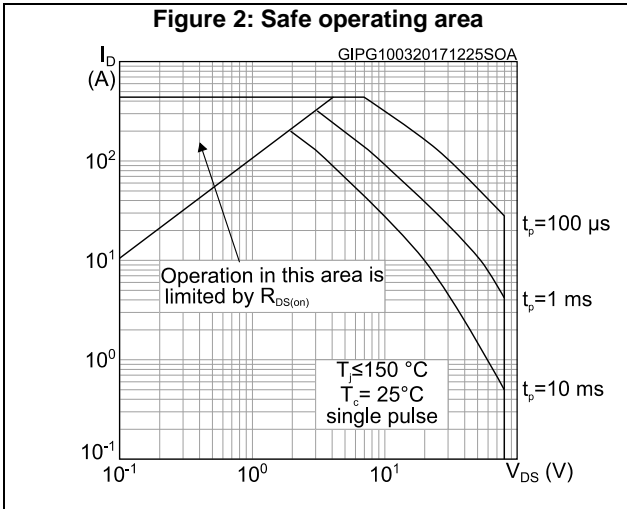
Table 7: Source drain diode

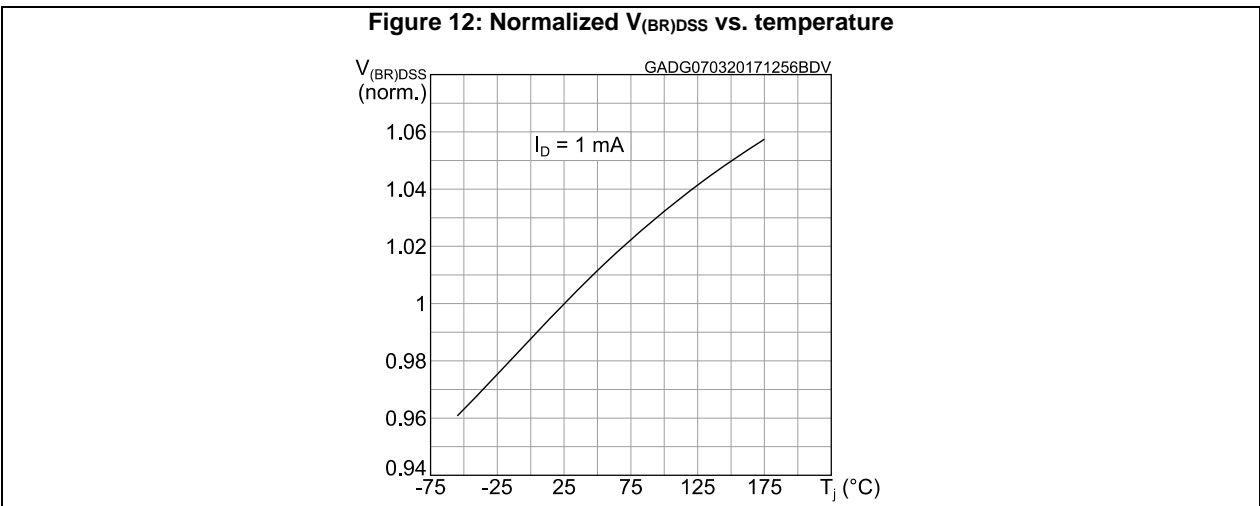
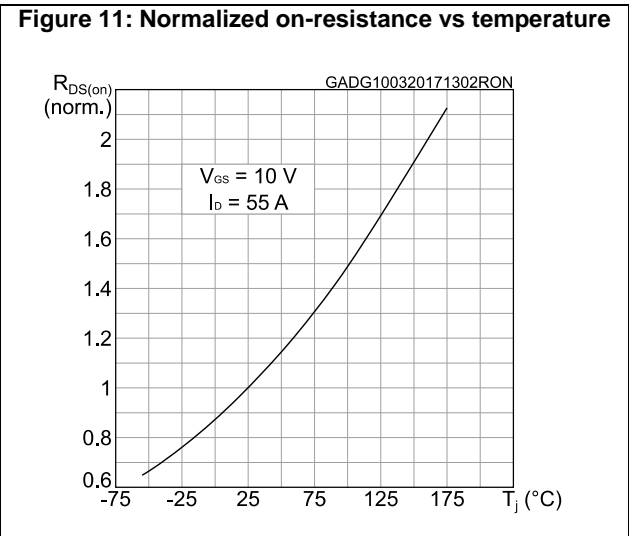
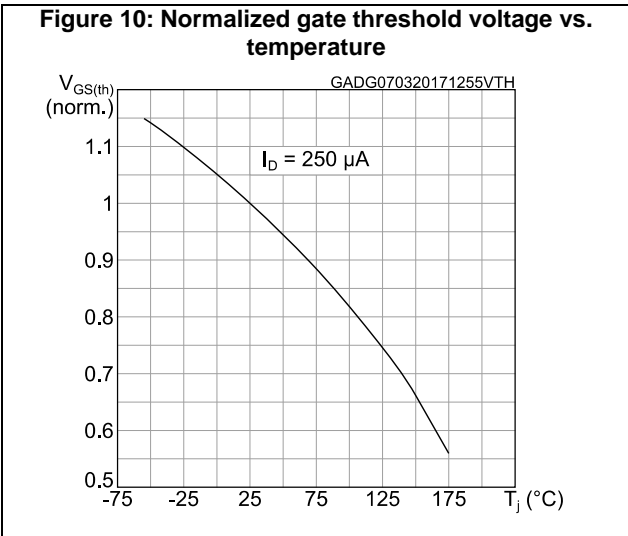
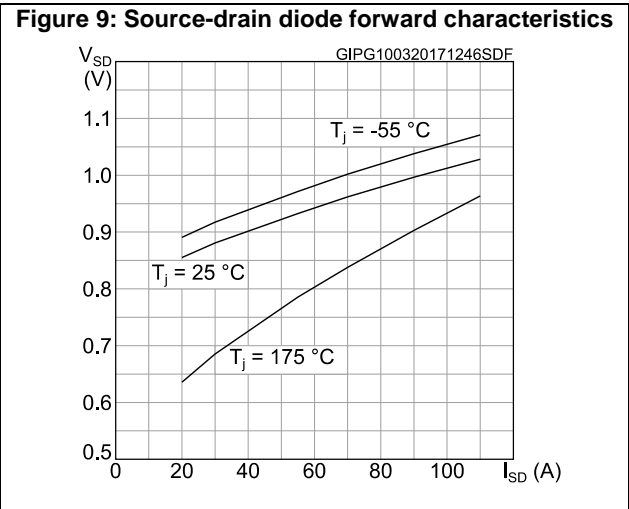
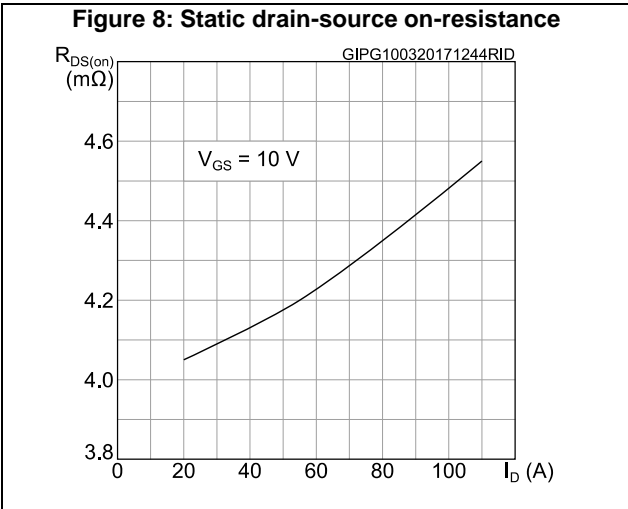
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}$ (1)	Forward on voltage	$I_{SD}= 110\text{ A}$ , $V_{GS}= 0\text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD}= 110\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}= 80\text{ V}$ , $T_j= 150\text{ }^\circ\text{C}$ <i>Figure 15: "Test circuit for inductive load switching and diode recovery times"</i>	-	45		ns
$Q_{rr}$	Reverse recovery charge		-	54		nC
$I_{RRM}$	Reverse recovery current		-	2.5		A

**Notes:**

(1)Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

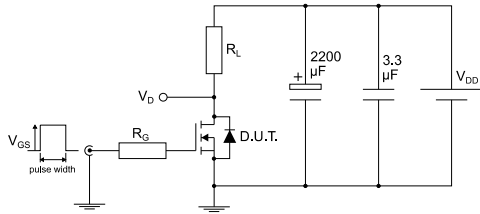
## 2.1 Electrical characteristics (curves)





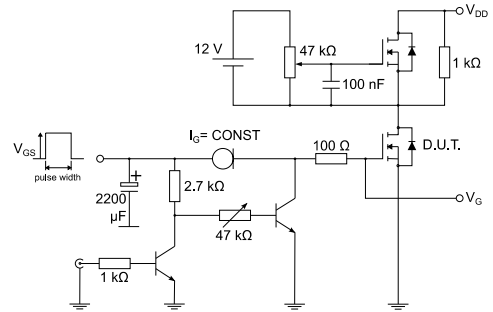
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



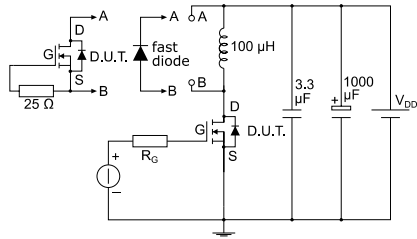
AM01468v1

**Figure 14: Test circuit for gate charge behavior**



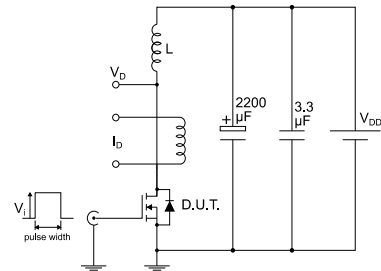
AM01469v1

**Figure 15: Test circuit for inductive load switching and diode recovery times**



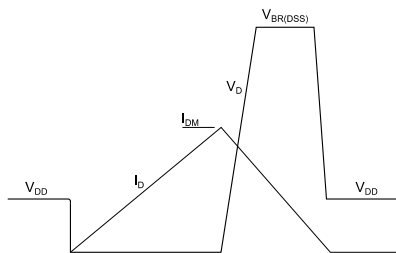
AM01470v1

**Figure 16: Unclamped inductive load test circuit**



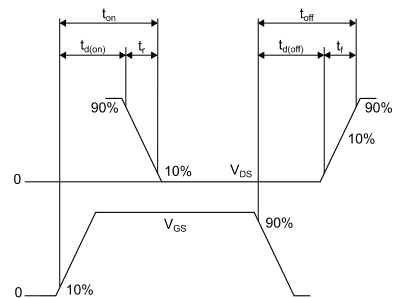
AM01471v1

**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

Figure 19: H<sup>2</sup>PAK-2 package outline

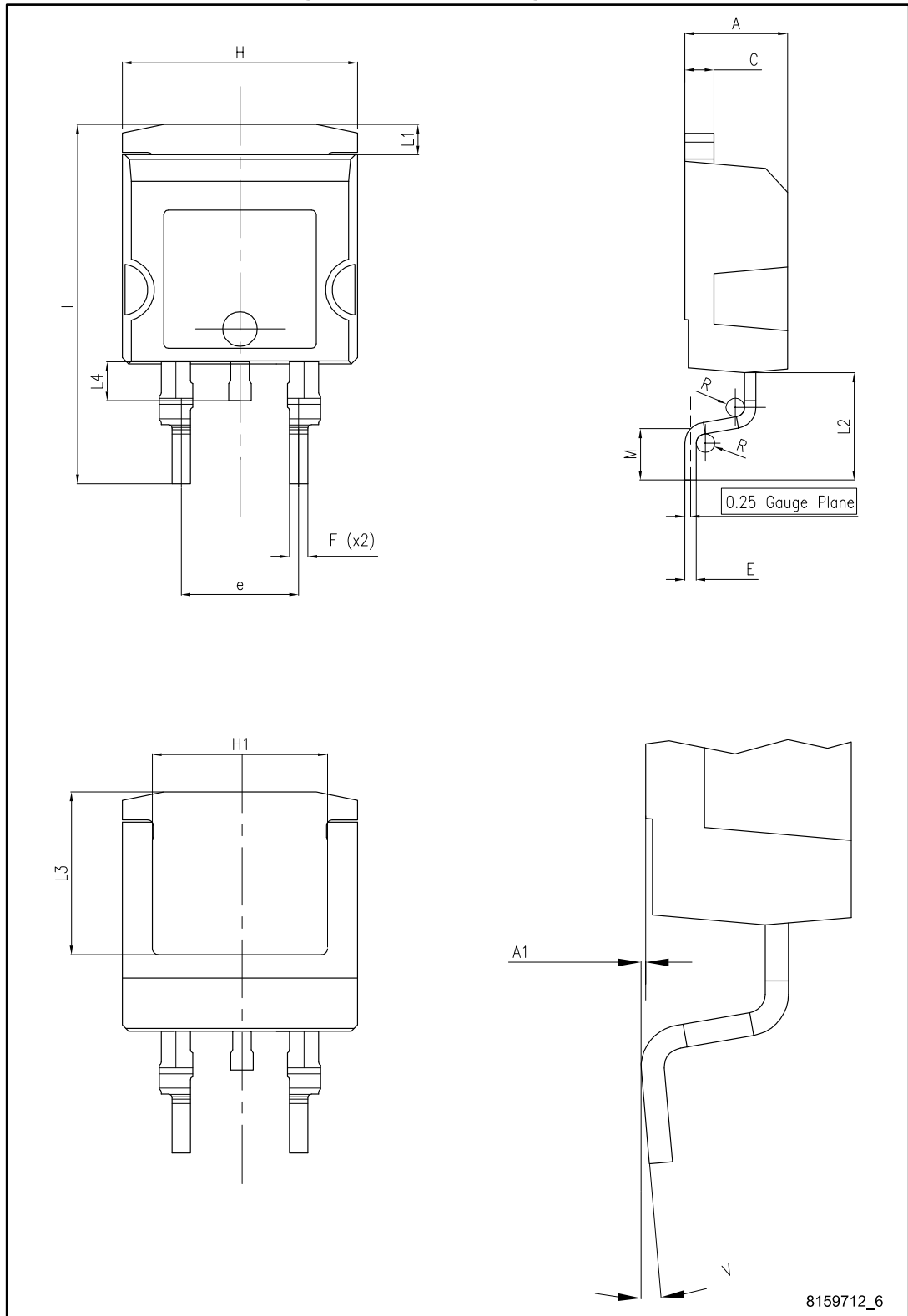
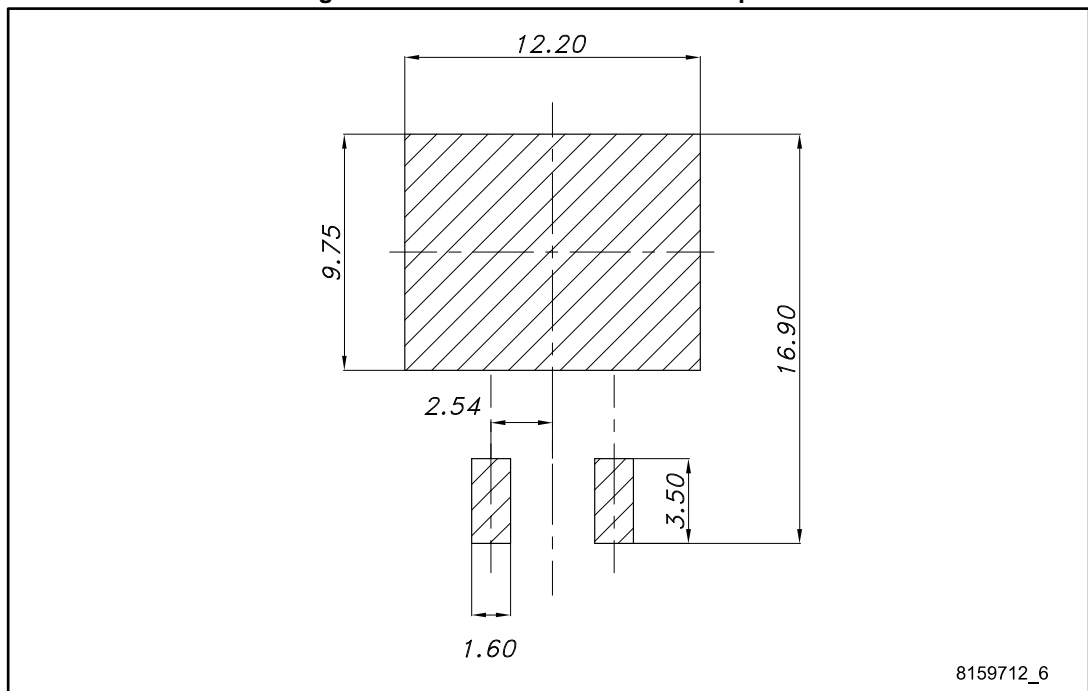


Table 8: H<sup>2</sup>PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H<sup>2</sup>PAK-2 recommended footprint



### 4.2 H<sup>2</sup>PAK-2 packing information

Figure 21: Tape outline

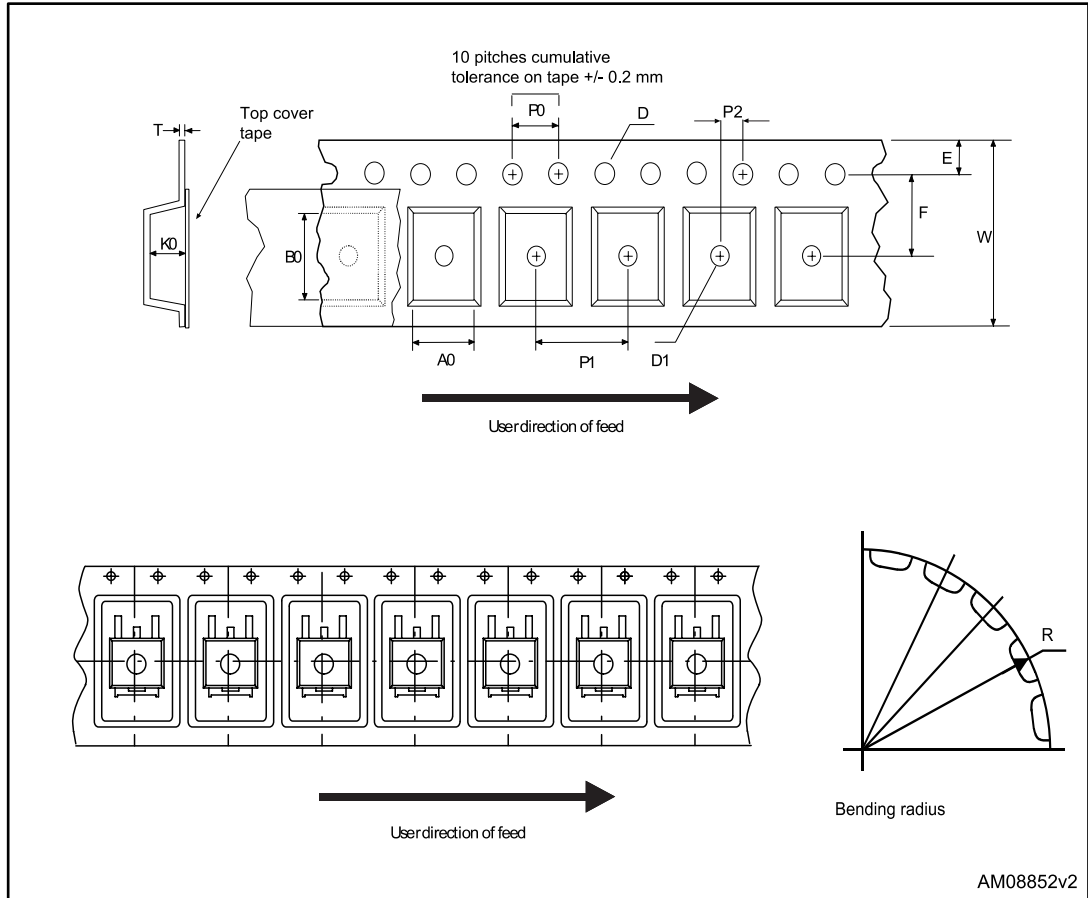


Figure 22: Reel outline

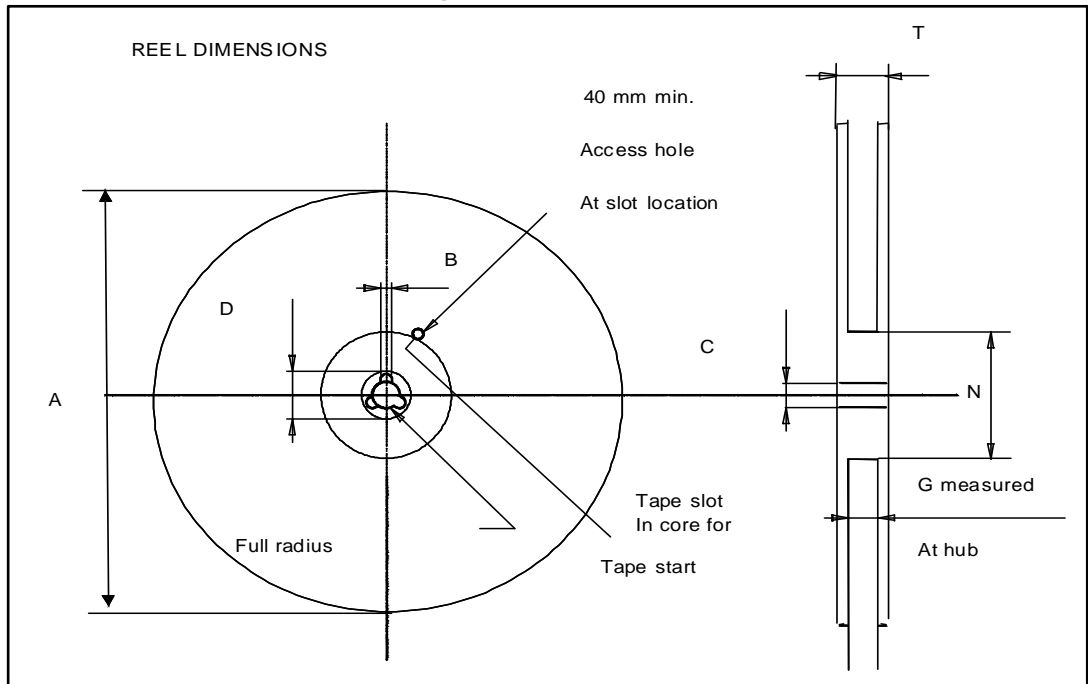


Table 9: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
10-Dec-2014	1	First release.
13-Mar-2017	2	Datasheet promoted from preliminary data to production data. Modified features table on cover page. Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> , <i>Table 4: "On/off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source drain diode"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> Minor text changes.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved

## Данный компонент на территории Российской Федерации

### Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9