

BUK9606-75B

N-channel TrenchMOS logic level FET Rev. 4 — 20 July 2011

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	75	V
I _D	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	[1] -	-	75	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	300	W
Static cha	aracteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$	-	4.7	5.5	mΩ
		$V_{GS} = 5 \text{ V; } I_D = 25 \text{ A;}$ $T_j = 25 \text{ °C;}$ see Figure 11; see Figure 12	-	5.2	6.1	mΩ



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Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	e ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le$ 75 V; R_{GS} = 50 Ω ; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	852	mJ
Dynamic (Dynamic characteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 60 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 13	-	37	-	nC

^[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]	mb	B
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9606-75B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _i ≥ 25 °C; T _i ≤ 175 °C	-	75	V
V _{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	75	V
V _{GS}	gate-source voltage		-15	15	V
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 5 V; see <u>Figure 1</u>	<u>[1]</u> _	75	Α
		$T_{mb} = 25 ^{\circ}\text{C}; V_{GS} = 5 \text{V}; \text{see} \frac{\text{Figure 1}}{\text{Figure 1}};$	[2] _	153	Α
		see Figure 3	<u>[1]</u> -	75	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see Figure 3	-	612	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	300	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drai	in diode				
Is	source current	T _{mb} = 25 °C	[2] _	153	Α
			<u>[1]</u> -	75	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	612	Α
Avalanche i	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$I_D = 75$ A; $V_{sup} \le 75$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped	-	852	mJ
		,()			

- [1] Continuous current is limited by package.
- [2] Current is limited by power dissipation chip rating.

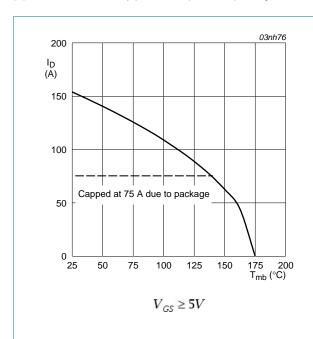


Fig 1. Continuous drain current as a function of mounting base temperature

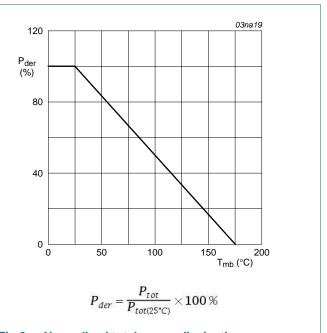
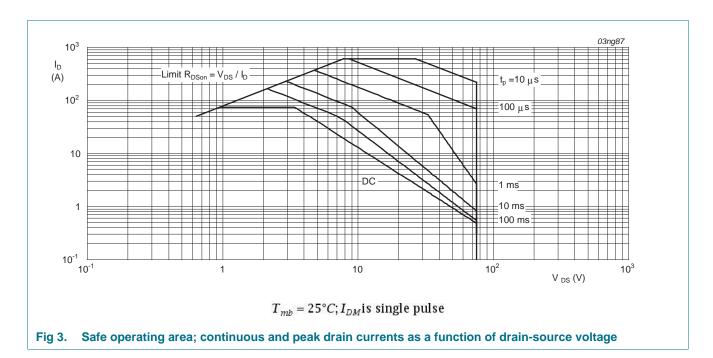


Fig 2. Normalized total power dissipation as a function of mounting base temperature

BUK9606-75B

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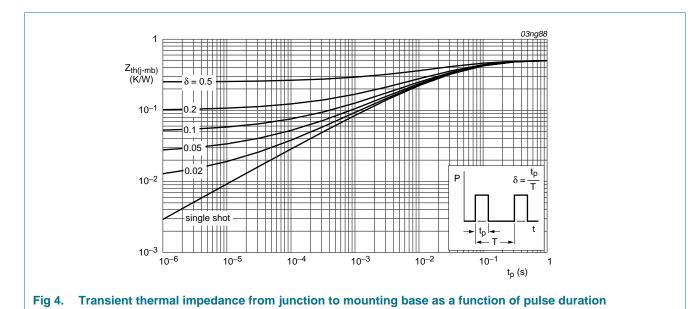
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5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.5	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	75	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	70	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see <u>Figure 10</u>	1.1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see <u>Figure 10</u>	0.5	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see <u>Figure 10</u>	-	-	2.3	V
I _{DSS}	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
		$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
R _{DSon}	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	-	6.6	mΩ
	resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 °C;$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	12.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	4.7	5.5	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	5.2	6.1	mΩ
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 5 \text{ V};$	-	95	-	nC
Q_{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 13</u>	-	17	-	nC
Q_GD	gate-drain charge		-	37	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	8770	11693	рF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 14</u>	-	842	1010	pF
C _{rss}	reverse transfer capacitance		-	336	460	pF
d(on)	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	68	-	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	144	-	ns
t _{d(off)}	turn-off delay time		-	273	-	ns
t _f	fall time		-	116	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die; $T_j = 25$ °C	-	4.5	-	nΗ
		from upper edge of drain mounting base to centre of die; $T_j = 25$ °C	-	2.5	-	nΗ
L _S	internal source inductance	from source lead to source bond pad; $T_j = 25~^{\circ}\text{C}$	-	7.5	-	nΗ

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drai	in diode					
V _{SD}	source-drain voltage	$I_S = 40 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ see <u>Figure 15</u>	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	68	-	ns
Qr	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ °C}$	-	176	-	nC

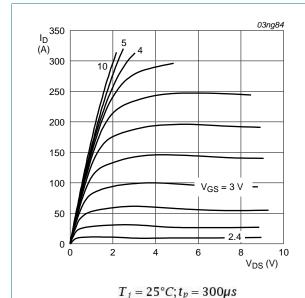


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

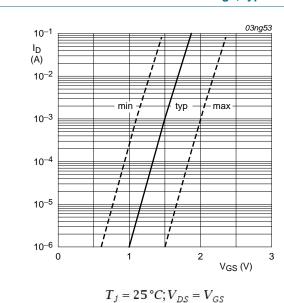
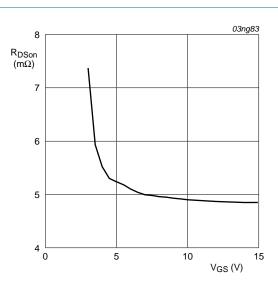
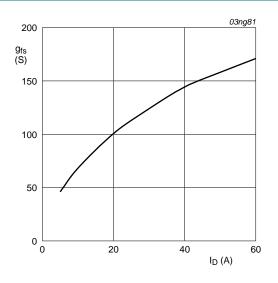


Fig 7. Sub-threshold drain current as a function of gate-source voltage



 $T_j=25^{\circ}C; I_D=25A$

Fig 6. Drain-source on-state resistance as a function of gate-source voltages; typical values



 $T_j = 25$ °C; $V_{DS} = 25V$

Fig 8. Forward transconductance as a function of drain current; typical values

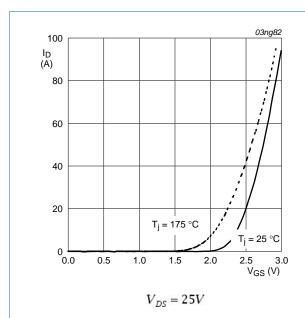


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

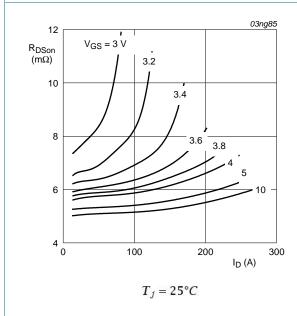
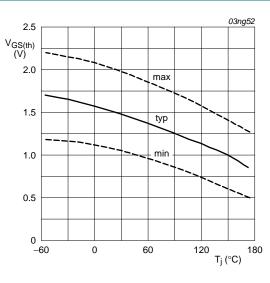


Fig 11. Drain-source on-state resistance as a function of drain current; typical values



 $I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature

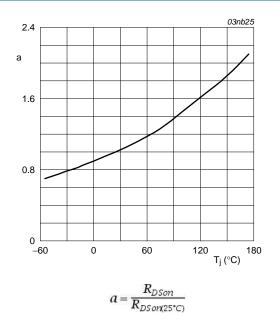


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

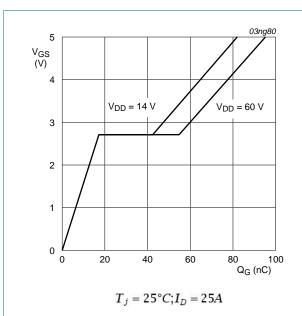
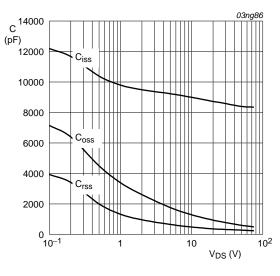


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

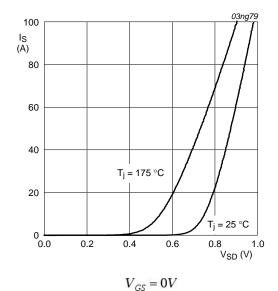


Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

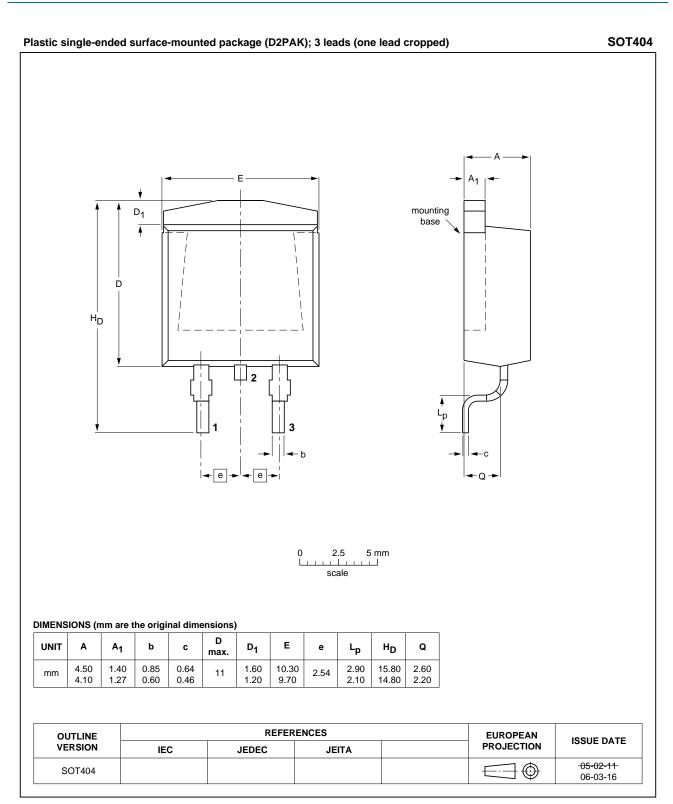


Fig 16. Package outline SOT404 (D2PAK)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9606-75B v.4	20110720	Product data sheet	-	BUK9606-75B v.3
Modifications: • Various changes to content.				
BUK9606-75B v.3	20110207	Product data sheet	-	BUK95_9606_75B v.2

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Document status [1] [2]	Product status [3]	Definition
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