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May 2014

FDMS9620S

Dual N-Channel PowerTrench[®] MOSFET Q1: 30V, 16A, 21.5m Ω Q2: 30V, 18A, 13m Ω

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 21.5m Ω at V_{GS} = 10V, I_D = 7.5A
- Max $r_{DS(on)} = 29.5 \text{m}\Omega$ at $V_{GS} = 4.5 \text{V}$, $I_D = 6.5 \text{A}$

Q2: N-Channel

- Max $r_{DS(on)} = 13m\Omega$ at $V_{GS} = 10V$, $I_D = 10A$
- Max $r_{DS(on)}$ = 17m Ω at V_{GS} = 4.5V, I_D = 8.5A
- Low Qg high side MOSFET
- Low r_{DS(on)} low side MOSFET
- Thermally efficient dual Power 56 package
- Pinout optimized for simple PCB design
- RoHS Compliant



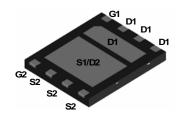
General Description

This device includes two specialized MOSFETs in a unique dual Power 56 package. It is designed to provide an optimal Synchronous Buck power stage in terms of efficiency and PCB utilization. The low switching loss "High Side" MOSFET is complemented by a Low Conduction Loss "Low Side" SyncFET.

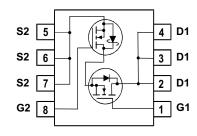
Applications

Synchronous Buck Converter for:

- Notebook System Power
- General Purpose Point of Load







MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Paramete	r		Q1	Q2	Units
V_{DS}	Drain to Source Voltage			30	30	V
V_{GS}	Gate to Source Voltage			±20	±20	V
	Drain Current -Continuous	T _C = 25°C		16	18	
I _D	-Continuous	T _A = 25°C	(Note 1a)	7.5	10	Α
	-Pulsed			60	60	
Б	Power Dissipation for Single Operation	T _A = 25°C	(Note 1a)	'		W
P_{D}		T _A = 25°C	(Note 1b)			VV
T _J , T _{STG}	Operating and Storage Junction Temperatur	e Range		-55 to	+150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		8.2	3.1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (No	ote 1a)	50		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (No	ote 1b)	12	.0	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS9620S	FDMS9620S	Power 56	13"	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Off Chara	octeristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0V$ $I_D = 1 m A, V_{GS} = 0 V$	Q1 Q2	30 30			V
ΔBV _{DSS} ΔΤ _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C I _D = 1mA, referenced to 25°C	Q1 Q2		23 23		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24V, V _{GS} = 0V	Q1 Q2			1 500	μА
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	Q1 Q2			±100 ±100	nA
On Chara	cteristics						
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$ $V_{GS} = V_{DS}, I_D = 1mA$	Q1 Q2	1 1	1.6 1.6	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C I _D = 1mA, referenced to 25°C	Q1 Q2		-4 -4		mV/°C
-	Drain to Source On Resistance	$V_{GS} = 10V, I_D = 7.5A$ $V_{GS} = 4.5V, I_D = 6.5A$ $V_{GS} = 10V, I_D = 7.5A, T_J = 125^{\circ}C$	Q1		18 23 25	21.5 29.5 32	mO
r _{DS(on)}	Diani to Source Off Resistance	$V_{GS} = 10V, I_D = 10A$ $V_{GS} = 4.5V, I_D = 8.5A$ $V_{GS} = 10V, I_D = 10A, T_J = 125^{\circ}C$	Q2		9 13 14	13 17 22	– mΩ
9 _{FS}	Forward Transconductance	$V_{DD} = 10V, I_D = 7.5A$ $V_{DD} = 10V, I_D = 10A$	Q1 Q2		25 27		S

Dynamic Characteristics

C _{iss}	Input Capacitance		Q1	500	665	pF
Ciss	input Capacitance	Q2	700	935	рі	
C	Output Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHZ	Q1	100	135	pF
C _{oss} Output Capacitance	Output Capacitance		Q2	500	665	рг
C	Reverse Transfer Capacitance		Q1	65	100	nE
C _{rss}	Reverse Transfer Capacitance		Q2	100	150	pF
В	Gate Resistance	f = 1041 l=	Q1	0.9		0
R_g	R _g Gate Resistance	f = 1MHz	Q2	1.8		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		Q1 Q2	11 15	20 27	ns
t _r	Rise Time		Q1 Q2	7	14 24	ns
t _{d(off)}	Turn-Off Delay Time	$V_{DD} = 15V, I_D = 1A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	Q1 Q2	23 27	37 44	ns
t _f	Fall Time		Q1 Q2	2.3 7	10 14	ns
Qg	Total Gate Charge	Q1 V _{DD} = 15V, V _{GS} = 10V ,I _D = 7.5A	Q1 Q2	10 18	14 25	nC
Q _{gs}	Gate to Source Gate Charge	Q2 V _{DD} = 15V, V _{GS} = 10V ,I _D = 10A	Q1 Q2	1.7 2.8		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2	2.0 3.6		nC

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Parameter

Drain-S	Source Diode Characteristics						
Is	Maximum Continuous Drain-Source Dio	de Forward Current		Q1 Q2		2.1 3.5	Α
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 2.1A$ ($V_{GS} = 0V, I_S = 3.5A$ ((Note 2) (Note 2)	Q1 Q2	0.7 0.5	1.2 1.0	V
t _{rr}	Reverse Recovery Time	Q1 I _F = 7.5A, di/dt = 100A/μs		Q1 Q2	13 14		ns
Q _{rr}	Reverse Recovery Charge	Q2 I _F = 10A, di/dt = 300A/μs		Q1 Q2	4 9		nC

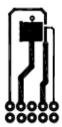
Test Conditions

Symbol

Notes:
 1: R_{θ,IA} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θ,IC} is guaranteed by design while R_{θ,CA} is determined by the user's board design.



a.50°C/W when mounted on a 1 in² pad of 2 oz copper



b. 120°C/W when mounted on a minimum pad of 2 oz copper

Min

Type

Тур

Max

Units

2: Pulse Test: Pulse Width < 300μ s, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel)T_J = 25°C unless otherwise noted

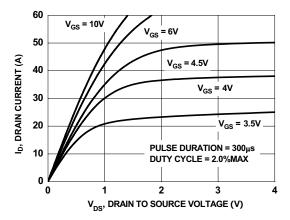


Figure 1. On Region Characteristics

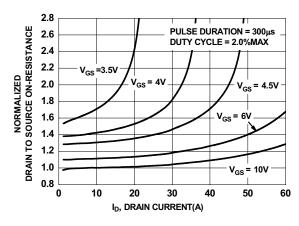


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

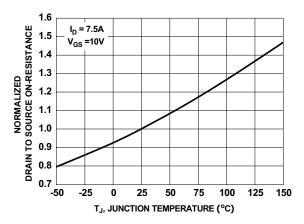


Figure 3. Normalized On Resistance vs Junction Temperature

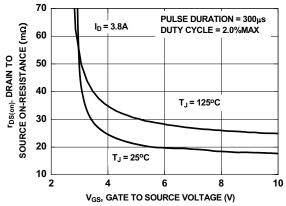


Figure 4. On-Resistance vs Gate to Source Voltage

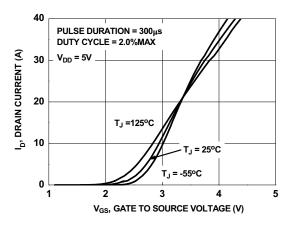


Figure 5. Transfer Characteristics

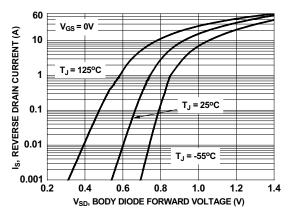


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel)T_J = 25°C unless otherwise noted

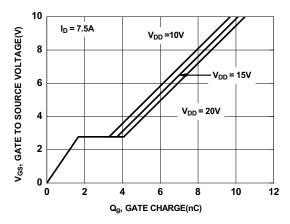


Figure 7. Gate Charge Characteristics

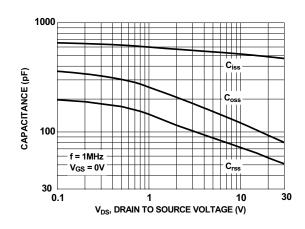


Figure 8. Capacitance vs Drain to Source Voltage

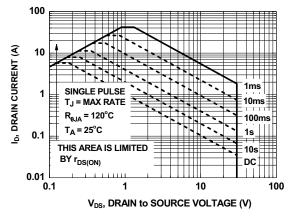


Figure 9. Forward Bias Safe Operating Area

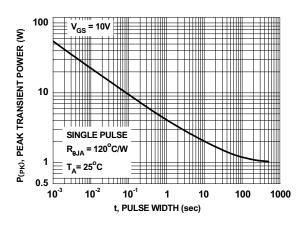


Figure 10. Single Pulse Maximum Power Dissipation

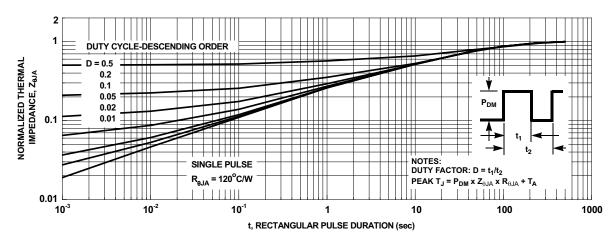


Figure 11. Transient Thermal Response Curve

Typical Characteristics (Q2 SyncFET)

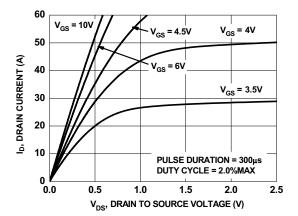


Figure 12. On-Region Characteristics

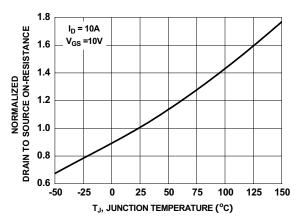


Figure 14. Normalized On-Resistance vs Junction Temperature

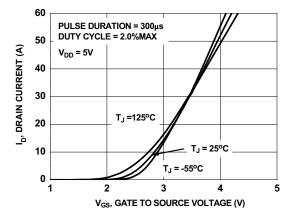


Figure 16. Transfer Characteristics

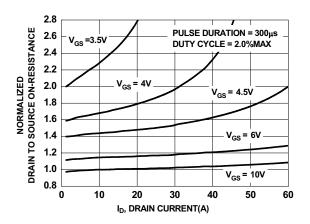


Figure 13. Normalized on-Resistance vs Drain Current and Gate Voltage

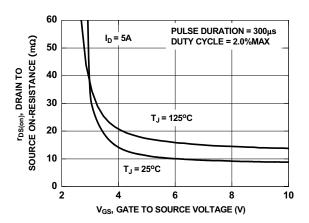


Figure 15. On-Resistance vs Gate to Source Voltage

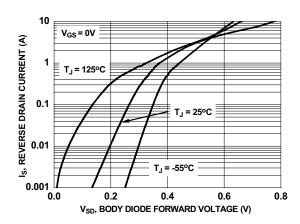


Figure 17. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

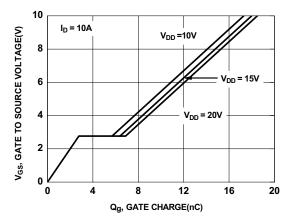


Figure 18. Gate Charge Characteristics

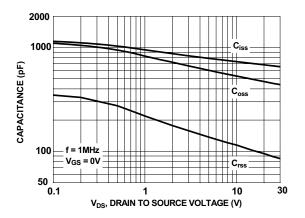
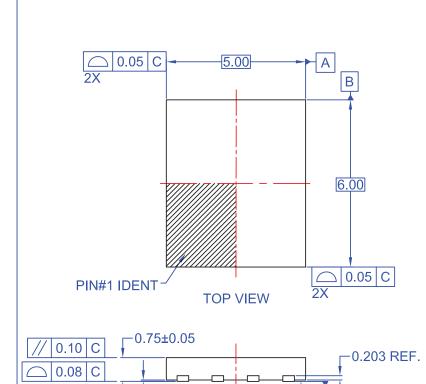
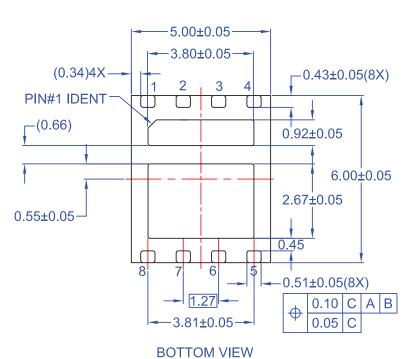


Figure 19. Capacitance vs Drain to Source Voltage



0.025±0.025-

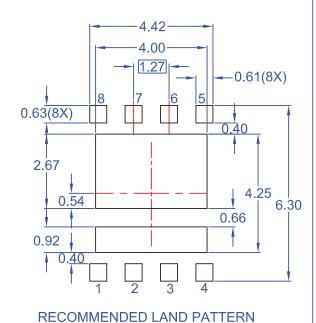


SIDE VIEW

С

SEATING

PLANE



NOTE:

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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9