

## IR2302(S) & (PbF) HALF-BRIDGE DRIVER

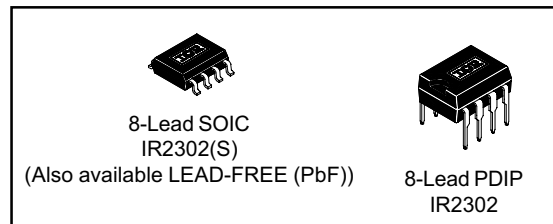
### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 5 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels
- 8-Lead SOIC also available LEAD-FREE (PbF).

### Description

The IR2302(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

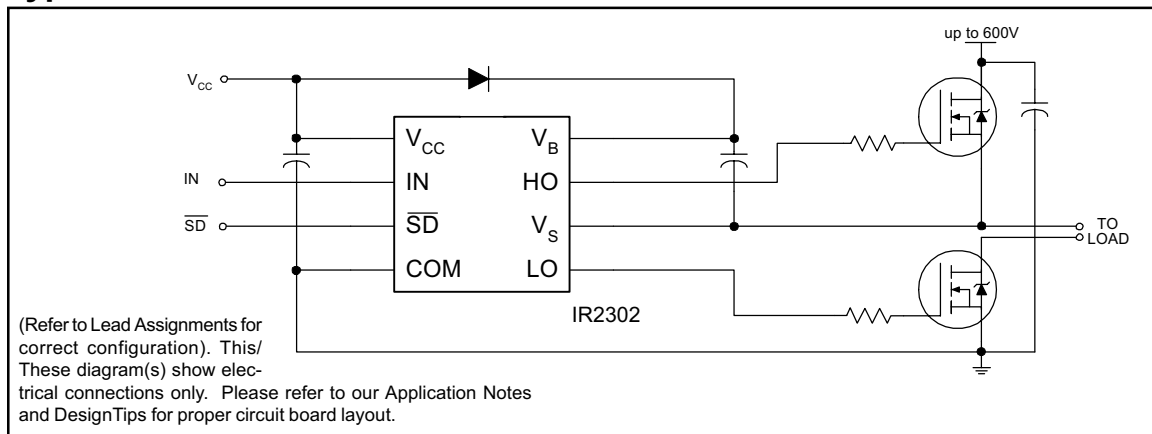
### Packages



### 2106/2301//2108//2109/2302/2304 Feature Comparison

| Part      | Input logic | Cross-conduction prevention logic | Dead-Time             | Ground Pins |
|-----------|-------------|-----------------------------------|-----------------------|-------------|
| 2106/2301 | HIN/LIN     | no                                | none                  | COM         |
| 21064     |             |                                   |                       | VSS/COM     |
| 2108      | HIN/LIN     | yes                               | Internal 540ns        | COM         |
| 21084     |             |                                   | Programmable 0.54~5μs | VSS/COM     |
| 2109/2302 | IN/SD       | yes                               | Internal 540ns        | COM         |
| 21094     |             |                                   | Programmable 0.54~5μs | VSS/COM     |
| 2304      | HIN/LIN     | yes                               | Internal 100ns        | COM         |

### Typical Connection



# IR2302(s) & (PbF)

International  
IR Rectifier

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol     | Definition                                               | Min.        | Max.           | Units              |
|------------|----------------------------------------------------------|-------------|----------------|--------------------|
| $V_B$      | High side floating absolute voltage                      | -0.3        | 625            | V                  |
| $V_S$      | High side floating supply offset voltage                 | $V_B - 25$  | $V_B + 0.3$    |                    |
| $V_{HO}$   | High side floating output voltage                        | $V_S - 0.3$ | $V_B + 0.3$    |                    |
| $V_{CC}$   | Low side and logic fixed supply voltage                  | -0.3        | 25             |                    |
| $V_{LO}$   | Low side output voltage                                  | -0.3        | $V_{CC} + 0.3$ |                    |
| $V_{IN}$   | Logic input voltage (IN & $\overline{SD}$ )              | COM - 0.3   | $V_{CC} + 0.3$ |                    |
| $dV_S/dt$  | Allowable offset supply voltage transient                | —           | 50             | V/ns               |
| $P_D$      | Package power dissipation @ $T_A \leq +25^\circ\text{C}$ | —           | 1.0            | W                  |
|            | (8 Lead PDIP)<br>(8 Lead SOIC)                           | —           | 0.625          |                    |
| $R_{thJA}$ | Thermal resistance, junction to ambient                  | —           | 125            | $^\circ\text{C/W}$ |
|            | (8 Lead PDIP)<br>(8 Lead SOIC)                           | —           | 200            |                    |
| $T_J$      | Junction temperature                                     | —           | 150            | $^\circ\text{C}$   |
| $T_S$      | Storage temperature                                      | -50         | 150            |                    |
| $T_L$      | Lead temperature (soldering, 10 seconds)                 | —           | 300            |                    |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

| Symbol   | Definition                                  | Min.      | Max.       | Units            |
|----------|---------------------------------------------|-----------|------------|------------------|
| $V_B$    | High side floating supply absolute voltage  | $V_S + 5$ | $V_S + 20$ | V                |
| $V_S$    | High side floating supply offset voltage    | Note 1    | 600        |                  |
| $V_{HO}$ | High side floating output voltage           | $V_S$     | $V_B$      |                  |
| $V_{CC}$ | Low side and logic fixed supply voltage     | 5         | 20         |                  |
| $V_{LO}$ | Low side output voltage                     | 0         | $V_{CC}$   |                  |
| $V_{IN}$ | Logic input voltage (IN & $\overline{SD}$ ) | COM       | $V_{CC}$   |                  |
| $T_A$    | Ambient temperature                         | -40       | 150        | $^\circ\text{C}$ |

Note 1: Logic operational for  $V_S$  of -5 to +600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF, and  $T_A$  = 25°C unless otherwise specified.

| Symbol    | Definition                                                                                       | Min. | Typ. | Max. | Units | Test Conditions    |
|-----------|--------------------------------------------------------------------------------------------------|------|------|------|-------|--------------------|
| $t_{on}$  | Turn-on propagation delay                                                                        | 550  | 750  | 950  | nsec  | $V_S = 0V$         |
| $t_{off}$ | Turn-off propagation delay                                                                       | —    | 200  | 280  |       | $V_S = 0V$ or 600V |
| $t_{sd}$  | Shut-down propagation delay                                                                      | —    | 200  | 280  |       |                    |
| MT        | Delay matching, HS & LS turn-on/off                                                              | —    | 0    | 50   |       |                    |
| $t_r$     | Turn-on rise time                                                                                | —    | 130  | 220  |       | $V_S = 0V$         |
| $t_f$     | Turn-off fall time                                                                               | —    | 50   | 80   |       | $V_S = 0V$         |
| DT        | Deadtime: LO turn-off to HO turn-on( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ ) | 400  | 540  | 680  |       |                    |
| MDT       | Deadtime matching = $DT_{LO} - HO - DT_{HO-LO}$                                                  | —    | 0    | 60   |       |                    |

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to COM and are applicable to the respective input leads: IN and  $\overline{SD}$ . The  $V_O$ ,  $I_O$  and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

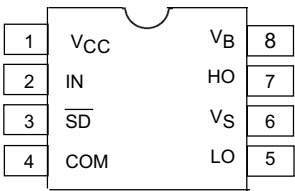
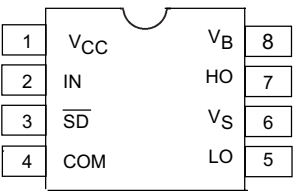
| Symbol                     | Definition                                                         | Min. | Typ. | Max. | Units   | Test Conditions               |
|----------------------------|--------------------------------------------------------------------|------|------|------|---------|-------------------------------|
| $V_{IH}$                   | Logic "1" input voltage for HO & logic "0" for LO                  | 2.9  | —    | —    | V       | $V_{CC} = 10V$ to 20V         |
| $V_{IL}$                   | Logic "0" input voltage for HO & logic "1" for LO                  | —    | —    | 0.8  |         | $V_{CC} = 10V$ to 20V         |
| $V_{SD,TH+}$               | $\overline{SD}$ input positive going threshold                     | 2.9  | —    | —    |         | $V_{CC} = 10V$ to 20V         |
| $V_{SD,TH-}$               | $\overline{SD}$ input negative going threshold                     | —    | —    | 0.8  |         | $V_{CC} = 10V$ to 20V         |
| $V_{OH}$                   | High level output voltage, $V_{BIAS} - V_O$                        | —    | 0.8  | 1.4  |         | $I_O = 20$ mA                 |
| $V_{OL}$                   | Low level output voltage, $V_O$                                    | —    | 0.3  | 0.6  |         | $I_O = 20$ mA                 |
| $I_{LK}$                   | Offset supply leakage current                                      | —    | —    | 50   | $\mu A$ | $V_B = V_S = 600V$            |
| $I_{QBS}$                  | Quiescent $V_{BS}$ supply current                                  | 20   | 60   | 100  |         | $V_{IN} = 0V$ or 5V           |
| $I_{QCC}$                  | Quiescent $V_{CC}$ supply current                                  | 0.4  | 1.0  | 1.6  | $mA$    | $V_{IN} = 0V$ or 5V           |
| $I_{IN+}$                  | Logic "1" input bias current                                       | —    | 5    | 20   | $\mu A$ | $IN = 5V, \overline{SD} = 0V$ |
| $I_{IN-}$                  | Logic "0" input bias current                                       | —    | —    | 2    |         | $IN = 0V, \overline{SD} = 5V$ |
| $V_{CCUV+}$<br>$V_{BSUV+}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold | 3.3  | 4.1  | 5    | V       |                               |
| $V_{CCUV-}$<br>$V_{BSUV-}$ | $V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold | 3    | 3.8  | 4.7  |         |                               |
| $V_{CCUVH}$<br>$V_{BSUVH}$ | Hysteresis                                                         | 0.1  | 0.3  | —    |         |                               |
| $I_{O+}$                   | Output high short circuit pulsed current                           | 120  | 200  | —    | $mA$    | $V_O = 0V, PW \leq 10 \mu s$  |
| $I_{O-}$                   | Output low short circuit pulsed current                            | 250  | 350  | —    |         | $V_O = 15V, PW \leq 10 \mu s$ |



## Lead Definitions

| Symbol                 | Description                                                                         |
|------------------------|-------------------------------------------------------------------------------------|
| IN                     | Logic input for high and low side gate driver outputs (HO and LO), in phase with HO |
| $\overline{\text{SD}}$ | Logic input for shutdown                                                            |
| $V_B$                  | High side floating supply                                                           |
| HO                     | High side gate drive output                                                         |
| $V_S$                  | High side floating supply return                                                    |
| $V_{CC}$               | Low side and logic fixed supply                                                     |
| LO                     | Low side gate drive output                                                          |
| COM                    | Low side return                                                                     |

## Lead Assignments

|                                                                                                        |                                                                                                                                              |
|--------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>8 Lead PDIP</p> |  <p>8 Lead SOIC<br/>(Also available LEAD-FREE (PbF))</p> |
| <b>IR2302</b>                                                                                          | <b>IR2302S</b>                                                                                                                               |

# IR2302(s) & (PbF)

International  
**IR** Rectifier

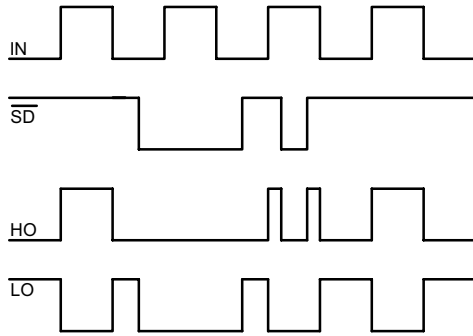


Figure 1. Input/Output Timing Diagram

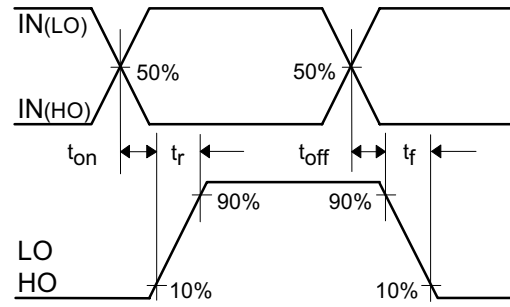


Figure 2. Switching Time Waveform Definitions

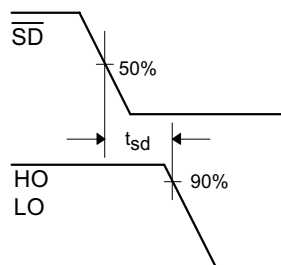


Figure 3. Shutdown Waveform Definitions

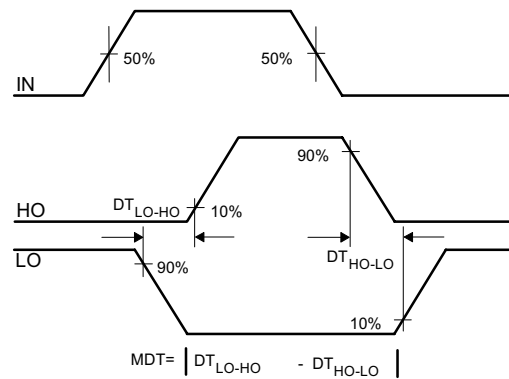


Figure 4. Deadtime Waveform Definitions

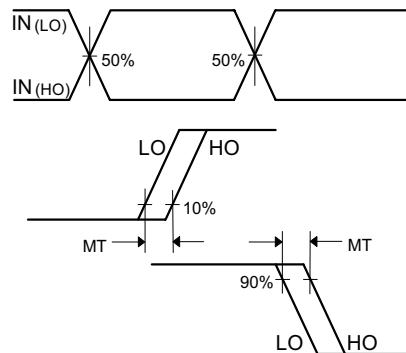


**Figure 5. Delay Matching Waveform Definitions**

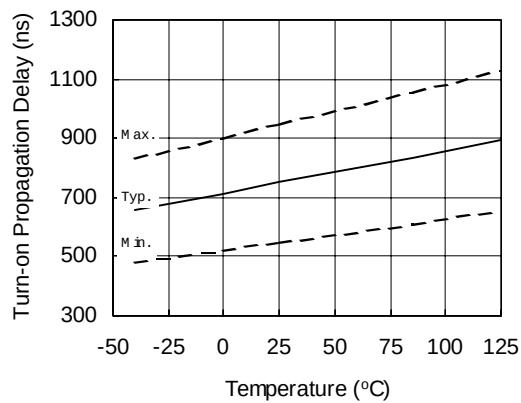


**Figure 6A. Turn-on Propagation Delay vs. Temperature**

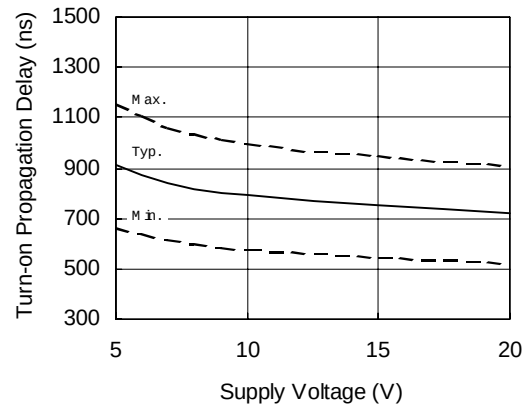


**Figure 6B. Turn-on Propagation Delay vs. Supply Voltage**

# IR2302(s) & (PbF)

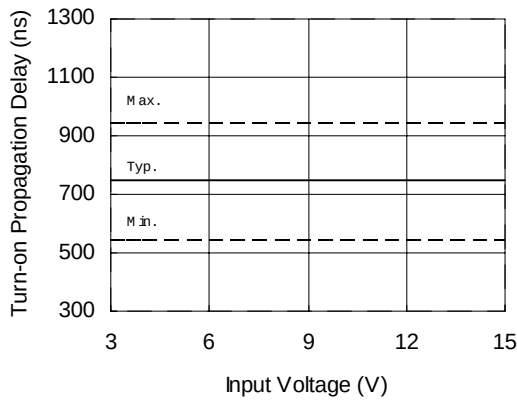


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

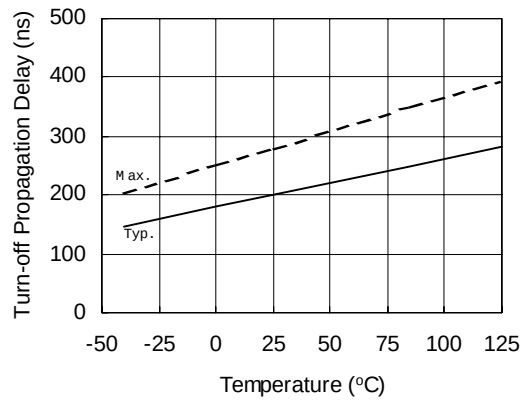


Figure 7A. Turn-off Propagation Delay vs. Temperature

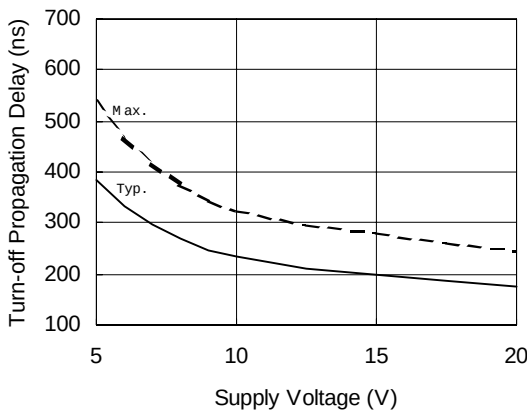


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

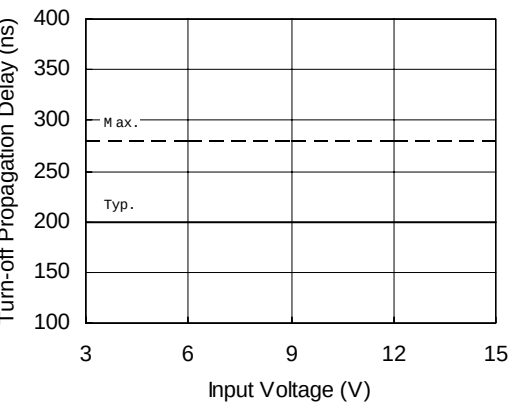


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

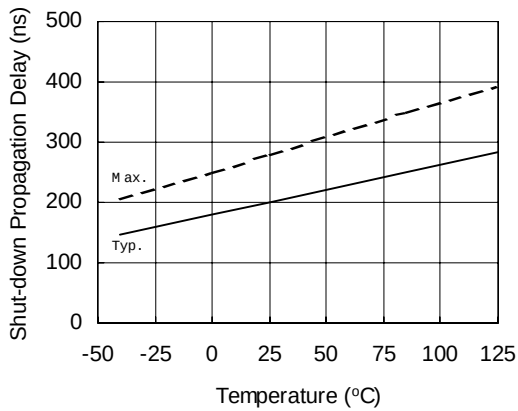


**Figure 8A. Shut-down Propagation Delay vs. Temperature**

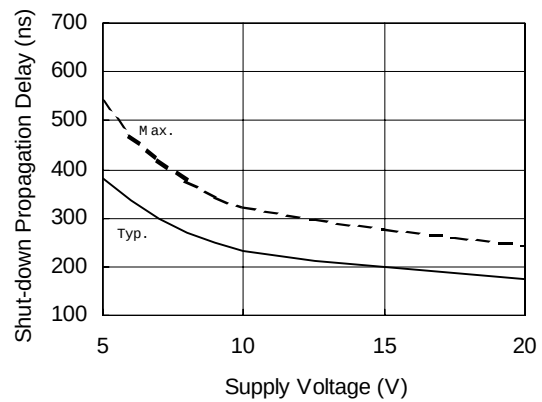


**Figure 8B. Shut-down Propagation Delay vs. Supply Voltage**

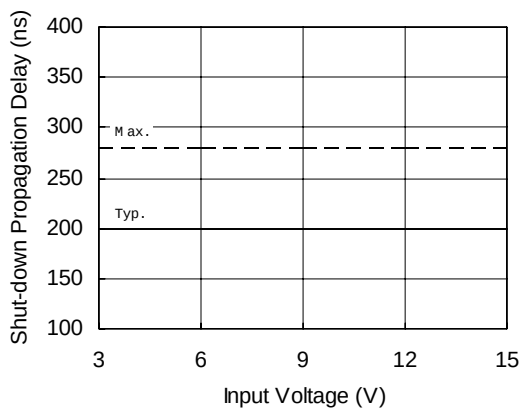


**Figure 8C. Shut-down Propagation Delay vs. Input Voltage**

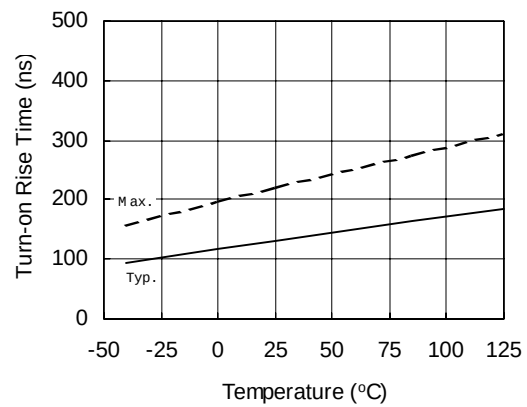


**Figure 9A. Turn-on Rise Time vs. Temperature**

# IR2302(s) & (PbF)

International  
**IR** Rectifier

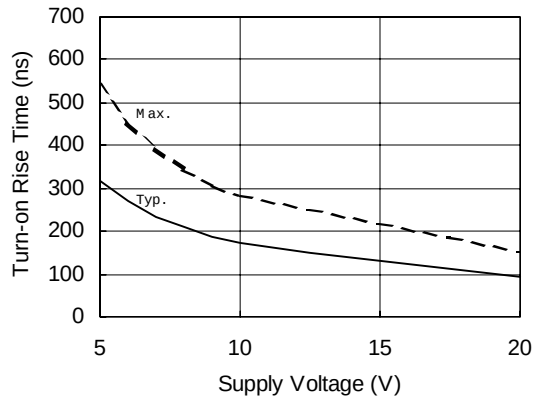


**Figure 9B. Turn-on Rise Time  
vs. Supply Voltage**

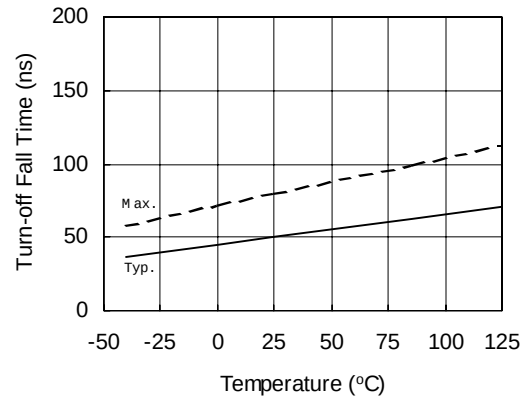


**Figure 10A. Turn-off Fall Time  
vs. Temperature**

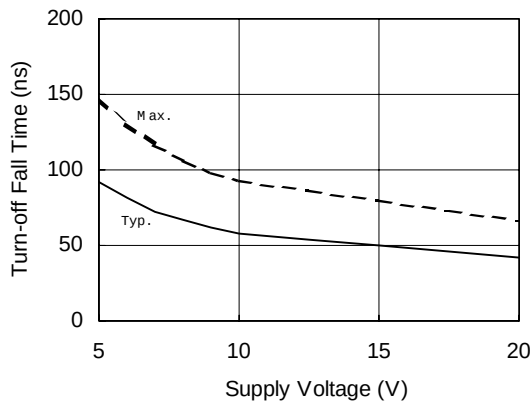


**Figure 10B. Turn-off Fall Time  
vs. Supply Voltage**

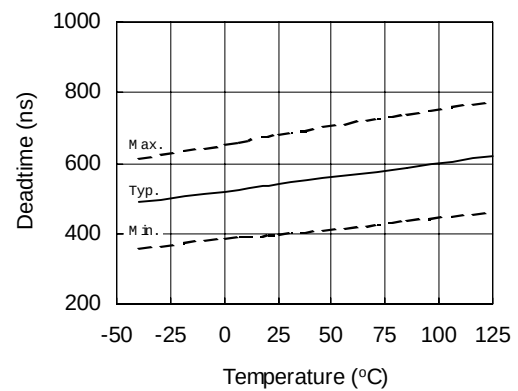


**Figure 11A. Deadtime  
vs. Temperature**

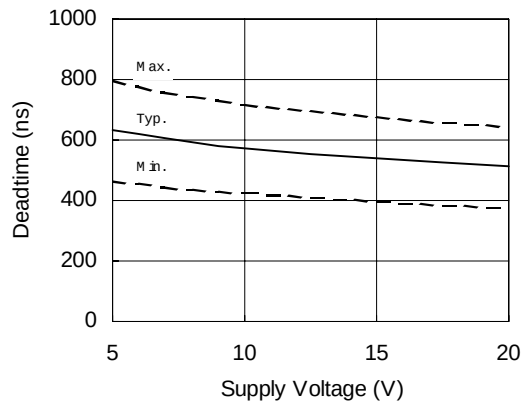


**Figure 11B. Deadtime vs. Supply Voltage**

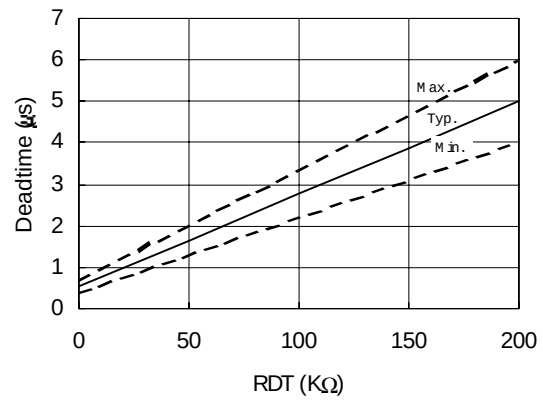


**Figure 11C. Deadtime vs. RDT**

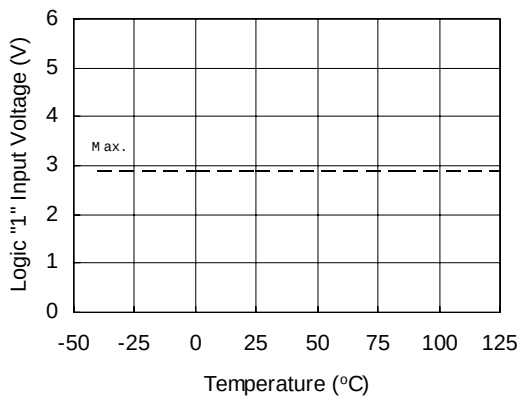


**Figure 12A. Logic "1" Input Voltage vs. Temperature**

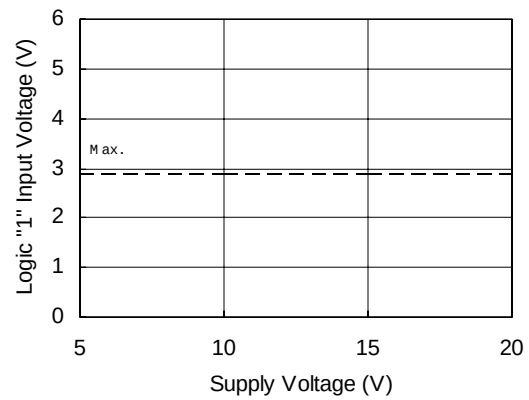


**Figure 12B. Logic "1" Input Voltage vs. Supply Voltage**

# IR2302(s) & (PbF)

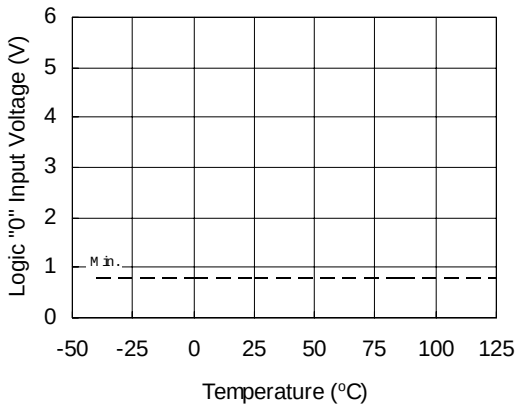


Figure 13A. Logic "0" Input Voltage vs. Temperature

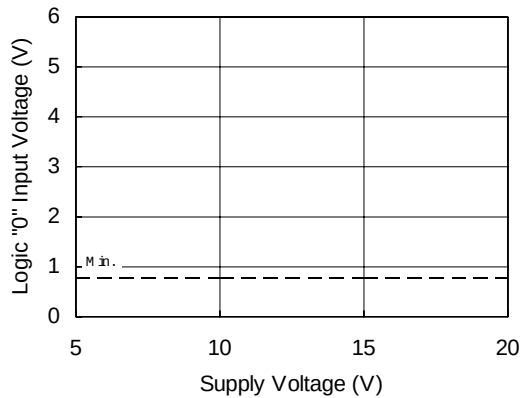


Figure 13B. Logic "0" Input Voltage vs. Supply Voltage

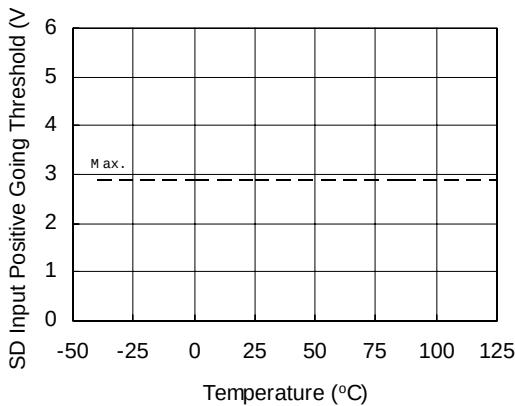


Figure 14A. SD Input Positive Going Threshold vs. Temperature

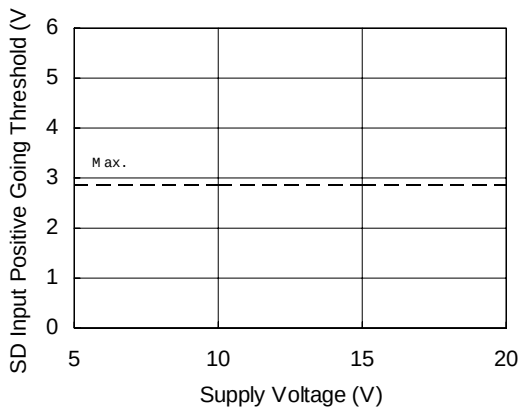


Figure 14B. SD Input Positive Going Threshold vs. Supply Voltage

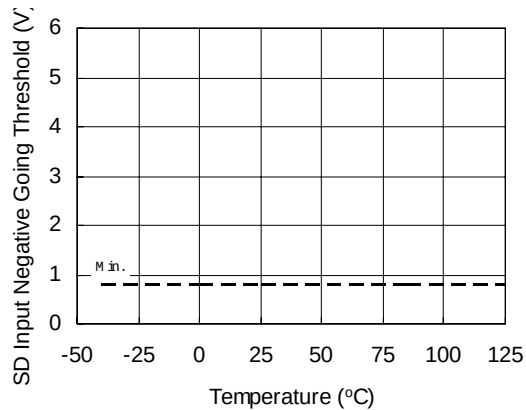


**Figure 15A. SD Input Negative Going Threshold vs. Temperature**

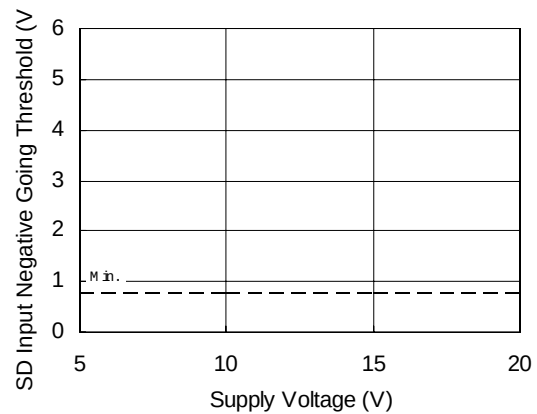


**Figure 15B. SD Input Negative Going Threshold vs. Supply Voltage**

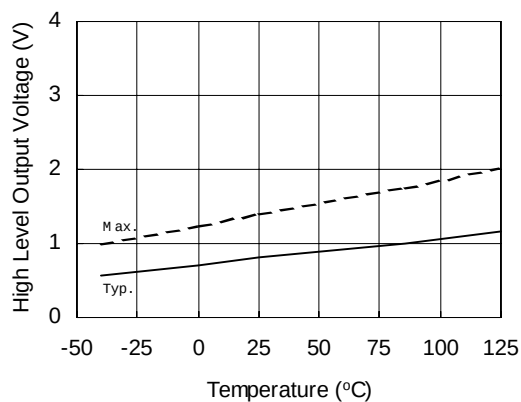


**Figure 16A. High Level Output Voltage vs. Temperature**

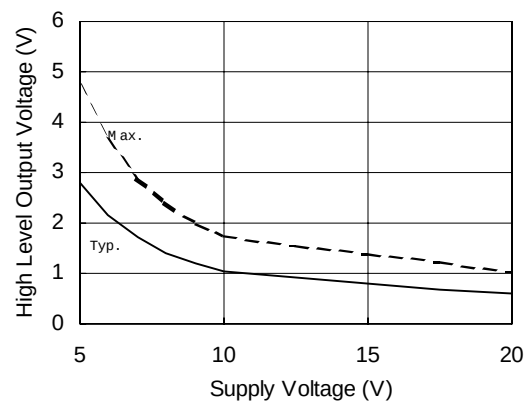


**Figure 16B. High Level Output Voltage vs. Supply Voltage**

# IR2302(s) & (PbF)

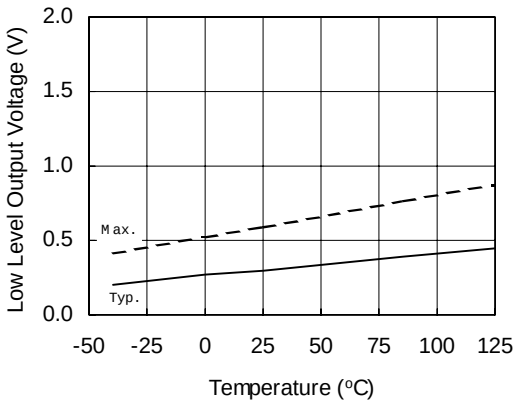


Figure 17A. Low Level Output Voltage vs. Temperature

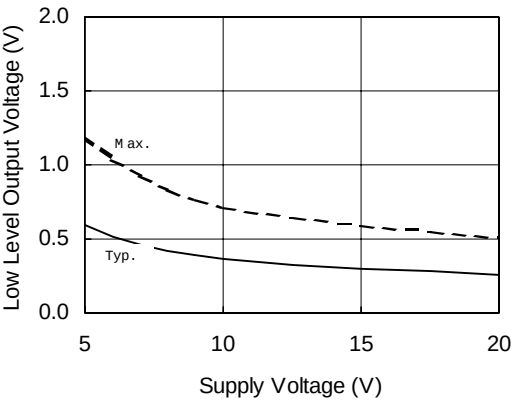


Figure 17B. Low Level Output Voltage vs. Supply Voltage

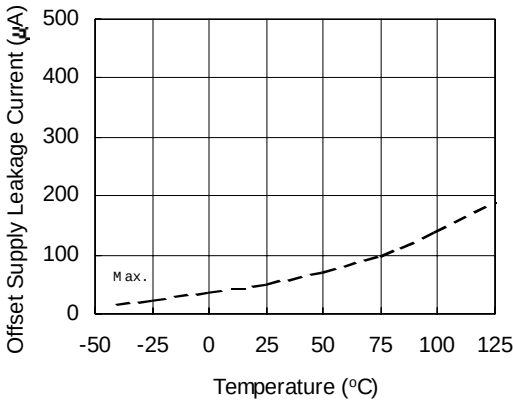


Figure 18A. Offset Supply Leakage Current vs. Temperature

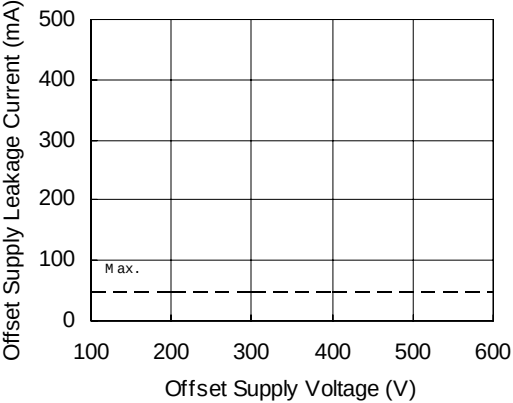


Figure 18B. Offset Supply Leakage Current vs. Offset Supply Voltage

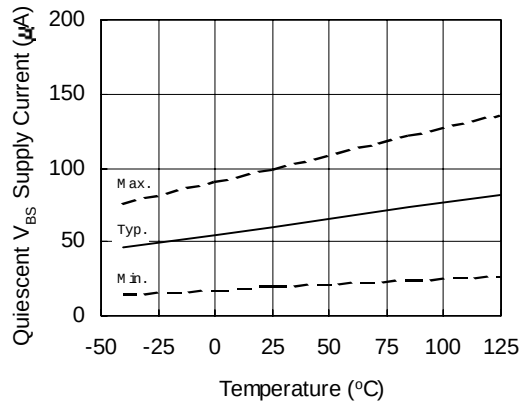


**Figure 19A. Quiescent  $V_{BS}$  Supply Current vs. Temperature**

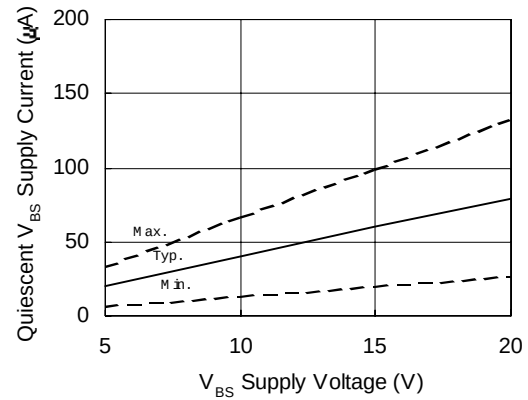


**Figure 19B. Quiescent  $V_{BS}$  Supply Current vs.  $V_{BS}$  Supply Voltage**

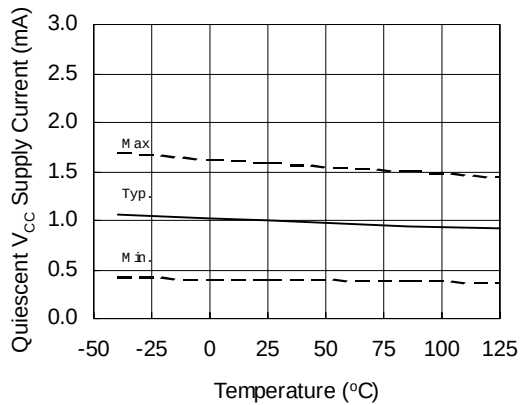


**Figure 20A. Quiescent  $V_{CC}$  Supply Current vs. Temperature**

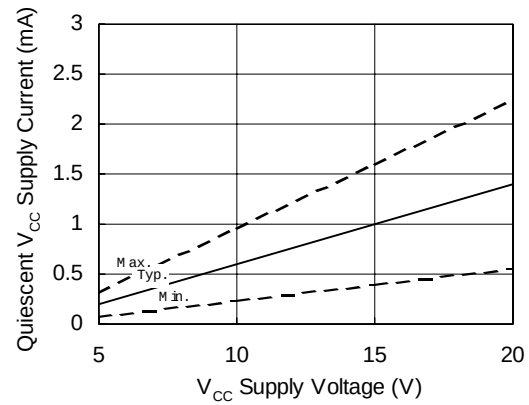


**Figure 20B. Quiescent  $V_{CC}$  Supply Current vs.  $V_{CC}$  Supply Voltage**

# IR2302(s) & (PbF)

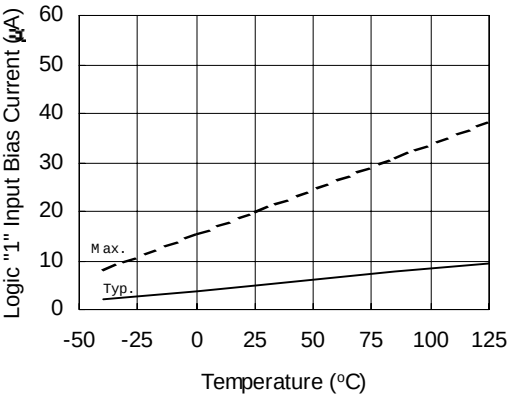


Figure 21A. Logic "1" Input Bias Current vs. Temperature

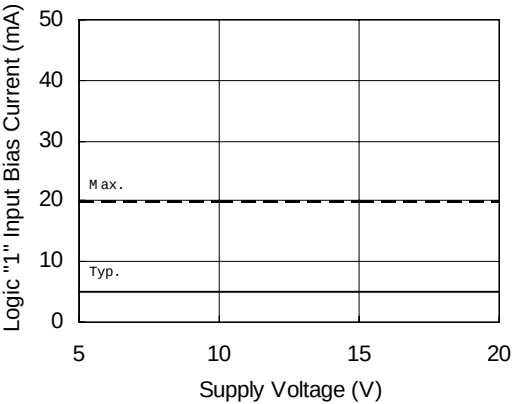


Figure 21B. Logic "1" Input Bias Current vs. Supply Voltage

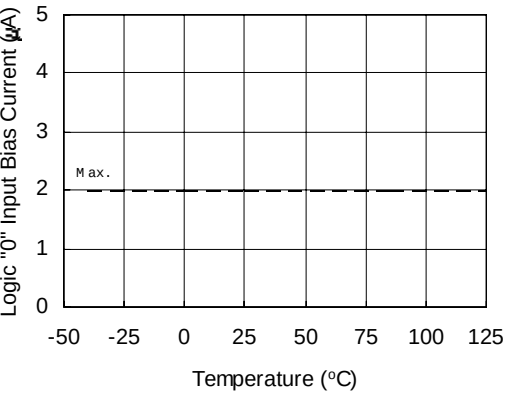


Figure 22A. Logic "0" Input Bias Current vs. Temperature

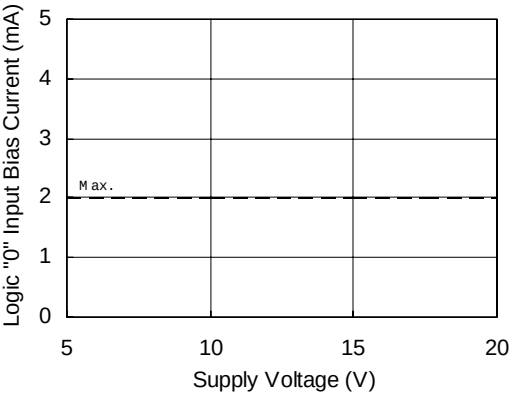


Figure 22B. Logic "0" Input Bias Current vs. Supply Voltage

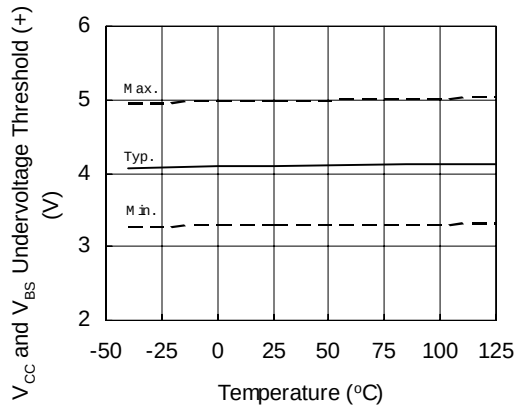


**Figure 23.  $V_{CC}$  and  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**

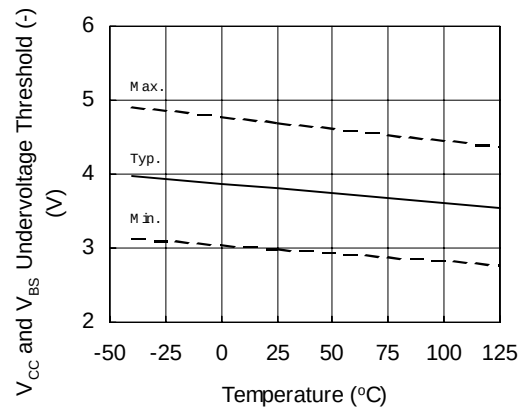


**Figure 24.  $V_{CC}$  and  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**

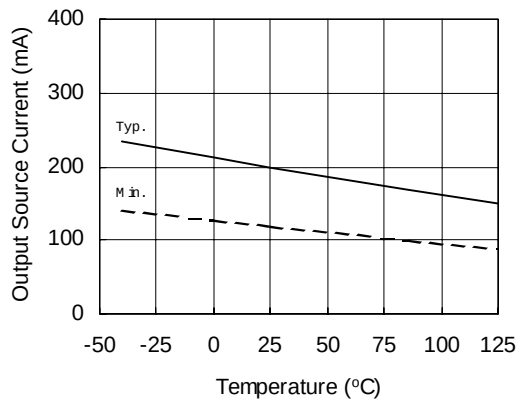


**Figure 25A. Output Source Current vs. Temperature**

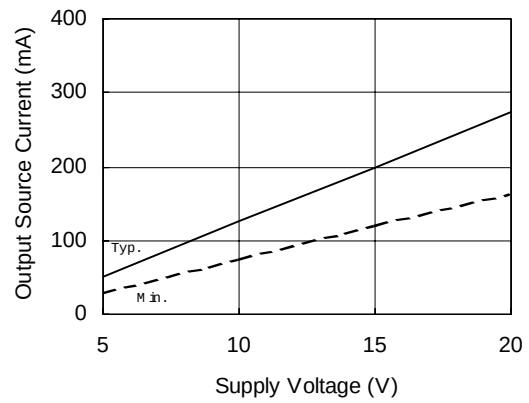


**Figure 25B. Output Source Current vs. Supply Voltage**

# IR2302(s) & (PbF)

International  
**IR** Rectifier

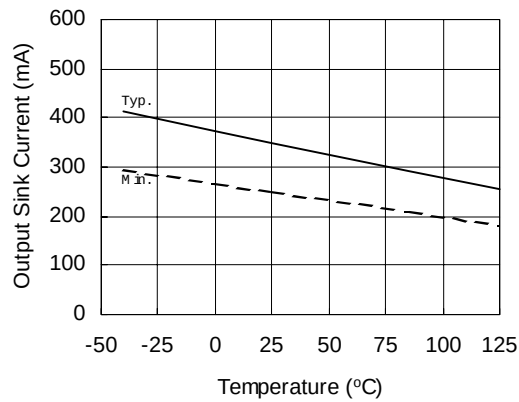


**Figure 26A. Output Sink Current vs. Temperature**

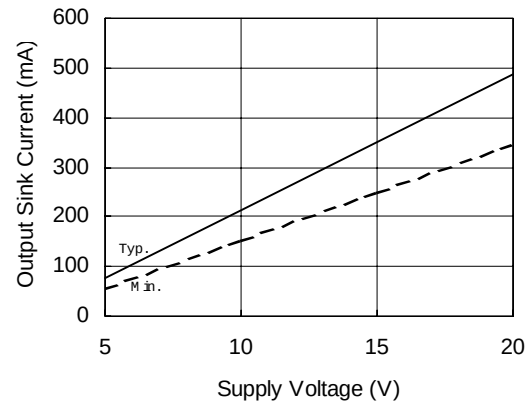


**Figure 26B. Output Sink Current vs. Supply Voltage**

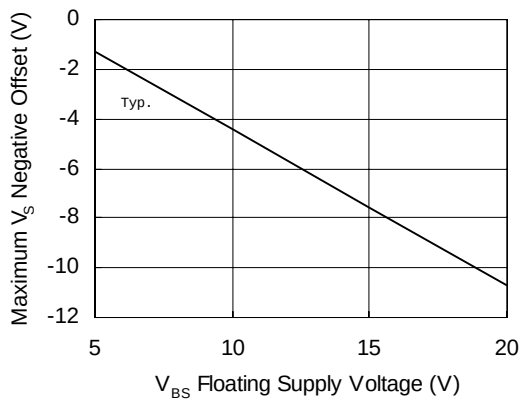


**Figure 27. Maximum V<sub>s</sub> Negative Offset vs. V<sub>BS</sub> Floating Supply Voltage**

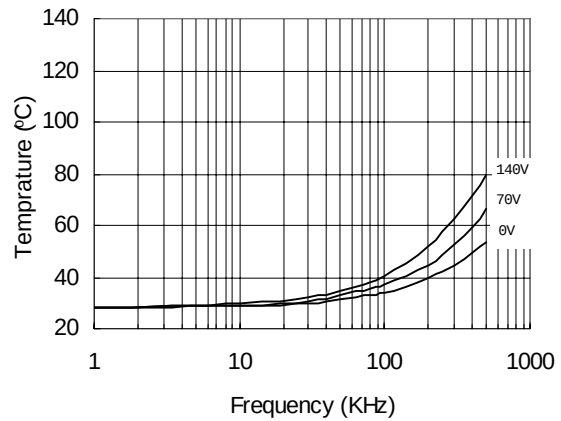


**Figure 28. IR2302 vs. Frequency (IRFBC20),  
R<sub>gate</sub> = 33Ω, V<sub>CC</sub> = 15V**

## IR2302(s) & (PbF)

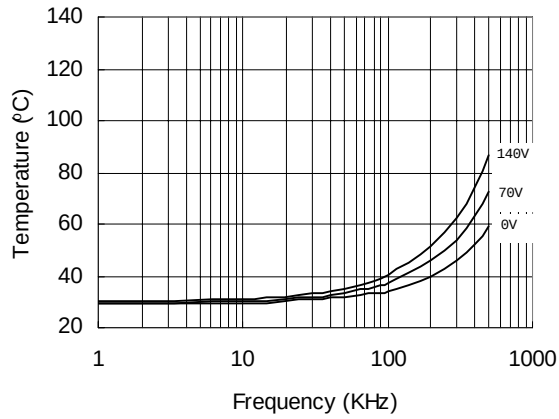


Figure 29. IR2302 vs. Frequency (IRFBC30),  
 $R_{gate}=22\Omega$ ,  $V_{CC}=15V$

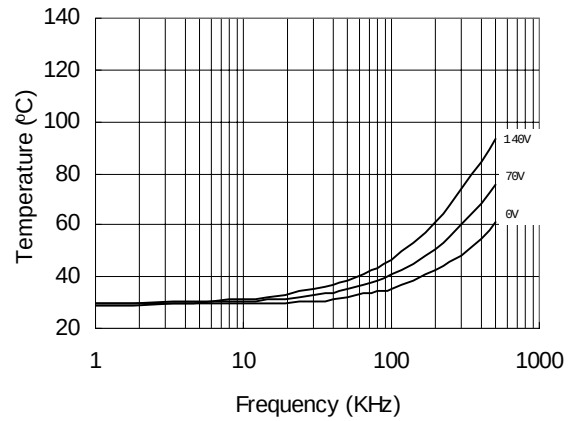


Figure 30. IR2302 vs. Frequency (IRFBC40),  
 $R_{gate}=15\Omega$ ,  $V_{CC}=15V$

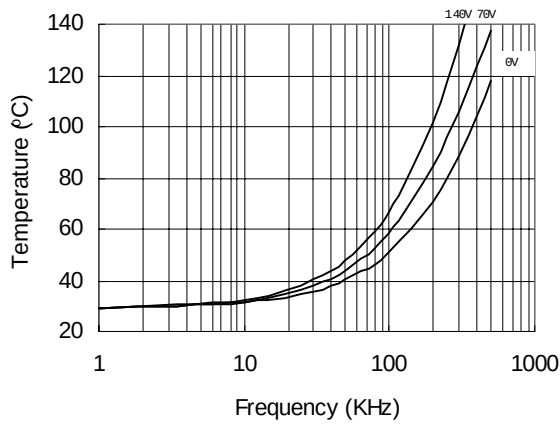


Figure 31. IR2302 vs. Frequency (IRFPE50),  
 $R_{gate}=10\Omega$ ,  $V_{CC}=15V$

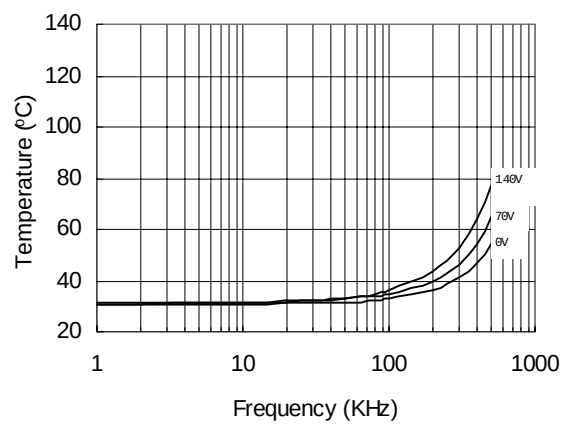


Figure 32. IR2302S vs. Frequency (IRFBC20),  
 $R_{gate}=33\Omega$ ,  $V_{CC}=15V$

# IR2302(s) & (PbF)

International  
**IR** Rectifier

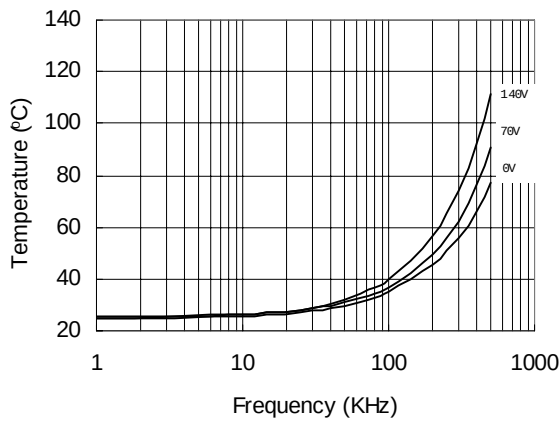


Figure 33. IR2302S vs. Frequency (IRFBC30),  
 $R_{gate}=22\Omega$ ,  $V_{CC}=15V$

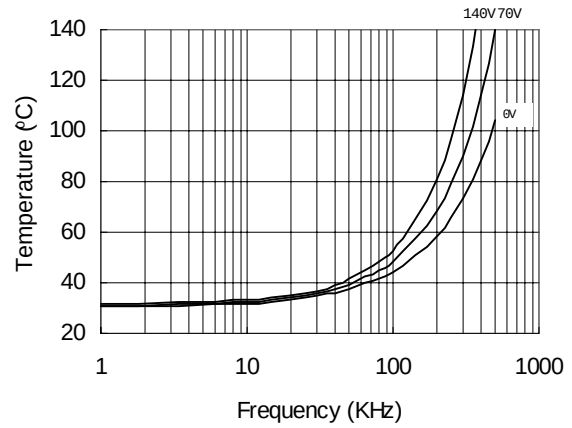


Figure 34. IR2302S vs. Frequency (IRFBC40),  
 $R_{gate}=15\Omega$ ,  $V_{CC}=15V$

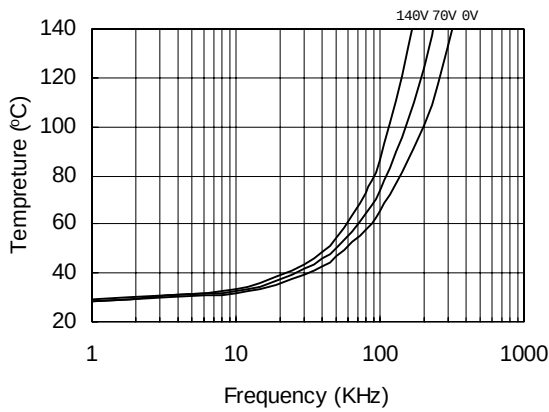
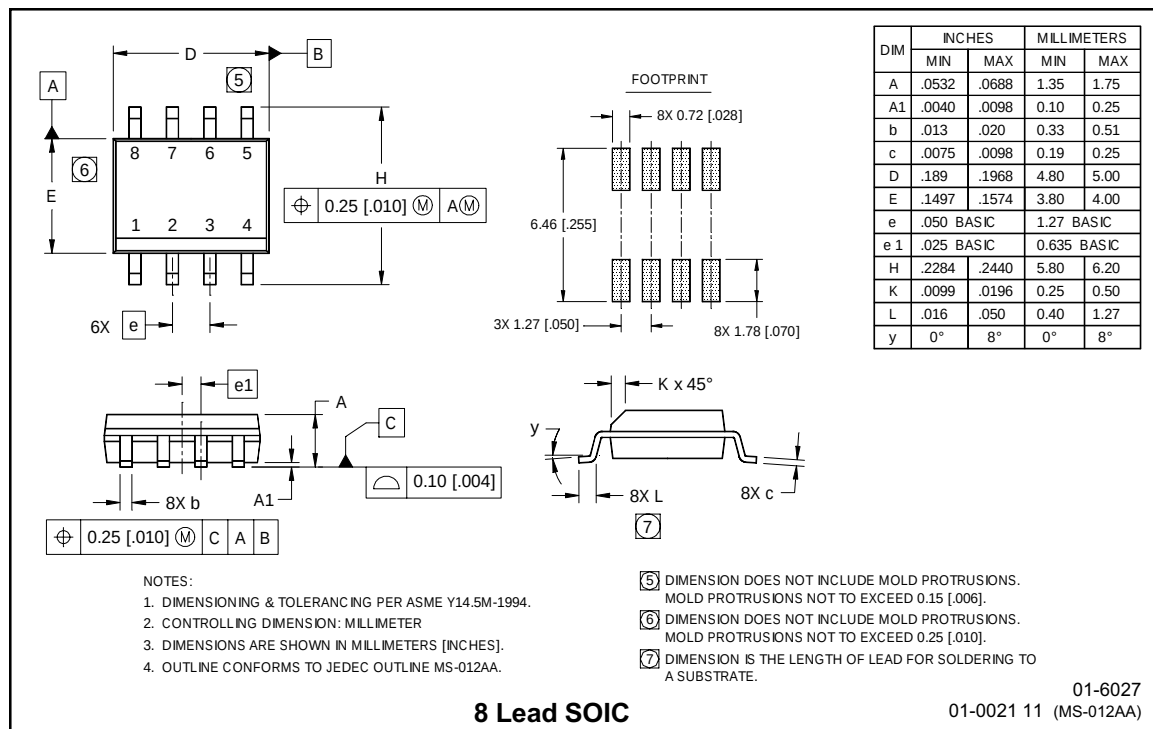
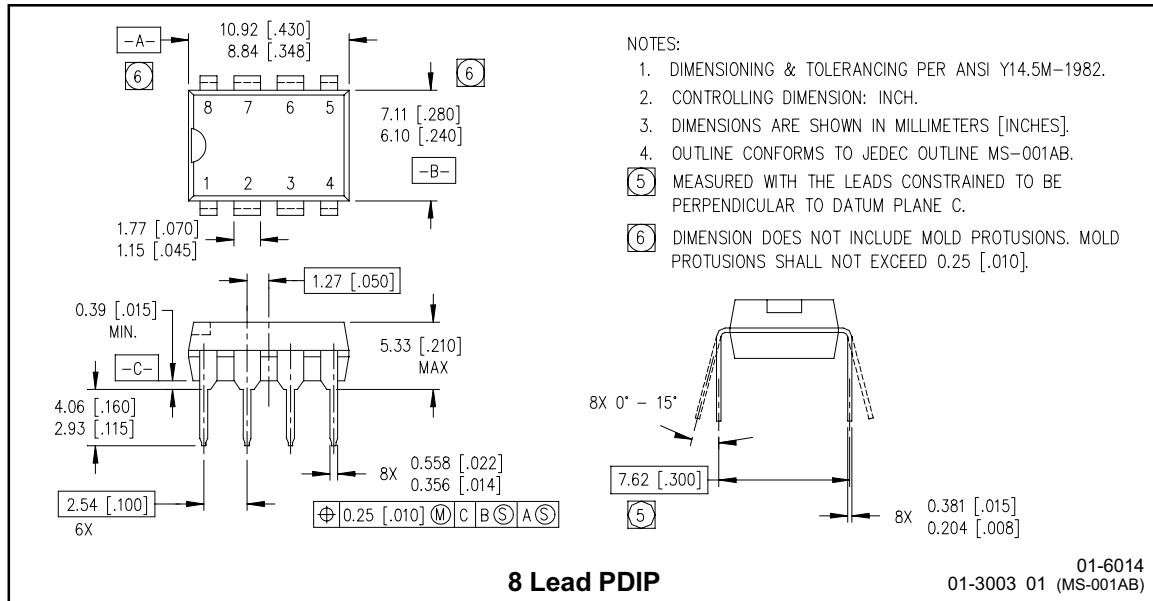


Figure 35. IR2302S vs. Frequency  
(IRFPE50),  $R_{gate}=10\Omega$ ,  $V_{CC}=15V$

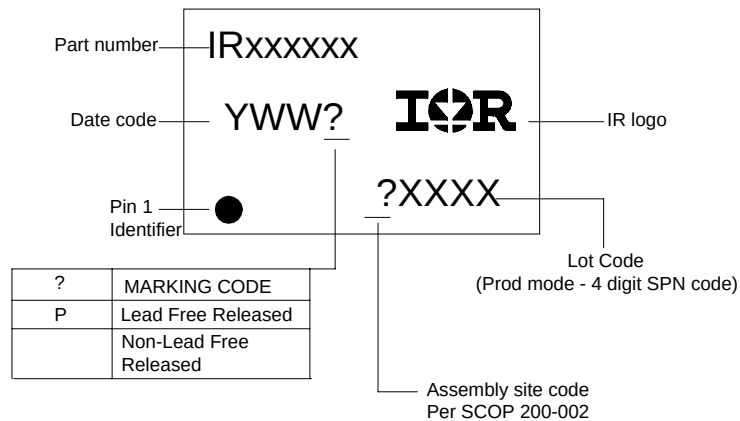
## Case Outlines



# IR2302(s) & (PbF)

International  
**IR** Rectifier

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

8-Lead PDIP IR2302 order IR2302  
8-Lead SOIC IR2302S order IR2302S

### Leadfree Part

8-Lead PDIP R2302 not available  
8-Lead SOIC IR2302S order IR2302SPbF

International  
**IR** Rectifier

This product has been designed and qualified for the Industrial market.

Qualification Standards can be found on IR's Web Site <http://www.irf.com>

Data and specifications subject to change without notice.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

8/16/2004

## Данный компонент на территории Российской Федерации

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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