8-Channel, 1 MSPS, 10-Bit SAR ADC

AD7298-1

FEATURES

10-bit SAR ADC
- **8 single-ended inputs**
- **Channel sequencer functionality**
- **Fast throughput of 1 MSPS**
- **Analog input range: 0 V to 2.5 V**

Temperature range: −40°C to +125°C
Specified for V_{DD} of 2.8 V to 3.6 V
Logic voltage V_{DRIVE} = 1.65 V to 3.6 V
Power-down current: <10 µA
Internal 2.5 V reference
Internal power-on reset
High speed serial interface SPI
20-lead LFCSP

FUNCTIONAL BLOCK DIAGRAM

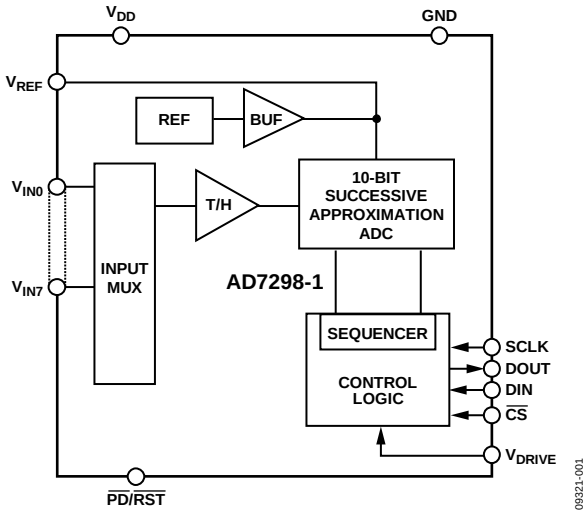

Figure 1.

GENERAL DESCRIPTION

The AD7298-1 is a 10-bit, high speed, low power, 8-channel, successive approximation ADC. The part operates from a single 3.3 V power supply and features throughput rates up to 1 MSPS. The device contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 30 MHz.

The AD7298-1 offers a programmable sequencer, which enables the selection of a preprogrammable sequence of channels for conversion. The device has an on-chip, 2.5 V reference that can be disabled to allow the use of an external reference.

The device offers a 4-wire serial interface compatible with SPI and DSP interface standards.

The AD7298-1 uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part also offers flexible power/throughput rate management options. The part is offered in a 20-lead LFCSP package.

PRODUCT HIGHLIGHTS

1. Ideally Suited to Monitoring System Variables in a Variety of Systems. This includes telecommunications, and process and industrial control.
2. High Throughput Rate of 1 MSPS with Low Power Consumption.
3. Eight Single-Ended Inputs with a Channel Sequencer. A consecutive sequence of channels can be selected on which the ADC cycles and converts.

Rev. A

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REVISION HISTORY

1/11—Rev. 0 to Rev. A

Removed Input Impedance Parameter ... 3
Added Input Capacitance Parameter of 8 pF ... 3
Changes to Figure 10 ... 10
Changed C1 Value to 8 pF in Analog Input Section ... 13
Changes to Figure 22 ... 14

10/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.8 V to 3.6 V, V_{DRIVE} = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, V_{REF} = 2.5 V internal, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[1]	61	61.5		dB	
Signal-to-Noise-(and-Distortion) Ratio (SINAD)[2]	61	61.5		dB	
Total Harmonic Distortion (THD)[2]		−82	−75	dB	
Spurious-Free Dynamic Range (SFDR)		−83	−76	dB	
Intermodulation Distortion (IMD)					f_A = 40.1 kHz, f_B = 41.5 kHz
Second-Order Terms		−86		dB	
Third-Order Terms		−86		dB	
Channel-to-Channel Isolation		−90		dB	f_{IN} = 50 kHz, f_{NOISE} = 60 kHz
SAMPLE AND HOLD					
Aperture Delay[3]			12	ns	
Aperture Jitter[3]		40		ps	
Full Power Bandwidth		30		MHz	At 3 dB
		10		MHz	At 0.1 dB
DC ACCURACY					
Resolution	10			Bits	
Integral Nonlinearity (INL)[2]		±0.25	±0.5	LSB	
Differential Nonlinearity (DNL)[2]		±0.3	±0.5	LSB	Guaranteed no missed codes to 10 bits
Offset Error[2]		±0.5	±1.125	LSB	
Offset Error Matching[2]		±0.625	±1.125	LSB	
Offset Temperature Drift		4		ppm/°C	
Gain Error[2]		±0.25	±1	LSB	
Gain Error Matching[2]		±0.16	±0.625	LSB	
Gain Temperature Drift		0.5		ppm/°C	
ANALOG INPUT					
Input Voltage Ranges	0		V_{REF}	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance		32		pF	When in track mode
		8		pF	When in hold mode
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[4]	2.4925	2.5	2.5075	V	±0.3% maximum at 25°C
Long-Term Stability		150		ppm	For 1000 hours
Output Voltage Hysteresis		50		ppm	
Reference Input Voltage Range	1		2.5	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to the V_{REF} pin
V_{REF} Output Impedance		1		Ω	
V_{REF} Temperature Coefficient		12	35	ppm/°C	
V_{REF} Noise		60		µV rms	Bandwidth = 10 MHz
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}			V	
Input Low Voltage, V_{INL}			0.3 × V_{DRIVE}	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		3		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.3$			V	$V_{DRIVE} < 1.8$
	$V_{DRIVE} - 0.2$			V	$V_{DRIVE} \geq 1.8$
Output Low Voltage, V_{OL}			0.4	V	
Floating State Leakage Current		±0.01	±1	μA	
Floating State Output Capacitance[3]		8		pF	
CONVERSION RATE					
Conversion Time		1	$t_2 + (16 \times t_{SCLK})$	μs	For V_{IN0} to V_{IN7} with one cycle latency
Track-and-Hold Acquisition Time[2, 3]			100	ns	Full-scale step input
Throughput Rate			1	MSPS	f_{SCLK} = 20 MHz; for analog voltage conversions, one cycle latency
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	2.8	3	3.6	V	
V_{DRIVE}	1.65	3	3.6	V	
I_{TOTAL}[5]					V_{DD} = 3.6 V, V_{DRIVE} = 3.6 V
Normal Mode (Operational)		5.8	6.4	mA	
Normal Mode (Static)		4.1	4.6	mA	
Partial Power-Down Mode		2.7	3.3	mA	
Full Power-Down Mode		1	1.6	μA	T_A = −40°C to +25°C
			10	μA	T_A = −40°C to +125°C
Power Dissipation[6]					
Normal Mode (Operational)		17.4	19.2	mW	V_{DD} = 3 V, V_{DRIVE} = 3 V
			23	mW	
Normal Mode (Static)		14.8	16.6	mW	
Partial Power-Down Mode		9.8	11.9	mW	
Full Power-Down Mode		3.6	5.8	μW	T_A = −40°C to +25°C
			36	μW	T_A = −40°C to +125°C

[1] All specifications expressed in decibels are referred to full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] Refers to the V_{REF} pin specified for 25°C.
[5] I_{TOTAL} is the total current flowing in V_{DD} and V_{DRIVE}.
[6] Power dissipation is specified with $V_{DD} = V_{DRIVE}$ = 3.6 V, unless otherwise noted.

TIMING SPECIFICATIONS

V_{DD} = 2.8 V to 3.6 V, V_{DRIVE} = 1.65 V to 3.6 V, V_{REF} = 2.5 V internal, T_A = −40°C to +125°C, unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Conditions/Comments
$t_{CONVERT}$	$t_2 + (16 \times t_{SCLK})$	µs max	Conversion time
	820	ns typ	Each ADC channel V_{IN0} to V_{IN7}, f_{SCLK} = 20 MHz
f_{SCLK}[1]	50	kHz min	Frequency of external serial clock
	20	MHz max	Frequency of external serial clock
t_{QUIET}	6	ns min	Minimum quiet time required between the end of the serial read and the start of the next voltage conversion in repeat and nonrepeat mode.
t_2	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[1]	15	ns max	Delay from $\overline{CS}$ (falling edge) until DOUT three-state disabled
t_4[1]			Data access time after SCLK falling edge
	35	ns max	V_{DRIVE} = 1.65 V to 3 V
	28	ns max	V_{DRIVE} = 3 V to 3.6 V
t_5	$0.4 \times t_{SCLK}$	ns min	SCLK low pulse width
t_6	$0.4 \times t_{SCLK}$	ns min	SCLK high pulse width
t_7[1]	14	ns min	SCLK to DOUT valid hold time
t_8[1]	16/34	ns min/ns max	SCLK falling edge to DOUT high impedance
t_9	5	ns min	DIN setup time prior to SCLK falling edge
t_{10}	4	ns min	DIN hold time after SCLK falling edge
t_{11}[1]	30	ns max	Delay from $\overline{CS}$ rising edge to DOUT high impedance
$t_{POWER-UP}$	6	ms max	Internal reference power-up time from full power-down

[1] Measured with a load capacitance on DOUT of 15 pF.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND, GND1	−0.3 V to +5 V
V_{DRIVE} to GND, GND1	−0.3 V to + 5 V
Analog Input Voltage to GND1	−0.3 V to +3 V
Digital Input Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to GND1	−0.3 V to +3 V
AGND to GND	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb-free Temperature, Soldering Reflow	260(0)°C
ESD	3.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP	52	6.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

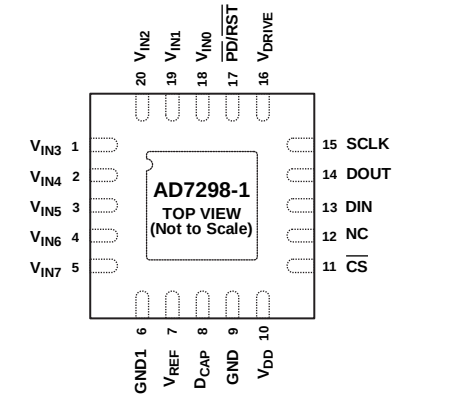

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 5, 18 to 20	V_{IN3}, V_{IN4} V_{IN5}, V_{IN6}, V_{IN7}, V_{IN0}, V_{IN1}, V_{IN2}	Analog Inputs. The AD7298-1 has eight single-ended analog inputs that are multiplexed into the on-chip track-and-hold. Each input channel can accept analog inputs from 0 V to 2.5 V. Any unused input channels should be connected to GND1 to avoid noise pickup.
6	GND1	Ground. Ground reference point for the internal reference circuitry on the AD7298-1. The external reference signals and all analog input signals should be referred to the GND1 voltage. The GND1 pin should be connected to the ground plane of a system. All ground pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The V_{REF} pin should be decoupled to this ground pin via a 10 µF decoupling capacitor.
7	V_{REF}	Internal Reference/External Reference Supply. The nominal internal reference voltage of 2.5 V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. Decoupling capacitors should be connected to this pin to decouple the reference buffer. For best performance, it is recommended to use a 10 µF decoupling capacitor on this pin to GND1. The internal reference can be disabled and an external reference supplied to this pin, if required. The input voltage range for the external reference is 2.0 V to 2.5 V.
8	D_{CAP}	Decoupling Capacitor Pins. Decoupling capacitors (1 µF recommended) are connected to this pin to decouple the internal LDO.
9	GND	Ground. Ground reference point for all analog and digital circuitry on the AD7298-1. The GND pin should be connected to the ground plane of the system. All ground pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both the D_{CAP} and V_{DD} pins should be decoupled to this GND pin.
10	V_{DD}	Supply Voltage, 2.8 V to 3.6 V. This supply should be decoupled to GND with 10 µF and 100 nF decoupling capacitors.
11	$\overline{CS}$	Chip Select, Active Low Logic Input. This pin is edge triggered on the falling edge of this input, the track-and-hold goes into hold mode, and a conversion is initiated. This input also frames the serial data transfer. When $\overline{CS}$ is low, the output bus is enabled and the conversion result becomes available on the DOUT output.
12	NC	No Connect.
13	D_{IN}	Data In, Logic Input. Data to be written to the AD7298-1 control register is provided on this input and is clocked into the register on the falling edge of SCLK.
14	DOUT	Serial Data Output. The conversion result from the AD7298-1 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7298-1 consists of four address bits indicating which channel the conversion result corresponds to, followed by the 10 bits of conversion data (MSB first).
15	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK for accessing the data from the AD7298-1.

Pin No.	Mnemonic	Description
16	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the voltage at which the interface operates. This pin should be decoupled to ground. The voltage range on this pin is 1.65 V to 3.6 V and may be less than the voltage at V_{DD} but should never exceed it by more than 0.3 V.
17	$\overline{PD}/\overline{RST}$	Power-Down Pin. This pin places the part into full power-down mode and enables power conservation when operation is not required. This pin can be used to reset the device by toggling the pin low for a minimum of 1 ns and a maximum of 100 ns. If the maximum time is exceeded, the part enters power-down mode. When placing the AD7298-1 into full power-down mode, the analog inputs must return to 0 V.
	EPAD	The exposed metal paddle on the bottom of the LFCSP package should be soldered to PCB ground for proper functionality and heat dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

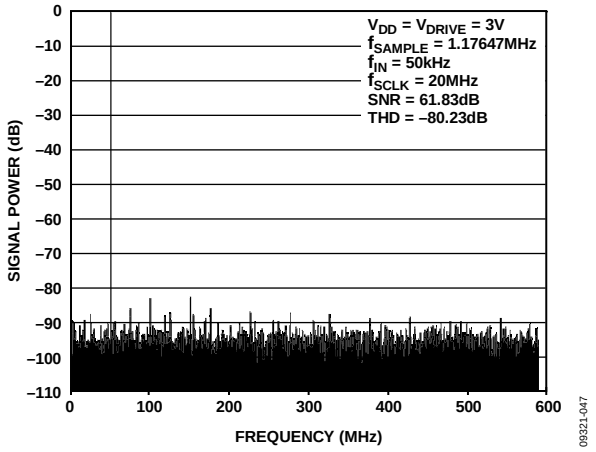

Figure 3. Typical FFT

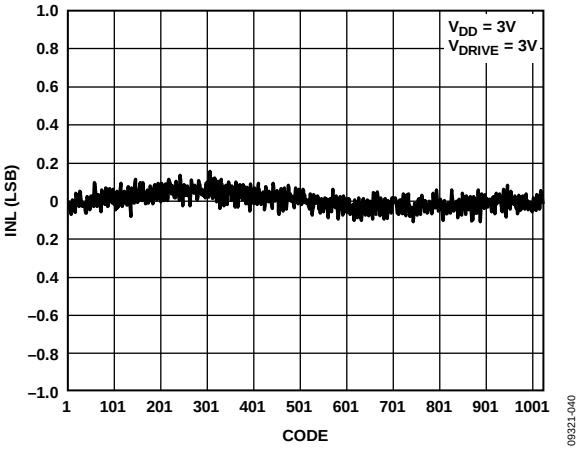

Figure 4. Typical ADC INL

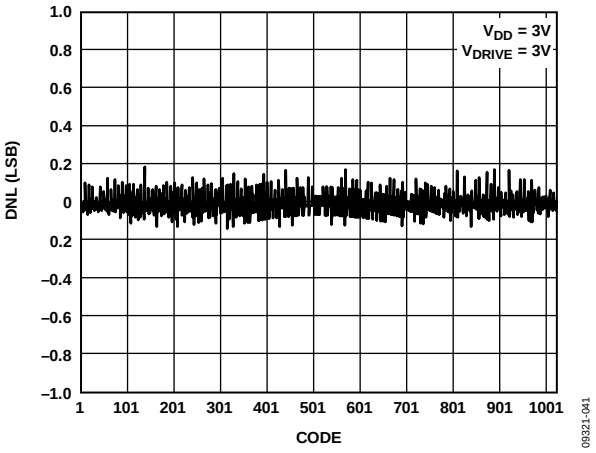

Figure 5. Typical ADC DNL

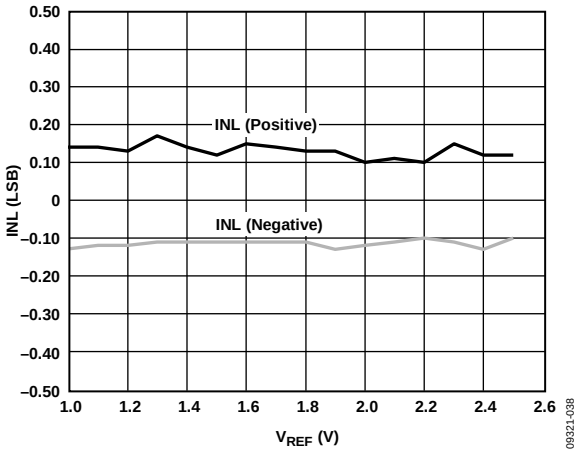

Figure 6. INL vs. V_{REF}

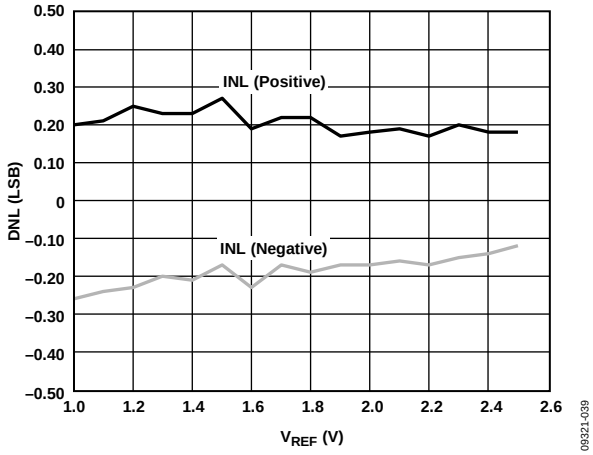

Figure 7. DNL vs. V_{REF}

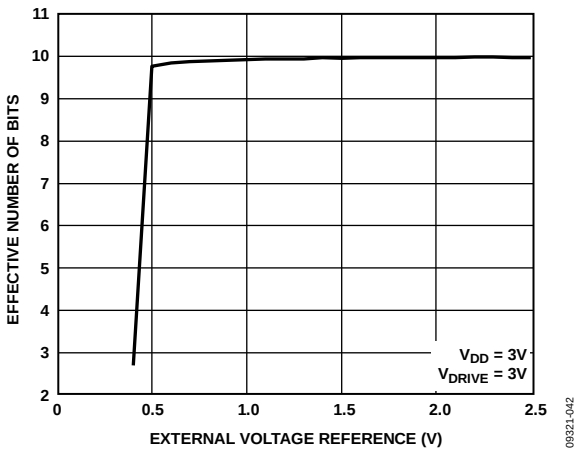

Figure 8. Effective Number of Bits vs. V_{REF}

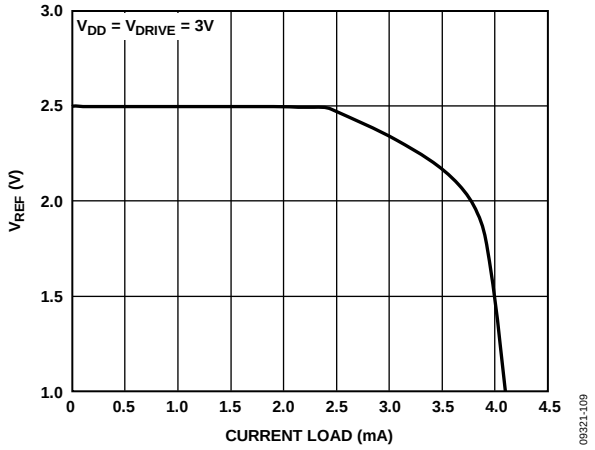

Figure 9. V_{REF} vs. Reference Output Current Drive

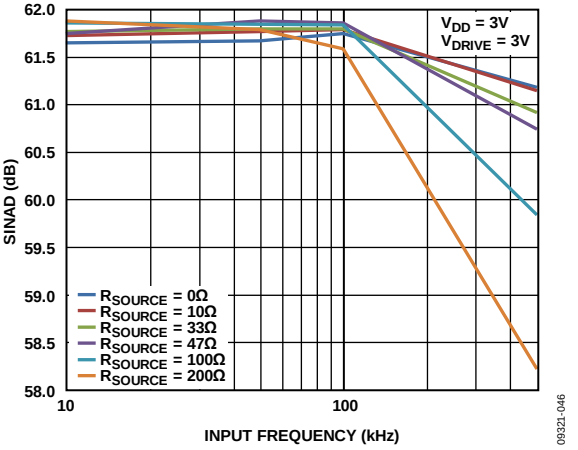

Figure 12. SINAD vs. Analog Input Frequency for Various Source Impedances

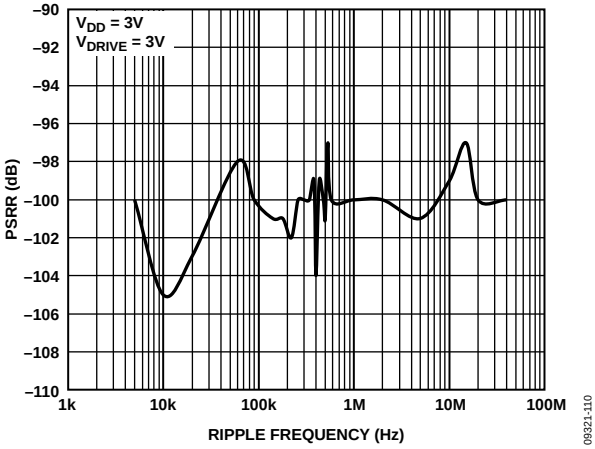

Figure 10. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

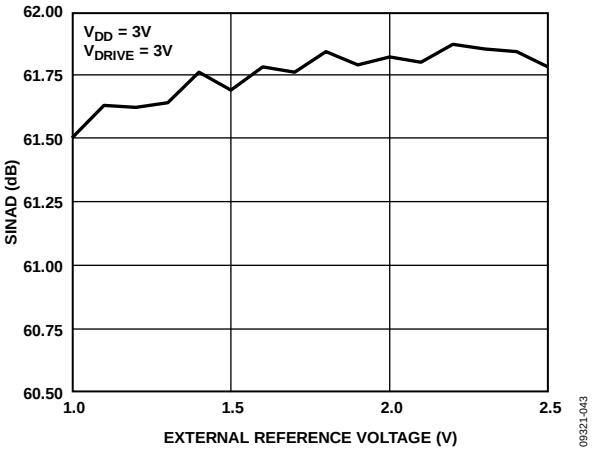

Figure 13. SINAD vs. Reference Voltage

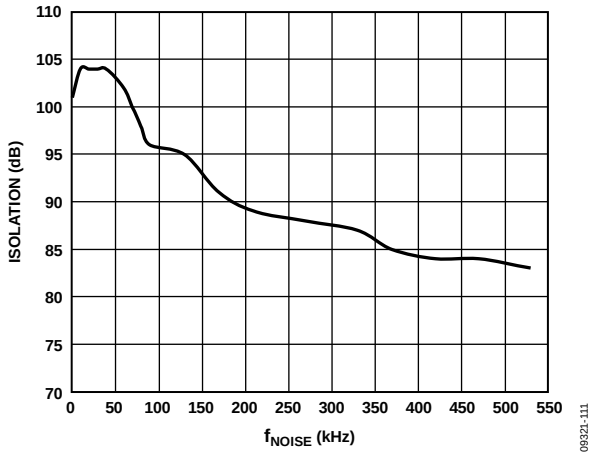

Figure 11. Channel-to-Channel Isolation, f_{IN} = 50 kHz

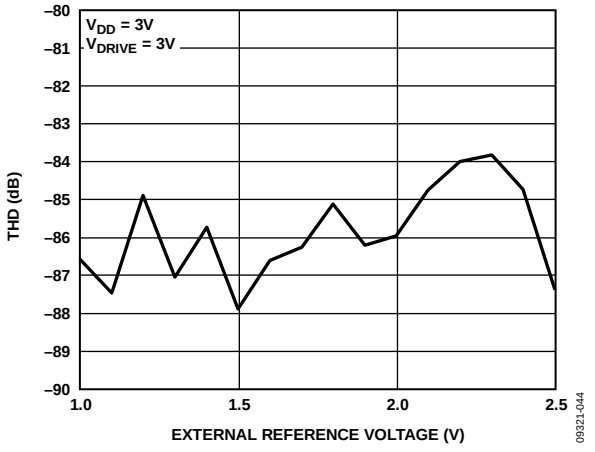

Figure 14. THD vs. Reference Voltage

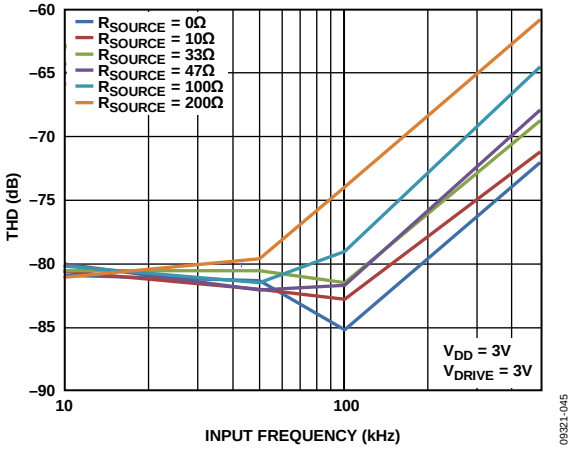

Figure 15. THD vs. Analog Input Frequency for Various Source Impedances

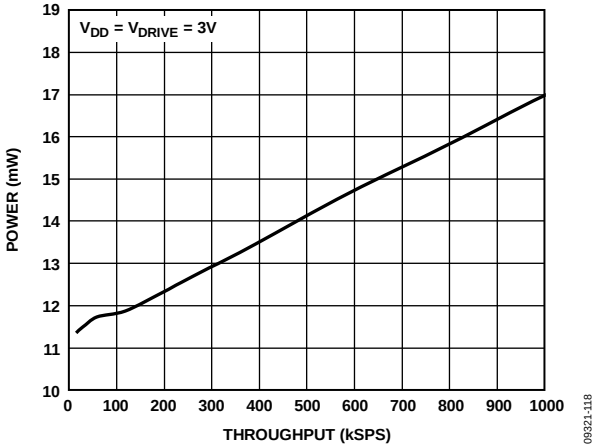

Figure 17. Power vs. Throughput in Normal Mode with V_{DD} = 3 V

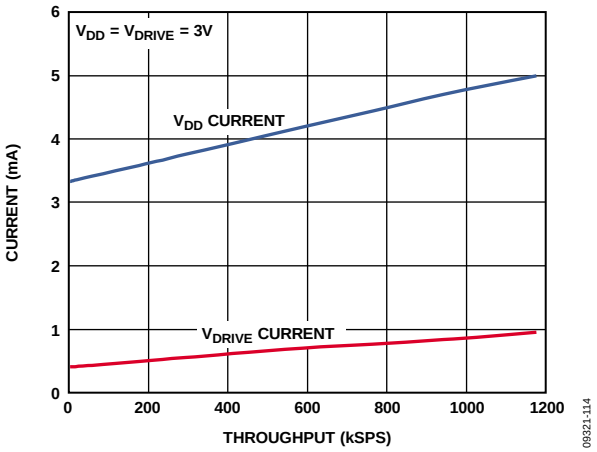

Figure 16. Average Supply Current vs. Throughput Rate

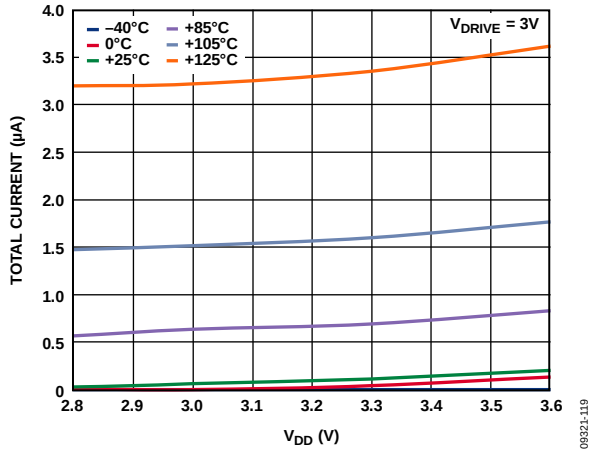

Figure 18. Full Shutdown Current vs. Supply Voltage for Various Temperatures

TERMINOLOGY

Signal-to-Noise-and-Distortion Ratio (SINAD)
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise-and-distortion ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(*Noise* + *Distortion*) = (6.02 N + 1.76) dB

Thus, the SINAD is 61.96 dB for an ideal 10-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7298-1, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, GND1 + 1 LSB.

Offset Error Matching
The difference in offset error between any two channels.

Gain Error
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Gain Error Matching
The difference in gain error between any two channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of the conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion.

Power Supply Rejection Ratio (PSRR)
PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency, f_S. The frequency of the input varies from 5 kHz to 25 MHz.

$$PSRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

CIRCUIT INFORMATION

The AD7298-1 is a high speed, 8-channel, 10-bit ADC. The part can be operated from a 2.8 V to 3.6 V supply and is capable of throughput rates of 1 MSPS per analog input channel.

The AD7298-1 provides the user with an on-chip, track-and-hold ADC and a serial interface housed in a 20-lead LFCSP. The AD7298-1 has eight, single-ended input channels with channel repeat functionality, which allows the user to select a channel sequence through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range for the AD7928-1 is 0 V to V_{REF}. The AD7298-1 operates with one cycle latency, which means that the conversion result is available in the serial transfer following the cycle in which the conversion is performed.

The AD7298-1 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the partial power-down bit, PPD, in the control register and using the $\overline{PD}/\overline{RST}$ pin.

CONVERTER OPERATION

The AD7298-1 is a 10-bit successive approximation ADC based around a capacitive DAC. Figure 19 and Figure 20 show simplified schematics of the ADC. The ADC is comprised of control logic, SAR, and a capacitive DAC that are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 19 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

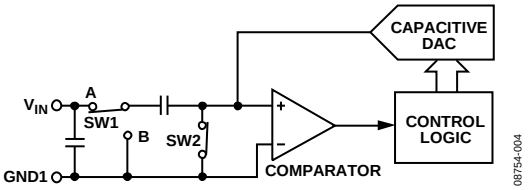

Figure 19. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 20), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 22 shows the transfer function of the ADC.

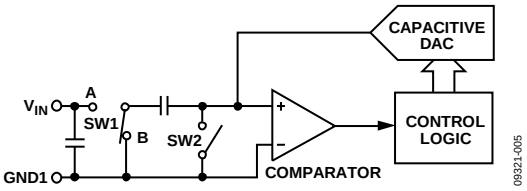

Figure 20. ADC Conversion Phase

ANALOG INPUT

Figure 21 shows an equivalent circuit of the analog input structure of the AD7298-1. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the internally generated LDO voltage of 2.5 V (D_{CAP}) by more than 300 mV. This causes the diodes to become forward-biased and to start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. Capacitor C1, in Figure 21, is typically about 8 pF and can primarily be attributed to pin capacitance. The R1 resistor is a lumped component made up of the on resistance of a switch (track-and-hold switch) and includes the on resistance of the input multiplexer. The total resistance is typically about 155 Ω. The capacitor, C2, is the ADC sampling capacitor and has a capacitance of 34 pF typically.

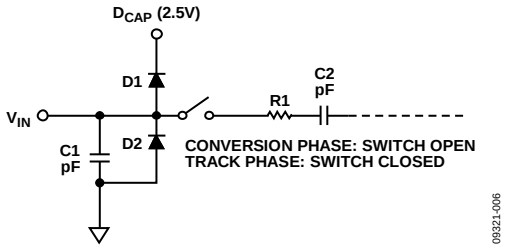

Figure 21. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application performance criteria.

ADC Transfer Function

The output coding of the AD7298-1 is straight binary for the analog input channel conversion results. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so forth). The LSB size is V_{REF}/1024 for the AD7298-1. The ideal transfer characteristic for the AD7298-1 for straight binary coding is shown in Figure 22.

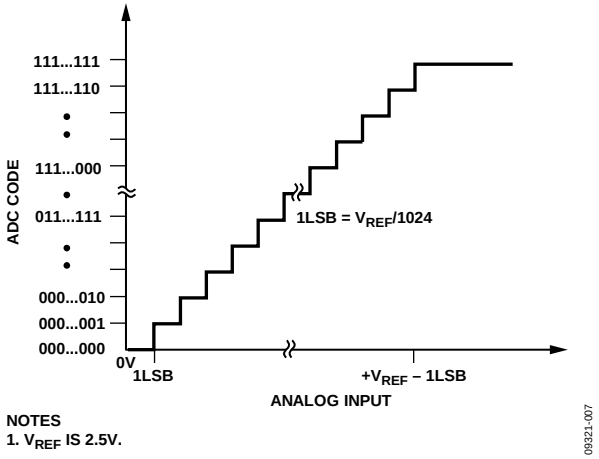

Figure 22. Straight Binary Transfer Characteristic

V_{DRIVE}

The AD7298-1 also provides the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 1.8 V and 3 V processors. For example, if the AD7298-1 were operated with a V_{DD} of 3.3 V, the V_{DRIVE} pin could be powered from a 1.8 V supply. This enables the AD7298-1 to operate with a larger dynamic range with a V_{DD} of 3.3 V while still being able to interface to 1.8 V processors. Take care to ensure V_{DRIVE} does not exceed V_{DD} by more than 0.3 V (see the Absolute Maximum Ratings section).

THE INTERNAL OR EXTERNAL REFERENCE

The AD7298-1 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The EXT_REF bit in the control register is used to determine whether the internal reference is used. If the EXT_REF bit is selected in the control register, an external reference can be supplied through the V_{REF} pin. At power-up, the internal reference is enabled. Suitable external reference sources for the AD7298-1 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When the AD7298-1 is operated in internal reference mode, the 2.5 V internal reference is available at the V_{REF} pin, which should be decoupled to GND1 using a 10 µF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system.

The internal reference is capable of sourcing up to 2 mA of current when the converter is static. The reference buffer requires 5.5 ms to power up and charge the 10 µF decoupling capacitor during the power-up time.

CONTROL REGISTER

The control register of the AD7298-1 is a 16-bit, write-only register. Data is loaded from the DIN pin of the AD7298-1 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7298-1 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 16 falling clock edges (after the falling edge of $\overline{CS}$) is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 6 and Table 7. At power-up, the default content of the control register is all zeros.

Table 6. Control Register Bit Functions

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
WRITE	REPEAT	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	0	DONTC	DONTC	EXT_REF	DONTC	PPD

Table 7. Control Register Bit Function Description

Bit	Mnemonic	Description
D15	WRITE	The value written to this bit determines whether the subsequent 15 bits are loaded to the control register. If this bit is a 1, the following 15 bits are written to the control register. If this bit is a 0, then the remaining 15 bits are not loaded to the control register, and it remains unchanged.
D14	REPEAT	This bit enables the repeated conversion of the selected sequence of channels.
D13 to D6	CH0 to CH7	These eight channel selection bits are loaded at the end of the current conversion and select which analog input channel is to be converted in the next serial transfer, or they can select the sequence of channels for conversion in the subsequent serial transfers. Each CHx bit corresponds to an analog input channel. A channel or sequence of channels is selected for conversion by writing a 1 to the appropriate CHx bit/bits. Channel address bits corresponding to the conversion result are output on DOUT prior to the 10 bits of data. The next channel to be converted is selected by the mux on the 14th SCLK falling edge.
D5	0	Zero should be written to this bit.
D4, D3, D1	DONTC	Don't care.
D2	EXT_REF	Writing Logic 1 to this bit, enables the use of an external reference. The input voltage range for the external reference is 1 V to 2.5 V. The external reference should not exceed 2.5 V or the device performance is affected.
D0	PPD	This partial power-down mode is selected by writing a 1 to this bit in the control register. In this mode, some of the internal analog circuitry is powered down. The AD7298-1 retains the information in the control register while in partial power-down mode. The part remains in this mode until a 0 is written to this bit.

Table 8. Channel Address Bits

ADD3	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	V_{IN0}
0	0	0	1	V_{IN1}
0	0	1	0	V_{IN2}
0	0	1	1	V_{IN3}
0	1	0	0	V_{IN4}
0	1	0	1	V_{IN5}
0	1	1	0	V_{IN6}
0	1	1	1	V_{IN7}

MODES OF OPERATION

The AD7298-1 offers different modes of operation that are designed to provide additional flexibility for the user. These options can be chosen by programming the content of the control register to select the desired mode.

TRADITIONAL MULTICHANNEL MODE OF OPERATION

The AD7298-1 can operate as a traditional multichannel ADC, where each serial transfer selects the next channel for conversion. One must write to the control register to configure and select the desired input channel prior to initiating any conversions. In the traditional mode of operation, the $\overline{CS}$ signal is used to frame the first write to the converter on the DIN pin. In this mode of operation, the REPEAT bit in the control register is set to a low logic level (0), therefore the REPEAT function is not in use. The data, which appears on the DOUT pin during the initial write to the control register, is invalid. The first $\overline{CS}$ falling edge initiates a write to the control register to configure the device; a conversion is then initiated for the selected analog input channel (V_{IN0}) on the subsequent (second) $\overline{CS}$ falling edge; and the third $\overline{CS}$ falling edge will have the result (V_{IN2}) available for reading. The AD7298-1 operates with one cycle latency, therefore the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion was initiated.

As the device operates with one cycle latency, the control register configuration sets up the configuration for the next conversion, which is initiated on the next $\overline{CS}$ falling edge, but the first bit of the corresponding result is not clocked out until the subsequent falling $\overline{CS}$ edge, as shown in Figure 23.

If more than one channel is selected in the control register, the AD7298-1 converts all selected channels sequentially in ascending order on successive $\overline{CS}$ falling edges. Once all the selected channels in the control register are converted, the AD7298-1 ceases converting until the user rewrites to the control register to select the next channel for conversion. This operation is shown in Figure 24. DOUT returns all 1s if the sequence of conversions is completed or if no channel is selected.

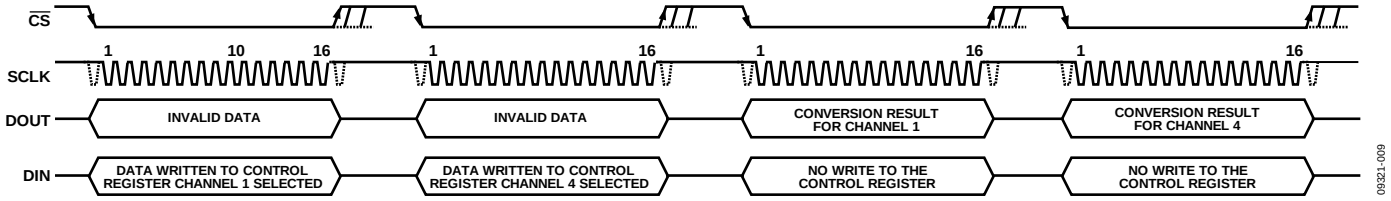

Figure 23. Configuring a Conversion and Read with the AD7298-1, One Channel Selected for Conversion

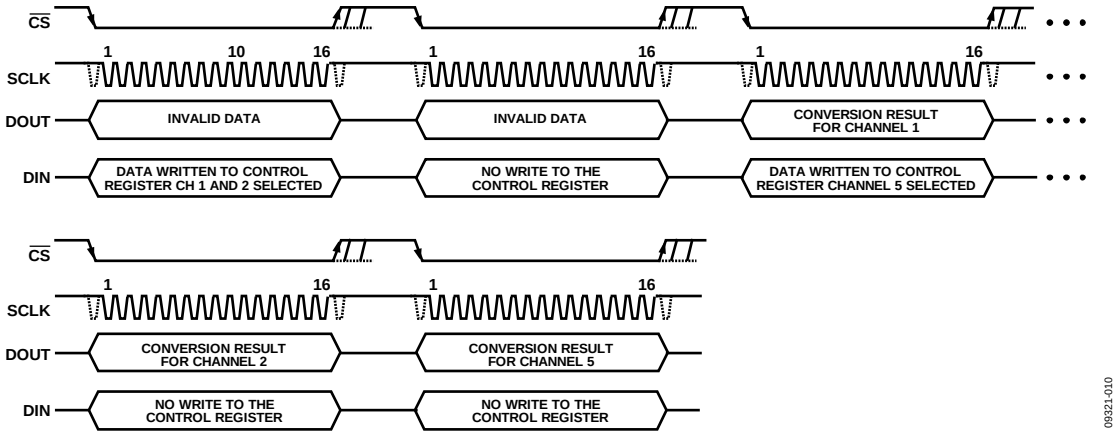

Figure 24. Configuring a Conversion and Read with the AD7298-1, Numerous Channels Selected for Conversion

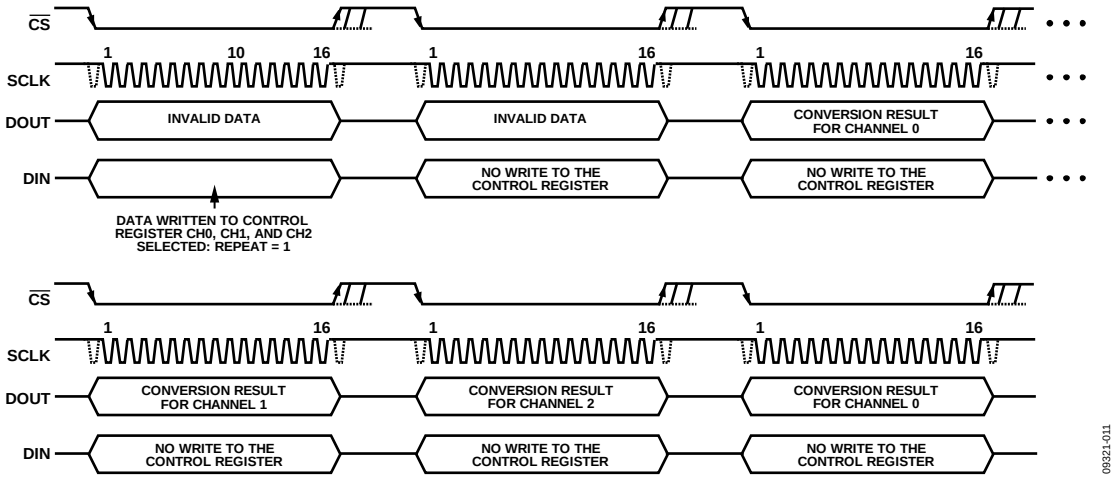

Figure 25. Configuring a Conversion and Read in Repeat Mode

REPEAT OPERATION

The REPEAT bit in the control register allows the user to select a sequence of channels on which the AD7298-1 continuously converts. When the REPEAT bit is set in the control register, the AD7298-1 continuously cycles through the selected channels in ascending order, beginning with the lowest channel and converting all channels selected in the control register. On completion of the sequence, the AD7298-1 returns to the first selected channel in the control register and recommences the sequence.

The conversion sequence of the selected channels in the repeat mode of operation continues until the control register of the AD7298-1 is reprogrammed. It is not necessary to write to the control register once a repeat operation is initiated unless a change in the AD7298-1 configuration is required. The WRITE bit must be set to zero, or the DIN line tied low to ensure that the control register is not accidentally overwritten or the automatic conversion sequence interrupted.

A write to the control register during the repeat mode of operation resets the cycle even if the selected channels are unchanged. Thus, the next conversion by the AD7298-1 after a write operation will be the first selected channel in the sequence.

To select a sequence of channels, the associated channel bit must be set to a logic high state (1) for each analog input whose conversion is required. For example, if the REPEAT bit = 1, then CH0, CH1, and CH2 = 1. The V_{IN0} analog input is converted on the first $\overline{CS}$ falling edge following the write to the control register, the V_{IN1} channel is converted on the subsequent $\overline{CS}$ falling edge, and the V_{IN0} conversion result is available for reading. The third $\overline{CS}$ falling edge following the write operation initiates a conversion on V_{IN2} and has the V_{IN1} result available for reading. The AD7298-1 operates with one cycle latency, therefore the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion is initiated.

This mode of operation simplifies the operation of the device by allowing consecutive channels to be converted without having to reprogram the control register or write to the part on each serial transfer. Figure 25 illustrates how to set up the AD7298-1 to continuously convert on a particular sequence of channels. To exit the repeat mode of operation and revert to the traditional mode of operation of a multichannel ADC, ensure that the REPEAT bit = 0 on the next serial write.

POWER-DOWN MODES

The AD7298-1 has a number of power conservation modes of operation that are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements. The power-down modes of operation of the AD7298-1 are controlled by the power-down (PPD) bit in the control register and the $\overline{PD}/\overline{RST}$ pin on the device. When power supplies are first applied to the AD7298-1, care should be taken to ensure that the part is placed in the required mode of operation.

Normal Mode

Normal mode is intended for the fastest throughput rate performance because the user does not have to be concerned about any power-up times since the AD7298-1 remains fully powered on at all times. Figure 26 shows the general diagram of the normal mode operation of the AD7298-1. The conversion is initiated on the falling edge of $\overline{CS}$ and the track-and-hold enters hold mode. On the 14th SCLK falling edge, the track-and-hold returns to track mode and starts acquiring the analog input, as described in the Serial Interface section. The data presented to the AD7298-1 on the DIN line during the first 16 clock cycles of the data transfer are loaded into the control register (provided the WRITE bit is 1). The part remains fully powered up in normal mode at the end of the conversion as long as the PPD bit is set to 0 in the write transfer during that conversion.

To ensure continued operation in normal mode, the PPD bit should be loaded with 0 on every data write operation. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. For specified performance, the throughput rate should not exceed 1 MSPS. When a conversion is complete and the $\overline{CS}$ has returned high, a minimum of the quiet time, t_{QUIET}, must elapse before bringing $\overline{CS}$ low again to initiate another conversion and access the previous conversion result.

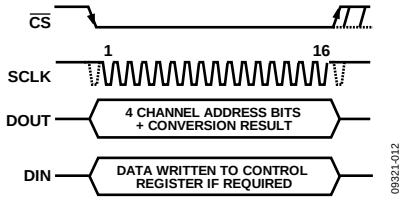

Figure 26. Normal Mode Operation

Partial Power-Down Mode

In this mode, part of the internal circuitry on the AD7298-1 is powered down. The AD7298-1 enters partial power-down on the $\overline{CS}$ rising edge once the current serial write operation containing 16 SCLK clock cycles is completed. To enter partial power-down, the PPD bit in the control register should be set to 1 on the last required read transfer from the AD7298-1. Once in partial power-down mode, the AD7298-1 transmits all 1s on the DOUT pin if $\overline{CS}$ is toggled low.

The AD7298-1 remains in partial power-down until the power-down bit, PPD, in the control register is changed to Logic Level 0. The AD7298-1 begins powering up on the rising edge of $\overline{CS}$ following the write to the control register disabling the power-down bit. Once t_{QUIET} has elapsed, a full 16 SCLK writes to the control register must be completed to update its content with the desired channel configuration for the subsequent conversion. A valid conversion is then initiated on the next $\overline{CS}$ falling edge.

Because the AD7298-1 has one cycle latency, the first conversion result after exiting partial power-down mode is available in the fourth serial transfer, as shown in Figure 27. The first cycle updates the PPD bit, the second cycle updates the configuration and Channel ID bits, the third completes the conversion, and the fourth accesses the DOUT valid result. The use of this mode enables a reduction in the overall power consumption of the device.

Full Power-Down Mode

In this mode, all internal circuitry on the AD7298-1 is powered down, and no information is retained in the control register or any other internal register.

The AD7298-1 is placed into full power-down mode by bringing the logic level on the $\overline{PD}/\overline{RST}$ pin low for greater than 100 ns. When placing the AD7298-1 in full power-down mode, the ADC inputs must return to 0 V. The $\overline{PD}/\overline{RST}$ pin is asynchronous to the clock; therefore, it can be triggered at any time. The part can be powered up for normal operation by bringing the $\overline{PD}/\overline{RST}$ pin logic level back to a high logic state.

The full power-down feature can be used to reduce the average power consumed by the AD7298-1 when operating at lower throughput rates. The user should ensure that $t_{POWER-UP}$ has elapsed prior to programming the control register and initiating a valid conversion.

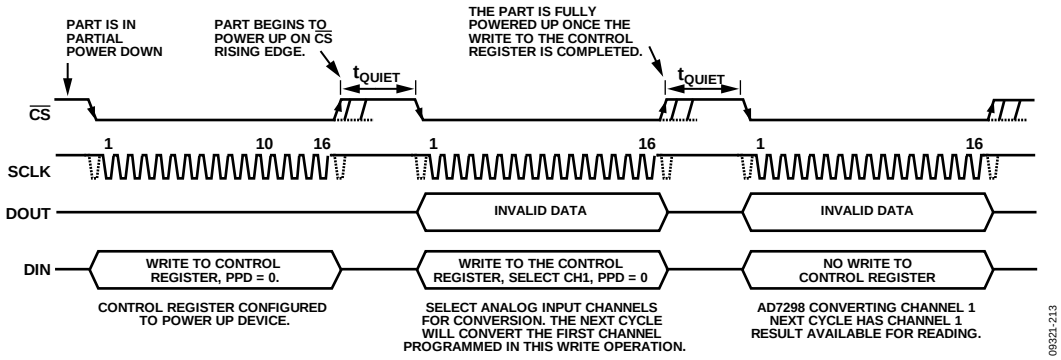

Figure 27. Partial Power-Down Mode of Operation

POWERING UP THE AD7298-1

The AD7298-1 contains a power-on reset circuit that sets the control register to its default setting of all zeros; therefore, the internal reference is enabled and the device is configured for the normal mode of operation. At power-up, the internal reference is by default enabled, which takes up to 6 ms (maximum) to power up.

If an external reference is being used, the user does not need to wait for the internal reference to power up fully. The AD7298-1 digital interface is fully functional after 500 μs from the initial power-up. Therefore, the user can write to the control register after 500 μs to switch to external reference mode. The AD7298-1 is then immediately ready to convert once the external reference is available on the V_{REF} pin.

When supplies are first applied to the AD7298-1, the user must wait the specified 500 μs before programming the control register to select the desired channels for conversion.

RESET

The AD7298-1 includes a reset feature that can be used to reset the device and the contents of all internal registers, including the control register, to their default state.

To activate the reset operation, the $\overline{PD}/\overline{RST}$ pin should be brought low for no longer than 100 ns. It is asynchronous with the clock; therefore, it can be triggered at any time. If the $\overline{PD}/\overline{RST}$ pin is held low for greater than 100 ns, the part enters full power-down mode. It is imperative that the $\overline{PD}/\overline{RST}$ pin be held at a stable logic level at all times to ensure normal operation.

SERIAL INTERFACE

Figure 28 shows the detailed timing diagram for the serial interface to the AD7298-1. The serial clock provides the conversion clock and controls the transfer of information to and from the AD7298-1 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. The track-and-hold goes back into track mode on the 14th SCLK falling edge as shown in Figure 28 at Point B. On the 16th SCLK falling edge or on the rising edge of $\overline{CS}$, the DOUT line goes back into three-state.

If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated, the DOUT line goes back into three-state, and the control register is not updated; otherwise, DOUT returns to three-state on the 16th SCLK falling edge. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7298-1.

For the AD7298-1, four channel address bits (ADD3 to ADD0) that identify which channel the conversion result corresponds to, precede the 10 bits of data (see Table 8).

When $\overline{CS}$ goes low, it provides the first address bit to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second address bit. Thus, the first falling clock edge on the serial clock has the first address bit provided for reading and also clocks out the second address bit. The three remaining address bits and 12 data bits are clocked out by subsequent SCLK falling edges. The final bit in the data transfer is valid for reading on the 16th falling edge having been clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge depending on the SCLK frequency. The first rising edge of SCLK after the $\overline{CS}$ falling edge would have the first address bit provided, and the 15th rising SCLK edge would have last data bit provided.

Writing information to the control register takes place on the first 16 falling edges of SCLK in a data transfer, assuming the MSB (that is, the WRITE bit) has been set to 1. The 16-bit word read from the AD7298-1 always contains four channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result.

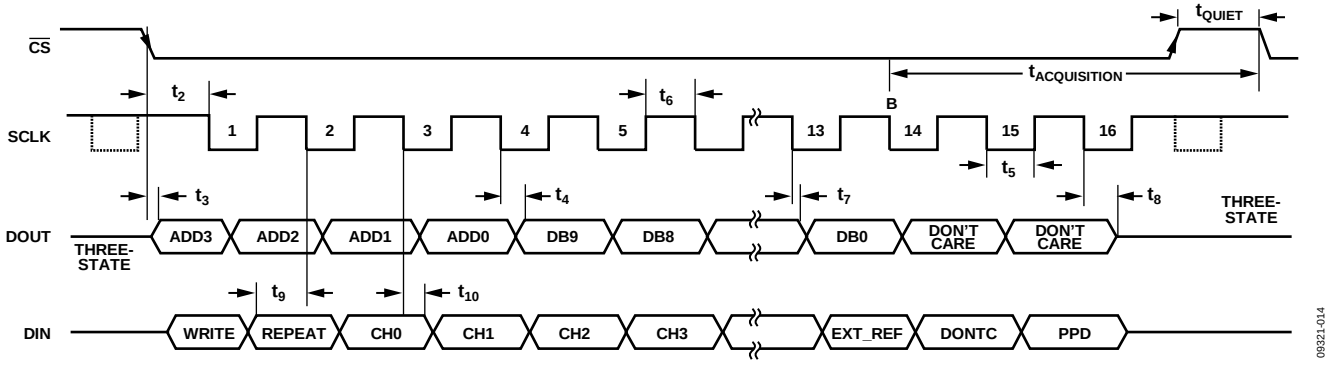

Figure 28. Serial Interface Timing Diagram

LAYOUT AND CONFIGURATION

For optimum performance, carefully consider the power supply and ground return layout on any PCB where the AD7298-1 is used. The PCB containing the AD7298-1 should have separate analog and digital sections, each having its own area of the board. The AD7298-1 should be located in the analog section on any PCB.

Decouple the power supply to the AD7298-1 to ground with 10 μF and 0.1 μF capacitors. Place the capacitors as physically close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. It is important that the 0.1 μF capacitor has low effective series resistance (ESR) and low effective series inductance (ESL); common ceramic types of capacitors are suitable. The 0.1 μF capacitors provide a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. The 10 μF capacitors are the tantalum bead type.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other components with fast switching digital signals from other parts of the board by a digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board.

The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side; however, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

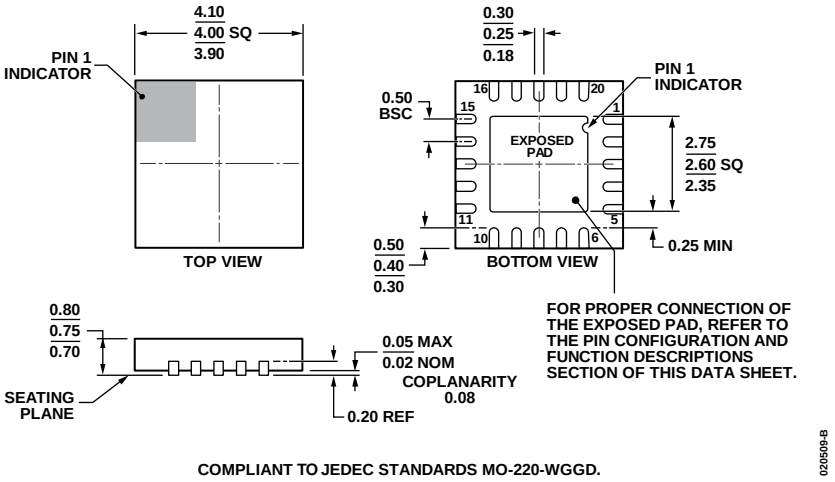

Figure 29. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very, Very Thin Quad
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7298-1BCPZ	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-8
AD7298-1BCPZ-RL	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-8

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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