CY15B004Q

# 4-Kbit (512 × 8) Serial (SPI) Automotive F-RAM

## Features

- 4-Kbit ferroelectric random access memory (F-RAM) logically organized as 512 × 8
  - High-endurance 10 trillion ($10^{13}$) read/writes
  - 121-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Very fast serial peripheral interface (SPI)
  - Up to 16 MHz frequency
  - Direct hardware replacement for serial flash and EEPROM
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Sophisticated write protection scheme
  - Hardware protection using the Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Low power consumption
  - 200 µA active current at 1 MHz
  - 6 µA (typ) standby current at +85 °C
- Low-voltage operation: $V_{DD}$ = 3.0 V to 3.6 V
- Automotive-E temperature: –40 °C to +125 °C
- 8-pin small outline integrated circuit (SOIC) package
- AEC Q100 Grade 1 compliant
- Restriction of hazardous substances (RoHS) compliant

## Functional Description

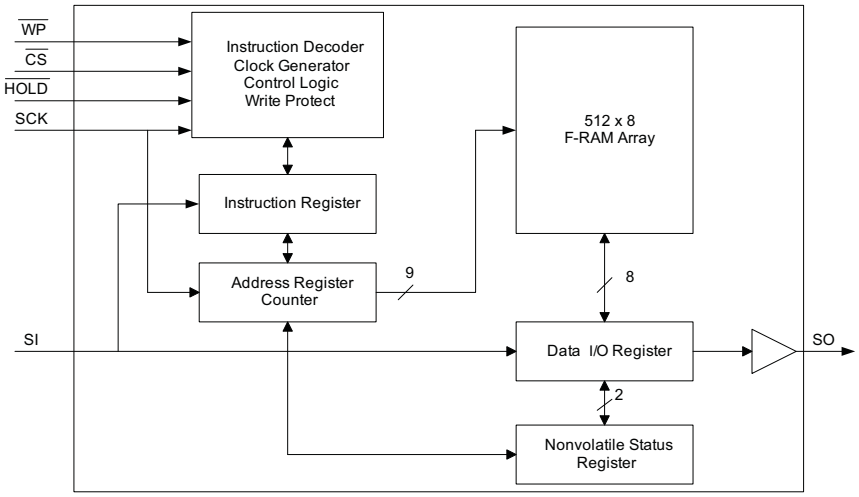
The CY15B004Q is a 4-Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 121 years while eliminating the complexities, overhead, and system level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

Unlike serial flash and EEPROM, the CY15B004Q performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The CY15B004Q is capable of supporting $10^{13}$ read/write cycles, or 10 million times more write cycles than EEPROM.

These capabilities make the CY15B004Q ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss.

The CY15B004Q provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The CY15B004Q uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The device specifications are guaranteed over an automotive-e temperature range of –40 °C to +125 °C.

## Logic Block Diagram



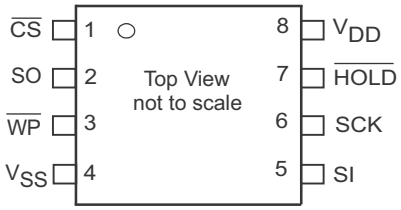

Errata: The Write Enable Latch (WEL) bit in the Status Register of CY15B004Q part doesn't clear after executing the memory write (WRITE) operation at memory location(s) from 0x100 to 0x1FF. For more information, see Errata on page 19. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

## Contents

**Pinout** ..... **3**
**Pin Definitions** ..... **3**
**Functional Overview** ..... **4**
**Memory Architecture** ..... **4**
**Serial Peripheral Interface – SPI Bus** ..... **4**
SPI Overview ..... 4
SPI Modes ..... 5
Power Up to First Access ..... 6
Command Structure ..... 6
WREN - Set Write Enable Latch ..... 6
WRDI - Reset Write Enable Latch ..... 6
**Status Register and Write Protection** ..... **6**
RDSR - Read Status Register ..... 7
WRSR - Write Status Register ..... 7
**Memory Operation** ..... **8**
Write Operation ..... 8
Read Operation ..... 8
HOLD Pin Operation ..... 9
Endurance ..... 10
**Maximum Ratings** ..... **11**
**Operating Range** ..... **11**
**DC Electrical Characteristics** ..... **11**
**Data Retention and Endurance** ..... **12**
**Example of an F-RAM Life Time in an AEC-Q100 Automotive Application** ..... **12**
**Capacitance** ..... **12**
**Thermal Resistance** ..... **12**
**AC Test Conditions** ..... **12**
**AC Switching Characteristics** ..... **13**
**Power Cycle Timing** ..... **15**
**Ordering Information** ..... **16**
Ordering Code Definitions ..... 16
**Package Diagrams** ..... **17**
**Acronyms** ..... **18**
**Document Conventions** ..... **18**
Units of Measure ..... 18
**Errata** ..... **19**
Part Numbers Affected ..... 19
Qualification Status ..... 19
Errata Summary ..... 19
**Document History Page** ..... **21**
**Sales, Solutions, and Legal Information** ..... **22**
Worldwide Sales and Design Support ..... 22
Products ..... 22
PSoC® Solutions ..... 22
Cypress Developer Community ..... 22
Technical Support ..... 22

## Pinout

**Figure 1. 8-pin SOIC pinout**




## Pin Definitions

| Pin Name | I/O Type | Description |
|---|---|---|
| $\overline{CS}$ | Input | **Chip Select**. This active LOW input activates the device. When HIGH, the device enters low-power standby mode, ignores other inputs, and tristates the output. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{CS}$ must occur before every opcode. |
| SCK | Input | **Serial Clock**. All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Because the device is synchronous, the clock frequency may be any value between 0 and 16 MHz and may be interrupted at any time. |
| SI[1] | Input | **Serial Input**. All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet $I_{DD}$ specifications. |
| SO[1] | Output | **Serial Output**. This is the data output pin. It is driven during a read and remains tristated at all other times including when $\overline{HOLD}$ is LOW. Data transitions are driven on the falling edge of the serial clock. |
| $\overline{WP}$ | Input | **Write Protect**. This active LOW pin prevents all write operation, including Status Register. If HIGH, write access is determined by the other write protection features, as controlled through the Status Register. A complete explanation of write protection is provided in Status Register and Write Protection on page 7. This pin must be tied to $V_{DD}$ if not used. |
| $\overline{HOLD}$ | Input | **$\overline{HOLD}$ Pin**. The $\overline{HOLD}$ pin is used when the host CPU must interrupt a memory operation for another task. When $\overline{HOLD}$ is LOW, the current operation is suspended. The device ignores any transition on SCK or $\overline{CS}$. All transitions on $\overline{HOLD}$ must occur while SCK is LOW. This pin must be tied to $V_{DD}$ if not used. |
| $V_{SS}$ | Power supply | Ground for the device. Must be connected to the ground of the system. |
| $V_{DD}$ | Power supply | Power supply input to the device. |

**Note**
1. SI may be connected to SO for a single pin data interface.

## Functional Overview

The CY15B004Q is a serial F-RAM memory. The memory array is logically organized as 512 × 8 bits and is accessed using an industry standard serial peripheral interface (SPI) bus. The functional operation of the F-RAM is similar to serial flash and serial EEPROMs. The major difference between the CY15B004Q and a serial flash or EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

## Memory Architecture

When accessing the CY15B004Q, the user addresses 512 locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an opcode including the upper address bit, and a word address. The word address consist of the lower 8-address bits. The complete address of 9 bits specifies each byte address uniquely.

Most functions of the CY15B004Q are either controlled by the SPI interface or handled by on-board circuitry. The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike a serial flash or EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in the interface section.

**Note** The CY15B004Q contains no power management circuits other than a simple internal power-on reset circuit. It is the user's responsibility to ensure that $V_{DD}$ is within datasheet tolerances to prevent incorrect operation. It is recommended that the part is not powered down with chip enable active.

## Serial Peripheral Interface – SPI Bus

The CY15B004Q is a SPI slave device and operates at speeds up to 16 MHz. This high-speed serial bus provides high-performance serial communication to a SPI master. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The CY15B004Q operates in SPI Mode 0 and 3.

### SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms in the SPI protocol are as follows:

*SPI Master*

The SPI master device controls the operations on a SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All of the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

*SPI Slave*

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The CY15B004Q operates as an SPI slave and may share the SPI bus with other SPI slave devices.

*Chip Select ($\overline{CS}$)*

To select any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

**Note** A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

*Serial Clock (SCK)*

The Serial Clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

The CY15B004Q enables SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of a SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

*Data Transmission (SI/SO)*

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The

master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The CY15B004Q has two separate pins for SI and SO, which can be connected with the master as shown in Figure 2.

For a microcontroller that has no dedicated SPI bus, a general-purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (HIGH) the $\overline{HOLD}$ and $\overline{WP}$ pins. Figure 3 shows such a configuration, which uses only three pins.

**Figure 2. System Configuration with SPI port**

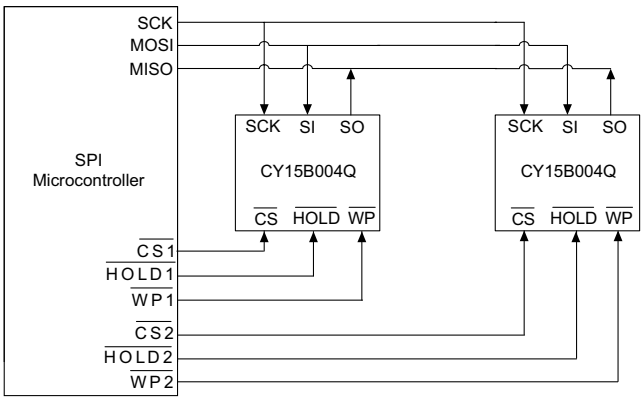
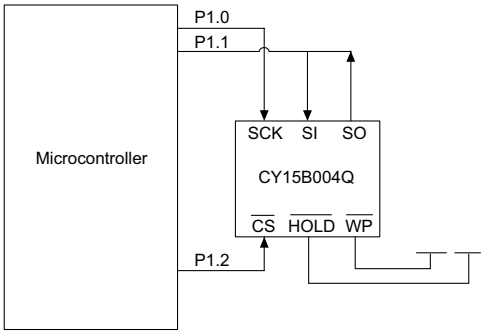



**Figure 3. System Configuration without SPI port**




*Most Significant Bit (MSB)*

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 4-Kbit serial F-RAM requires an opcode including the upper address bit, and a word address for any read or write operation.

The word address consist of the lower 8-address bits. The complete address of 9 bits specifies each byte address uniquely.

*Serial Opcode*

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY15B004Q uses the standard opcodes for memory accesses.

*Invalid Opcode*

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin until the next falling edge of $\overline{CS}$, and the SO pin remains tristated.

*Status Register*

CY15B004Q has an 8-bit Status Register. The bits in the Status Register are used to configure the device. These bits are described in Table 3 on page 7.

## SPI Modes

CY15B004Q may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK.

The two SPI modes are shown in Figure 4 and Figure 5. The status of the clock when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3.

**Figure 4. SPI Mode 0**

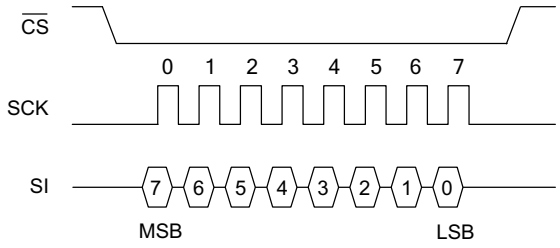
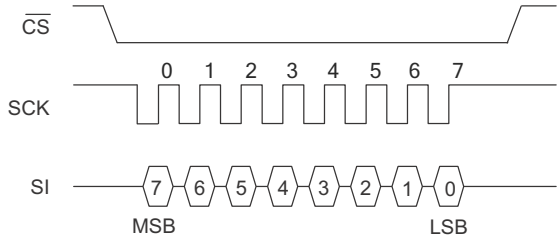



**Figure 5. SPI Mode 3**




## Power Up to First Access

The CY15B004Q is not accessible for a $t_{PU}$ time after power up. Users must comply with the timing parameter $t_{PU}$, which is the minimum time from $V_{DD}$ (min) to the first $\overline{CS}$ LOW.

## Command Structure

There are six commands, called opcodes, that can be issued by the bus master to the CY15B004Q. They are listed in Table 1. These opcodes control the functions performed by the memory.

**Table 1. Opcode commands**

| Name | Description | Opcode |
|---|---|---|
| WREN | Set write enable latch | 0000 0110b |
| WRDI | Write disable | 0000 0100b |
| RDSR | Read Status Register | 0000 0101b |
| WRSR | Write Status Register | 0000 0001b |
| READ | Read memory data | 0000 A011b |
| WRITE | Write memory data | 0000 A010b |

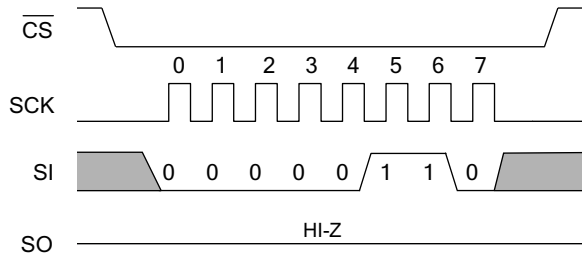
## WREN - Set Write Enable Latch

The CY15B004Q will power up with writes disabled. The WREN command must be issued before any write operation. Sending the WREN opcode allows the user to issue subsequent opcodes for write operations. These include writing the Status Register (WRSR) and writing the memory (WRITE).

Sending the WREN opcode causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL = '1' indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit – only the WREN opcode can set this bit. The WEL bit will be automatically cleared on the rising edge of $\overline{CS}$ following a WRDI, a WRSR, or a WRITE operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 6 illustrates the WREN command bus configuration.

**Note:** The Write Enable Latch (WEL) bit in the Status Register of CY15B004Q part doesn't clear after executing the memory write (WRITE) operation at memory location(s) from 0x100 to 0x1FF. For more information, see Errata on page 19.

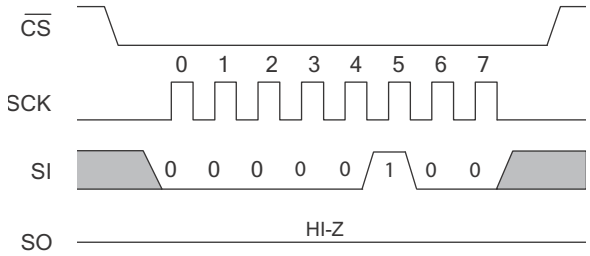
**Figure 6. WREN Bus Configuration**




## WRDI - Reset Write Enable Latch

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL is equal to '0'. Figure 7 illustrates the WRDI command bus configuration.

**Figure 7. WRDI Bus Configuration**



## Status Register and Write Protection

The write protection features of the CY15B004Q are multi-tiered and are enabled through the status register. First, a WREN opcode must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the $\overline{WP}$ pin and the Status Register. When $\overline{WP}$ is LOW, the entire part is write-protected. When $\overline{WP}$ is HIGH, the memory protection is subject to the Status Register. Writes to the Status Register are performed using the WREN and WRSR commands and subject to the $\overline{WP}$ pin. The Status Register is organized as follows. (The default value shipped from the factory for bits in the Status Register is ‘0’).

**Table 2. Status Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| X (0) | X (0) | X (0) | X (0) | BP1 (0) | BP0 (0) | WEL (0) | X (0) |

**Table 3. Status Register Bit Definition**

| Bit | Definition | Description |
|---|---|---|
| Bit 0 | Don’t care | This bit is non-writable and always returns ‘0’ upon read. |
| Bit 1 (WEL) | Write Enable Latch | WEL indicates if the device is write enabled. This bit defaults to ‘0’ (disabled) on power-up.<br>WEL = ‘1’ --> Write enabled<br>WEL = ‘0’ --> Write disabled |
| Bit 2 (BP0) | Block Protect bit ‘0’ | Used for block protection. For details, see Table 4. |
| Bit 3 (BP1) | Block Protect bit ‘1’ | Used for block protection. For details, see Table 4. |
| Bit 4-7 | Don’t care | These bits are non-writable and always return ‘0’ upon read. |

Bits 0 and 4–7 are fixed at ‘0’; none of these bits can be modified. Note that bit 0 (“Ready or Write in progress” bit in serial flash and EEPROM) is unnecessary, as the F-RAM writes in real-time and is never busy, so it reads out as a ‘0’. The BP1 and BP0 control the software write-protection features and are nonvolatile bits. The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in Table 4.

**Table 4. Block Memory Write Protection**

| BP1 | BP0 | Protected Address Range |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | 180h to 1FFh (upper 1/4) |
| 1 | 0 | 100h to 1FFh (upper 1/2) |
| 1 | 1 | 000h to 1FFh (all) |

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The BP1 and BP0 bits allow software to selectively write protect the array. These settings are only used when the $\overline{WP}$ pin is inactive and the WREN command has been issued.

Table 5 summarizes the write protection conditions.

**Table 5. Write Protection**

| WEL | $\overline{WP}$ | Protected Blocks | Unprotected Blocks | Status Register |
|---|---|---|---|---|
| 0 | X | Protected | Protected | Protected |
| 1 | 0 | Protected | Protected | Protected |
| 1 | 1 | Protected | Unprotected | Unprotected |

### RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading the status register provides information about the current state of the write-protection features. Following the RDSR opcode, the CY15B004Q will return one byte with the contents of the Status Register.

### WRSR - Write Status Register

The WRSR command allows the SPI bus master to write into the Status Register and change the write protect configuration by setting the BP0 and BP1 bits as required. Before issuing a WRSR command, the $\overline{WP}$ pin must be HIGH or inactive. Note that on the CY15B004Q, $\overline{WP}$ prevents writing to the Status Register and the memory array. Before sending the WRSR command, the user must send a WREN command to enable writes. Executing a WRSR command is a write operation and therefore, clears the Write Enable Latch.

**Figure 8. RDSR Bus Configuration**

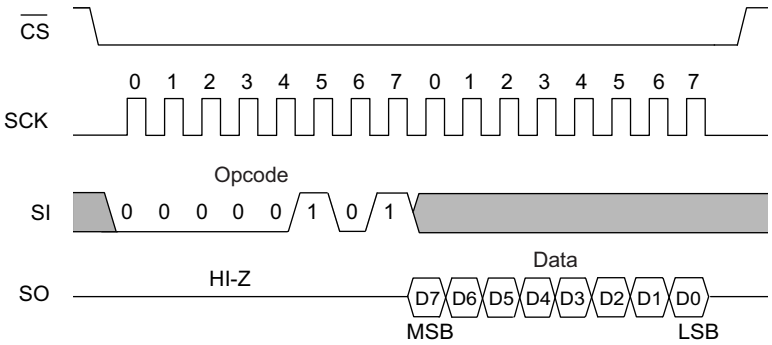
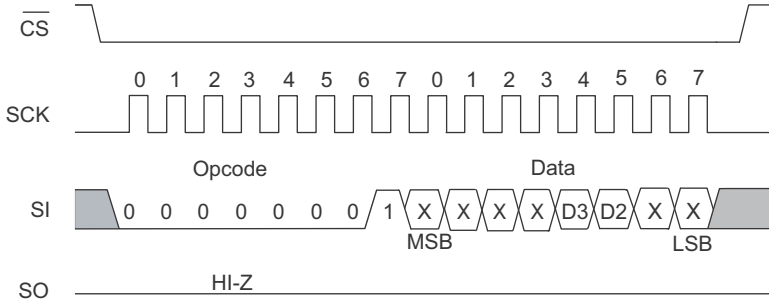



**Figure 9. WRSR Bus Configuration (WREN not shown)**




## Memory Operation

The SPI interface, which is capable of a high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike serial flash and EEPROMs, the CY15B004Q can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

### Write Operation

All writes to the memory begin with a WREN opcode. The WRITE opcode includes the upper bit of the memory address. Bit 3 in the opcode corresponds to the upper address bit (A8). The next byte is the lower 8-bits of the address (A7–A0). In total, the 9-bits specify the address of the first byte of the write operation. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps $\overline{CS}$ LOW. If the last address of 1FFh is reached, the counter will roll over to 000h. Data is written MSB first. The rising edge of $\overline{CS}$ terminates a write operation. A write operation is shown in Figure 10 on page 9.

**Note** When a burst write reaches a protected block address, the automatic address increment stops and all the subsequent data bytes received for write will be ignored by the device.

EEPROMs use page buffers to increase their write throughput. This compensates for the technology's inherently slow write operations. F-RAM memories do not have page buffers because each byte is written to the F-RAM array immediately after it is clocked in (after the eighth clock). This allows any number of bytes to be written without page buffer delays.

**Note** If the power is lost in the middle of the write operation, only the last completed byte will be written.

### Read Operation

After the falling edge of $\overline{CS}$, the bus master can issue a READ opcode. The READ opcode includes the upper bit of the memory address. Bit 3 in the opcode corresponds to the upper address bit (A8). The next byte is the lower 8-bits of the address (A7–A0). In total, the 9-bits specify the address of the first byte of the read operation. After the opcode and address are issued, the device drives out the read data on the next eight clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and $\overline{CS}$ is LOW. If the last address of 1FFh is reached, the counter will roll over to 000h. Data is read MSB first. The rising edge of $\overline{CS}$ terminates a read operation and tristates the SO pin. A read operation is shown in Figure 11 on page 9.

**Figure 10. Memory Write (WREN not shown)**

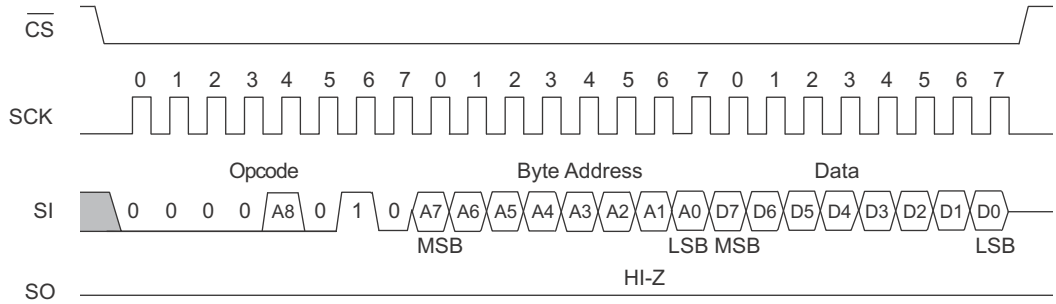
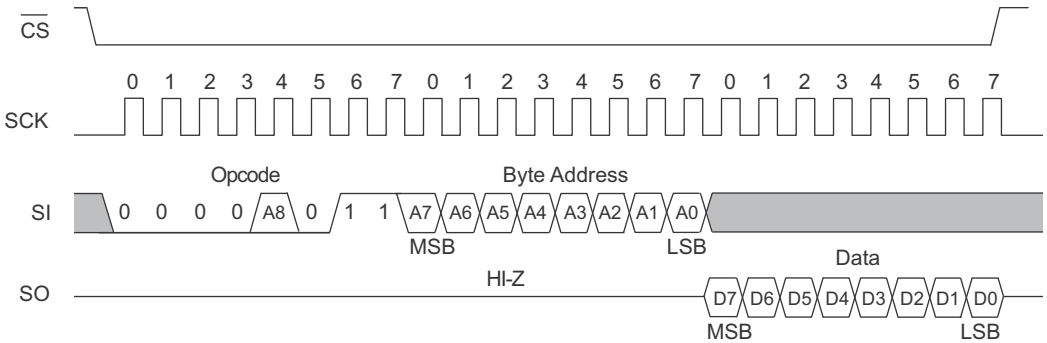


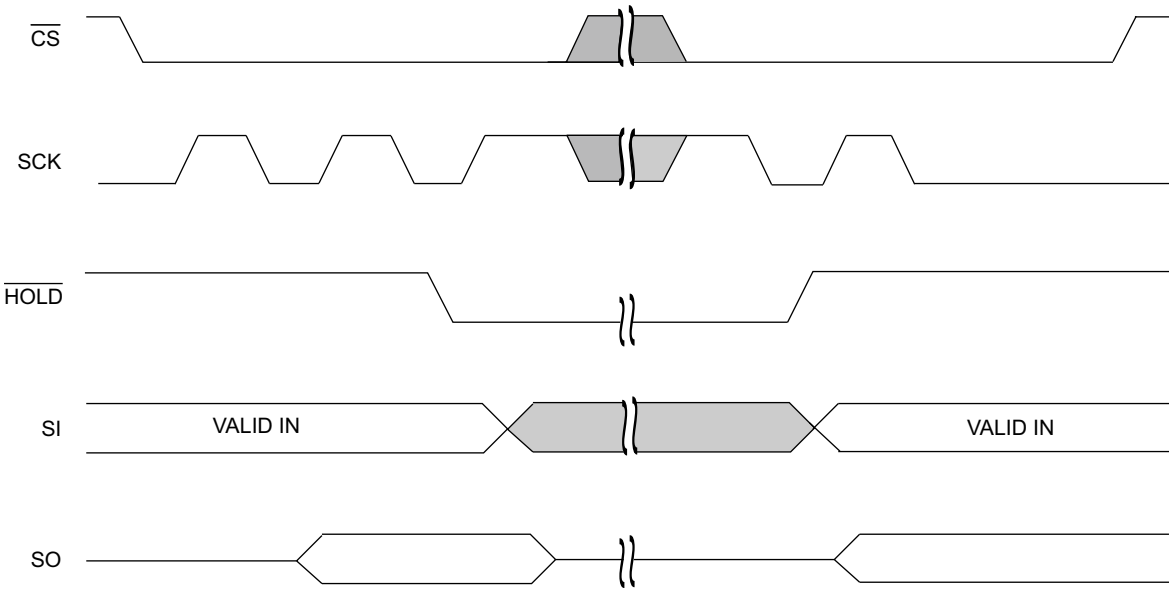

**Figure 11. Memory Read**




## $\overline{\text{HOLD}}$ Pin Operation

The $\overline{\text{HOLD}}$ pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the $\overline{\text{HOLD}}$ pin LOW while SCK is LOW, the current operation will pause. Taking the $\overline{\text{HOLD}}$ pin HIGH while SCK is LOW will resume an operation. The transitions of $\overline{\text{HOLD}}$ must occur while SCK is LOW, but the SCK and $\overline{\text{CS}}$ can toggle during a hold state.

**Figure 12. $\overline{\text{HOLD}}$ Operation** [2]




**Note**
2. Figure shows $\overline{\text{HOLD}}$ operation for input mode and output mode.

## Endurance

The CY15B004Q devices are capable of being accessed at least $10^{13}$ times, reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns of 64 rows of 64-bits each. The entire row is internally accessed once whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation. Table 6 shows endurance calculations for a 64-byte repeating loop, which includes an opcode, a starting address, and a sequential 64-byte data stream. This causes each byte to experience one endurance cycle through the loop.

**Table 6. Time to Reach Endurance Limit for Repeating 64-byte Loop**

| SCK Freq (MHz) | Endurance Cycles/sec | Endurance Cycles/year | Years to Reach Limit |
|---|---|---|---|
| 10 | 18,660 | $5.88 \times 10^{11}$ | 17.0 |
| 5 | 9,330 | $2.94 \times 10^{11}$ | 34.0 |
| 1 | 1,870 | $5.88 \times 10^{10}$ | 170.1 |

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +150 °C

Maximum accumulated storage time
At 150 °C ambient temperature ..... 1000 h
At 125 °C ambient temperature .....11000 h
At 85 °C ambient temperature ..... 121 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{DD}$ relative to $V_{SS}$ .....–1.0 V to +5.0 V

Input voltage ..... –1.0 V to +5.0 V and $V_{IN} < V_{DD}$+1.0 V

DC voltage applied to outputs
in High Z state ..... –0.5 V to $V_{DD}$ + 0.5 V

Transient voltage (< 20 ns)
on any pin to ground potential ..... –2.0 V to $V_{DD}$ + 2.0 V

Package power
dissipation capability ($T_A$ = 25 °C) ..... 1.0 W

Surface mount lead
soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Electrostatic Discharge Voltage [3]
Human Body Model (AEC-Q100-002 Rev. E) ..... 2 kV

Charged Device Model (AEC-Q100-011 Rev. B) ..... 500 V

Latch up current ..... > 140 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{DD}$ |
|---|---|---|
| Automotive-E | –40 °C to +125 °C | 3.0 V to 3.6 V |

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | Min | Typ [4] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply | | | 3.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | $V_{DD}$ supply current | SCK toggling between $V_{DD}$ – 0.3 V and $V_{SS}$, other inputs $V_{SS}$ or $V_{DD}$ – 0.3 V. SO = Open. | $f_{SCK}$ = 1 MHz | – | – | 0.2 | mA |
| | | | $f_{SCK}$ = 10 MHz | – | – | 2 | mA |
| | | | $f_{SCK}$ = 16 MHz | – | – | 3.0 | mA |
| $I_{SB}$ | $V_{DD}$ standby current | $\overline{CS}$ = $V_{DD}$. All other inputs $V_{SS}$ or $V_{DD}$. | $T_A$ = 85 °C | – | – | 6 | µA |
| | | | $T_A$ = 125 °C | – | – | 20 | µA |
| $I_{LI}$ | Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | | – | – | ±1 | µA |
| $I_{LO}$ | Output leakage current | $V_{SS} \le V_{OUT} \le V_{DD}$ | | – | – | ±1 | µA |
| $V_{IH}$ | Input HIGH voltage | | | 0.75 × $V_{DD}$ | – | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | | | – 0.3 | – | 0.25 × $V_{DD}$ | V |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = –2 mA | | $V_{DD}$ – 0.8 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 2 mA | | – | – | 0.4 | V |
| $V_{HYS}$[5] | Input Hysteresis ($\overline{CS}$ and SCK pin) | | | 0.05 × $V_{DD}$ | – | – | V |

**Notes**
3. Electrostatic Discharge voltages specified in the datasheet are the AEC-Q100 standard limits used for qualifying the device. To know the maximum value device passes for, please refer to the device qualification report available on the website.
4. Typical values are at 25 °C, $V_{DD}$ = $V_{DD}$(typ). Not 100% tested.
5. This parameter is characterized but not 100% tested.

## Data Retention and Endurance

| Parameter | Description | Test condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{DR}$ | Data retention | $T_A$ = 125 °C | 11000 | – | Hours |
| | | $T_A$ = 105 °C | 11 | – | Years |
| | | $T_A$ = 85 °C | 121 | – | |
| $NV_C$ | Endurance | Over operating temperature | $10^{13}$ | – | Cycles |

## Example of an F-RAM Life Time in an AEC-Q100 Automotive Application

An application does not operate under a steady temperature for the entire usage life time of the application. Instead, it is often expected to operate in multiple temperature environments throughout the application's usage life time. Accordingly, the retention specification for F-RAM in applications often needs to be calculated cumulatively. An example calculation for a multi-temperature thermal profiles is given below.

| Tempeature T | Time Factor t | Acceleration Factor with respect to Tmax A [6] | Profile Factor P | Profile Life Time L (P) |
|---|---|---|---|---|
| | | $A = \frac{L(T)}{L(Tmax)} = e^{\frac{Ea}{k}\left(\frac{1}{T} - \frac{1}{Tmax}\right)}$ | $P = \frac{1}{\left(\frac{t1}{A1} + \frac{t2}{A2} + \frac{t3}{A3} + \frac{t4}{A4}\right)}$ | $L(P) = P \times L(Tmax)$ |
| T1 = 125 °C | t1 = 0.1 | A1 = 1 | 8.33 | > 10.46 Years |
| T2 = 105 °C | t2 = 0.15 | A2 = 8.67 | | |
| T3 = 85 °C | t3 = 0.25 | A3 = 95.68 | | |
| T4 = 55 °C | t4 = 0.50 | A4 = 6074.80 | | |

## Capacitance

| Parameter [7] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_O$ | Output pin capacitance (SO) | $T_A$ = 25 °C, f = 1 MHz, $V_{DD} = V_{DD}$(typ) | 8 | pF |
| $C_I$ | Input pin capacitance | | 6 | pF |

## Thermal Resistance

| Parameter [7] | Description | Test Conditions | 8-pin SOIC | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 148 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 48 | °C/W |

## AC Test Conditions

Input pulse levels .....10% and 90% of $V_{DD}$

Input rise and fall times .....5 ns

Input and output timing reference levels .....0.5 × $V_{DD}$

Output load capacitance ..... 30 pF

**Notes**

6. Where k is the Boltzmann constant 8.617 × $10^{-5}$ eV/K, Tmax is the highest temperature specified for the product, and T is any temperature within the F-RAM product specification. All temperatures are in Kelvin in the equation.
7. This parameter is characterized but not 100% tested.

## AC Switching Characteristics

Over the Operating Range

| Parameters [8] | | Description | Min | Max | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Cypress Parameter | Alt. Parameter | | | | | | |
| $f_{SCK}$ | – | SCK Clock frequency | 0 | 10 | 0 | 16 | MHz |
| $t_{CH}$ | – | Clock HIGH time | 40 | – | 25 | – | ns |
| $t_{CL}$ | – | Clock LOW time | 40 | – | 25 | – | ns |
| $t_{CSU}$ | $t_{CSS}$ | Chip select setup | 10 | – | 10 | – | ns |
| $t_{CSH}$ | $t_{CSH}$ | Chip select hold | 10 | – | 10 | – | ns |
| $t_{OD}$[9, 10] | $t_{HZCS}$ | Output disable time | – | 30 | – | 20 | ns |
| $t_{ODV}$ | $t_{CO}$ | Output data valid time | – | 35 | – | 25 | ns |
| $t_{OH}$ | – | Output hold time | 0 | – | 0 | – | ns |
| $t_D$ | – | Deselect time | 100 | – | 60 | – | ns |
| $t_R$[11, 12] | – | Data in rise time | – | 50 | – | 50 | ns |
| $t_F$[11, 12] | – | Data in fall time | – | 50 | – | 50 | ns |
| $t_{SU}$ | $t_{SD}$ | Data setup time | 5 | – | 5 | – | ns |
| $t_H$ | $t_{HD}$ | Data hold time | 5 | – | 5 | – | ns |
| $t_{HS}$ | $t_{SH}$ | $\overline{HOLD}$ setup time | 10 | – | 10 | – | ns |
| $t_{HH}$ | $t_{HH}$ | $\overline{HOLD}$ hold time | 10 | – | 10 | – | ns |
| $t_{HZ}$[9, 10] | $t_{HHZ}$ | $\overline{HOLD}$ LOW to HI-Z | – | 30 | – | 20 | ns |
| $t_{LZ}$[10] | $t_{HLZ}$ | $\overline{HOLD}$ HIGH to data active | – | 30 | – | 20 | ns |

**Notes**

8. Test conditions assume a signal transition time of 5 ns or less, timing reference levels of 0.5 × $V_{DD}$, input pulse levels of 10% to 90% of $V_{DD}$, and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance shown in AC Test Conditions on page 12.
9. $t_{OD}$ and $t_{HZ}$ are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
10. This parameter is characterized but not 100% tested.
11. Rise and fall times measured between 10% and 90% of waveform.
12. These parameters are guaranteed by design and are not tested.

**Figure 13. Synchronous Data Timing (Mode 0)**

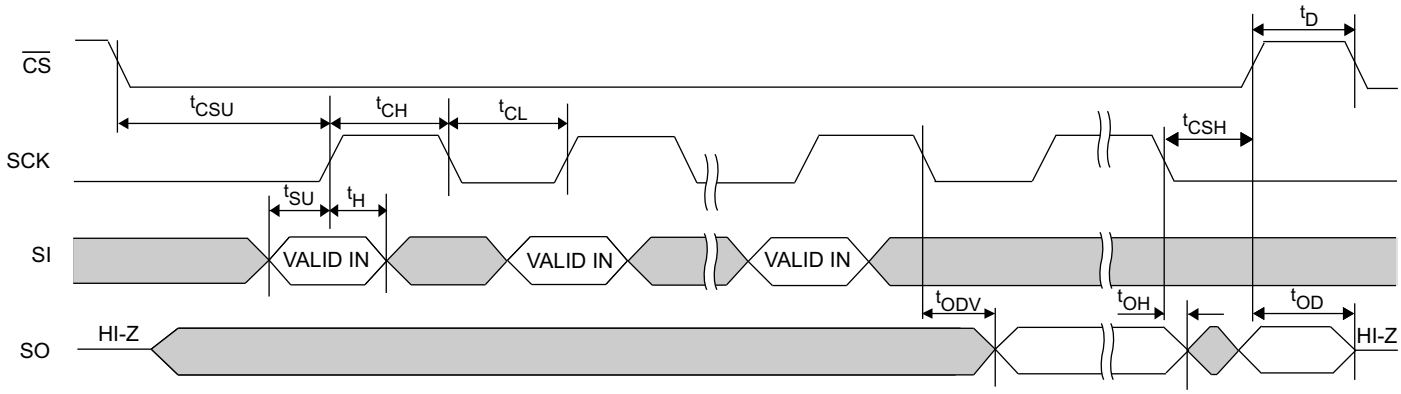
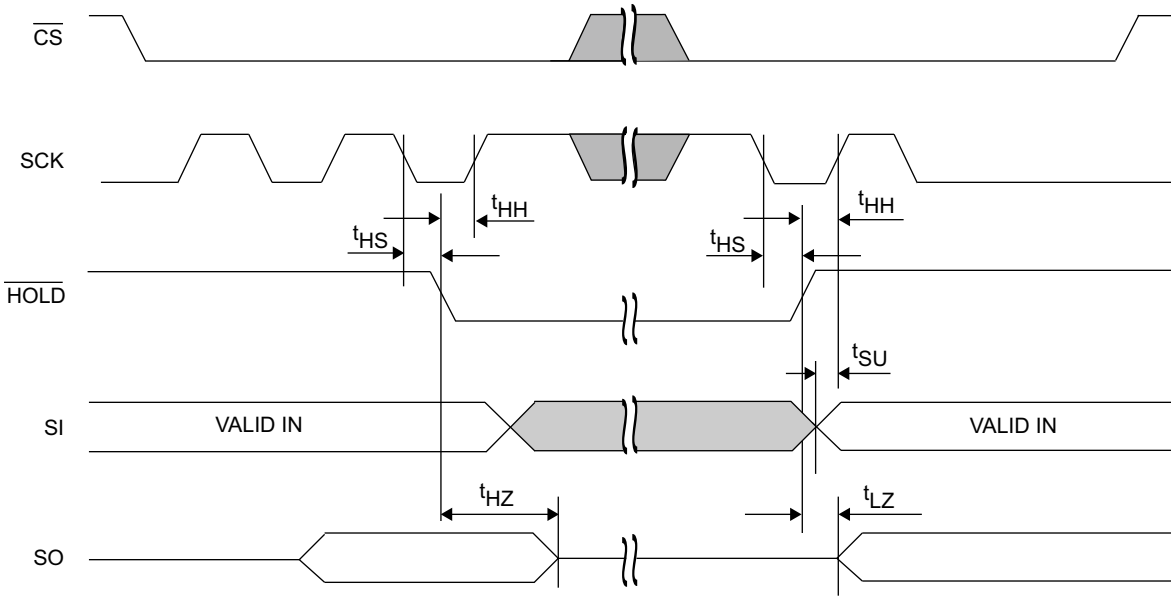



**Figure 14. $\overline{\text{HOLD}}$ Timing**

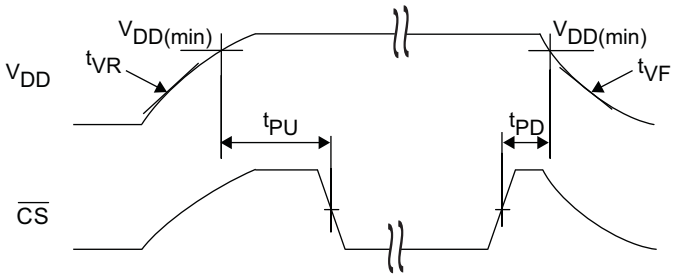


## Power Cycle Timing

Over the Operating Range

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PU}$ | Power-up $V_{DD}$(min) to first access ($\overline{CS}$ LOW) | 1 | – | ms |
| $t_{PD}$ | Last access ($\overline{CS}$ HIGH) to power-down ($V_{DD}$(min)) | 0 | – | µs |
| $t_{VR}$ [13] | $V_{DD}$ power-up ramp rate | 30 | – | µs/V |
| $t_{VF}$ [13] | $V_{DD}$ power-down ramp rate | 20 | – | µs/V |

**Figure 15. Power Cycle Timing**




**Note**
13. Slope measured at any point on $V_{DD}$ waveform.

## Ordering Information

| Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|
| CY15B004Q-SXE | 51-85066 | 8-pin SOIC | Automotive-E |

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

### Ordering Code Definitions

CY 15 B 004 Q - S X E X

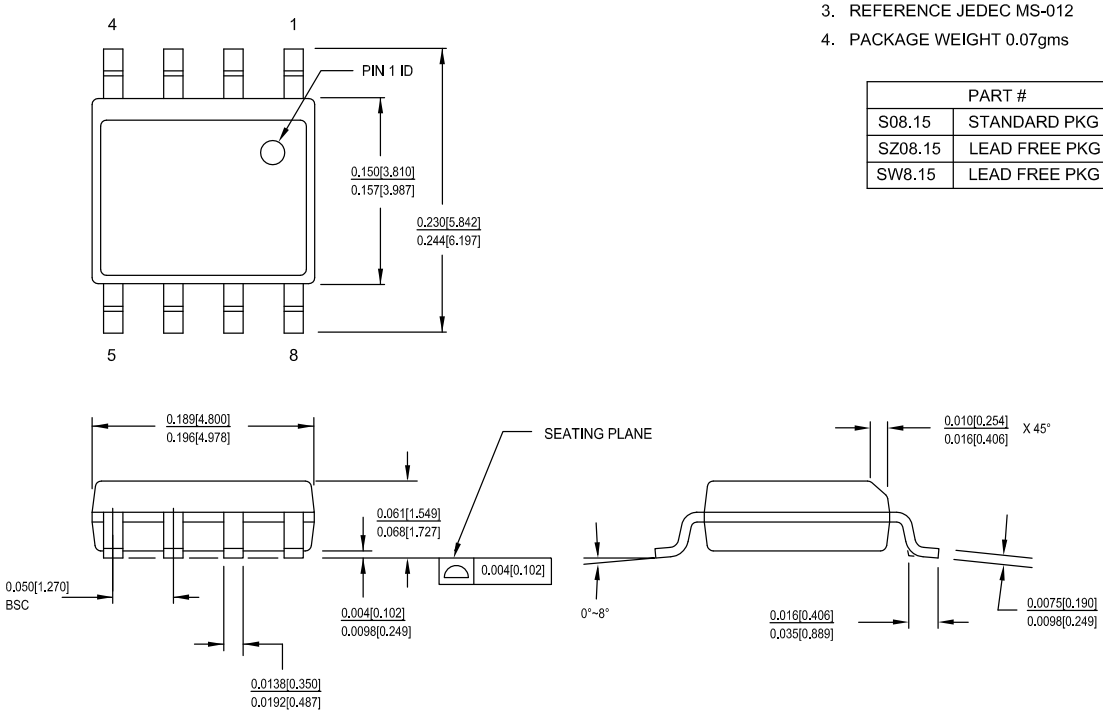
- X: Option: X = blank or T
  blank = Standard; T = Tape and Reel
- E: Temperature Range:
  E = Automotive-E (–40 °C to +125 °C)
- X: X = Pb-free
- S: Package Type: S = 8-pin SOIC
- Q: Q = SPI F-RAM
- 004: Density: 004 = 4-kbit
- B: Voltage: B = 3.0 V to 3.6 V
- 15: F-RAM
- CY: Company ID: CY = Cypress

## Package Diagrams

**Figure 16. 8-pin SOIC (150 Mils) Package Outline, 51-85066**

1. DIMENSIONS IN INCHES[MM] MIN. / MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART # | |
|---|---|
| S08.15 | STANDARD PKG |
| SZ08.15 | LEAD FREE PKG |
| SW8.15 | LEAD FREE PKG |




51-85066 *H

## Acronyms

| Acronym | Description |
|---|---|
| AEC | Automotive Electronics Council |
| CPHA | clock phase |
| CPOL | clock polarity |
| EEPROM | electrically erasable programmable read-only memory |
| EIA | Electronic Industries Alliance |
| I/O | input/output |
| JEDEC | Joint Electron Devices Engineering Council |
| JESD | JEDEC Standards |
| LSB | least significant bit |
| MSB | most significant bit |
| F-RAM | ferroelectric random access memory |
| RoHS | Restriction of Hazardous Substances |
| SPI | serial peripheral interface |
| SOIC | small outline integrated circuit |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | Degrees Celsius |
| Hz | hertz |
| kHz | kilohertz |
| KΩ | kilohms |
| Kbit | kilobits |
| kV | kilovolts |
| MHz | megahertz |
| µA | microamperes |
| µs | microseconds |
| mA | milliamperes |
| ms | milliseconds |
| ns | nanoseconds |
| Ω | ohms |
| % | percent |
| pF | picofarads |
| V | volts |
| W | watts |

# Errata

This section describes the errata for the 4Kb SPI F-RAM (512 × 8, SPI) products. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document with the device datasheet for complete functional differences.

Contact your local Cypress Sales Representative if you have questions. You can also send your related queries directly to FRAM@cypress.com.

## Part Numbers Affected

| Part Number | Device Characteristics |
|---|---|
| CY15B004Q | 512 × 8, 3.0 V to 3.6 V, single power supply, serial (SPI) interface F-RAM in 8-pin SOIC package. |

## Qualification Status

Production parts.

## Errata Summary

The following table defines the errata applicability.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|---|---|
| The Write Enable Latch (WEL) bit in the Status Register of CY15B004Q part doesn't clear after executing the memory write (WRITE) operation at memory location(s) from 0x100 to 0x1FF. | CY15B004Q-SXE | Rev *A | None. This behavior is applicable to all listed parts in the production. |

1. The Write Enable Latch (WEL) bit in the Status Register of CY15B004Q part doesn't clear after executing the memory write (WRITE) operation at memory location(s) from 0x100 to 0x1FF.

■ **Problem Definition**

As per the CY15B004Q datasheet "sending the WREN opcode causes the internal Write Enable Latch (WEL) to be set. A flag bit in the status register, called WEL, indicates the state of the latch. WEL = 1 indicates that writes are permitted. Attempting to write the WEL bit in the status register has no effect. Completing any write operation will automatically clear the write-enable latch and will prevent further writes without another WREN command".

However, in the CY15B004Q part, the WEL bit doesn't clear automatically after writing at any memory location(s) from 0x100 to 0x1FF. That means, after completing the write cycle with the opcode byte 0x0A, WEL bit in status register is still set and hence a further write can be issued without sending the WREN opcode.

**Status Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| X (0) | X (0) | X (0) | X (0) | BP1 (0) | BP0 (0) | WEL (0) | X (0) |

**Status Register Bit Definition**

| Bit | Definition | Description |
|---|---|---|
| Bit 0 | Don't care | This bit is non-writable and always returns '0' upon read. |
| Bit 1 (WEL) | Write Enable Latch | WEL indicates if the device is write enabled. This bit defaults to '0' (disabled) on power-up.<br>WEL = '1' --> Write enabled<br>WEL = '0' --> Write disabled |
| Bit 2 (BP0) | Block Protect bit '0' | Used for block protection. For details, see Table 4 on page 7. |
| Bit 3 (BP1) | Block Protect bit '1' | Used for block protection. For details, see Table 4 on page 7. |
| Bit 4-7 | Don't care | These bits are non-writable and always return '0' upon read. |

The internal state machine of CY15B004Q is intended to clear the WEL bit after executing write opcodes (WRITE and WRSR). However, as explained above, the WEL doesn't clear when executing the memory write (WRITE) at location/s from 0x100 to 0x1FF. The 4Kb memory requires 9 address bits to map the entire memory array (512 × 8). To optimize the command cycle and to maintain the compatibility with the industry standard 4Kb SPI EEPROMs, the MSB of the address ($9^{th}$ bit) in the 4Kb device is embedded into write (WRITE) and read (READ) opcodes as shown below.

**For address range – 0x00 to 0xFF:**

WRITE opcode – 0000 A010 = 0x0000 0010 (or 0x02 in hex, A = '0')

READ opcode – 0000 A011 = 0x0000 0011 (or 0x03 in hex, A = '0')

**For address range – 0x100 to 0x1FF:**

WRITE opcode – 0000 A010 = 0x0000 1010 (or 0x0A in hex, A = '1')

READ opcode – 0000 A011 = 0x0000 1011 (or 0x0B in hex, A = '1')

Due to a logic bug in the CY15B004Q state machine, the opcode byte 0x0A does not trigger clearing of WEL bit, hence the WEL bit remains set even after executing the memory write at address location/s from 0x100 to 0x1FF.

■ **Parameters Affected**

None.

■ **Trigger Condition(S)**

Execute the Write Enable command (WREN) followed by the write command (WRITE) to memory address range 0x100 to 0x1FF.

■ **Scope of Impact**

None. It only allows a subsequent write (WRITE or WRSR) without sending a prior WREN command.

■ **Workaround**

To ensure that the WEL bit is cleared after every write, the SPI host controller can issue the Write Disable (WRDI) opcode at the end of every write cycle (after $\overline{CS}$ goes high). The WRDI command clears the WEL (if set) and disables all writes until the WEL is set by sending the WREN opcode before initiating a new write operation.

■ **Fix Status**

There is no fix planned and all the CY15B004Q part in production will continue with the above errata.

## Document History Page

| Document Title: CY15B004Q, 4-Kbit (512 × 8) Serial (SPI) Automotive F-RAM<br>Document Number: 002-10032 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 5032342 | GVCH | 12/15/2015 | New data sheet. |
| *A | 5124930 | GVCH | 02/04/2016 | Updated DC Electrical Characteristics:<br>Changed maximum value of $I_{DD}$ parameter corresponding to Test Condition "$f_{SCK}$ = 16 MHz" from 3.2 mA to 3.0 mA. |
| *B | 5573964 | GVCH | 01/23/2017 | Changed status from Summary to Final.<br>Updated Serial Peripheral Interface – SPI Bus:<br>Updated WREN - Set Write Enable Latch:<br>Updated description (Added note regarding Errata).<br>Updated Maximum Ratings:<br>Updated Electrostatic Discharge Voltage:<br>Changed value of "Human Body Model" from 4 kV to 2 kV.<br>Changed value of "Charged Device Model" from 1.25 kV to 500 V.<br>Removed "Machine Model" related information.<br>Updated Ordering Information:<br>Updated part numbers.<br>Added Errata.<br>Updated to new template. |
| *C | 5685431 | GVCH | 04/05/2017 | Updated Maximum Ratings:<br>Added Note 3 and referred the same note in "Electrostatic Discharge Voltage".<br>Updated to new template. |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

### PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

### Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

### Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2015–2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

**Данный компонент на территории Российской Федерации**

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9