

# SID11x1K SCALE-iDriver Family

Up to 8 A Single Channel IGBT/MOSFET Gate Driver Providing Reinforced Galvanic Isolation up to 650 V Blocking Voltage

## Product Highlights

### Highly Integrated, Compact Footprint

- Split outputs providing up to 8 A peak drive current
- Integrated FluxLink™ technology
- Rail-to-rail stabilized output voltage
- Unipolar supply voltage for secondary-side
- Suitable for 600 V / 650 V / 1200 V IGBT and MOSFET switches
- Providing basic isolation up to 1200 V blocking voltage
- Up to 75 kHz switching frequency
- Low propagation delay time 260 ns
- Propagation delay jitter  $\pm 5$  ns
- $-40$  °C to  $125$  °C operating ambient temperature
- High common-mode transient immunity
- eSOP package with 9.5 mm creepage and clearance

### Advanced Protection / Safety Features

- Undervoltage lock-out (UVLO) protection for primary and secondary-side and fault feedback
- Short-circuit protection using  $V_{CESAT}$  monitoring and fault feedback
- Advanced Soft Shut Down (ASSD)

### Full Safety and Regulatory Compliance

- 100% production partial discharge test
- 100% production HIPOT compliance testing at 6 kV RMS 1 s
- Reinforced insulation meets VDE 0884-10

### Green Package

- Halogen free and RoHS compliant

### Applications

- Delivery vehicles
- General purpose drives
- General industrial equipment

## Description

The SID11x1K is a single channel IGBT and MOSFET driver in an eSOP package. Reinforced galvanic isolation is provided by Power Integrations' innovative solid insulator FluxLink technology. 8 A peak output drive current enables the product to drive devices up to 600 A (typical) without requiring any additional active components. For gate drive requirements that exceed the stand-alone capability of the SID11x1K's, an external amplifier (booster) may be added. Stable positive and negative voltages for gate control are provided by one unipolar isolated voltage source.

Additional features such as short-circuit protection (DESAT) with Advanced Soft Shut Down (ASSD), undervoltage lock-out (UVLO) for primary-side and secondary-side and rail-to-rail output with temperature and process compensated output impedance guarantee safe operation even in harsh conditions.

Controller (PWM and fault) signals are compatible with 5 V CMOS logic, which may also be adjusted to 15 V levels by using external resistor divider.

## Product Portfolio

Product <sup>1</sup>	Peak Output Drive Current
SID1151K	5.0 A
SID1181K	8.0 A

Table 1. SCALE-iDriver Portfolio.

Notes:

1. Package: eSOP-R16B.



Figure 2. eSOP-R16B Package.

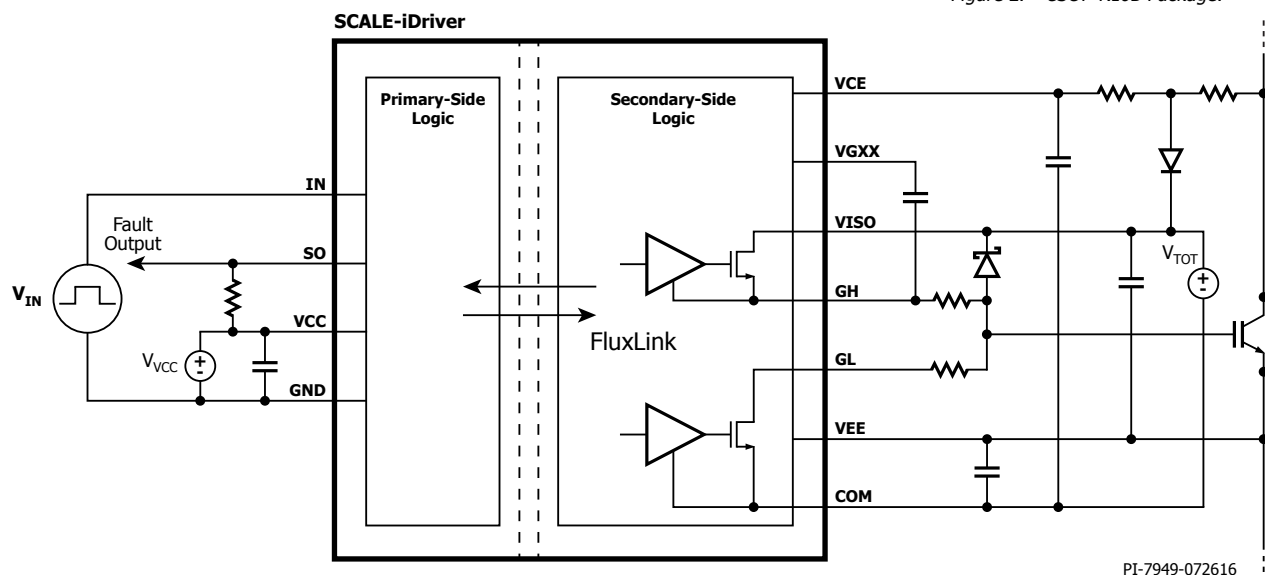
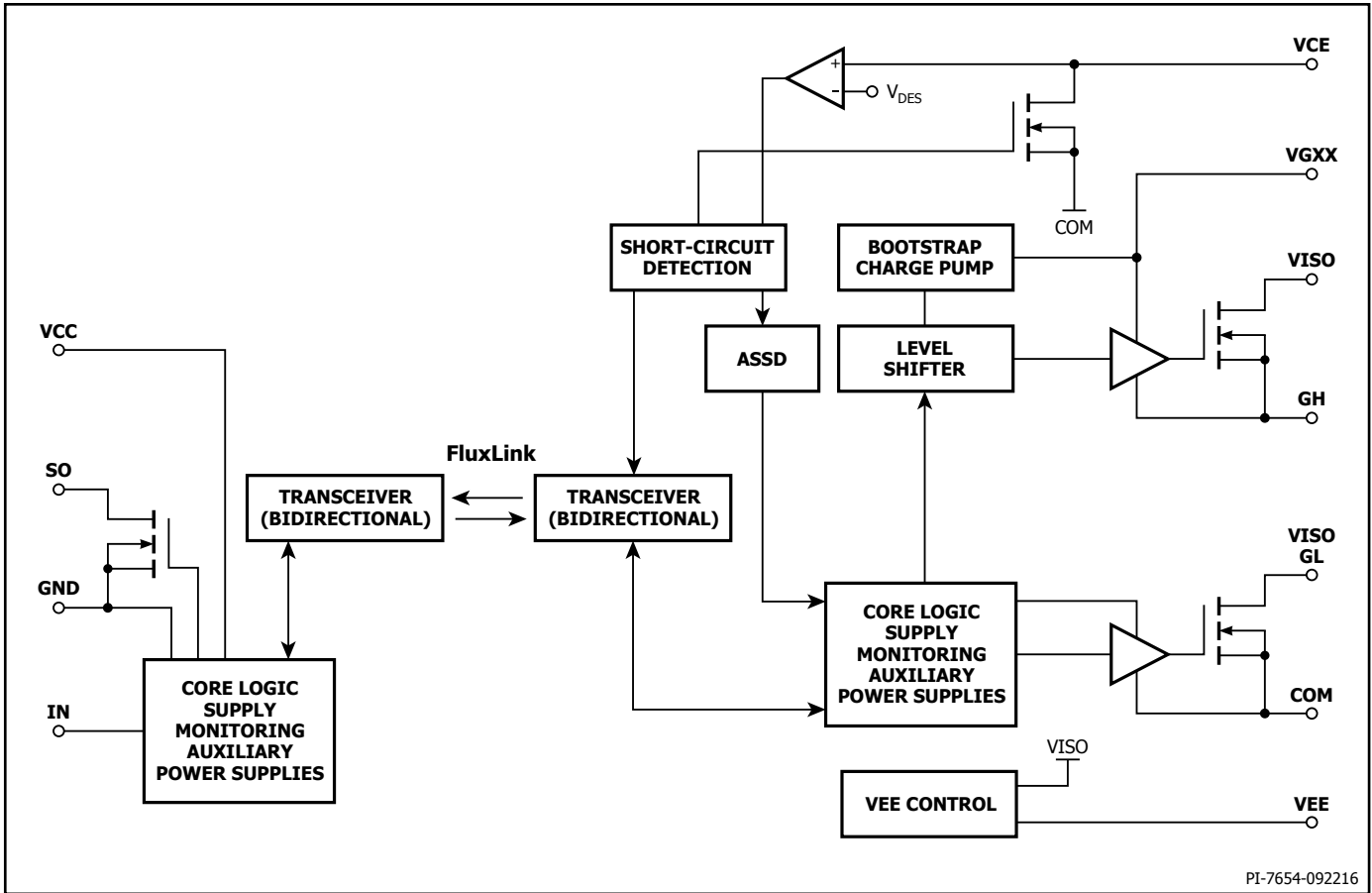


Figure 1. Typical Application Schematic.

PI-7949-072616



PI-7654-092216

Figure 3. Functional Block Diagram.

## Pin Functional Description

### VCC Pin (Pin 1):

This pin is the primary-side supply voltage connection.

### GND Pin (Pin 3-6):

This pin is the connection for the primary-side ground potential. All primary-side voltages refer to the pin.

### IN Pin (Pin 7):

This pin is the input for the logic command signal.

### SO Pin (Pin 8):

This pin is the output for the logic fault signal (open drain).

### NC Pin (Pin 9):

This pin must be un-connected. Minimum PCB pad size for soldering is required.

### VEE Pin (Pin 10):

Common (IGBT emitter/MOSFET source) output supply voltage.

### VCE Pin (Pin 11):

This pin is the desaturation monitoring voltage input connection.

### VGXX Pin (Pin 12):

This pin is the bootstrap and charge pump supply voltage source.

### GH Pin (Pin 13):

This pin is the driver output – sourcing current (turn-on) connection.

### VISO Pin (Pin 14):

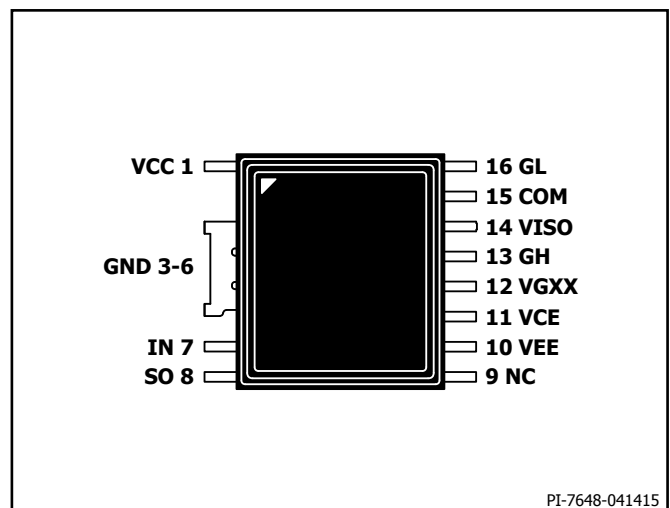
This pin is the input for the secondary-side positive supply voltage.

### COM Pin (Pin 15):

This pin provides the secondary-side reference potential.

### GL Pin (Pin 16):

This pin is the driver output – sinking current (turn-off).



PI-7648-041415

Figure 4. Pin Configuration.

### SCALE-iDriver Functional Description

The single channel SCALE-iDriver™ family is designed to drive IGBTs and MOSFETs or other semiconductor power switches with a blocking voltage of up to 1200 V and provide reinforced isolation between micro-controller and the power semiconductor switch. The logic input (PWM) command signals applied via the IN pin and the primary supply voltage supplied via the VCC pin are both referenced to the GND pin. The working status of the power semiconductor switch and SCALE-iDriver is monitored via the SO pin.

PMW command signals are transferred from the primary (IN) to secondary-side via FluxLink isolation technology. The GH pin supplies a positive gate voltage and charges the semiconductor gate during the turn-on process. The GL pin supplies the negative voltage and discharges the gate during the turn-off process.

Short-circuit protection is implemented using a desaturation detection technique monitored via the VCE pin. When the SCALE-iDriver detects a short-circuit, the semiconductor turn-off process is activated using an Advanced Soft Shut Down (ASSD) technique.

#### Power Supplies

The SID11x1K requires two power supplies. One is the primary-side ( $V_{CC}$ ) which powers the primary-side logic and communication with the secondary (insulated) side. Another supply voltage is required for the secondary-side,  $V_{TOT}$  is applied between the VISO pin and the COM pin.  $V_{TOT}$  needs to be insulated from the primary-side and must provide at least the same insulation capabilities as the SCALE-iDriver.  $V_{TOT}$  must have a low capacitive coupling to the primary or any other secondary-side. The positive gate-emitter voltage  $V_{VISO}$  is provided by VISO which is internally generated and stabilized to 15 V (typically) with respect to VEE. The negative gate-emitter voltage  $V_{VEE}$  is provided by VEE with respect to COM. Due to the limited current sourcing capabilities of the VEE pin, any additional load needs to be applied between the VISO and COM pins. No additional load between VISO and VEE pins or between VEE and COM pins is allowed.

#### Input and Fault Logic (Primary-Side)

The input (IN) and output (SO) logic is designed to work directly with micro-controllers using 5 V CMOS logic. If the physical distance between the controller and the SCALE-iDriver is large or if a different logic level is required the resistive divider in Figure 5, or Schmitt-trigger ICs (Figures 13 and 14) can be used. Both solutions adjust the logic level as necessary and will also improve the driver's noise immunity.

Gate driver commands are transferred from the IN pin to the GH and GL pins with a propagation delay  $t_{p(LH)}$  and  $t_{p(HL)}$ .

During normal operation, when there is no fault detected, the SO pin stays at high impedance (open). Any fault is reported by connecting the SO pin to GND. The SO pin stays low as long as the  $V_{VCC}$  voltage (primary-side) stays below  $UVLO_{VCC}$ , where the propagation delay is negligible. If desaturation is detected (there is a short-circuit), or the supply voltages  $V_{VISO}$ ,  $V_{VEE}$  (secondary-side) drop below  $UVLO_{VISO}$ ,  $UVLO_{VEE}$ , the SO status changes with a delay time  $t_{FAULT}$  and keeps status low for a time defined as  $t_{SO}$ . In case of a fault condition the driver applies the off-state (the GL pin is connected to COM). During the  $t_{SO}$  period, command signal transitions from the IN pin are ignored. A new turn-on command transition is required before the driver will enter the on-state.

The SO pin current is defined as  $I_{SO}$ ; voltage during low status is defined as  $V_{SO(FAULT)}$ .

#### Output (Secondary-Side)

The gate of the power semiconductor switch to be driven can be connected to the SCALE-iDriver output via pins GH and GL, using two different resistor values. Turn-on gate resistor  $R_{GON}$  needs to be

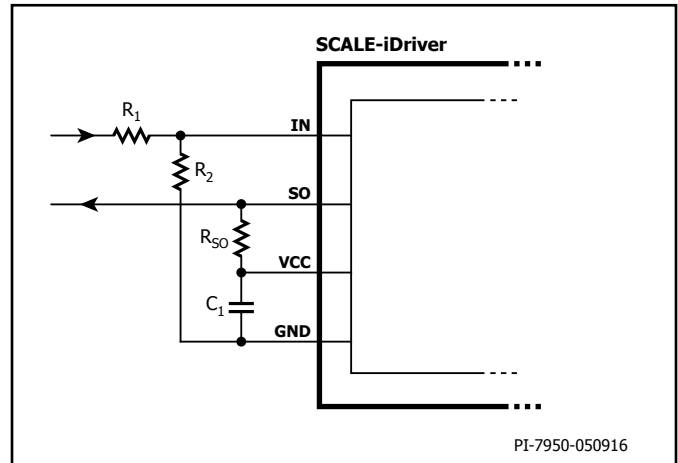


Figure 5. Increased Threshold Voltages  $V_{IN+LT}$  and  $V_{IN+HT}$  For  $R_1 = 3.3 \text{ k}\Omega$  and  $R_2 = 1 \text{ k}\Omega$  the IN Logic Level is 15 V.

connected to the GH pin and turn-off gate resistor  $R_{GOFF}$  to the GL pin. If both gate resistors have the same value, the GL and GH pins can be connected together. Note: The SCALE-iDriver data sheet defines the  $R_{GH}$  and  $R_{GL}$  values as total resistances connected to the respective pins GH and GL. Note that most power semiconductor data sheets specify an internal gate resistor  $R_{GINT}$  which is already integrated into the power semiconductor switch. In Addition to  $R_{GINT}$ , external resistor devices  $R_{GON}$  and  $R_{GOFF}$  are specified to setup the gate current levels to the application requirements. Consequently,  $R_{GH}$  is the sum of  $R_{GON}$  and  $R_{GINT}$  as shown in Figures 9 and 10. Careful consideration should be given to the power dissipation and peak current associated with the external gate resistors.

The GH pin output current source ( $I_{GH}$ ) of SID1181K is capable of handling up to 7.3 A during turn-on, and the GL pin output current source ( $I_{GL}$ ) is able to sink up to 8.0 A during turn-off. The SCALE-iDriver's internal resistances are described as  $R_{GHI}$  and  $R_{GLI}$  respectively. If the gate resistors for SCALE-iDriver family attempt to draw a higher peak current, the peak current will be internally limited to a safe value, see Figures 6 and 7. Figure 8 shows the peak current

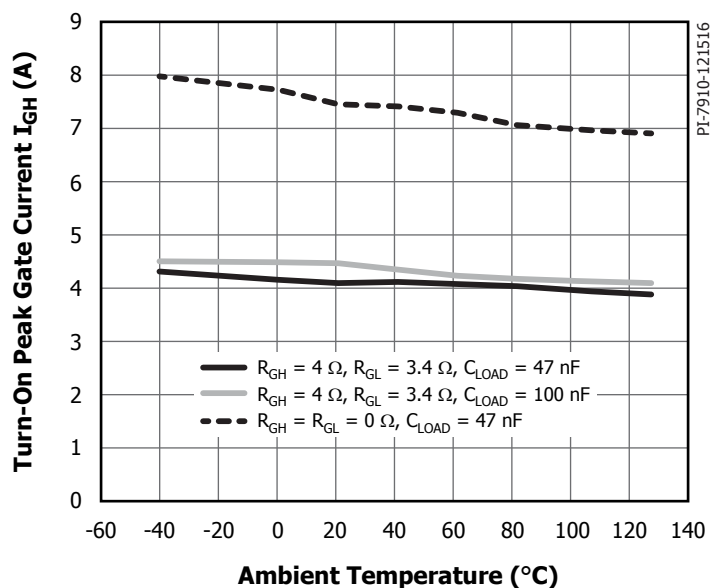


Figure 6. Turn-On Peak Output Current (Source) vs. Ambient Temperature. Conditions:  $V_{CC} = 5 \text{ V}$ ,  $V_{TOT} = 25 \text{ V}$ ,  $f_s = 20 \text{ kHz}$ , Duty Cycle = 50%.

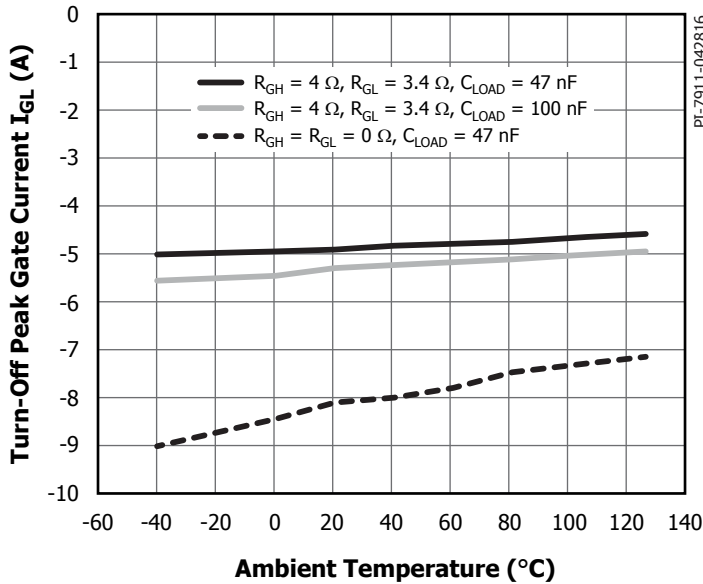


Figure 7. Turn-Off Peak Output Current (Sink) vs. Ambient Temperature. Conditions:  $V_{VCC} = 5\text{ V}$ ,  $V_{TOT} = 25\text{ V}$ ,  $f_s = 20\text{ kHz}$ , Duty Cycle = 50%

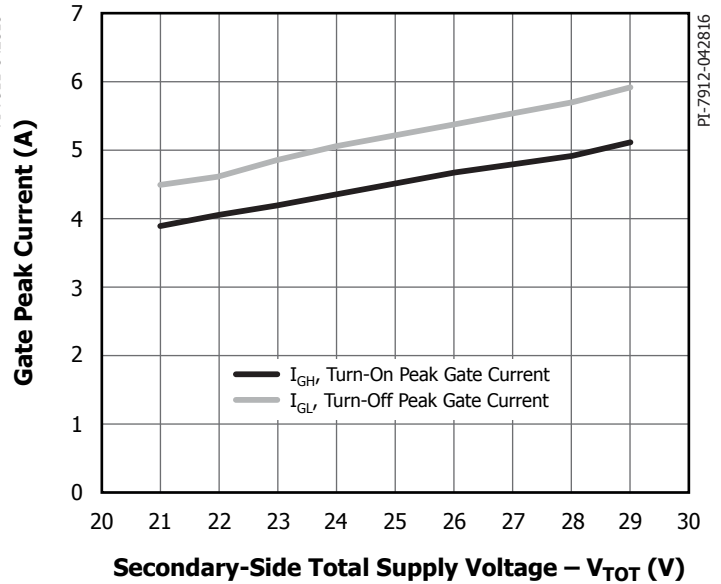


Figure 8. Turn-On and Turn-Off Peak Output Current vs. Secondary-Side Total Supply Voltage ( $V_{TOT}$ ). Conditions:  $V_{VCC} = 5\text{ V}$ ,  $T_j = 25\text{ °C}$ ,  $R_{GH} = 4\text{ Ω}$ ,  $R_{GL} = 3.4\text{ Ω}$ ,  $C_{LOAD} = 100\text{ nF}$ ,  $f_s = 1\text{ kHz}$ , Duty Cycle = 50%.

that can be achieved for a given supply voltage for same gate resistor values, load capacitance and layout design.

**Short-Circuit Protection**

The SCALE-iDriver uses the semiconductor desaturation effect to detect short-circuits and protects the device against damage by employing an Advanced Soft Shut Down (ASSD) technique. Desaturation can be detected using two different circuits, either with diode sense circuitry  $D_{VCE}$  (Figure 10) or with resistors  $R_{VCEX}$  (Figure 9). With the help of a well stabilized  $V_{VISO}$  and a Schottky diode ( $D_{STO}$ ) connected between semiconductor gate and VISO pin the short-circuit current value can be limited to a safe value.

During the off-state, the VCE pin is internally connected to the COM pin and  $C_{RES}$  is discharged (red curve in Figure 11 represents the potential of the VCE pin). When the power semiconductor switch receives a turn-on command, the collector-emitter voltage ( $V_{CE}$ ) decreases from the off-state level same as the DC-link voltage to a normally much lower on-state level (see blue curve in Figure 11) and  $C_{RES}$  begins to be charged up to the  $V_{CE}$  saturation level ( $V_{CE\text{SAT}}$ ).  $C_{RES}$  charging time depends on the resistance of  $R_{VCEX}$  (Figure 9), DC-link voltage and  $C_{RES}$  and  $R_{VCE}$  value. The  $V_{CE}$  voltage during on-state is continuously observed and compared with a reference voltage,  $V_{DES}$ . The  $V_{DES}$  level is optimized for IGBT applications. As soon as  $V_{CE} > V_{DES}$  (red circle in Figure 11), the driver turns off the power semiconductor switch with a controlled collector current slope, limiting the  $V_{CE}$  overvoltage excursions to below the maximum collector-emitter voltage ( $V_{CE\text{ES}}$ ). Turn-on commands during this time and during  $t_{SO}$  are ignored, and the SO pin is connected to GND.

The response time  $t_{RES}$  is the  $C_{RES}$  charging time and describes the delay between  $V_{CE}$  asserting and the voltage on the VCE pin rising (see Figure 11). Response time should be long enough to avoid false tripping during semiconductor turn-on and is adjustable via  $R_{RES}$  and  $C_{RES}$  (Figure 10) or  $R_{VCE}$  and  $C_{RES}$  (Figure 9) values. It should not be longer than the period allowed by the semiconductor manufacturer.

**Safe Power-Up and Power-Down**

During driver power-up and power-down, several unintended input / output states may occur. In order to avoid these effects, it is recommended that the IN pin is kept at logic low during power-up

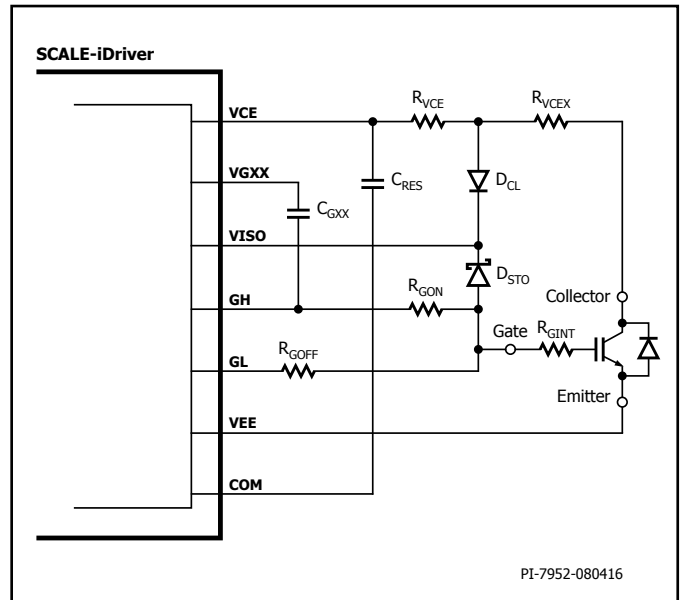


Figure 9. Short-Circuit Protection using a Resistor Chain  $R_{VCEX}$

and power-down. Any supply voltage related to VCC, VISO, VEE and VGXX pins should be stabilized using ceramic capacitors  $C_1$ ,  $C_{S1X}$ ,  $C_{S2X}$ ,  $C_{GXX}$  respectively as shown in Figures 13 and 14. After supply voltages reach their nominal values, the driver will begin to function after a time delay  $t_{START}$ .

**Short-Pulse Operation**

If command signals applied to the IN pin are shorter than the minimum specified by  $t_{GE(MIN)}$ , the SCALE-iDriver output signals, GH and GL pins, will be extended to value  $t_{GE(MIN)}$ . The duration of pulses longer than  $t_{GE(MIN)}$  will not be changed.

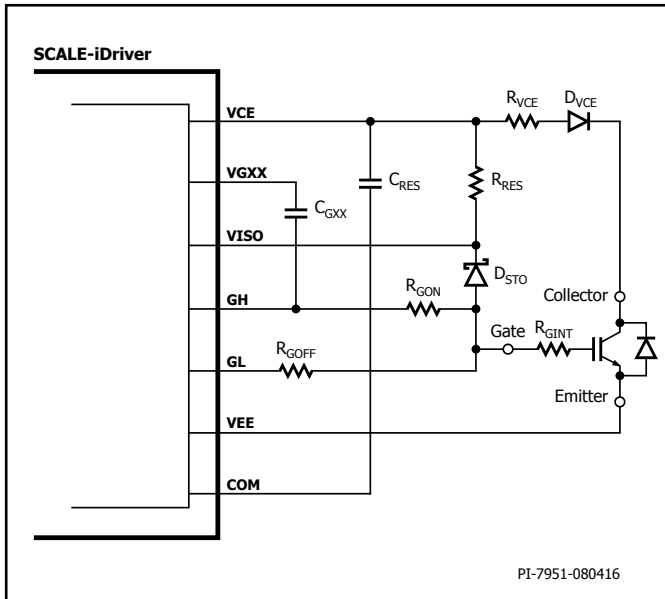


Figure 10. Short-Circuit Protection Using Rectifier Diode  $D_{VCE}$

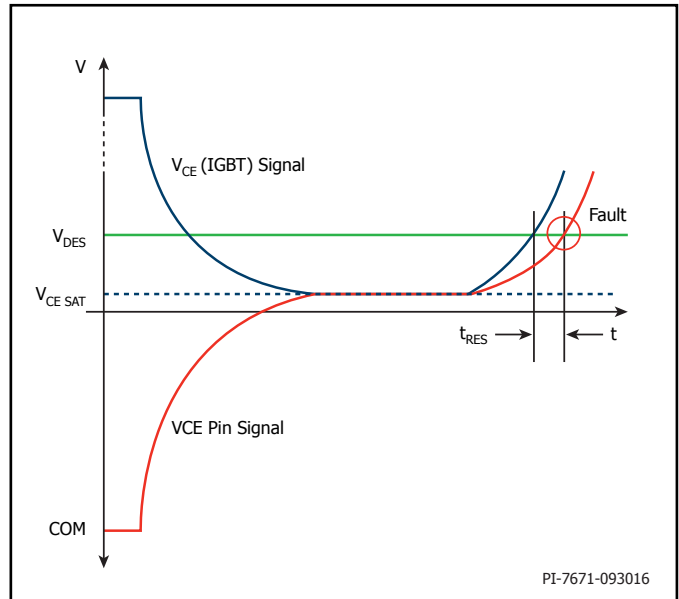


Figure 11. Short-Circuit Protection Using Resistors Chain  $R_{VCE}$

**Advanced Soft Shut Down (ASSD)**

This function is activated when a short-circuit is detected. It protects the power semiconductor switch against destruction by ending the turn-on state and limiting the current slope in order to keep momentary  $V_{CE}$  overvoltages below  $V_{CES}$ . This function is particularly suited to IGBT applications. Figure 12 shows how the ASSD function operates. The  $V_{CE}$  desaturation is visible during time period P1 (yellow line). During this time, the gate-emitter voltage (green line) is kept very stable. Collector current (pink line) is also well stabilized and limited

to a safe value. At the end of period P1,  $V_{GE}$  is reduced during  $t_{FSSD1}$ . Due to collector current decrease a small  $V_{CE}$  overvoltage is seen. During  $t_{FSSD1}$   $V_{GE}$  is further reduced and the gate of the power semiconductor switch is further discharged. During  $t_{FSSD2}$  additional small  $V_{CE}$  overvoltage events may occur. Once  $V_{GE}$  drops below the gate threshold of the IGBT, the collector current has decayed almost to zero and the remaining gate charge is removed – ending the short-circuit event. The whole short-circuit current detection and safe switch-off is lower than 10  $\mu s$  (8  $\mu s$  in this example).

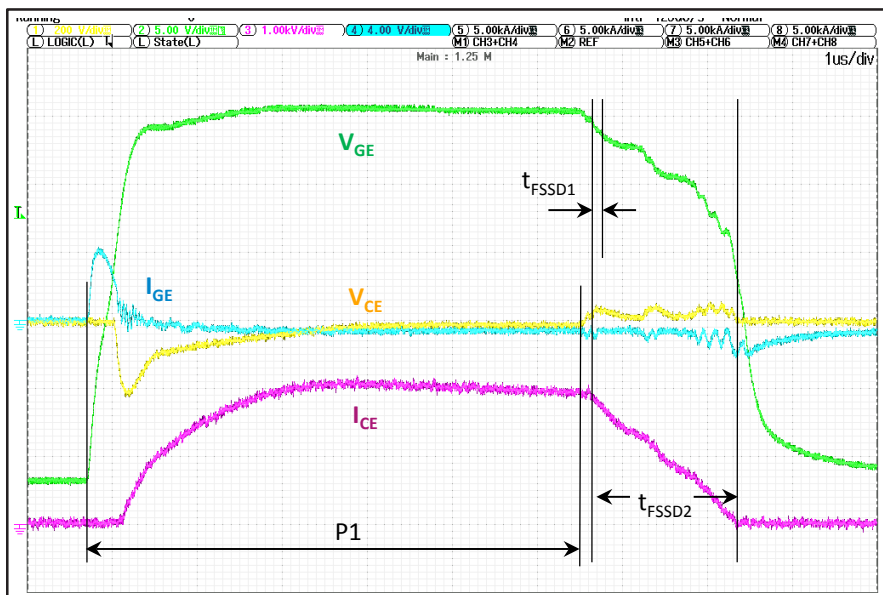


Figure 12. Advanced Soft Shut Down Function.



To avoid parasitic power-switch-conduction during system power-on, the gate is connected to COM through 22 kΩ resistor.

Figure 13 shows how switch desaturation can be measured using resistors  $R_{VCE2} - R_{VCE11}$ . In this example all the resistors have a value of 100 kΩ using 1206 package. The total resistance is 1 MΩ. The resistors should be chosen to limit current to between 0.6 mA to 0.8 mA at maximum DC-link voltage. The sum of  $R_{VCE2} - R_{VCE11}$  should be approximately 1 MΩ for 1200 V semiconductors and 500 kΩ for 600 V semiconductors. In each case the resistor string must provide sufficient creepage and clearance distances between collector of the semiconductor and SCALE-iDriver. The low leakage diode  $D_{CL}$  keeps the short-circuit duration constant over a wide DC-link voltage range.

Response time is set up through  $R_{VCE}$  and  $C_{RES}$  (typically 120 kΩ and 33 pF respectively for 1200 V semiconductors). If short-circuit detection proves to be too sensitive, the  $C_{RES}$  value can be increased. The maximum short-circuit duration must be limited to the maximum value given in the semiconductor data sheet.

Figure 14 illustrates how diodes  $D_{VCE1}$  and  $D_{VCE2}$  may be used to measure switch desaturation. For insulation, two diodes in SMD packages are used (STTH212U for example).  $R_{RES}$  connected to VISO guarantees current flow through the diodes when the semiconductor is in the on-state. When the switch desaturates,  $C_{RES}$  starts to be charged through  $R_{RES}$ . In this configuration the response time is controlled by  $R_{RES}$  and  $C_{RES}$ . In this application example  $C_{RES} = 33$  pF and  $R_{RES} = 62$  kΩ; if desaturation is too sensitive or the short-circuit duration too long, both  $C_{RES}$  and  $R_{RES}$  can be adjusted.

It is important to ensure that PCB traces do not cover the area below the desaturation resistors or diodes  $D_{VCE1}$  and  $D_{VCE2}$ . This is a critical design requirement to avoid coupling capacitance with the SCALE-iDriver's VCE pin and isolation issues within the PCB.

Gate resistors are located physically close to the power semiconductor switch. As these components can get hot, it is recommended that they are placed away from the SCALE-iDriver.

### Power Dissipation and IC Junction Temperature Estimation

First calculation in designing the power semiconductor switch gate driver stage is to calculate the required gate power -  $P_{DRV}$ . The power is calculated based on equation 1:

$$P_{DRV} = Q_{GATE} \times f_S \times V_{TOT} \quad (1)$$

where,

$Q_{GATE}$  – Controlled power semiconductor switch gate charge (derived for the particular gate potential range defined by  $V_{TOT}$ ). See semiconductor manufacturer data sheet.

$f_S$  – Switching frequency which is same as applied to the IN pin of SCALE-iDriver.

$V_{TOT}$  – SCALE-iDriver secondary-side supply voltage.

In addition to  $P_{DRV}$ ,  $P_p$  (primary-side IC power dissipation) and  $P_{SNL}$  (secondary-side IC power dissipation without capacitive load) must be considered. Both are ambient temperature and switching frequency dependent (see typical performance characteristics).

$$P_p = V_{VCC} \times I_{VCC} \quad (2)$$

$$P_{SNL} = V_{TOT} \times I_{VISO} \quad (3)$$

During IC operation, the  $P_{DRV}$  power is shared between turn-on ( $R_{GH}$ ), turn-off ( $R_{GL}$ ) external gate resistors and internal driver resistances  $R_{GHI}$  and  $R_{GLI}$ . For junction temperature estimation purposes, the dissipated power under load ( $P_{OL}$ ) inside the IC can be calculated accordingly to equation 4:

$$P_{OL} = 0.5 \times Q_{GATE} \times f_S \times V_{TOT} \times \left( \frac{R_{GHI}}{R_{GHI} + R_{GH}} + \frac{R_{GHL}}{R_{GHL} + R_{GL}} \right) \quad (4)$$

$R_{GH}$  and  $R_{GL}$  represent sum of external ( $R_{GON}$ ,  $R_{GOFF}$ ) and power semiconductor internal gate resistance ( $R_{GINT}$ ):

$$R_{GH} = R_{GON} + R_{GINT}$$

$$R_{GL} = R_{GOFF} + R_{GINT}$$

Total IC power dissipation ( $P_{DIS}$ ) is estimated as sum of equations 2, 3 and 4:

$$P_{DIS} = P_p + P_{SNL} + P_{OL} \quad (5)$$

The operating junction temperature ( $T_J$ ) for given ambient temperature ( $T_A$ ) can be estimated according to equation 6:

$$T_J = \theta_{JA} \times P_{DIS} + T_A \quad (6)$$

### Example

An example is given below,

$f_S = 20$  kHz,  $T_A = 85$  °C,  $V_{TOT} = 25$  V,  $V_{VCC} = 5$  V.

$Q_{GATE} = 2.5$  μC (the gate charge value here should correspond to selected  $V_{TOT}$ ),  $R_{GINT} = 2.5$  Ω,  $R_{GON} = R_{GOFF} = 1.8$  Ω.

$P_{DRV} = 2.5$  μC × 20 kHz × 25 V = 1.25 W, according to equation 1.

$P_p = 5$  V × 13.5 mA = 67 mW, according to equation 2 (see Figure 16).

$P_{SNL} = 25$  V × 7.5 mA = 185 mW, according to equation 3 (see Figure 17).

The dissipated power under load is:

$$P_{OL} = 0.5 \times 2.5 \mu C \times 20 \text{ kHz} \times 25 \text{ V} \times \left( \frac{1.45 \Omega}{1.45 \Omega + 4.3 \Omega} + \frac{1.2 \Omega}{1.2 \Omega + 4.3 \Omega} \right) \cong 0.3 \text{ W},$$

according to equation 4.

$R_{GHI} = 1.45$  Ω as maximum data sheet value.

$R_{GHL} = 1.2$  Ω as maximum data sheet value.

$R_{GH} = R_{GL} = 1.8$  Ω + 2.5 Ω = 4.3 Ω.

$P_{DIS} = 67$  mW + 185 mW + 300 mW = 552 mW according to equation 5.

$T_J = 67$  °C/W × 552 mW + 85 °C = 122 °C according to equation 6.

Estimated junction temperature for this design would be approximately 122 °C and is lower than the recommended maximum value. As the gate charge is not adjusted to selected  $V_{TOT}$  and internal IC resistor values are maximum values, it is understood that the example represents worst-case conditions.



Table 2 describes the recommended capacitor and resistor characteristics and layout requirements to achieve optimum performances of SCALE-iDriver.

VCE Resistor Chain				
Pin	Return Pin	Recommended Value	Symbol	Remark
Command Signal	IC <sub>1</sub>	Application specific	R <sub>1</sub>	Needed if command signals >5 V are used. For 15 V input logic a value of 3.3 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
R <sub>1</sub>	GND	Application specific	R <sub>2</sub>	Needed if command signals >5 V are used. For 15 V input logic a value of 1.2 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
SO	VCC	4.7 kΩ	R <sub>SO</sub>	Pull-up resistor, the use of 1% / 0.1 W / 50 V in 0603 package is recommended.
VCC	GND	4.7 μF	C <sub>1</sub>	VCC blocking capacitors C <sub>1</sub> must be placed close to the IC. Enlarged loop could result in inadequate VCC supply voltage during operation. For C <sub>1</sub> X7R / 25 V / 10% in a 1206 package is recommended.
VCC	GND	470 nF	C <sub>2</sub>	VCC blocking capacitors C <sub>2</sub> must be placed close to the IC. Enlarged loop could result in inadequate VCC supply voltage during operation. For C <sub>2</sub> X7R / 25 V / 10% in a 0608 package is recommended.
R <sub>1</sub>	GND	Application specific	C <sub>F</sub>	If used, the tau determines to $\tau = (R_1 \times R_2 \times C_F) / (R_1 + R_2)$ . The use of NP0, COG / 50 V / 5% in 0603 package is recommended.
R <sub>1</sub>	IN	Application specific	IC <sub>1</sub>	In case bad signal quality at the command signal input is expected, a schmitt trigger could be used to improve the signal quality at the IN pin. As a reference Nexperia 74LVC1G17-Q100 could be used.
VEE	COM	Application specific	C <sub>S1x</sub>	C <sub>S1x</sub> should be at least 3 μF multiplied by the total gate charge of the power semiconductor switch (Q <sub>GATE</sub> ) divided by 1 μC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VISO	VEE	Application specific	C <sub>S2x</sub>	C <sub>S2x</sub> should be at least 3 μF multiplied by the total gate charge of the power semiconductor switch (Q <sub>GATE</sub> ) divided by 1 μC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VCE	COM	Application specific	C <sub>RES</sub>	Short-circuit response time capacitor. 33 pF is a typical application value, higher values will increase the response time while smaller values will decrease it. To determine the correct value short-circuit testing in double pulse configuration is recommended. Furthermore the use of NP0, COG / 50 V / 5% in 0603 package is recommended. Any net and any other layer should provide sufficient distance to in order to C <sub>RES</sub> avoid parasitic effects.
VGXX	GH	10 nF	C <sub>GXX</sub>	To avoid misoperation, this pin should not be connected to anything else. This capacitor needs to be as close to IC pins as possible. The use of X7R / 25 V / 10% in 0603 package is recommended.
D <sub>CL</sub>	VCE	120 kΩ	R <sub>VCE1</sub>	Short-circuit response time resistor. The use of 1% / 0.1 W / 50 V in 0603 package is recommended. Any net and any other layer should provide sufficient distance to R <sub>VCE1</sub> in order to avoid parasitic effects.

Table 2. PCB Layout and Component Guidelines Referring to Figure 13.



Power Semiconductor Collector	$R_{VCE1}$	10 x 120 k $\Omega$	$R_{VCE2} - R_{VCE10}$	For a DC-link voltage of 800 V, the short-circuit resistor chain have a overall value of 1.2 M $\Omega$ giving a current of 0.67 mA. Other values are also possible but it has to be considered that the current through the chain shall be 0.6 to 0.8 mA. The use of 1% / 0.25 W / 200 V in 1206 package is recommended. Any net and any other layer should provide sufficient distance to $R_{VCE2} - R_{VCE10}$ in order to avoid parasitic effects.
Power Semiconductor Gate	COM	22 k $\Omega$	$R_{DIS}$	"To avoid parasitic power-switch-conduction during system power-on, the gate is connected to COM through 22 k $\Omega$ . The use of 1% / 0.1 W / 50 V in 0603 package is recommended."
VISO	Power Semiconductor Gate	Schottky Diode	$D_{STO}$	"To ensure gate voltage stabilization and collector current limitation during a short-circuit, the gate is connected to the VISO pin through the Schottky diode $D_{STO}$ . $D_{STO}$ should be connected close to capacitor $C_{S1}$ as well as the power semiconductor gate. Enlarged loop could result in increased short-circuit current. The use of Nexperia PMEG4010CEJ is recommended."
$R_{VCE1}$	VISO	Diode	$D_{CL}$	Clamping diode to the secondary-side power supply voltage. The use of Nexperia BAS416 is recommended. Any net and any other layer should provide sufficient distance to $D_{CL}$ in order to avoid parasitic effects.
Power Semiconductor Gate	GH	Application specific	$R_{GON}$	As the turn-on gate resistor can get hot, the component shall be placed away from the gate driver IC.
Power Semiconductor Gate	GL	Application specific	$R_{GOFF}$	As the turn-off gate resistor can get hot, the component shall be placed away from the gate driver IC.

Table 2 (cont). PCB Layout and Component Guidelines Referring to Figure 13.

**VCE Diode Chain**

Pin	Return Pin	Recommended Value	Symbol	Remark
Command Signal	IC <sub>1</sub>	Application specific	R <sub>1</sub>	Needed if command signals >5 V are used. For 15 V input logic a value of 3.3 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
R <sub>1</sub>	GND	Application specific	R <sub>2</sub>	Needed if command signals >5 V are used. For 15 V input logic a value of 1.2 kΩ is recommended. The use of 1% / 0.1 W / 50 V in 0603 package is recommended.
SO	VCC	4.7 kΩ	R <sub>SO</sub>	Pull up resistor, the use of 1% / 0.1 W / 50 V in 0603 package is recommended.
VCC	GND	4.7 μF	C <sub>1</sub>	VCC blocking capacitors C <sub>1</sub> must be placed close to the IC. Enlarged loop could result in inadequate VCC supply voltage during operation. For C <sub>1</sub> X7R / 25 V / 10% in a 1206 package is recommended.
VCC	GND	470 nF	C <sub>2</sub>	VCC blocking capacitors C <sub>2</sub> must be placed close to the IC. Enlarged loop could result in inadequate VCC supply voltage during operation. For C <sub>2</sub> X7R / 25 V / 10% in a 0608 package is recommended.
R <sub>1</sub>	GND	Application specific	C <sub>F</sub>	If used, the tau determines to $\tau = (R_1 \times R_2 \times C_F) / (R_1 + R_2)$ . The use of NPO, C0G / 50 V / 5% in 0603 package is recommended.
R <sub>1</sub>	IN	Application specific	IC <sub>1</sub>	In case bad signal quality at the command signal input is expected, a schmitt trigger could be used to improve the signal quality at the IN pin. As a reference Nexperia 74LVC1G17-Q100 could be used.
VEE	COM	Application specific	C <sub>S1x</sub>	C <sub>S1x</sub> should be at least 3 μF multiplied by the total gate charge of the power semiconductor switch (Q <sub>GATE</sub> ) divided by 1 μC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VISO	VEE	Application specific	C <sub>S2x</sub>	C <sub>S2x</sub> should be at least 3 μF multiplied by the total gate charge of the power semiconductor switch (Q <sub>GATE</sub> ) divided by 1 μC. The use of X7R / 25 V / 10% in 1206 package is recommended. This capacitor needs to be placed close to the IC pins.
VCE	COM	Application specific	C <sub>RES</sub>	Short-circuit response time capacitor. 33 pF is a typical application value, higher values will increase the response time while smaller values will decrease it. It can be adjusted in the range 33 pF to 330 pF. To determine the correct value short-circuit testing in double pulse configuration is recommended. Furthermore the use of NPO, C0G / 50 V / 5% in 0603 package is recommended. Any net and any other layer should provide sufficient distance to in order to C <sub>RES</sub> avoid parasitic effects.
VGXX	GH	10 nF	C <sub>GXX</sub>	To avoid misoperation, this pin should not be connected to anything else. This capacitor needs to be as close to IC pins as possible. The use of X7R / 25 V / 10% in 0603 package is recommended.
D <sub>VCE2</sub>	VCE	330 Ω	R <sub>VCE</sub>	The use of 1% / 0.1 W / 50 V in 0603 package is recommended. Any net and any other layer should provide sufficient distance to R <sub>VCE</sub> in order to avoid parasitic effects.

Table 3. PCB Layout and Component Guidelines Referring to Figure 14.

VCE	VISO	Application specific	$R_{RES}$	This resistor in combination with $C_{RES}$ sets the short-circuit response time. It can be adjusted in the range from 24 k $\Omega$ to 62 k $\Omega$ . The use of 1% / 0.1 W / 50 V in 0603 package is recommended. Any net and any other layer should provide sufficient distance to $R_{RES}$ in order to avoid parasitic effects.
Power Semiconductor Gate	COM	22 k $\Omega$	$R_{DIS}$	"To avoid parasitic power-switch-conduction during system power-on, the gate is connected to COM through 22 k $\Omega$ . The use of 1% / 0.1 W / 50 V in 0603 package is recommended."
Power Semiconductor Collector	$R_{RES}$	Application specific	$D_{VCE1}/D_{VCE2}$	High-voltage diodes for the short-circuit detection. Creepage and clearance distances need to be considered. STTH212U or comparable could be used. Any net and any other layer should provide sufficient distance to $D_{VCE1}$ and $D_{VCE2}$ in order to avoid parasitic effects.
VISO	Power Semiconductor Gate	Schottky Diode	$D_{STO}$	"To ensure gate voltage stabilization and collector current limitation during a short-circuit, the gate is connected to the VISO pin through the Schottky diode $D_{STO}$ . $D_{STO}$ should be connected close to capacitor $C_{S1}$ as well as the power semiconductor gate. Enlarged loop could result in increased short-circuit current. The use of Nexperia PMEG4010CEJ is recommended."
$R_{VCE1}$	VISO	Diode	$D_{CL}$	Clamping diode to the secondary-side power supply voltage. The use of Nexperia BAS416 is recommended. Any net and any other layer should provide sufficient distance to $D_{CL}$ in order to avoid parasitic effects.
Power Semiconductor Gate	GH	Application specific	$R_{GON}$	As the turn on gate resistor can get hot, the component shall be placed away from the gate driver IC.
Power Semiconductor Gate	GL	Application specific	$R_{GOFF}$	As the turn off gate resistor can get hot, the component shall be placed away from the gate driver IC.

Table 3 (cont). PCB Layout and Component Guidelines Referring to Figure 14.

Parameter	Symbol	Conditions	Min	Max	Units
<b>Absolute Maximum Ratings<sup>1</sup></b>					
Primary-Side Supply Voltage <sup>2</sup>	$V_{VCC}$	VCC to GND	-0.5	6.5	V
Secondary-Side Total Supply Voltage	$V_{TOT}$	VISO to COM	-0.5	30	V
Secondary-Side Positive Supply Voltage	$V_{VISO}$	VISO to VEE	-0.5	17.5	V
Secondary-Side Negative Supply Voltage	$V_{VEE}$	VEE to COM	-0.5	15	V
Logic Input Voltage (command signal)	$V_{IN}$	IN to GND	-0.5	$V_{VCC} + 0.5$	V
Logic Output Voltage (fault signal)	$V_{SO}$	SO to GND	-0.5	$V_{VCC} + 0.5$	V
Logic Output Current (fault signal)	$I_{SO}$	Positive Current Flowing into the Pin		10	mA
VCE Pin Voltage	$V_{VCE}$	VCE – COM	-0.5	$V_{TOT} + 0.5$	V
Switching Frequency	$f_s$			75	kHz
Storage Temperature	$T_s$		-65	150	°C
Operating Junction Temperature	$T_j$		-40	150 <sup>3</sup>	°C
Operating Ambient Temperature	$T_A$		-40	125	°C
Operating Case Temperature	$T_C$		-40	125	°C
Input Power Dissipation <sup>4</sup>	$P_p$	$V_{VCC} = 5\text{ V}, V_{TOT} = 28\text{ V},$ $T_A = 25\text{ °C}$ $f_s = 75\text{ kHz}$		115	mW
Output Power Dissipation <sup>4</sup>	$P_s$			1675	
Total IC Power Dissipation <sup>4</sup>	$P_{DJS}$			1790	

**NOTES:**

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Defined as peak voltage measured directly on VCC pin.
3. Transmission of command signals could be affected by PCB layout parasitic inductances at junction temperatures higher than recommended.
4. Input Power Dissipation refers to equation 2. Output Power Dissipation is secondary-side IC power dissipation without capacitive load ( $P_{SNL}$ , equation 3) and dissipated power under load ( $P_{OL}$ , equation 4). Total IC power dissipation is sum of  $P_p$  and  $P_s$ .

**Thermal Resistance**

Thermal Resistance: eSOP-R16B Package:

$(\theta_{JA})$  ..... 67 °C/W<sup>1</sup>  
 $(\theta_{JC})$  ..... 34 °C/W<sup>2</sup>

Notes:

1. 2 oz. (610 g/m<sup>2</sup>) copper clad.
2. The case temperature is measured at the plastic surface at the top of the package.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		$T_j = -40\text{ °C to }+125\text{ °C}$ See Note 1 (Unless Otherwise Specified)					
<b>Recommended Operation Conditions</b>							
Primary-Side Supply Voltage	$V_{VCC}$	VCC – GND		4.75		5.25	V
Secondary-Side Total Supply Voltage	$V_{TOT}$	VISO – COM		22		28	V
Logic Low Input Voltage	$V_{IL}$					0.5	V
Logic High Input Voltage	$V_{IH}$			3.3			V
Switching Frequency	$f_s$			0		75	kHz
Operating IC Junction Temperature	$T_j$			-40		125	°C
<b>Electrical Characteristics</b>							
Logic Low Input Threshold Voltage	$V_{IN+LT}$	$f_s = 0\text{ Hz}$		0.6	1.25	1.8	V
Logic High Input Threshold Voltage	$V_{IN+HT}$	$f_s = 0\text{ Hz}$		1.7	2.2	3.05	V
Logic Input Voltage Hysteresis	$V_{IN+HS}$	$f_s = 0\text{ Hz}$		0.1			V
Input Bias Current	$I_{IN}$	$V_{IN} = 5\text{ V}$		56	113	165	$\mu\text{A}$
		$V_{IN} > 3\text{ V}$ See Note 12			106		
Supply Current (Primary-Side)	$I_{VCC}$	$V_{IN} = 0\text{ V}$		4	11	17	mA
		$V_{IN} = 5\text{ V}$			16	23	
		$f_s = 20\text{ kHz}$			14.5	20	
		$f_s = 75\text{ kHz}$			16.3	23	
Supply Current (Secondary-Side)	$I_{VISO}$	$V_{IN} = 0\text{ V}$			6	8	mA
		$V_{IN} = 5\text{ V}$			7	9	
		$f_s = 20\text{ kHz}$			7.4	10	
		$f_s = 75\text{ kHz}$			10.3	14	
Power Supply Monitoring Threshold (Primary-Side)	UVLO <sub>VCC</sub>	Clear Fault			4.28	4.65	V
		Set Fault		3.85	4.12		
		Hysteresis, See Notes 3, 4		0.02			
Power Supply Monitoring Threshold (Secondary-Side, Positive Rail $V_{VISO}$ )	UVLO <sub>VISO</sub>	Clear Fault			12.85	13.5	V
		Set Fault, Note 3		11.7	12.35		
		Hysteresis		0.3			
Power Supply Monitoring Blanking Time, $V_{VISO}$	UVLO <sub>VISO(BL)</sub>	Voltage Drop 13.5 V to 11.5 V See Note 12		0.5			$\mu\text{s}$
Power Supply Monitoring Threshold (Secondary-Side, Negative Rail $V_{VEE}$ )	UVLO <sub>VEE</sub>	Clear Fault, $V_{TOT} = 20\text{ V}$			5.15	5.5	V
		Set Fault, $V_{TOT} = 20\text{ V}$		4.67	4.93		
		Hysteresis		0.1			

Parameter	Symbol	Conditions		Min	Typ	Max	Units	
		$T_J = -40\text{ °C to }+125\text{ °C}$ See Note 1 (Unless Otherwise Specified)						
<b>Electrical Characteristics (cont.)</b>								
<b>Power Supply Monitoring Blanking Time, <math>V_{VEE}</math></b>	$UVLO_{VEE(BL)}$	Voltage Drop 5.5 V to 4.5 V See Note 12		0.5			$\mu\text{S}$	
<b>Secondary-Side Positive Supply Voltage Regulation</b>	$V_{VISO(HS)}$	$21\text{ V} \leq V_{TOT} \leq 30\text{ V}$ , $ i(V_{VEE})  \leq 1.5\text{ mA}$		14.4	15.07	15.75	V	
<b>VEE Source Capability</b>	$I_{VEE(SO)}$	$V_{TOT} = 15\text{ V}$ , $V_{VEE}$ set to 0 V		0.1			mA	
		$V_{TOT} = 25\text{ V}$ , $V_{VEE}$ set to 7.5 V See Note 13		1.85	3.3	4.5		
<b>VEE Sink Capability</b>	$I_{VEE(SI)}$	$V_{TOT} = 25\text{ V}$ , $V_{VEE}$ set to 12.5 V See Note 13		1.74	3.1	4.5	mA	
<b>DESAT Detection Level</b>	$V_{DES}$	VCE-VEE, $V_{IN} = 5\text{ V}$		7.2	7.8	8.3	V	
<b>DESAT Sink Current</b>	$I_{DES}$	$V_{VCE} = 10\text{ V}$ , $V_{IN} = 0\text{ V}$		15	28	50	mA	
<b>DESAT Bias Current</b>	$I_{DES(BS)}$	$V_{VCE} - V_{VEE} = 4.5\text{ V}$ , $V_{IN} = 5\text{ V}$		-0.5		3	$\mu\text{A}$	
<b>VCE Pin Capacitance</b>	$C_{VCE}$	Between VCE and COM pins, See Note 12				12.5	pF	
<b>Turn-On Propagation Delay</b>	$t_{P(LH)}$	$T_J = 25\text{ °C}$ , See Note 5		180	253	340	ns	
		$T_J = 125\text{ °C}$ , See Note 5		210	278	364		
<b>Turn-Off Propagation Delay</b>	$t_{P(HL)}$	$T_J = 25\text{ °C}$ , See Note 6		200	262	330	ns	
		$T_J = 125\text{ °C}$ , See Note 6		211	287	359		
<b>Minimum Turn-On and Off Pulses</b>	$t_{GE(MIN)}$	See Note 12				650	ns	
<b>Output Rise Time</b>	$t_R$	No $C_G$ , See Note 7			22	45	ns	
		$C_G = 10\text{ nF}$ , See Note 7	SID1151K See Note 12					225
			SID1181K		55	90		150
		$C_G = 47\text{ nF}$ , See Note 7	SID1151K See Note 12					975
SID1181K			300	465	650			
<b>Output Fall Time</b>	$t_F$	No $C_G$ , See Note 8			18	45	ns	
		$C_G = 10\text{ nF}$ , See Note 8	SID1151K See Note 12					225
			SID1181K		40	81		150
		$C_G = 47\text{ nF}$ , See Note 8	SID1151K See Note 12					975
SID1181K			300	460	650			

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		$T_J = -40\text{ }^\circ\text{C to }+125\text{ }^\circ\text{C}$ See Note 1 (Unless Otherwise Specified)					
<b>Electrical Characteristics (cont.)</b>							
ASSD Rate of Change	$t_{\text{FSSD1}}$	VGE change from 14.5 V to 14 V, See Note 12			60		ns
	$t_{\text{FSSD2}}$	VGE change from 14.5 V to 2.5 V, See Note 12		950	1828	2800	
Propagation Delay Jitter		See Note 12			$\pm 5$		ns
Fault Signalization Delay Time	$t_{\text{FAULT}}$	See Note 10			190	750	ns
SO Fault Signalization time	$t_{\text{SO}}$			6.8	10	13.4	$\mu\text{s}$
Power-On Start-Up Time	$t_{\text{START}}$	See Note 11				10	ms
Gate Sourcing Peak Current GH Pin	$I_{\text{GH}}$	$V_{\text{GH}} \geq V_{\text{TOT}} - 8.8\text{ V}$ $C_{\text{G}} = 470\text{ nF}$ See Note 13	SID1151K See Note 12	2.4			A
			SID1181K	3.6	4.6	5.5	
		$R_{\text{G}} = 0, C_{\text{G}} = 47\text{ nF}$ See Notes 2, 12, 13	SID1151K		4.8		
			SID1181K		7.3		
Gate Sinking Peak Current GL Pin	$I_{\text{GL}}$	$V_{\text{GL}} \leq 7.5\text{ V}$ $C_{\text{G}} = 470\text{ nF}$ $V_{\text{GL}}$ is Referenced to COM	SID1151K See Note 12	2.6			A
			SID1181K	4	4.8	5.5	
		$R_{\text{G}} = 0, C_{\text{G}} = 47\text{ nF}$ See Notes 2, 12	SID1151K		5.2		
			SID1181K		7.8		
Turn-On Internal Gate Resistance	$R_{\text{GHI}}$	$I(\text{GH}) = -250\text{ mA}$ $V_{\text{IN}} = 5\text{ V}$	SID1151K See Note 12			2.4	$\Omega$
			SID1181K		0.76	1.2	
Turn-Off Internal Gate Resistance	$R_{\text{GLI}}$	$I(\text{GL}) = 250\text{ mA}$ $V_{\text{IN}} = 0\text{ V}$	SID1151K See Note 12			2	$\Omega$
			SID1181K		0.68	1.1	
Turn-On Gate Output Voltage	$V_{\text{GH(ON)}}$	$I(\text{GH}) = 10\text{ mA}$ $V_{\text{IN}} = 5\text{ V}$ , See Note 13	SID1151K See Note 12	$V_{\text{TOT}} - 0.04$			V
			SID1181K				
Turn-Off Gate Output Voltage (Referred to COM Pin)	$V_{\text{GL(OFF)}}$	$I(\text{GL}) = -10\text{ mA}$ $V_{\text{IN}} = 0\text{ V}$	SID1151K See Note 12			0.04	V
			SID1181K				
SO Output Voltage	$V_{\text{SO(FAULT)}}$	Fault Condition, $I_{\text{SO}} = 3.4\text{ mA}$ , $V_{\text{VCC}} \geq 3.9\text{ V}$			210	450	mV



Parameter	Symbol	Conditions	Min	Typ	Max	Units
		$T_J = -40\text{ °C to }+125\text{ °C}$ See Note 1 (Unless Otherwise Specified)				
<b>Package Characteristics (See Notes 12, 14)</b>						
<b>Distance Through the Insulation</b>	DTI	Minimum Internal Gap (Internal Clearance)	0.4			mm
<b>Minimum Air Gap (Clearance)</b>	L1 (IO1)	Shortest Terminal-to-Terminal Distance Through Air	9.5			mm
<b>Minimum External Tracking (Creepage)</b>	L2 (IO2)	Shortest Terminal-to-Terminal Distance Across the Package Surface	9.5			mm
<b>Tracking Resistance (Comparative Tracking Index)</b>	CTI	DIN EN 60112 (VDE 0303-11): 2010-05 EN / IEC 60112:2003 + A1:2009	600			
<b>Isolation Resistance, Input to Output</b> See Note 16	$R_{IO}$	$V_{IO} = 500\text{ V}, T_J = 25\text{ °C}$	$10^{12}$			$\Omega$
		$V_{IO} = 500\text{ V}, 100\text{ °C} \leq T_J \leq T_{C(MAX)}$	$10^{11}$			
<b>Isolation Capacitance, Input to Output</b> See Note 16	$C_{IO}$			1		pF
<b>Package Insulation Characteristics</b>						
<b>Maximum Working Isolation Voltage</b>	$V_{IOWM}$				849	$V_{RMS}$
<b>Maximum Repetitive Peak Isolation Voltage</b>	$V_{IORM}$				1200	$V_{PEAK}$
<b>Input to Output Test Voltage</b>	$V_{PD}$	Method A, After Environmental Tests Subgroup 1, $V_{PR} = 1.3 \times V_{IORM}$ , $t = 10\text{ s}$ (qualification) Partial Discharge < 5 pC			1560	$V_{PEAK}$
		Method A, After Input/Output Safety Test Subgroup 2/3, $V_{PR} = 1.2 \times V_{IORM}$ , $t = 10\text{ s}$ , (qualification) Partial Discharge < 5 pC			1440	
		Method B1, 100% Production Test, $V_{PR} = 1.5 \times V_{IORM}$ , $t = 1\text{ s}$ Partial Discharge < 5 pC			1800	
<b>Maximum Transient Isolation Voltage</b>	$V_{IOTM}$	$V_{TEST} = V_{IOTM}$ , $t = 60\text{ s}$ (qualification), $t = 1\text{ s}$ (100% production)			6000	$V_{PEAK}$
<b>Maximum Surge Isolation Voltage</b>	$V_{IOSM}$	Test Method Per IEC 60065, 1.2/50 $\mu\text{s}$ Waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 9600\text{ V}$ (qualification)			6000	$V_{PEAK}$
<b>Insulation Resistance</b>	$R_S$	$V_{IO} = 500\text{ V}$ at $T_S$			$>10^9$	$\Omega$
<b>Maximum Case Temperature</b>	$T_S$				150	$^{\circ}\text{C}$
<b>Safety Total Dissipated Power</b>	$P_S$	$T_A = 25\text{ °C}$			1.79	W
<b>Pollution Degree</b>				2		
<b>Climatic Classification</b>				40/125/21		
<b>Withstanding Isolation Voltage</b>	$V_{ISO}$	$V_{TEST} = V_{ISO}$ , $t = 60\text{ s}$ (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\text{ V}_{RMS}$ , $t = 1\text{ s}$ (100% production)		5000		$V_{RMS}$

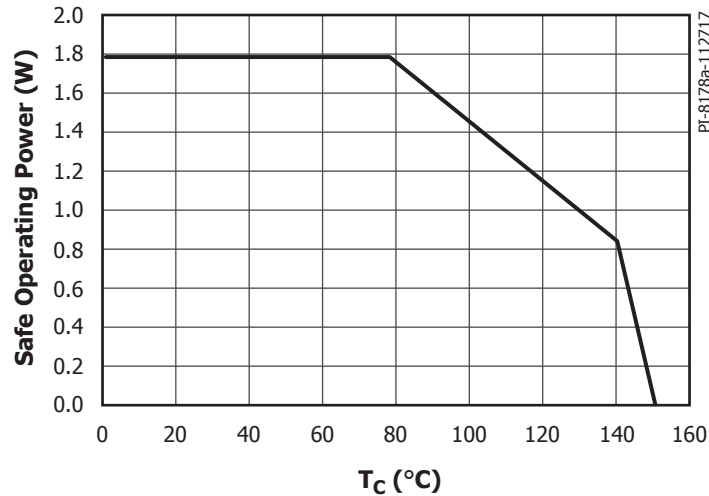


Figure 15. Thermal Derating Curve Showing Dependence of Limited Dissipated Power on Case Temperature (DIN V VDE V 0884-10).

Continuous device operating is allowed until  $T_J$  and/or  $T_C$  of 125 °C are reached. Thermal stress beyond those values but below thermal derating curve may lead to permanent functional product damage. Operating beyond thermal SR derating curve may affect product reliability.

NOTES:

1.  $V_{VCC} = 5\text{ V}$ ,  $V_{TOT} = 25\text{ V}$ ; GH and GL pins are shorted together.  $R_G = 4\ \Omega$ , No  $C_G$ ; VCC pin is connected to the SO pin through a 2 k $\Omega$  resistor. The VGXX pin is connected to the GH pin through a 10 nF capacitor. Typical values are defined at  $T_A = 25\text{ °C}$ ;  $f_s = 20\text{ kHz}$ , Duty Cycle = 50%. Positive currents are assumed to be flowing into pins.
2. Pulse width  $\leq 10\ \mu\text{s}$ , duty cycle  $\leq 1\%$ . The maximum value is controlled by the ASIC to a safe level. There is no need to limit the current by the application. The internal peak power is safely controlled for  $R_G \geq 0$  and power semiconductor module input gate capacitance  $C_{IES} \leq 47\text{ nF}$ .
3. During very slow  $V_{VCC}$  power-up and power-down related to  $V_{TOT}$ ,  $V_{VCC}$  and  $V_{VEE}$  respectively, several SO fault pulses may be generated.
4. SO pin connected to GND as long as  $V_{VCC}$  stays below minimum value. No signal transferred from primary to secondary-side.
5.  $V_{IN}$  potential changes from 0 V to 5 V within 10 ns. Delay is measured from 50% voltage increase on IN pin to 10% voltage increase on GH pin.
6.  $V_{IN}$  potential changes from 5 V to 0 V within 10 ns. Delay is measured from 50% voltage decrease on IN pin to 10% voltage decrease on GL pin.
7. Measured from 10% to 90% of  $V_{GE}$  ( $C_G$  simulates semiconductor gate capacitance). The  $V_{GE}$  is measured across  $C_G$ .
8. Measured from 90% to 10% of  $V_{GE}$  ( $C_G$  simulates semiconductor gate capacitance). The  $V_{GE}$  is measured across  $C_G$ .
9. ASSD function limits G-E voltage of controlled semiconductor in specified time. Conditions:  $C_G = 10\text{ nF}$ ,  $V_{TOT} = V_{VISO} = 15\text{ V}$ ,  $V_{VEE} = 0\text{ V}$  (VEE shorted to COM).
10. The amount of time needed to transfer fault event (UVLO or DESAT) from secondary-side to SO pin.
11. The amount of time after primary and secondary-side supply voltages ( $V_{VCC}$  and  $V_{TOT}$ ) reach minimal required level for driver proper operation. No signal is transferred from primary to secondary-side during that time, and no fault condition will be transferred from the secondary-side to the primary-side.
12. Guaranteed by design.
13. Positive current is flowing out of the pin.
14. Safety distances are application dependent and the creepage and clearance requirements should follow specific equipment isolation standards of an application. Board design should ensure that the soldering pads of an IC maintain required safety relevant distances.
15. Measured accordingly to IEC 61000-4-8 ( $f_s = 50\text{ Hz}$ , and 60 Hz) and IEC 61000-4-9.
16. All pins on each side of the barrier tied together creating a two-terminal device.

Typical Performance Characteristics

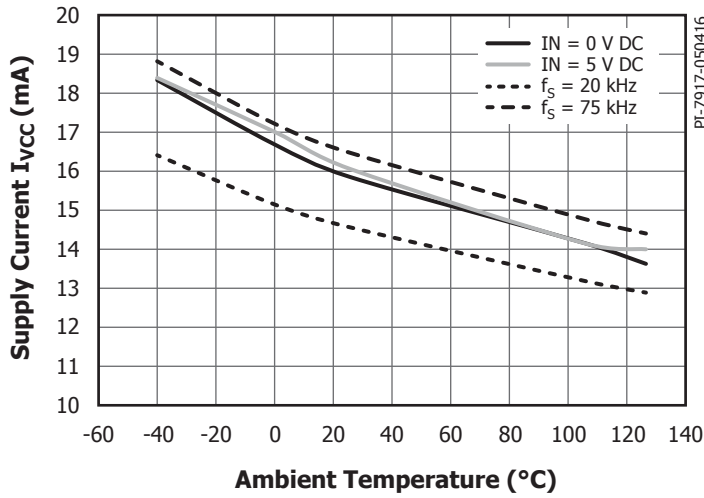


Figure 16. Supply Current Primary-Side  $I_{VCC}$  vs. Ambient Temperature. Conditions:  $V_{VCC} = 5\text{ V}$ ,  $V_{TOT} = 25\text{ V}$ , No-Load.

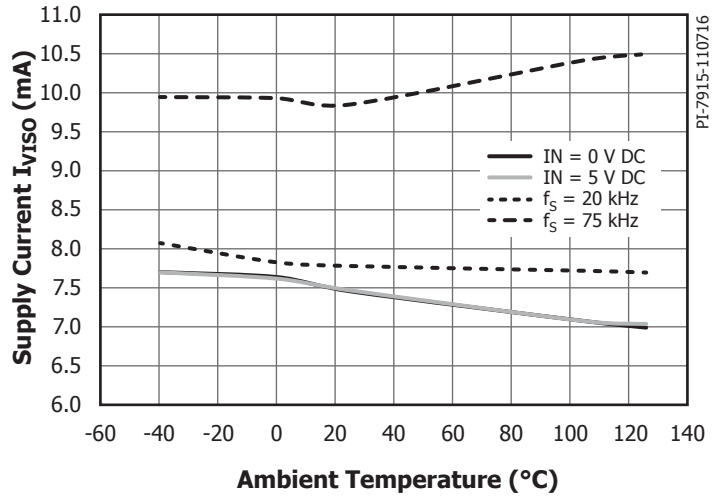


Figure 17. Supply Current Secondary-Side  $I_{VISO}$  vs. Ambient Temperature. Conditions:  $V_{VCC} = 5\text{ V}$ ,  $V_{TOT} = 25\text{ V}$ , No-Load.

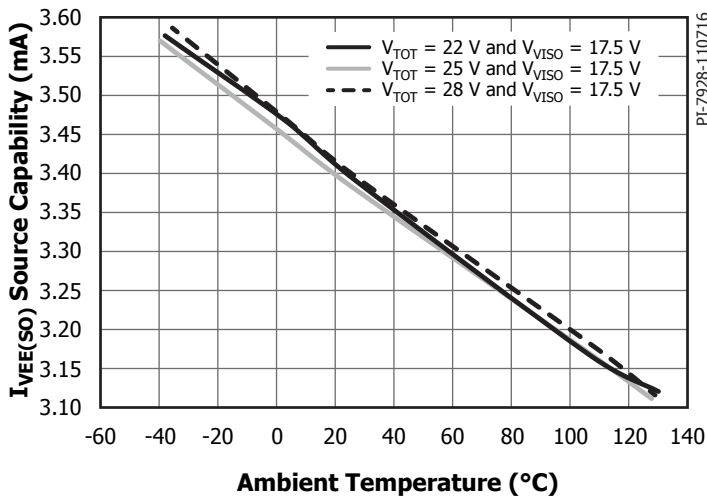


Figure 18. VEE Source Capability  $I_{VEE(SO)}$  vs. Ambient Temperature and  $V_{VISO}$ . Conditions:  $V_{VCC} = 5\text{ V}$ ,  $f_S = 20\text{ kHz}$ , Duty Cycle = 50%.

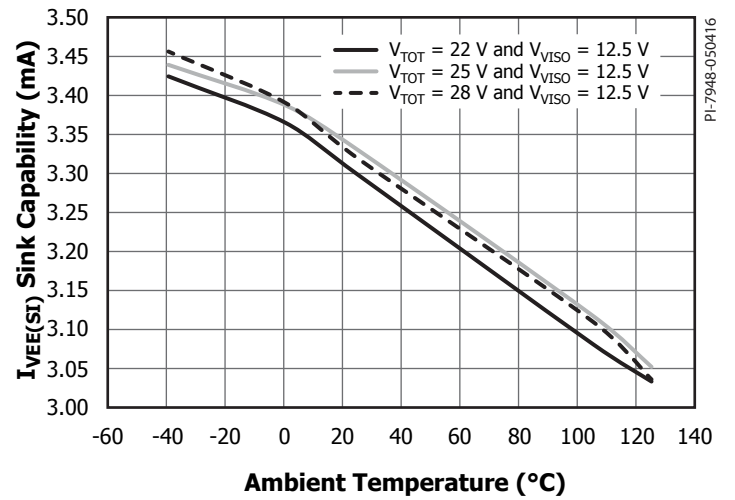
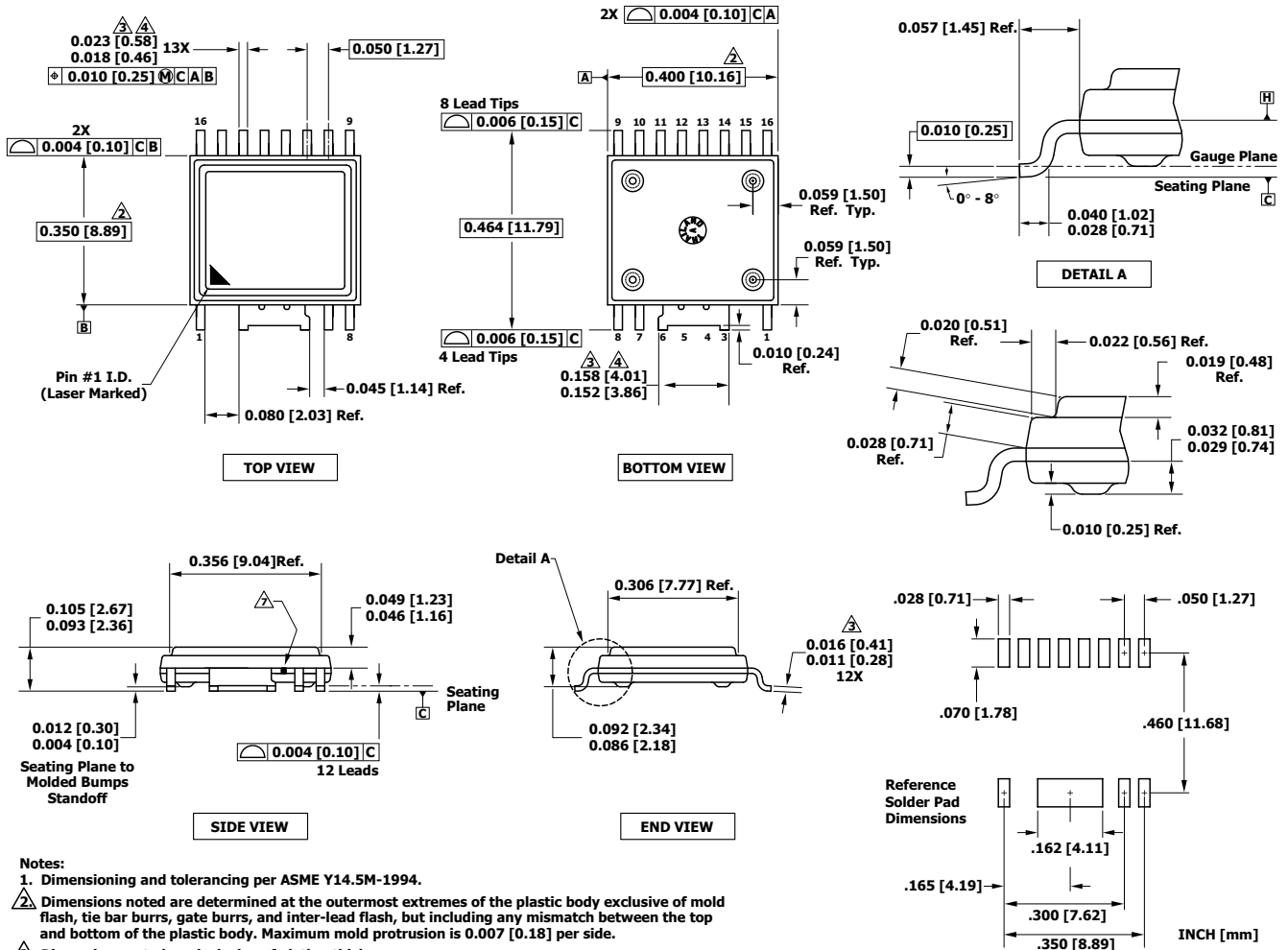


Figure 19. VEE Sink Capability  $I_{VEE(SI)}$  vs. Ambient Temperature and  $V_{VISO}$ . Conditions:  $V_{VCC} = 5\text{ V}$ ,  $f_S = 20\text{ kHz}$ , Duty Cycle = 50%.

eSOP-R16B



Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined in Datum H.
7. Exposed metal at the plastic package body outline/surface between leads 6 and 7, connected internally to wide lead 3/4/5/6.

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## MSL Table

Part Number	MSL Rating
SID11x1K	3

## ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > $1.5 \times V_{MAX}$ on all pins
Human Body Model ESD	JESD22-A114F	> ±2000 V on all pins
Charged Device Model ESD	JESD22-C101	> ±500 V on all pins

## IEC 60664-1 Rating Table

Parameter	Conditions	Specifications
Basic Isolation Group	Material Group	I
Installation Classification	Rated mains voltage $\leq 150 V_{RMS}$	I - IV
	Rated mains voltage $\leq 300 V_{RMS}$	I - IV
	Rated mains voltage $\leq 600 V_{RMS}$	I - III
	Rated mains voltage $\leq 1000 V_{RMS}$	I - II

## Electrical Characteristics (EMI) Table

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Common-Mode Transient Immunity, Logic High</b>	$CM_H$	Typical values measured according to Figures 33, 34. Maximum values are design values assuming trapezoid waveforms		-35 / 50	-100 / 100	kV/ $\mu$ s
<b>Common-Mode Transient Immunity, Logic Low</b>	$CM_L$	Typical values measured according to Figures 33, 34. Maximum values are design values assuming trapezoid waveforms		-35 / 50	-100 / 100	kV/ $\mu$ s
<b>Variable Magnetic Field Immunity</b>	$H_{HPEAK}$	See Note 15		1000		A/m
	$H_{LPEAK}$	See Note 15		1000		

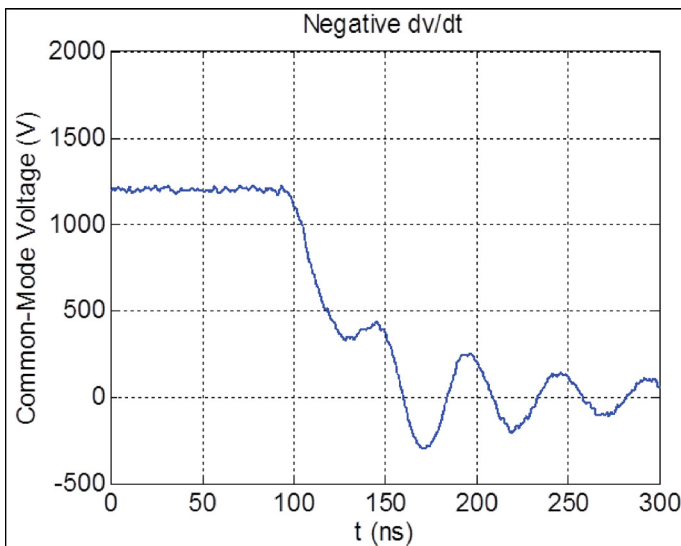


Figure 20. Applied Common Mode Pulses for Generating Negative dv/dt.

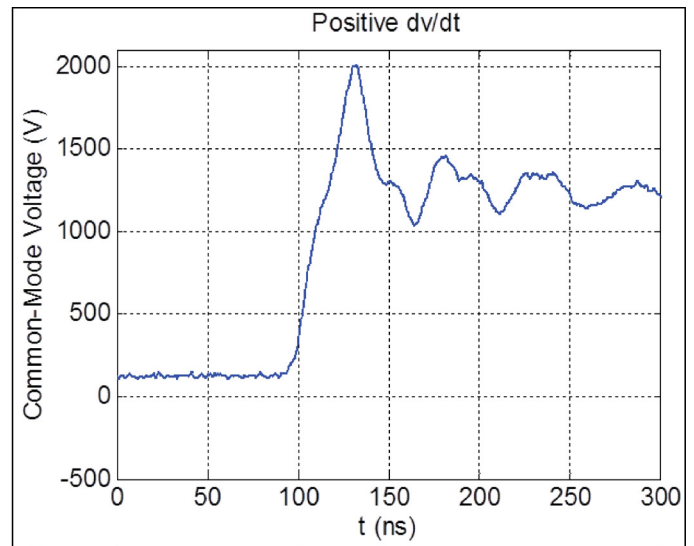
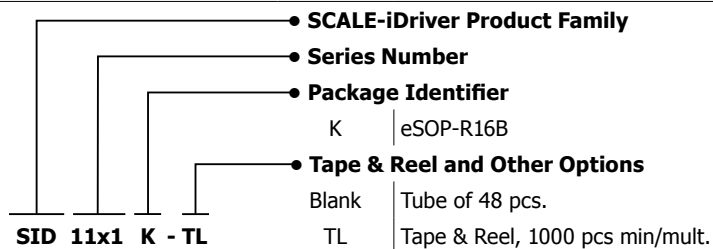


Figure 21. Applied Common Mode Pulses for Generating Positive dv/dt.

**Regulatory Information Table**

VDE	UL	CSA
Certified to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12	UR recognition under UL1577 Component Recognition Program pending	UR recognition to CSA Component Acceptance Notice 5A pending
Reinforced insulation for Max. Transient Isolation voltage 6 kV <sub>PEAK</sub> Max. Surge Isolation voltage 6 kV <sub>PEAK</sub> Max. Repetitive Peak Isolation voltage 1200 V <sub>PEAK</sub>	Single protection, 5000 V <sub>RMS</sub> dielectric voltage withstand	Single protection, 5000 V <sub>RMS</sub> dielectric voltage withstand
File No. 40048140	File No. E358471	File No. E358471

**Part Ordering Information**



Revision	Notes	Date
A	Code A initial release.	04/18
B	Updated with UL approval information in Regulatory Information table on page 21.	05/18

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