

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS E6

650V CoolMOS™ E6 Power Transistor
IPx65R380E6

Data Sheet

Rev. 2.0, 2010-01-02
Final

Industrial & Multimarket

650V CoolMOS™ E6 Power Transistor

IPD65R380E6, IPP65R380E6
IPA65R380E6

1 Description

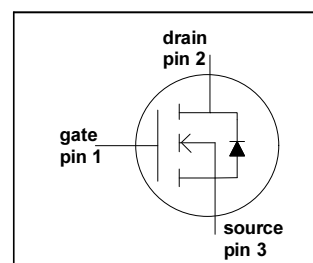
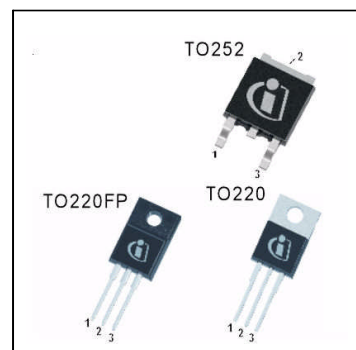
CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ E6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter, and cooler.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- JEDEC¹⁾ qualified, Pb-free plating, Halogen free²⁾

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.



Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	0.38	Ω
$Q_{g,typ}$	39	nC
$I_{D,pulse}$	29	A
$E_{oss} @ 400V$	2.8	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPD65R380E6	PG-TO252	65E6380	IFX CoolMOS Webpage IFX Design tools
IPP65R380E6	PG-TO220		
IPA65R380E6	PG-TO220 FullPAK		

1) J-STD20 and JESD22

2) except of PG-To252

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	10.6	A	$T_C = 25\text{ °C}$
				6.7		$T_C = 100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	29	A	$T_C = 25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	215	mJ	$I_D = 1.8\text{ A}, V_{DD} = 50\text{ V}$ (see table 21)
Avalanche energy, repetitive	E_{AR}	-	-	0.32		$I_D = 1.8\text{ A}, V_{DD} = 50\text{ V}$
Avalanche current, repetitive	I_{AR}	-	-	1.8	A	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 480\text{ V}$
Gate source voltage	V_{GS}	-20	-	20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation for Non FullPAK	P_{tot}	-	-	83	W	$T_C = 25\text{ °C}$
Power dissipation for FullPAK	P_{tot}	-	-	31	W	$T_C = 25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	
Mounting torque TO-220		-	-	60	Ncm	M3 and M3.5 screws
Mounting torque TO-220 FullPAK				50		M2.5 screws
Continuous diode forward current	I_S	-	-	9.2	A	$T_C = 25\text{ °C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	29	A	$T_C = 25\text{ °C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 480\text{ V}, I_{SD} \leq I_D$, $T_j = 125\text{ °C}$ (see table 22)
Maximum diode commutation speed ³⁾	di/dt			500	A/μs	

1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$

2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics TO-220

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	leded
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 4 Thermal characteristics TO-220FullPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.0	°C/W	leded
Thermal resistance, junction - ambient	R_{thJA}	-	-	80		
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

Table 5 Thermal characteristics TO-252

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	°C/W	SMD version, device on PCB, minimal footprint
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		
		-	35	-		SMD version, device on PCB, 6cm ² cooling area ¹⁾
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

1) Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1.0\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}$, $I_D=0.32\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
		-	10	-		$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.34	0.38	Ω	$V_{GS}=10\text{ V}$, $I_D=3.2\text{ A}$, $T_j=25\text{ °C}$
		-	0.89	-		$V_{GS}=10\text{ V}$, $I_D=3.2\text{ A}$, $T_j=150\text{ °C}$
Gate resistance	R_G	-	7.5	-	Ω	$f=1\text{ MHz}$, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	710	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	41	-		
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	32	-		$V_{GS}=0\text{ V}$, $V_{DS}=0\dots480\text{ V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	140	-		$I_D=\text{constant}$, $V_{GS}=0\text{ V}$ $V_{DS}=0\dots480\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400\text{ V}$, $V_{GS}=13\text{ V}$, $I_D=4.9\text{ A}$, $R_G=3.4\text{ }\Omega$ (see table 20)
Rise time	t_r	-	7	-		
Turn-off delay time	$t_{d(off)}$	-	57	-		
Fall time	t_f	-	8	-		

1) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

2) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IGate to source charge	Q_{gs}	-	4	-	nC	$V_{DD}=480\text{ V}$, $I_D=4.9\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	20	-		
Gate charge total	Q_g	-	39	-		
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0\text{ V}$, $I_F=4.9\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	280	-	ns	$V_R=400\text{ V}$, $I_F=4.9\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ (see table 22)
Reverse recovery charge	Q_{rr}	-	2.8	-	μC	
Peak reverse recovery current	I_{rrm}	-	17	-	A	

5 Electrical characteristics diagrams

Table 10

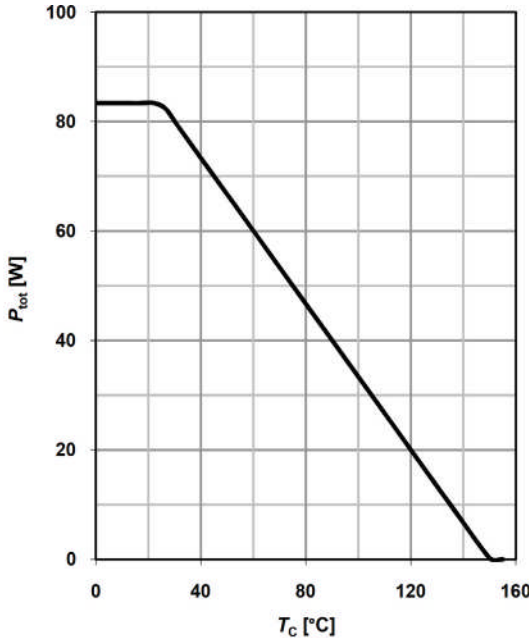
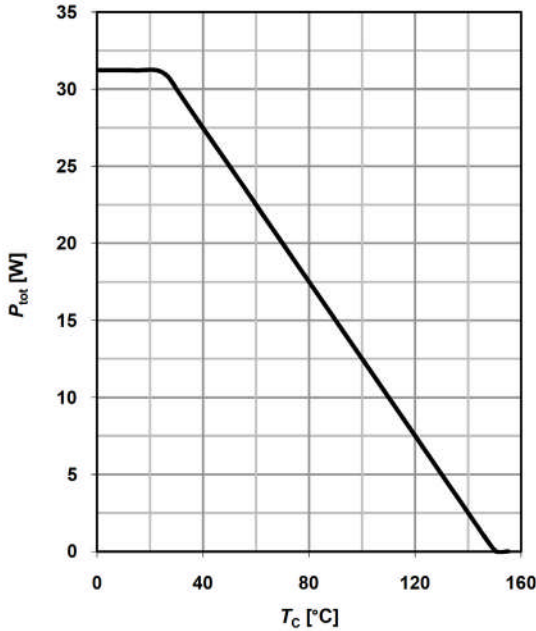
Power dissipation Non FullPAK	Power dissipation FullPAK
	
$P_{\text{tot}} = f(T_c)$	$P_{\text{tot}} = f(T_c)$

Table 11

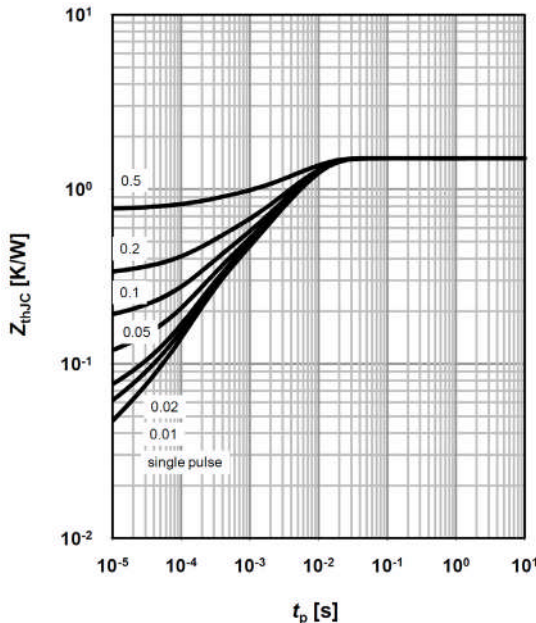
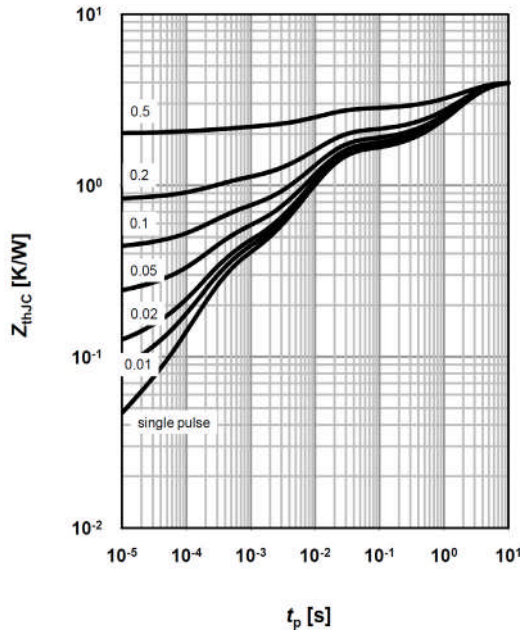
Max. transient thermal impedance Non FullPAK	Max. transient thermal impedance FullPAK
	
$Z_{(\text{thJC})} = f(t_p)$; parameter: $D = t_p / T$	$Z_{(\text{thJC})} = f(t_p)$; parameter: $D = t_p / T$

Table 12

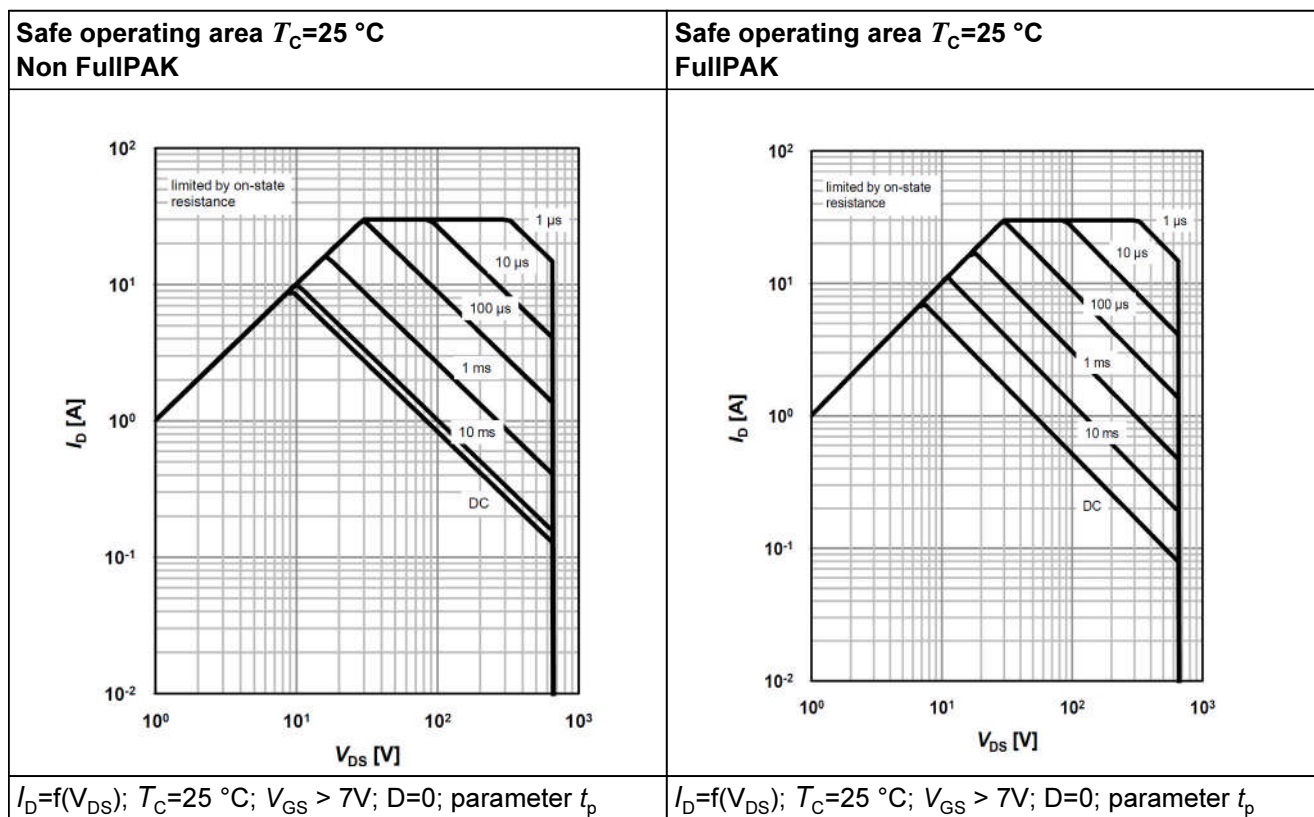


Table 13

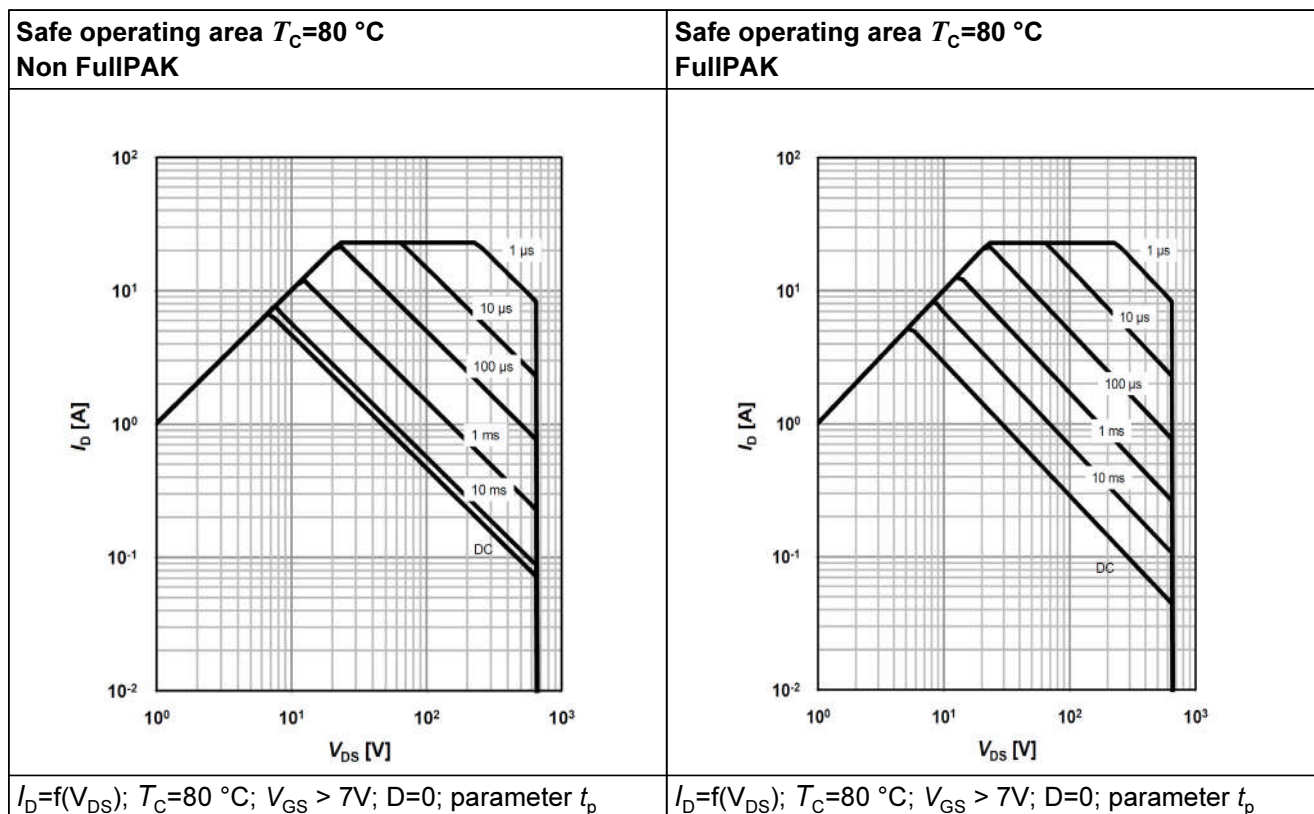


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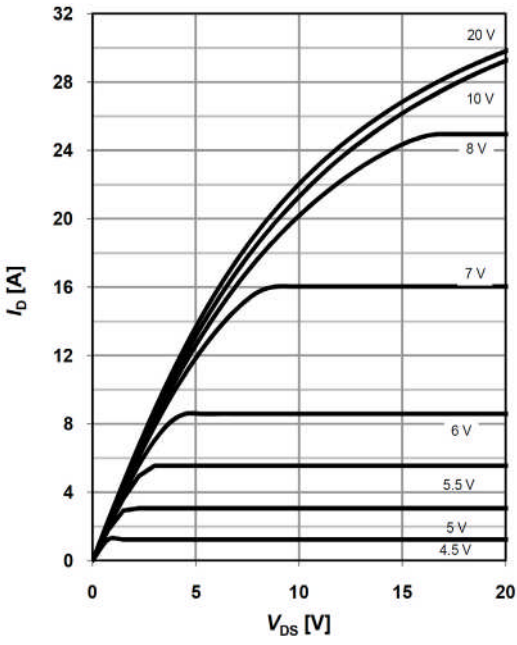
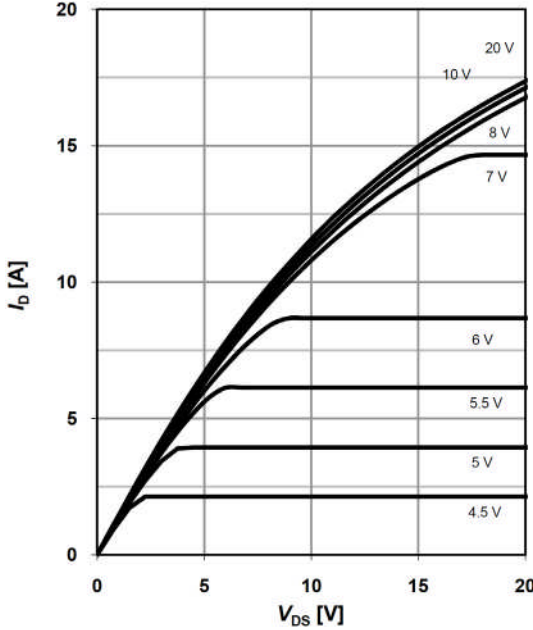
Typ. output characteristics $T_c=25\text{ °C}$	Typ. output characteristics $T_j=125\text{ °C}$
	
$I_D=f(V_{DS}); T_j=25\text{ °C}; \text{parameter: } V_{GS}$	$I_D=f(V_{DS}); T_j=125\text{ °C}; \text{parameter: } V_{GS}$

Table 15

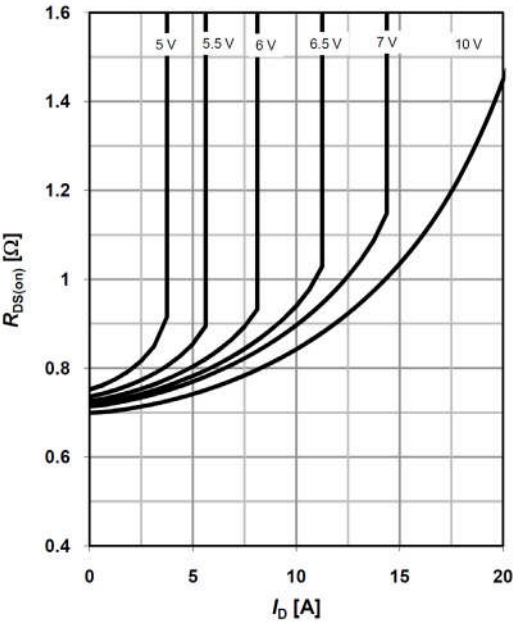
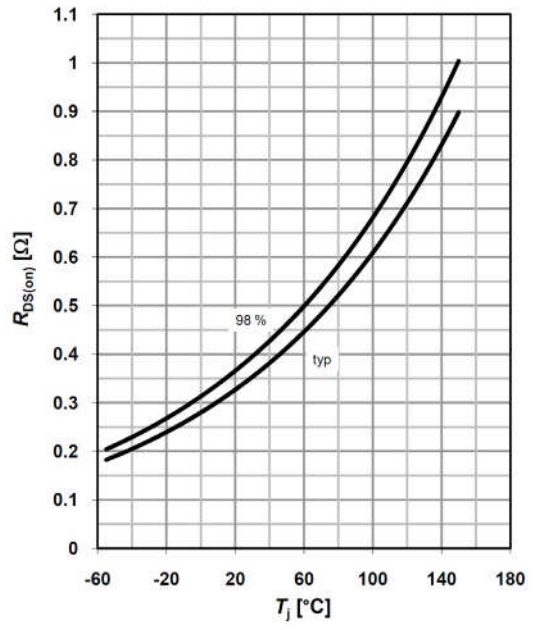
Typ. drain-source on-state resistance	Drain-source on-state resistance
	
$R_{DS(on)}=f(I_D); T_j=125\text{ °C}; \text{parameter: } V_{GS}$	$R_{DS(on)}=f(T_j); I_D=4.9\text{ A}; V_{GS}=10\text{ V}$

Table 16

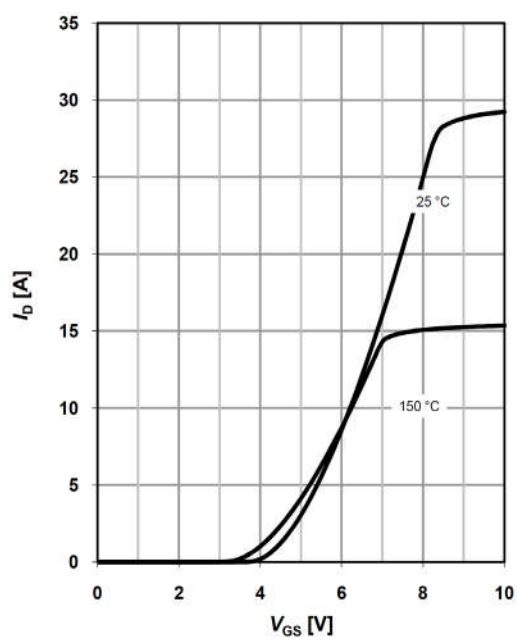
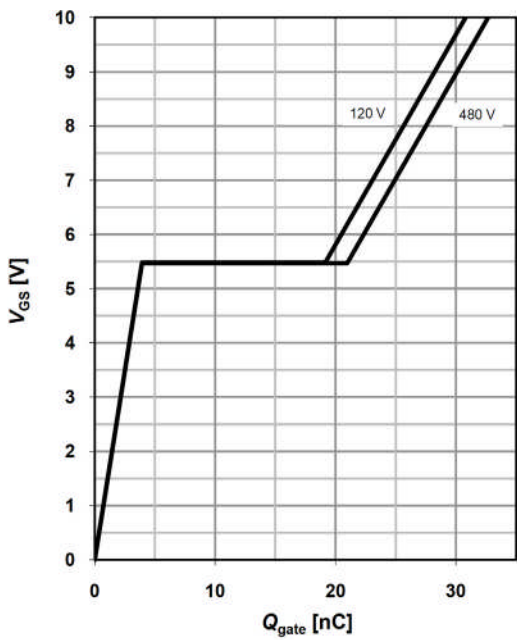
Typ. transfer characteristics	Typ. gate charge
	
$I_D = f(V_{GS}); V_{DS} = 20V$	$V_{GS} = f(Q_{gate}), I_D = 4.9 \text{ A pulsed}$

Table 17

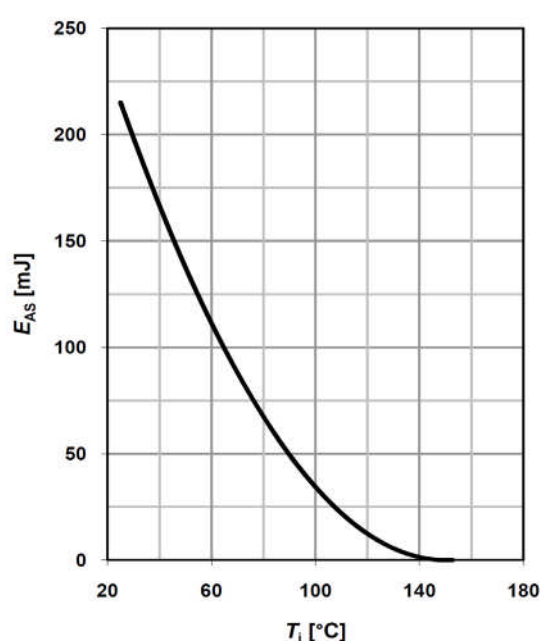
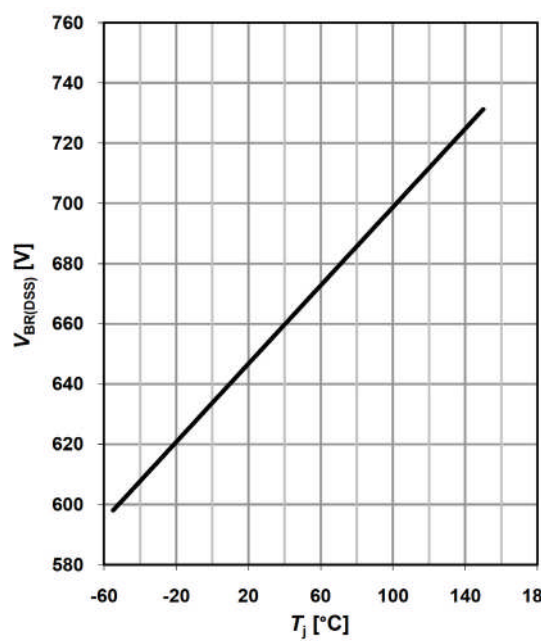
Avalanche energy	Drain-source breakdown voltage
	
$E_{AS} = f(T_j); I_D = 1.8 \text{ A}; V_{DD} = 50 \text{ V}$	$V_{BR(DSS)} = f(T_j); I_D = 1.0 \text{ mA}$

Table 18

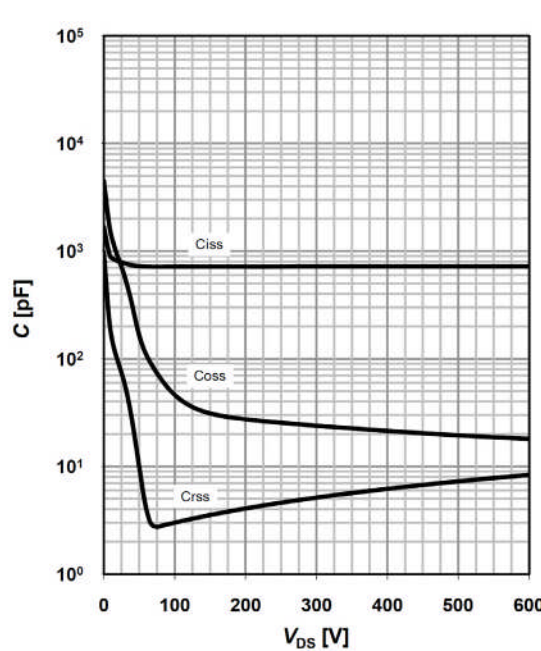
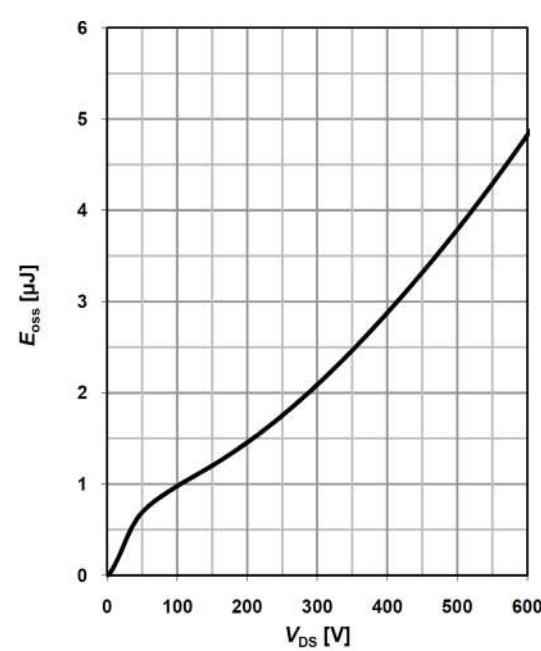
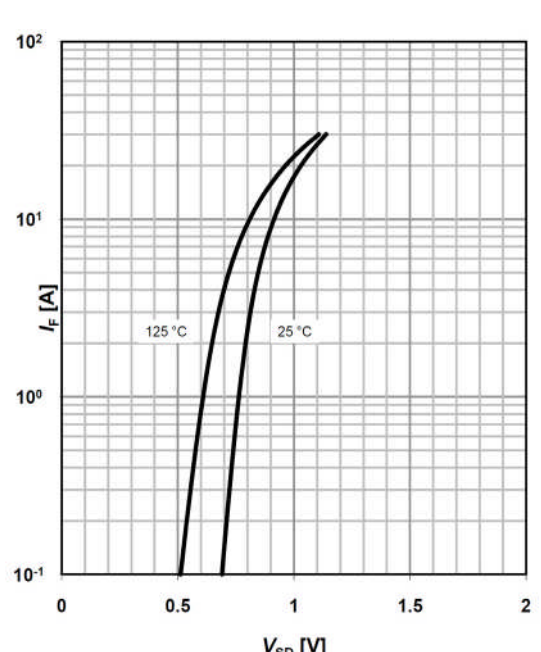
Typ. capacitances	Typ. C_{oss} stored energy
 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$	 $E_{oss} = f(V_{DS})$

Table 19

Forward characteristics of reverse diode
 $I_F = f(V_{SD}); \text{parameter: } T_j$

6 Test circuits

Table 20 Switching times test circuit and waveform for inductive load

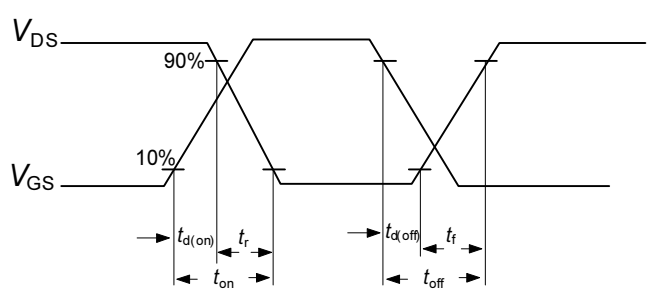
Switching times test circuit for inductive load	Switching time waveform
	

Table 21 Unclamped inductive load test circuit and waveform

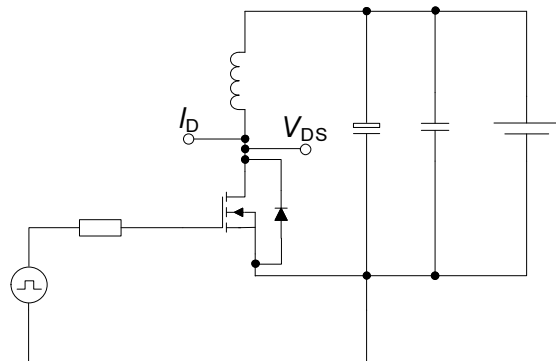
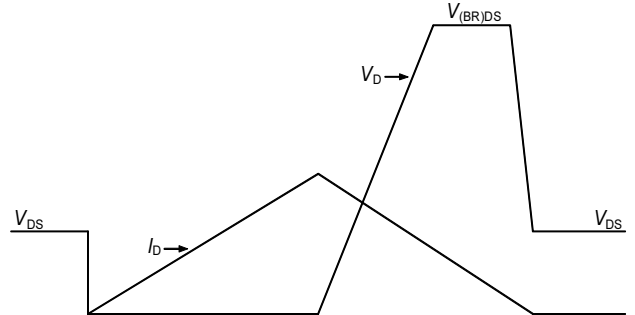
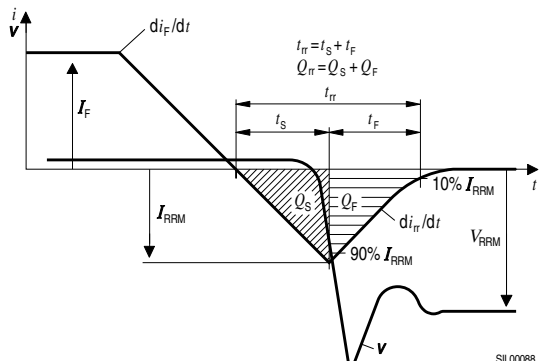
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Table 22 Test circuit and waveform for diode characteristics

Test circuit for diode characteristics	Diode recovery waveform
 $R_{G1} = R_{G2}$	 i v I_F I_{RRM} t_{rr} Q_{rr} $10\% I_{RRM}$ $90\% I_{RRM}$ V_{RRM} t_s t_F $t_{rr} = t_s + t_F$ $Q_{rr} = Q_s + Q_F$ di_F/dt di_{rr}/dt $SIL00088$

7 Package outlines

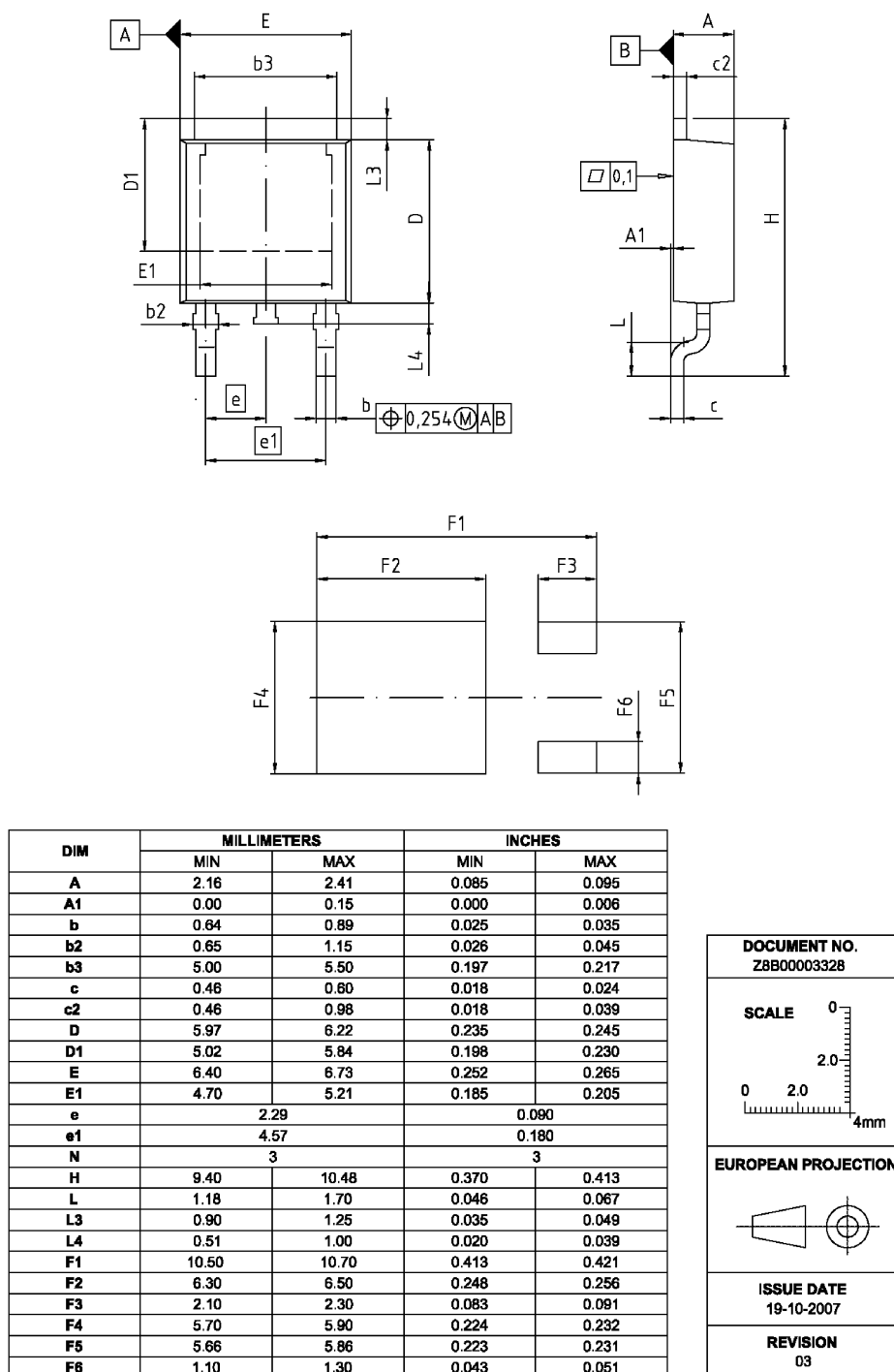
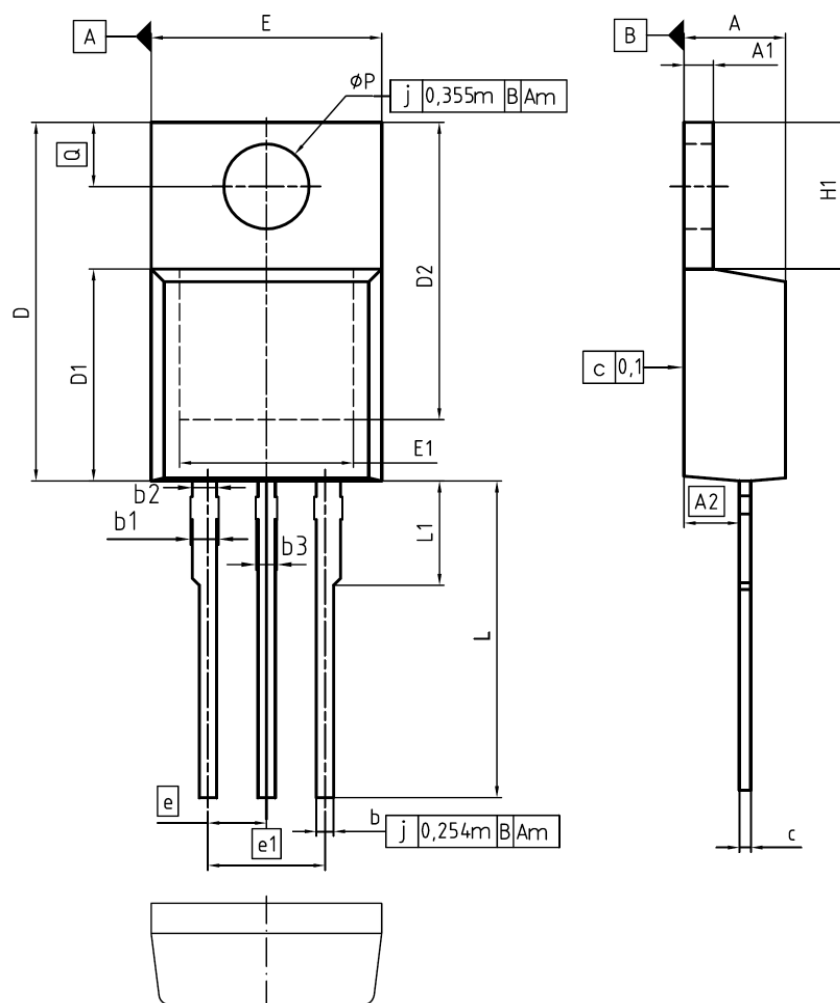


Figure 1 Outlines TO-252, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
phi P	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

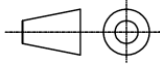
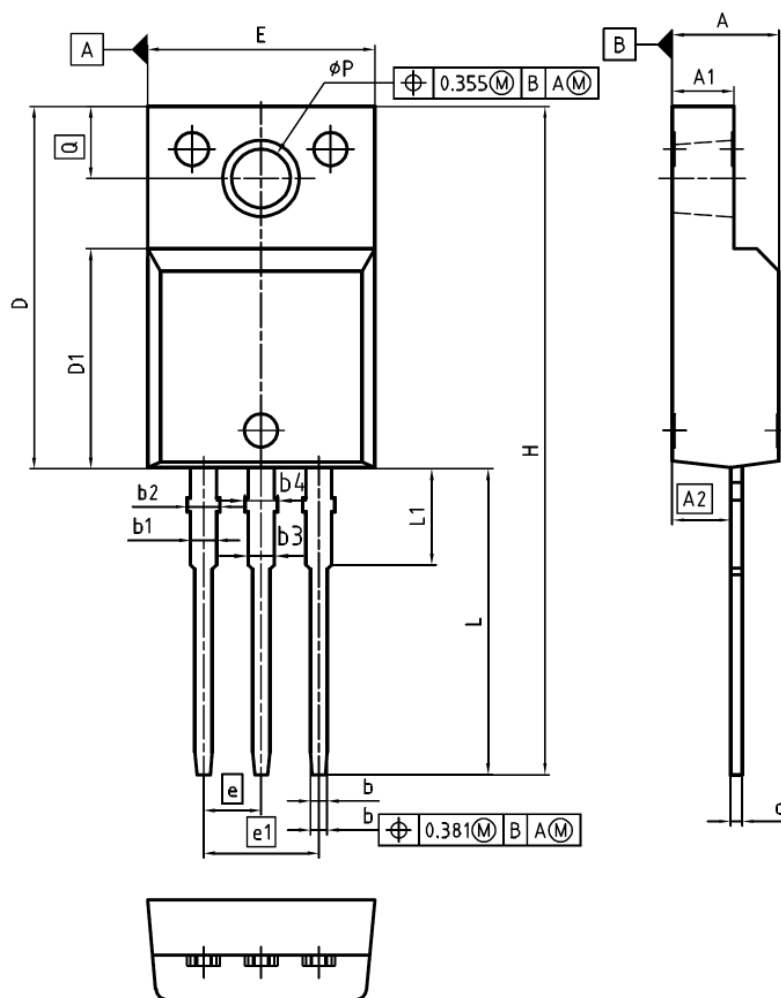
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EUROPEAN PROJECTION 
ISSUE DATE 23-08-2007
REVISION 05

Figure 2 Outlines TO-220, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
øP	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138

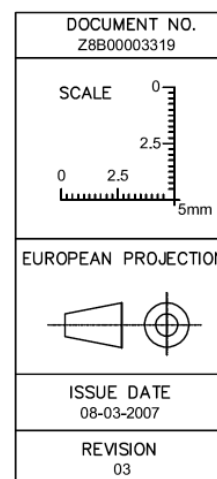


Figure 3 Outlines TO-220 FullPAK, dimensions in mm/inches

8 Revision History

Revision History: 2010-01-02, Rev. 2.0

Previous Revision:

Revision	Subjects (major changes since last revision)
2.0	Release of final data sheet

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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