

FEATURES

- 12-channel vertical driver
- 8 three-level drivers
- 4 two-level drivers
- Substrate clock driver
- Input logic supports a 1.6 V to 3.6 V range
- Output drivers support a -9.5 V to +15.5 V range
- 6 mm × 6 mm CSP_BGA package with 0.65 mm pitch

APPLICATIONS

- Digital still cameras
- Industrial cameras
- Surveillance cameras
- Medical imaging

GENERAL DESCRIPTION

The **ADDI9023** is a 12-channel vertical driver for charge-coupled device (CCD) imaging applications. It includes eight three-level drivers and four two-level drivers. The input configuration can support up to nine individual vertical timing phases and eight shift gate signals. A separate substrate clock channel (SUBCK) is also included. Typical load drive capability for each channel is 3 nF.

The **ADDI9023** is specified over an operating temperature range of -25°C to +85°C.

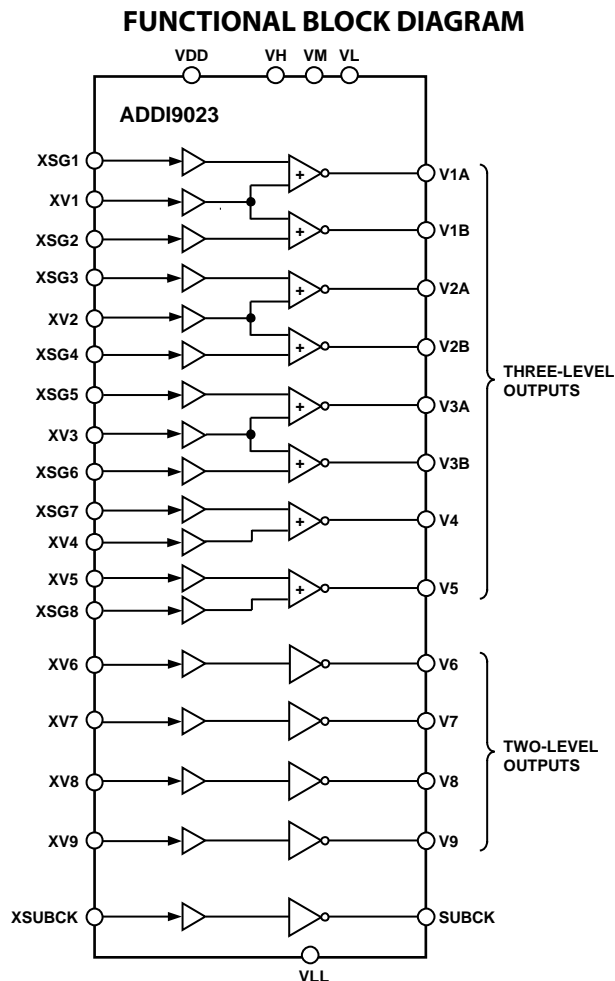


Figure 1.

Rev. 0

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REVISION HISTORY

4/12—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------|---|-----------|------|------|------|
| TEMPERATURE RANGE | | | | | |
| Operating | | -25 | | +85 | °C |
| Storage | | -65 | | +150 | °C |
| V-DRIVER POWER SUPPLY VOLTAGES | | | | | |
| VDD | Input logic supply | 1.6 | 3.0 | 3.6 | V |
| VH | V-driver high supply | 11.0 | 15.0 | 15.5 | V |
| VL | V-driver low supply | -9.5 | -7.5 | -5.5 | V |
| VM | V-driver midsupply | -1.5 | 0.0 | +1.5 | V |
| VLL | SUBCKV-driver low supply | -9.5 | -7.5 | -5.5 | V |
| VH to VL, VLL | Maximum voltage from VH to VL, VLL | | | 24 | V |
| DC POWER SUPPLY CURRENTS | | | | | |
| I_{VDD} | VH = +15 V, VM = 0 V, VL = VLL = -7.5 V XVx = XSGx = 0 V | | | 0.5 | mA |
| | XVx = XSGx = VDD | | | 0.5 | mA |
| I_{VH} | XVx = XSGx = 0 V | | | 0.4 | mA |
| | XVx = XSGx = VDD | | | 3.3 | mA |
| I_{VL} | XVx = XSGx = 0 V | | | 2.1 | mA |
| | XVx = XSGx = VDD | | | 0.1 | mA |
| I_{VM} | XVx = XSGx = 0 V | | | 0.3 | mA |
| | XVx = XSGx = VDD | | | 0.2 | mA |
| I_{VLL} | XSUBCK = 0 V | | | 0.3 | mA |
| | XSUBCK = VDD | | | 0.1 | mA |
| DIGITAL INPUTS | | | | | |
| High Level Input Voltage | VDD = 1.6 V to 3.6 V | VDD - 0.6 | | | V |
| Low Level Input Voltage | | | | 0.6 | V |
| High Level Input Current | | | 10 | 50 | μA |
| Low Level Input Current | | | 10 | 50 | μA |
| Input Capacitance | | | 10 | | pF |

OUTPUT DRIVER SPECIFICATIONS

VH = 15 V, VM = 0 V, VL, VLL = -7.5 V, T_A = 25°C.

Table 2.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|-------------------------------------|----------------------------------|-----|-----|-----|------|
| V1A TO V5 | | | | | | |
| Delay Time, VL to VM and VM to VL | t _{PLM} , t _{PML} | | | 37 | | ns |
| Delay Time, VM to VH and VH to VM | t _{PMH} , t _{PHM} | | | 43 | | ns |
| Rise Time, VL to VM | t _{RLM} | Load circuit: 20 Ω + 3 nF to GND | | 110 | | ns |
| Rise Time, VM to VH | t _{RMH} | Load circuit: 20 Ω + 3 nF to GND | | 240 | | ns |
| Fall Time, VM to VL | t _{FML} | Load circuit: 20 Ω + 3 nF to GND | | 180 | | ns |
| Fall Time, VH to VM | t _{FHM} | Load circuit: 20 Ω + 3 nF to GND | | 130 | | ns |
| Output Currents | | V1A to V5 = -7.25 V | | 14 | | mA |
| | | V1A to V5 = -0.25 V | | -23 | | mA |
| | | V1A to V5 = +0.25 V | | 23 | | mA |
| | | V1A to V5 = +14.75 V | | -10 | | mA |
| On Resistance | R _{ON} | | | | | |
| VH | | | | 23 | 35 | Ω |
| VM | | | | 11 | 20 | Ω |
| VL | | | | 17 | 25 | Ω |
| V6 TO V9 | | | | | | |
| Delay Time, VL to VM and VM to VL | t _{PLM} , t _{PML} | | | 37 | | ns |
| Rise Time, VL to VM | t _{RLM} | Load circuit: 20 Ω + 3 nF to GND | | 110 | | ns |
| Fall Time, VM to VL | t _{FML} | Load circuit: 20 Ω + 3 nF to GND | | 180 | | ns |
| Output Currents | | V6 to V9 = -7.25 V | | 14 | | mA |
| | | V6 to V9 = -0.25 V | | -23 | | mA |
| On Resistance | R _{ON} | | | | | |
| VM | | | | 11 | 20 | Ω |
| VL | | | | 17 | 25 | Ω |
| SUBCK OUTPUT | | | | | | |
| Delay Time, VLL to VH | t _{PLH} | | | 47 | | ns |
| Delay Time, VH to VLL | t _{PHL} | | | 47 | | ns |
| Rise Time, VLL to VH | t _{RLH} | Load circuit: 1 nF to GND | | 45 | | ns |
| Fall Time, VH to VLL | t _{FHL} | Load circuit: 1 nF to GND | | 45 | | ns |
| Output Currents | | SUBCK = -7.25 V | | 23 | | mA |
| | | SUBCK = +14.75 V | | -22 | | mA |
| VLL On Resistance | R _{ON} | | | 10 | 17 | Ω |

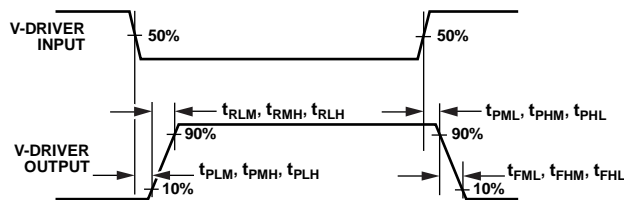


Figure 2. Definition of V-Driver Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|---|--------------------------|
| VDD to VSS | -0.3 V to +3.9 V |
| VH to VL, VLL | -0.3 V to +25.0 V |
| VH to VSS | -0.3 V to +17.0 V |
| VL to VSS | -17.0 V to +0.3 V |
| VM to VSS | -6.0 V to +3.0 V |
| VMM to VSS | -6.0 V to +3.0 V |
| VLL to VSS | -17.0 V to +0.3 V |
| V1A to V9 to VSS | VL - 0.3 V to VH + 0.3 V |
| VDREN to VSS | -0.3 V to VDD + 0.3 V |
| Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec) | 350°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

| Package Type | θ_{JA} | Unit |
|-----------------|---------------|------|
| 40-Lead CSP_BGA | 46 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

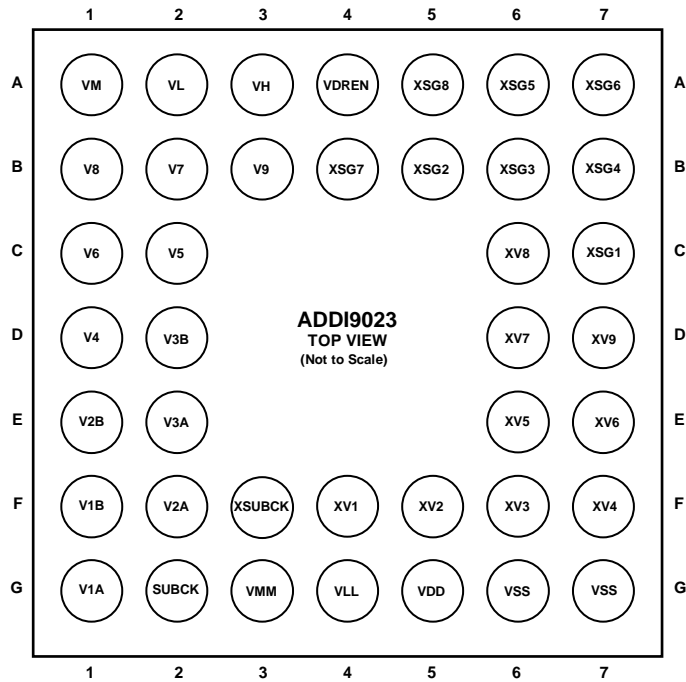


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|----------|-------------------|---|
| A1 | VM | P | V-Driver Midsupply. |
| A2 | VL | P | V-Driver Low Supply. |
| A3 | VH | P | V-Driver High Supply. |
| A4 | VDREN | DI | V-Driver Enable. Active high. |
| A5 | XSG8 | DI | Vertical Input. |
| A6 | XSG5 | DI | Vertical Input. |
| A7 | XSG6 | DI | Vertical Input. |
| B1 | V8 | VO2 | CCD Vertical Transfer Clock. |
| B2 | V7 | VO2 | CCD Vertical Transfer Clock. |
| B3 | V9 | VO2 | CCD Vertical Transfer Clock. |
| B4 | XSG7 | DI | Vertical Input. |
| B5 | XSG2 | DI | Vertical Input. |
| B6 | XSG3 | DI | Vertical Input. |
| B7 | XSG4 | DI | Vertical Input. |
| C1 | V6 | VO2 | CCD Vertical Transfer Clock. |
| C2 | V5 | VO3 | CCD Vertical Transfer Clock (XV5 + XSG8). |
| C6 | XV8 | DI | Vertical Input. |
| C7 | XSG1 | DI | Vertical Input. |
| D1 | V4 | VO3 | CCD Vertical Transfer Clock (XV4 + XSG7). |
| D2 | V3B | VO3 | CCD Vertical Transfer Clock (XV3 + XSG6). |
| D6 | XV7 | DI | Vertical Input. |
| D7 | XV9 | DI | Vertical Input. |
| E1 | V2B | VO3 | CCD Vertical Transfer Clock (XV2 + XSG4). |
| E2 | V3A | VO3 | CCD Vertical Transfer Clock (XV3 + XSG5). |
| E6 | XV5 | DI | Vertical Input. |
| E7 | XV6 | DI | Vertical Input. |

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|----------|-------------------|---|
| F1 | V1B | VO3 | CCD Vertical Transfer Clock (XV1 + XSG2). |
| F2 | V2A | VO3 | CCD Vertical Transfer Clock (XV2 + XSG3). |
| F3 | XSUBCK | DI | XSUBCK Input to SUBCK Buffer. |
| F4 | XV1 | DI | Vertical Input. |
| F5 | XV2 | DI | Vertical Input. |
| F6 | XV3 | DI | Vertical Input. |
| F7 | XV4 | DI | Vertical Input. |
| G1 | V1A | VO3 | CCD Vertical Transfer Clock (XV1 + XSG1). |
| G2 | SUBCK | VO2 | CCD Substrate Clock Output. |
| G3 | VMM | P | SUBCK Output Driver Ground. |
| G4 | VLL | P | V-Driver Low Supply for SUBCK Output. |
| G5 | VDD | P | Digital Logic Supply. |
| G6 | VSS | P | Digital Logic Ground. |
| G7 | VSS | P | Digital Logic Ground. |

¹ DI = digital input; P = power; VO2 = vertical driver output, two-level; VO3 = vertical driver output, three-level.

INPUT/OUTPUT LOGIC STATES

Table 6. V1A Output Polarity

| Vertical Driver Input | | V1A Output |
|-----------------------|------|------------|
| XV1 | XSG1 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 7. V1B Output Polarity

| Vertical Driver Input | | V1B Output |
|-----------------------|------|------------|
| XV1 | XSG2 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 8. V2A Output Polarity

| Vertical Driver Input | | V2A Output |
|-----------------------|------|------------|
| XV2 | XSG3 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 9. V2B Output Polarity

| Vertical Driver Input | | V2B Output |
|-----------------------|------|------------|
| XV2 | XSG4 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 10. V3A Output Polarity

| Vertical Driver Input | | V3A Output |
|-----------------------|------|------------|
| XV3 | XSG5 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 11. V3B Output Polarity

| Vertical Driver Input | | V3B Output |
|-----------------------|------|------------|
| XV3 | XSG6 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 12. V4 Output Polarity

| Vertical Driver Input | | V4 Output |
|-----------------------|------|-----------|
| XV4 | XSG7 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 13. V5 Output Polarity

| Vertical Driver Input | | V5 Output |
|-----------------------|------|-----------|
| XV5 | XSG8 | |
| L | L | VH |
| L | H | VM |
| H | L | VL |
| H | H | VL |

Table 14. V6 to V9 Output Polarity

| Vertical Driver Input | V6, V7, V8, or V9 Output |
|-----------------------|--------------------------|
| XV6, XV7, XV8, or XV9 | |
| L | VM |
| H | VL |

Table 15. SUBCK Output Polarity

| Vertical Driver Input | SUBCK Output |
|-----------------------|--------------|
| XSUBCK | |
| L | VH |
| H | VLL |

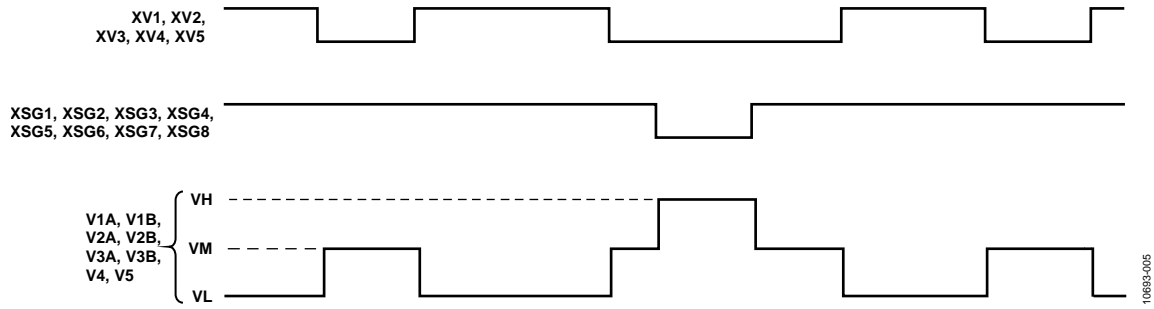


Figure 4. Three-Level V-Driver Output Polarities

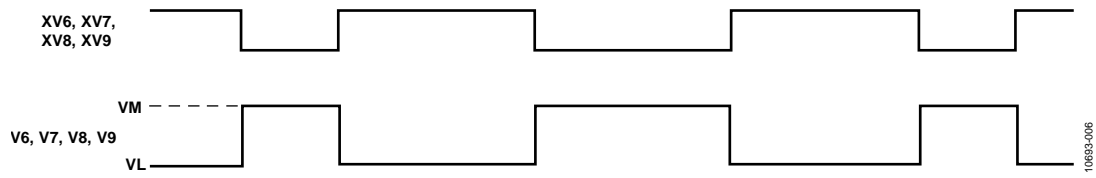


Figure 5. Two-Level V-Driver Output Polarities

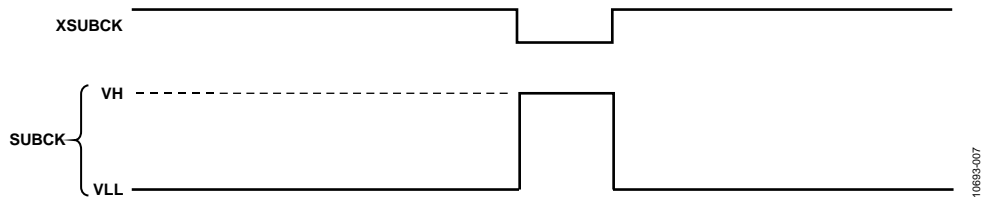


Figure 6. SUBCK Output Polarity

APPLICATIONS INFORMATION

POWER-UP SEQUENCE

When the [ADDI9023](#) is powered up, the following sequence is recommended (refer to Figure 7 for each step). Note that VH is powered on before VL but, depending on CCD restrictions, VH and VL can also be powered on simultaneously.

1. Turn on the VDD power supply, either 1.8 V or 3.3 V. After VDD settles, the logic inputs from the timing generator (XV, XSG, XSUBCK) can become active. Keep VDREN low during this time.
2. Turn on the VH power supply, typically +12 V to +15 V.

3. Turn on the VL/VLL power supply, typically -6 V to -9 V.
4. Take the VDREN pin high to enable the V-driver outputs. VDREN must remain high throughout normal vertical timing operation.

POWER-DOWN SEQUENCE

When the [ADDI9023](#) is powered down, reverse the procedure shown in Figure 7.

1. Take the VDREN pin low to disable the V-driver outputs.
2. Turn off the VL/VLL and VH power supplies.
3. Turn off the VDD power supply.

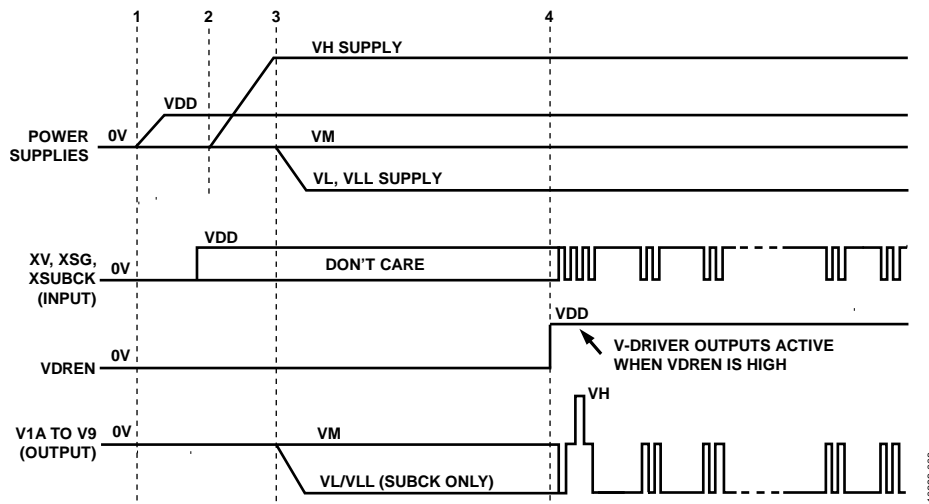


Figure 7. Recommended Power-Up Sequence

CIRCUIT LAYOUT INFORMATION

The recommended circuit configuration is shown in Figure 8. Each supply pin should have a high quality 0.1 μF capacitor connected to ground. The VH and VL supplies should have an

additional bypass capacitor, such as a 1.0 μF to 22 μF capacitor, depending on CCD and performance requirements. Connect the ground pins (VSS, VM, and VMM) to a common ground plane.

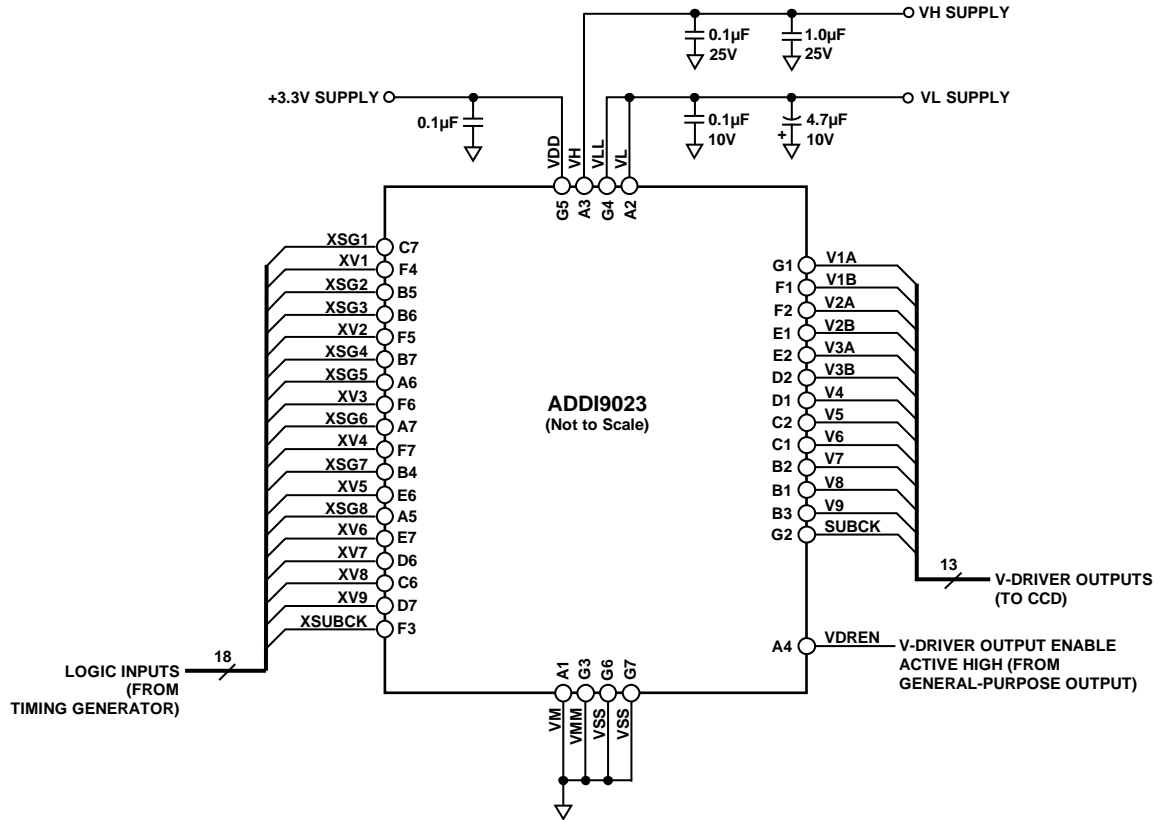
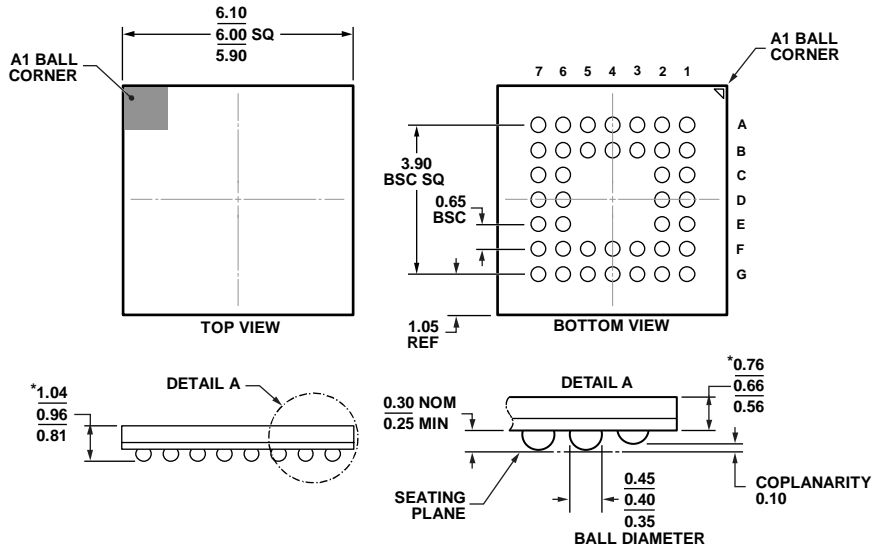


Figure 8. Typical Circuit Configuration

10693-009

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-225 WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 9. 40-Ball Chip Scale Package Ball Grid Array [CSP_BGA] BC-40-1

Dimensions shown in millimeters

04-3302012-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---------------------|----------------|
| ADDI9023BBCZ | -25°C to +85°C | 40-Lead CSP_BGA | BC-40-1 |
| ADDI9023BBCZRL | -25°C to +85°C | 40-Lead CSP_BGA | BC-40-1 |

¹ Z = RoHS Compliant Part.

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