

STK544UC62K-E

Intelligent Power Module (IPM) 600 V, 10 A



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Overview

This Inverter IPM includes the output stage of a 3-phase inverter, pre-drive circuits, bootstrap circuits, and protection circuits in one package.

Function

- SIP (single in-line package) of the transfer full mold structure.
- The emitter line of the each lower phase outputs to an external terminal with the option of control using 3-phase current detection with external resistors.
- Direct input of CMOS level control signals without an insulating circuit is possible.
- Protective circuits including over current and pre-drive low voltage protection are built in.
- A single power supply drive is enabled through the use of bootstrap circuits for upper IGBT gate drives.
- Built-in dead-time for shoot-thru protection.
- Internal substrate temperature is measured with an internal pulled up thermistor.

Certification

- UL1557 (File Number : E339285)

Specifications

Absolute Maximum Ratings at Tc = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------------|--------------------|---|--------------------|------|
| Supply voltage | V _{CC} | V+ to VRU(VRV,VRW), surge < 500 V *1 | 450 | V |
| Collector-emitter voltage | V _{CE} | V+ to U(V,W) or U(V,W) to VRU(VRV,VRW) | 600 | V |
| Output current | I _o | V+, VRU,VRV,VRW, U,V,W terminal current | ±10 | A |
| | | V+, VRU,VRV,VRW, U,V,W terminal current at Tc = 100°C | ±6 | A |
| Output peak current | I _{op} | V+, VRU,VRV,VRW, U,V,W terminal current for a pulse width of 1 ms | ±20 | A |
| Pre-driver voltage | VD1,2,3,4 | VB1 to U, VB2 to V, VB3 to W, V _{DD} to V _{SS} *2 | 20 | V |
| Input signal voltage | V _{IN} | HIN1, 2, 3, LIN1, 2, 3 terminals | -0.3 to 7 | V |
| ITRIP terminal voltage | V _{ITRIP} | ITRIP terminal | V _{SS} +5 | V |
| Maximum power dissipation | P _d | IGBT per 1 channel | 22 | W |
| Junction temperature | T _j | IGBT,FRD | 150 | °C |
| Storage temperature | T _{stg} | | -40 to +125 | °C |
| Operating case temperature | T _c | IPM case temperature | -40 to +100 | °C |
| Tightening torque | | Case mounting screws *3 | 0.9 | Nm |
| Withstand voltage | V _{is} | 50 Hz sine wave AC 1 minute *4 | 2000 | VRMS |

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between V+ and VRU(VRV,VRW) terminals.

*2 : VD1 = VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = V_{DD} to V_{SS} terminal voltage.

*3 : Flatness of the heat-sink should be less than -50 μm to +100 μm.

*4 : Test conditions : AC 2500 V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

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Electrical Characteristics at T_c = 25°C, VD1, VD2, VD3, VD4 = 15 V

| Parameter | Symbol | Conditions | Test circuit | Ratings | | | Unit |
|---|----------------------|--|--------------|---------|------|-----|------|
| | | | | min | typ | max | |
| Power output section | | | | | | | |
| Collector-emitter cut-off current | I _{CE} | V _{CE} = 600 V | Fig.1 | - | - | 0.1 | mA |
| Bootstrap diode reverse current | IR(BD) | VR(BD) = 600 V | | - | - | 0.1 | mA |
| Collector to emitter saturation voltage | V _{CE(SAT)} | I _o = 10 A, T _j = 25°C | Fig.2 | - | 1.4 | 2.3 | V |
| | | I _o = 5 A, T _j = 100°C | | - | 1.3 | - | |
| Diode forward voltage | V _F | I _o = 10 A, T _j = 25°C | Fig.3 | - | 1.3 | 2.2 | V |
| | | I _o = 5 A, T _j = 100°C | | - | 1.2 | - | |
| Bootstrap diode forward voltage | V _{F(BD)} | IF = 0.1 A | - | - | 2.0 | - | V |
| Bootstrap circuit resistance | R _{BC} | Resistor value for common boot charge line | - | - | 2 | - | Ω |
| | R _{BS} | Resistor values for separate boot charge lines | - | - | 10 | - | |
| Junction to case thermal resistance | θ _{j-c(T)} | IGBT | - | - | 4.5 | 5.5 | °C/W |
| | θ _{j-c(D)} | FRD | | - | 5.5 | 6.5 | |
| Thermal resistance case to sink | R _{th(c-s)} | 1W/mK thermal conductivity *1 | | - | - | 0.1 | |
| Protection section | | | | | | | |
| FAULT clearance delay time | FLTCLR | Form time fault condition clears | - | 6 | 9 | 12 | ms |
| Switching time | t _{ON} | I _o = 10 A | Fig.5 | - | 0.48 | - | μs |
| | t _{OFF} | Inductive load | | - | 0.54 | - | |

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : At 100 μm thickness of the thermal grease.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics Driver Function at T_c = 25°C

| Parameter | Symbol | Test circuit | Ratings | | | Unit |
|--|---------------------|--------------|---------|------|------|------|
| | | | min | typ | max | |
| Supply section | | | | | | |
| V _{DD} and V _{BS} supply undervoltage protection reset | V _{DDUV+} | - | 10.5 | 11.1 | 11.7 | V |
| | V _{BSUV+} | | | | | |
| V _{DD} and V _{BS} supply undervoltage protection set | V _{DDUV-} | - | 10.3 | 10.9 | 11.5 | V |
| | V _{BSUV-} | | | | | |
| V _{DD} and V _{BS} supply undervoltage hysteresis | V _{DDUVH} | - | 0.14 | 0.2 | - | V |
| | V _{BSUVH} | | | | | |
| Quiescent V _{DD} supply current | I _{QDD} | Fig.4 | - | 2.0 | 4.0 | mA |
| Quiescent V _{BS} supply current | I _{QBS} | | - | 0.08 | 0.4 | mA |
| Input section | | | | | | |
| Logic low input voltage | V _{INL} | - | - | - | 0.8 | V |
| Logic high input voltage | V _{INH} | - | 2.5 | - | - | V |
| Logic 0 input leakage current | I _{IN+} | - | 76 | 118 | 160 | μA |
| Logic 1 input leakage current | I _{IN-} | - | 97 | 150 | 203 | μA |
| ITRIP threshold voltage (OUT = LO or OUT = HI) | V _{ITRIP} | - | 3.67 | 4.17 | 4.67 | V |
| Dynamic section | | | | | | |
| Dead time (Internal dead time injected by driver) | DT | - | 220 | 300 | 380 | ns |
| ITRIP to shutdown propagation delay | t _{ITRIP} | - | 1.0 | 1.2 | 1.4 | μs |
| ITRIP blanking time | t _{ITRPBL} | - | - | 0.9 | - | μs |

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

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Switching Characteristics at $T_c = 25^\circ\text{C}$, $V_{D1}, V_{D2}, V_{D3}, V_{D4} = 15\text{ V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------------------|-----------|--|-------------|-----|-----|---------------|
| | | | min | typ | max | |
| Turn-on switching loss | E_{on} | $I_C = 5\text{ A}, V_+ = 400\text{ V}$ $V_{DD} = 15\text{ V}, L = 3.9\text{ mH},$ $T_c = 25^\circ\text{C}$ | - | 195 | - | μJ |
| Turn-off switching loss | E_{off} | | - | 122 | - | μJ |
| Total switching loss | E_{tot} | | - | 317 | - | μJ |
| Turn-on switching loss | E_{on} | $I_C = 5\text{ A}, V_+ = 400\text{ V},$ $V_{DD} = 15\text{ V}, L = 3.9\text{ mH},$ $T_c = 100^\circ\text{C}$ | - | 224 | - | μJ |
| Turn-off switching loss | E_{off} | | - | 186 | - | μJ |
| Total switching loss | E_{tot} | | - | 410 | - | μJ |
| Diode reverse recovery time | t_{rr} | $I_F = 5\text{ A}, V_+ = 400\text{ V}, V_{DD} = 15\text{ V},$ $L = 3.9\text{ mH}, T_c = 100^\circ\text{C}$ | - | 70 | - | ns |
| Reverse bias safe operating area | RBSOA | $I_o = 20\text{ A}, V_{CE} = 450\text{ V}$ | FULL SQUARE | | | - |
| Short circuit safe operating area | SCSOA | $V_{CE} = 400\text{ V}$ | 4 | - | - | μs |

$V_{DD} = V_{B1} = V_{B2} = V_{B3} = 15\text{ V}, V_{SS} = V_{S1} = V_{S2} = V_{S3} = 0\text{ V}$, outputs loaded with 1 nF , all voltage are referenced to V_{SS} ; unless otherwise noted.

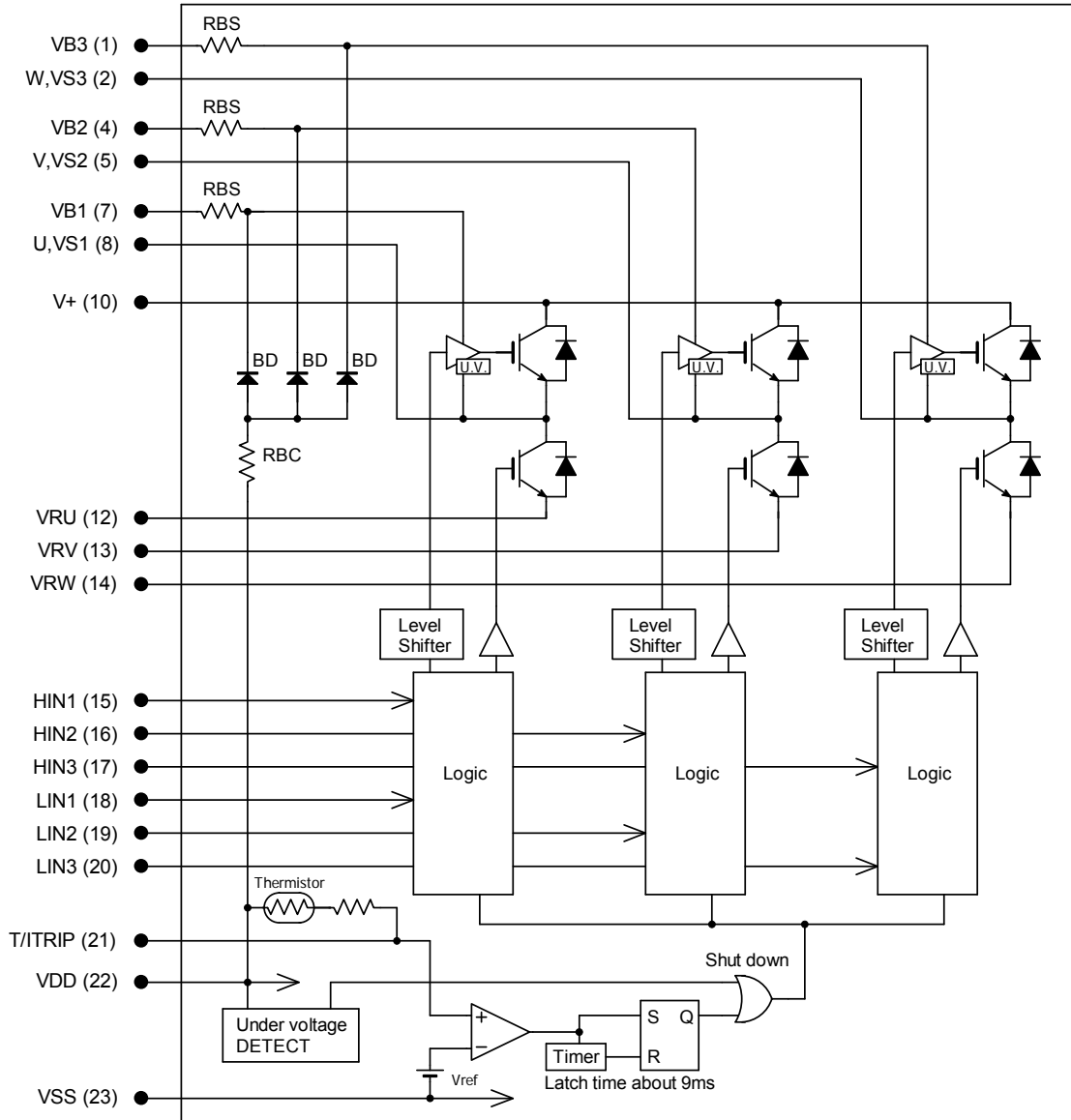
Internal NTC-Thermistor Characteristics

| Parameter | | Conditions | Typ. | Unit |
|---------------------------|--|------------------------------------|-----------------|----------------------------|
| R25 | Resistance | $T_c = 25^\circ\text{C}$ | $100 \pm 3\%$ | $\text{k}\Omega$ |
| R125 | Resistance | $T_c = 125^\circ\text{C}$ | $2.522 \pm 3\%$ | $\text{k}\Omega$ |
| B | B-Constant (25 to 50°C) | $R_2 = R_1 e^{[B(1/T_2 - 1/T_1)]}$ | $4250 \pm 1\%$ | K |
| Temperature range | | - | -40 to +125 | $^\circ\text{C}$ |
| Typ. Dissipation constant | | $T_c = 25^\circ\text{C}$ | 1 | $\text{mW}/^\circ\text{C}$ |

Notes

- The pre-drive power supply low voltage protection has approximately 200 mV of hysteresis and operates as follows.
 - Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'high'.
 - Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
- When assembling the IPM on the heat sink the tightening torque range is 0.6 Nm to 0.9 Nm.
- The pre-drive low voltage protection protects the device when the pre-drive supply voltage falls due to an operating malfunction.
- When use the over-current protection with external shunt resistor, please set the current protection level to be equal to or less than the rating of output peak current (I_{op}).

Equivalent Block Diagram



Module Pin-Out Description

| Pin | Name | Description |
|-----|--------|--|
| 1 | VB3 | High Side Floating Supply Voltage 3 |
| 2 | W, VS3 | Output 3, High Side Floating Supply Offset Voltage 3 |
| 3 | - | Without pin |
| 4 | VB2 | High Side Floating Supply Voltage 2 |
| 5 | V, VS2 | Output 2, High Side Floating Supply Offset Voltage 2 |
| 6 | - | Without pin |
| 7 | VB1 | High Side Floating Supply Voltage 1 |
| 8 | U, VS1 | Output 1, High Side Floating Supply Offset Voltage 1 |
| 9 | - | Without pin |
| 10 | V+ | Positive Bus Input Voltage |
| 11 | - | Without pin |
| - | - | - |

| Pin | Name | Description |
|-----|---------|---|
| 12 | VRU | Low Side Emitter Connection – Phase 1 |
| 13 | VRV | Low Side Emitter Connection – Phase 2 |
| 14 | VRW | Low Side Emitter Connection – Phase 3 |
| 15 | HIN1 | Logic Input High Side Gate Driver – Phase 1 |
| 16 | HIN2 | Logic Input High Side Gate Driver – Phase 2 |
| 17 | HIN3 | Logic Input High Side Gate Driver – Phase 3 |
| 18 | LIN1 | Logic Input Low Side Gate Driver – Phase 1 |
| 19 | LIN2 | Logic Input Low Side Gate Driver – Phase 2 |
| 20 | LIN3 | Logic Input Low Side Gate Driver – Phase 3 |
| 21 | T/Itrip | Temperature Monitor and Shut-down Pin |
| 22 | VDD | +15 V Main Supply |
| 23 | VSS | Negative Main Supply |

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Test Circuit

The tested phase U+ shows the upper side of the U phase and U- shows the lower side of the U phase.

■ I_{CE} / I_{R(BD)}

| | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 10 | 10 | 10 | 8 | 5 | 2 |
| N | 8 | 5 | 2 | 12 | 13 | 14 |

| | U(BD) | V(BD) | W(BD) |
|---|-------|-------|-------|
| M | 7 | 4 | 1 |
| N | 23 | 23 | 23 |

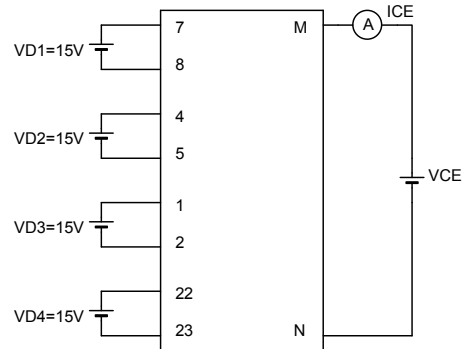


Fig. 1

■ V_{CE(SAT)} (test by pulse)

| | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 10 | 10 | 10 | 8 | 5 | 2 |
| N | 8 | 5 | 2 | 12 | 13 | 14 |
| m | 15 | 16 | 17 | 18 | 19 | 20 |

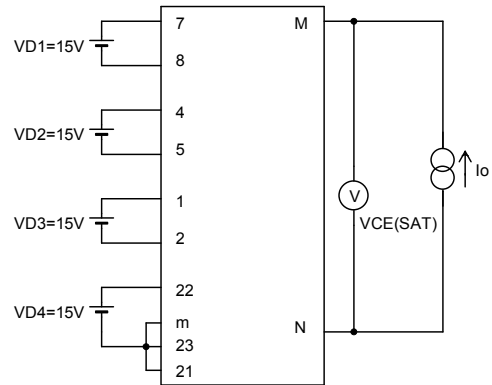


Fig. 2

■ V_F (test by pulse)

| | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 10 | 10 | 10 | 8 | 5 | 2 |
| N | 8 | 5 | 2 | 12 | 13 | 14 |

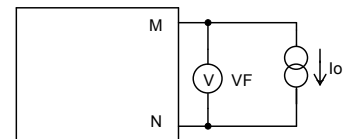


Fig. 3

■ I_D

| | VD1 | VD2 | VD3 | VD4 |
|---|-----|-----|-----|-----|
| M | 7 | 4 | 1 | 22 |
| N | 8 | 5 | 2 | 23 |

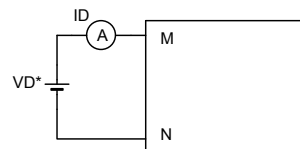


Fig. 4

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- Switching time (The circuit is a representative example of the lower side U phase.)

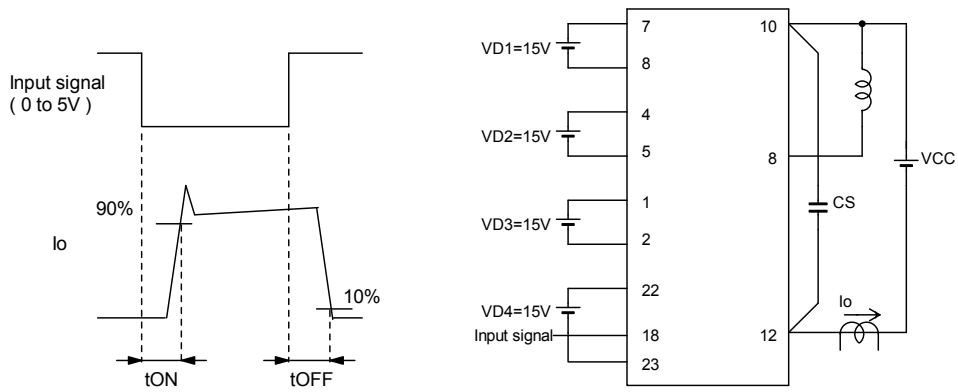


Fig. 5

- RB-SOA (The circuit is a representative example of the lower side U phase.)

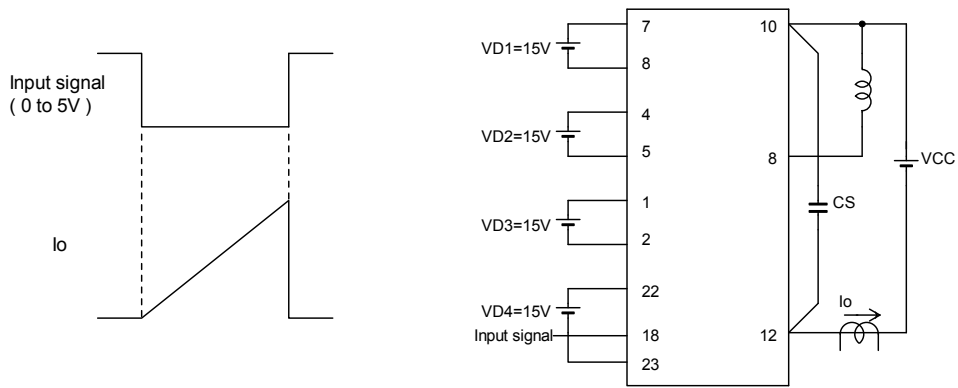


Fig. 6

Input / Output Timing Diagram

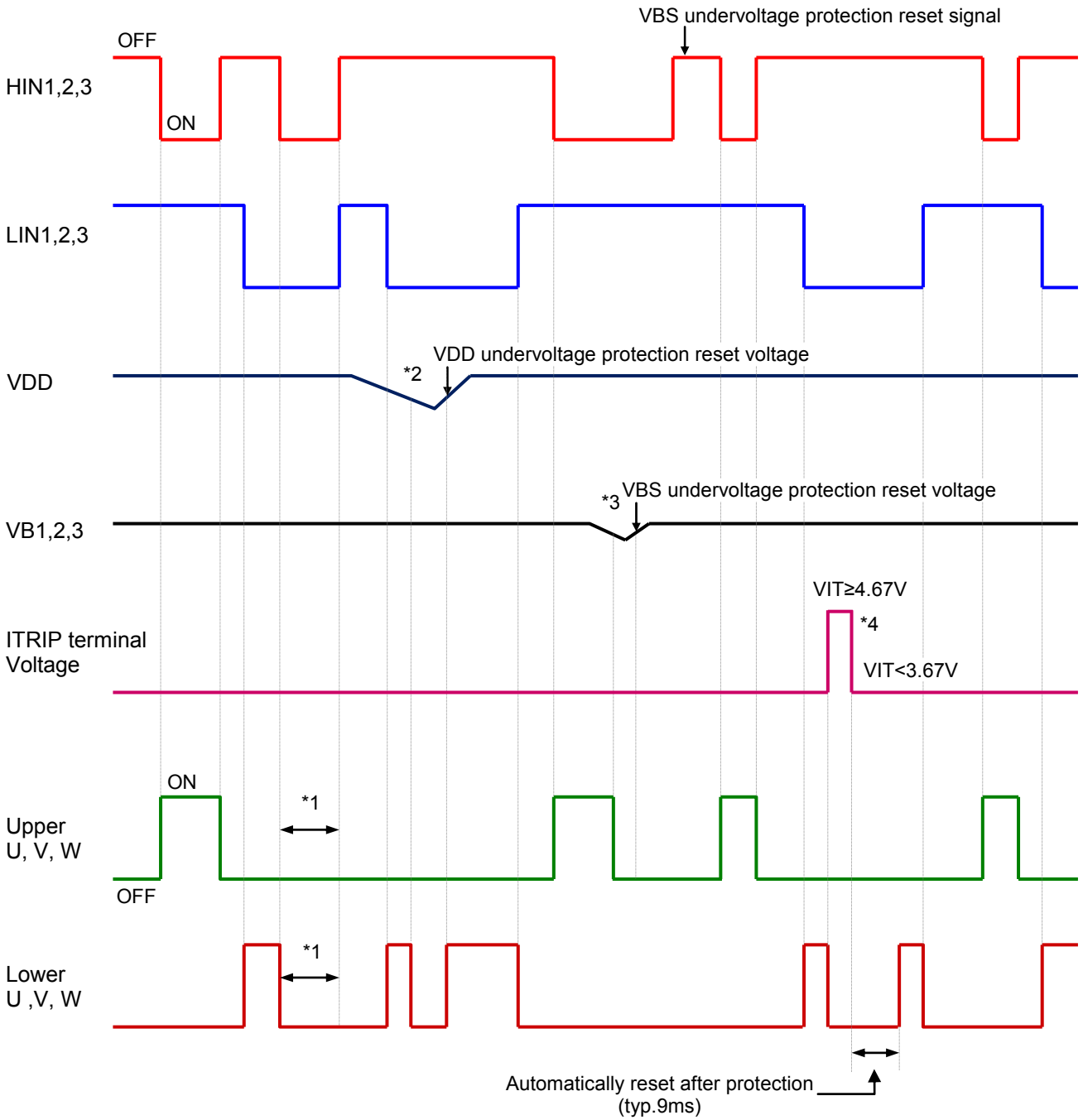
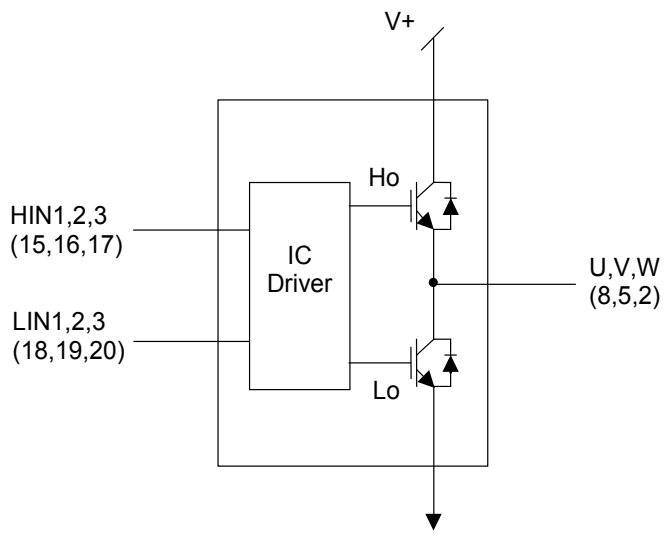


Fig. 7

Notes

- *1 : Shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.
- *2 : When V_{DD} decreases all gate output signals will go low and cut off all 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
- *3 : When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- *4 : When V_{ITRIP} exceeds threshold all IGBT's are turned off and normal operation resumes 9 ms (typ) after over current condition is removed.

Logic level table

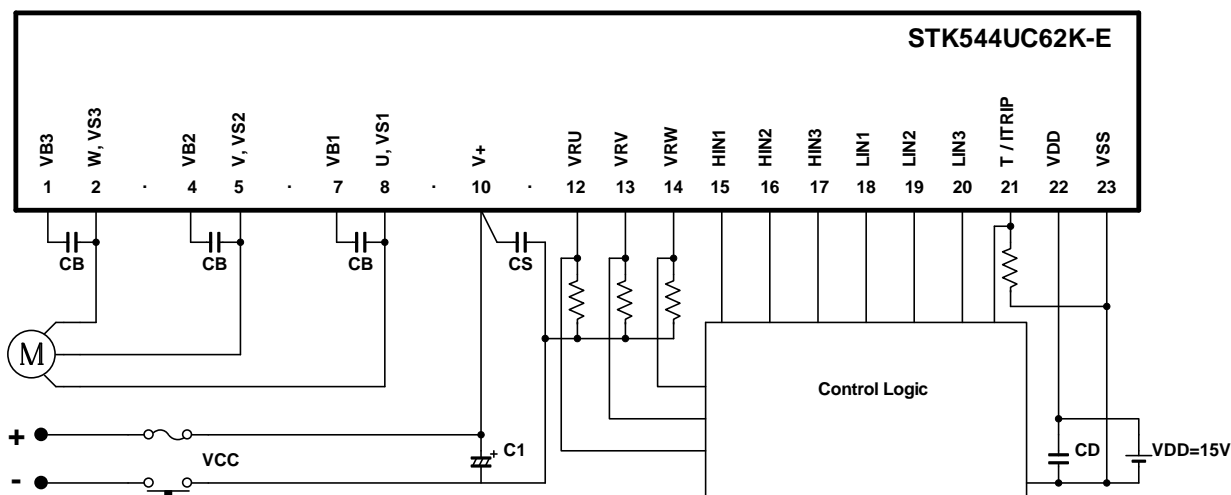


| Itrip | HIN1,2,3 | LIN1,2,3 | U,V,W |
|-------|----------|----------|-------|
| 0 | 0 | 1 | V+ |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X |
| 1 | X | X | X |

Fig. 8

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Sample Application Circuit



Recommended Operating Conditions at T_c = 25°C

| Item | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|----------------------|---|---------|-----|------|------|
| | | | min | typ | max | |
| Supply voltage | V _{CC} | Between V ₊ to VRU(VRV,VRW) | 0 | 280 | 450 | V |
| Pre-driver supply voltage | VD1,2,3 | Between VB1 to U,VB2 to V,VB3 to W | 12.5 | 15 | 17.5 | V |
| | VD4 | Between V _{DD} to V _{SS} *1 | 13.5 | 15 | 16.5 | |
| ON-state input voltage | V _{IN(ON)} | HIN1,HIN2,HIN3,LIN1,LIN2,LIN3 terminal | 0 | - | 0.3 | V |
| OFF-state input voltage | V _{IN(OFF)} | | 3.0 | - | 5.0 | |
| PWM frequency | f _{PWM} | - | 1 | - | 20 | kHz |
| Dead time | DT | Turn-off to turn-on (External) | 0.5 | - | - | μs |
| Mounting torque | - | 'M3' type screw | 0.6 | - | 0.9 | Nm |

*1 : Pre-drive power supply (VD4 = 15 ±1.5 V) must have the capacity of I_o = 20 mA (DC), 0.5 A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes internal bootstrap diode and resistor. By adding a capacitor CB, a single high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF, however, this value needs to be verified prior to production. When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of CS is in the range of 0.1 to 10 μF.
3. VRU, VRV, and VRW terminals are direct outputs of the emitter line of the each lower phase IGBT and can be used to monitor each phase's or collective current with external resistors. IF current is not monitored, each resistor should be short-circuited.
4. Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection.
5. Zner diode with 10 V is connected with the inside of the signal input terminal. When inputting voltage which exceeds 5 V, connect resistor between the side of the power and the signal input terminal, for the input current of the signal input terminal become equal to or less than 0.5 mA. This resistor is effective with the noise absorption of the signal terminal, too.
6. A fuse on V_{CC} is recommended.
7. Inside the IPM, a thermistor used as the temperature monitor is connected between V_{DD} terminal and T/ITRIP terminal, therefore, an external pull down resistor connected between the T/ITRIP terminal and V_{SS} terminal should be used. The temperature monitor example application is as follows, please refer the Fig.10, Fig.11, and Fig.12 below.
8. All data shown implements an example of the application circuit but does not guarantee a design for the mass production.

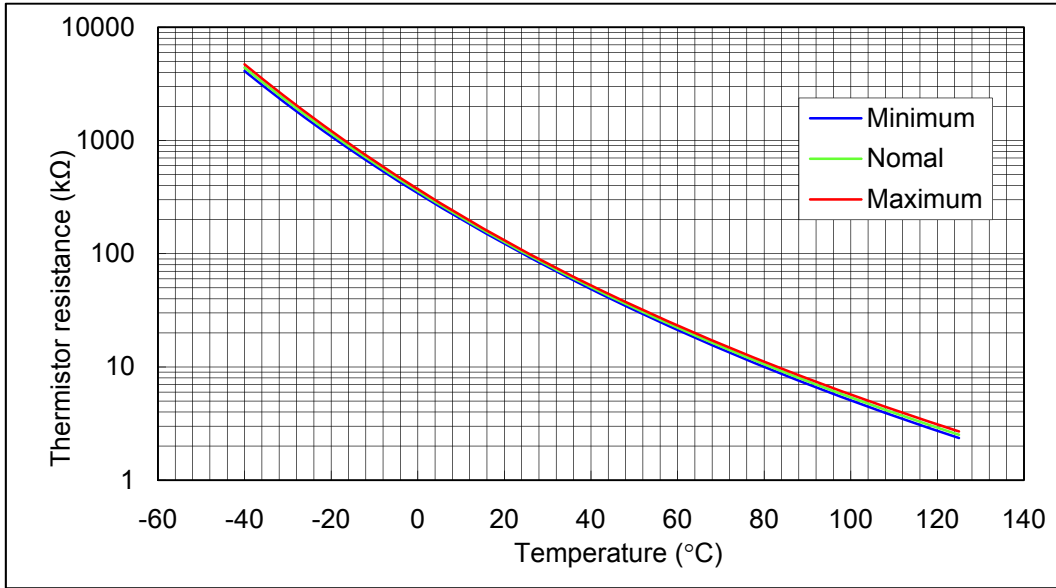


Fig. 10 Variation of thermistor resistance with temperature

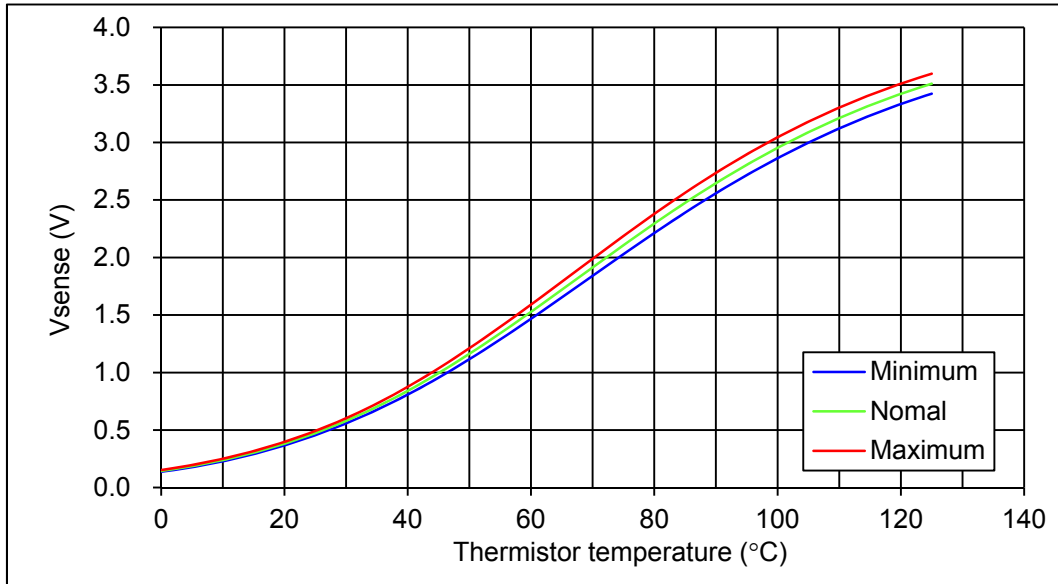


Fig. 11 Variation of temperature sense voltage with thermistor temperature by using external bias resistance of 4.3 kΩ ±1% and V_{DD} = 15 V

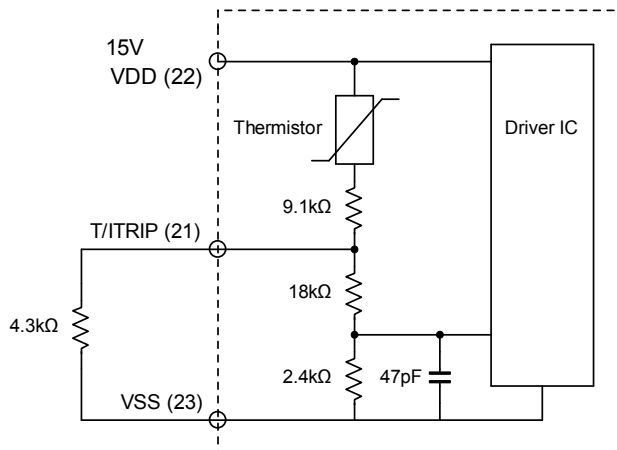


Fig. 12 Sample application circuit for temperature monitoring

The characteristic of PWM switching frequency

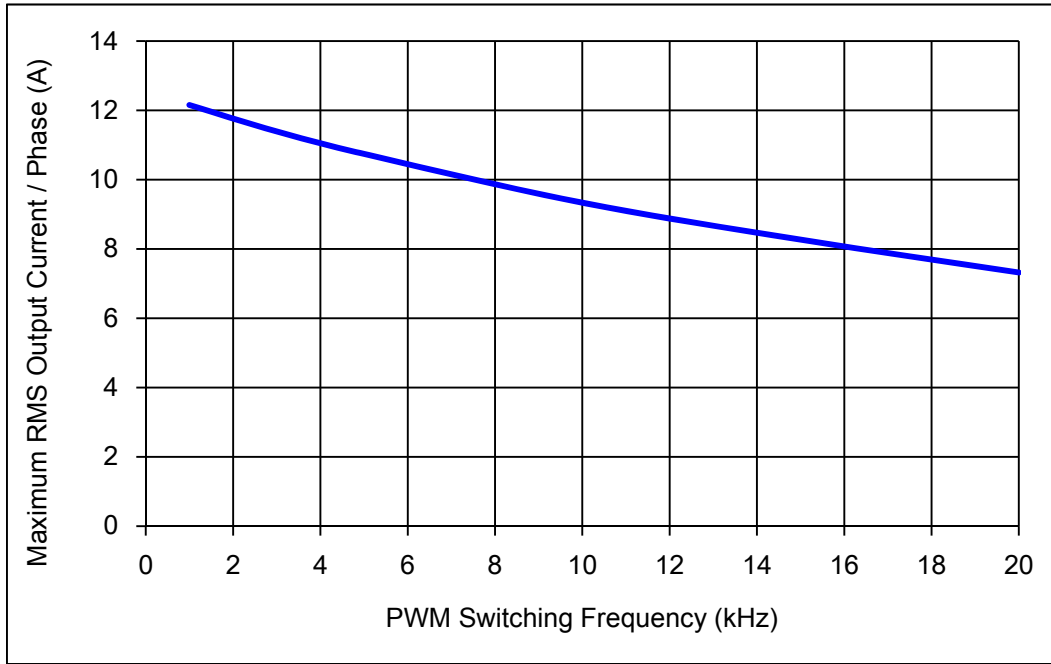


Fig. 13 Maximum sinusoidal phase current as function of switching frequency at $T_c = 100^\circ\text{C}$, $V_{CC} = 400\text{ V}$

Switching waveform

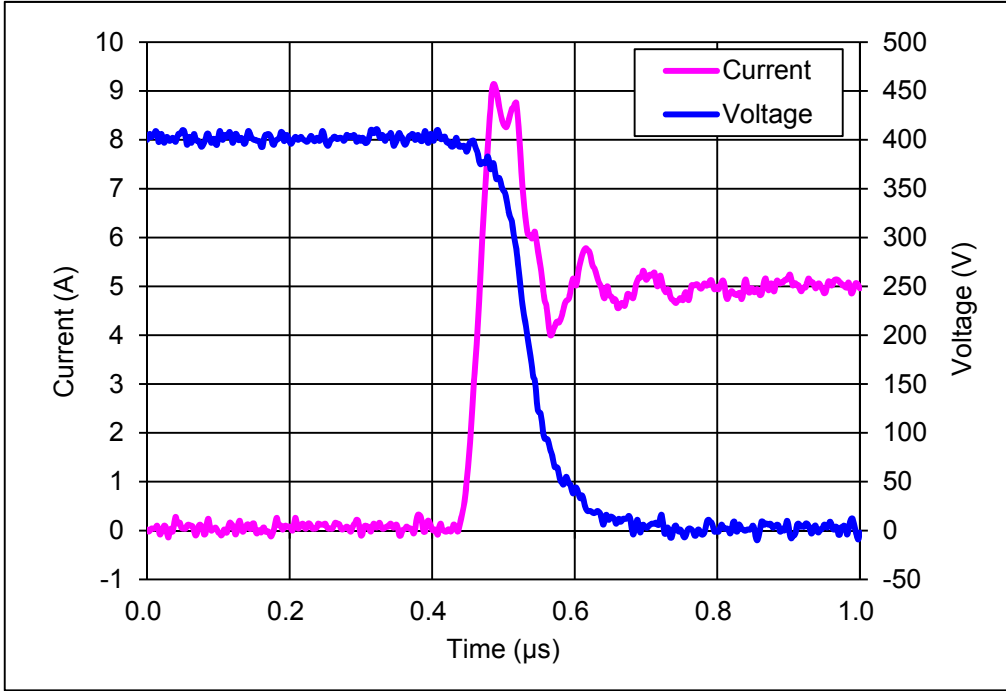


Fig. 14 IGBT Turn-on. Typical turn-on waveform at $T_c = 100^\circ\text{C}$, $V_{CC} = 400\text{ V}$

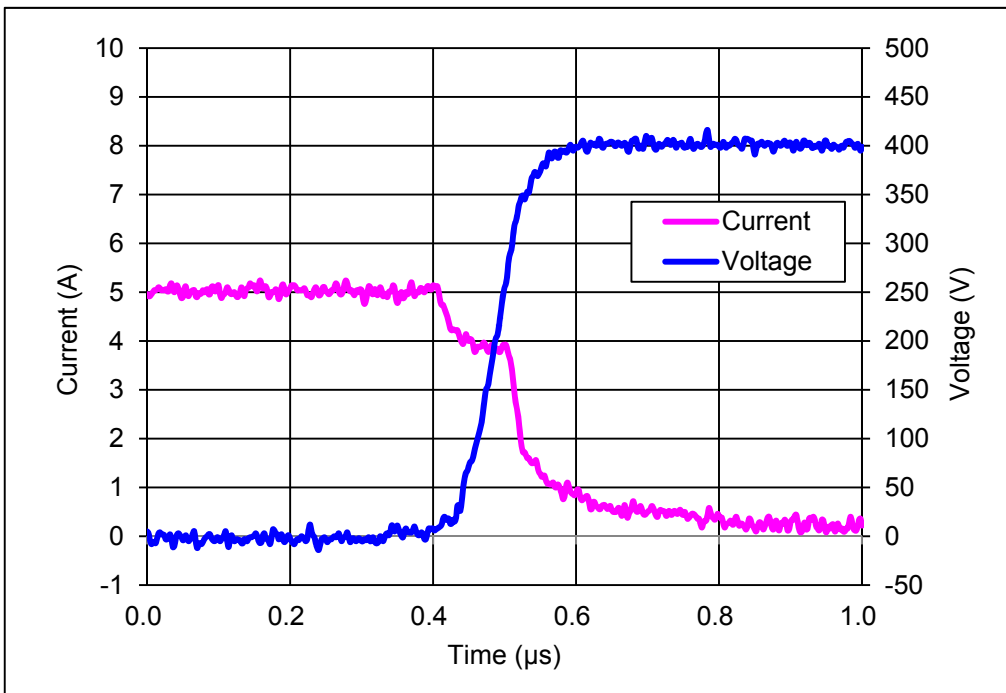


Fig. 15 IGBT Turn-off. Typical turn-off waveform at $T_c = 100^\circ\text{C}$, $V_{CC} = 400\text{ V}$

CB capacitor value calculation for bootstrap circuit

Calculate conditions

| Parameter | Symbol | Value | Unit |
|---|--------|-------|------|
| Upper side power supply | VBS | 15 | V |
| Total gate charge of output power IGBT at 15 V | QG | 89 | nC |
| Upper limit power supply low voltage protection | UVLO | 12 | V |
| Upper side power dissipation | IDMAX | 95 | μA |
| ON time required for CB voltage to fall from 15 V to UVLO | TONMAX | - | S |

Capacitance calculation formula

Thus, the following formula are true

$$VBS \times CB - QG - IDMAX \times TONMAX = UVLO \times CB$$

therefore,

$$CB = (QG + IDMAX \times TONMAX) / (VBS - UVLO)$$

The relationship between TONMAX and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, this value needs to be verified prior to production.

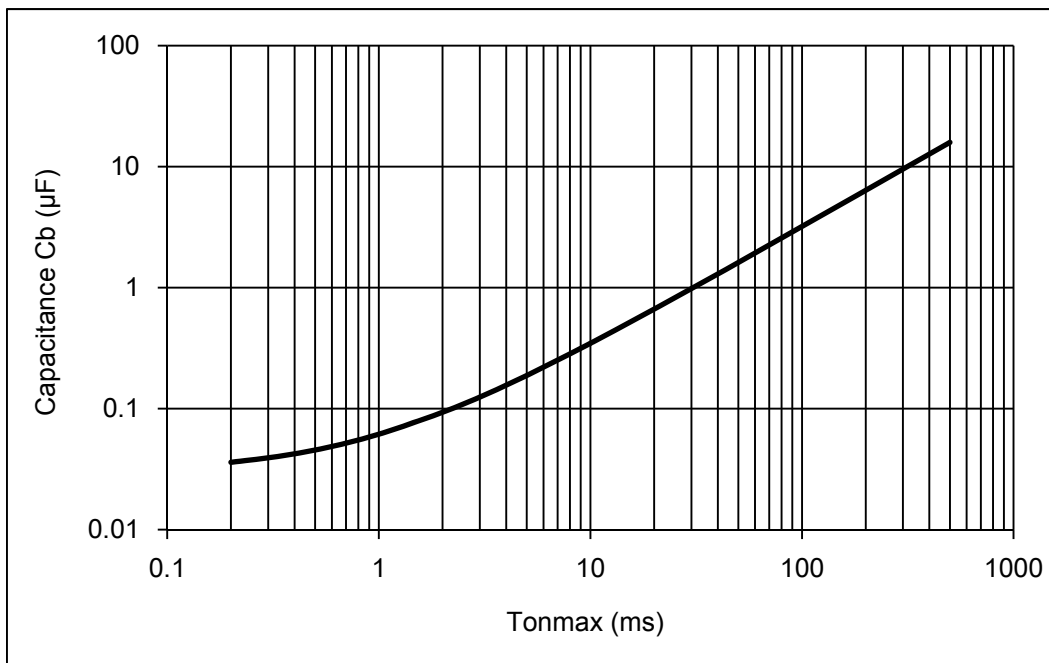


Fig. 16 TONMAX vs CB characteristic

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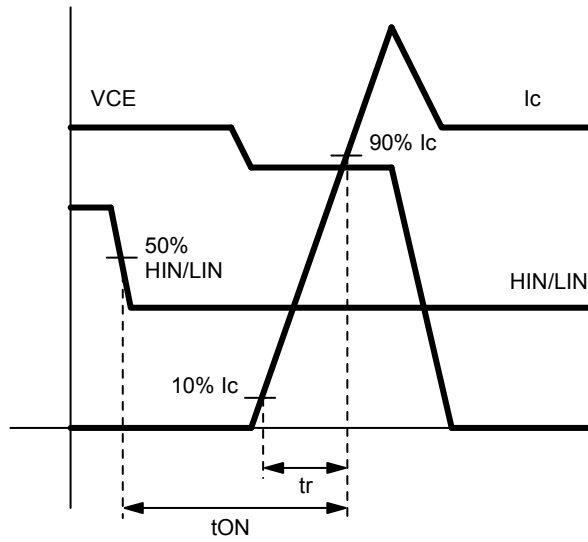


Fig. 17 Input to output propagation turn-on delay time

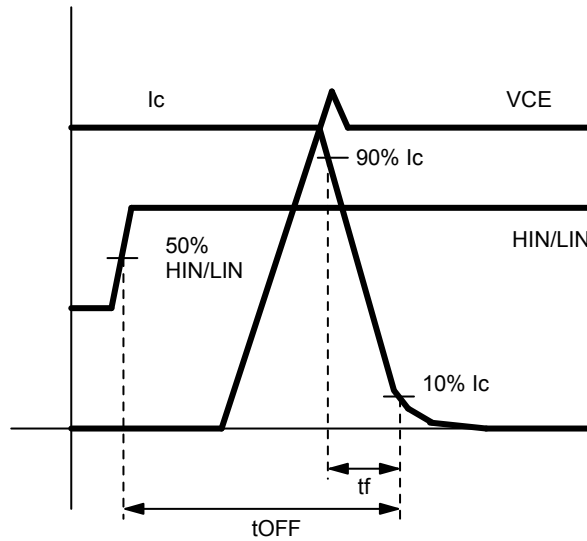


Fig. 18 Input to output propagation turn-off delay time

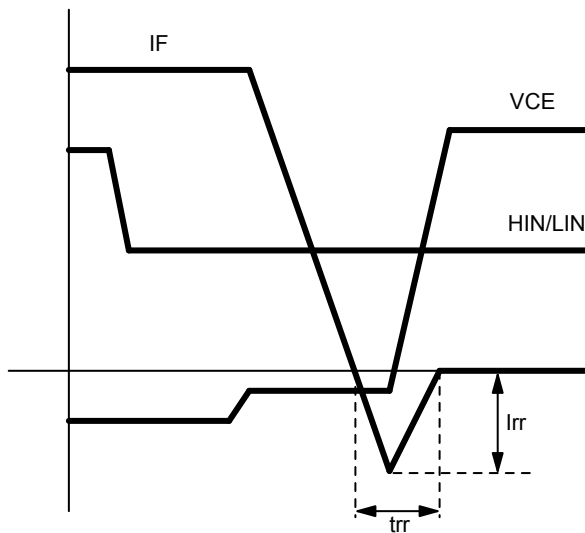
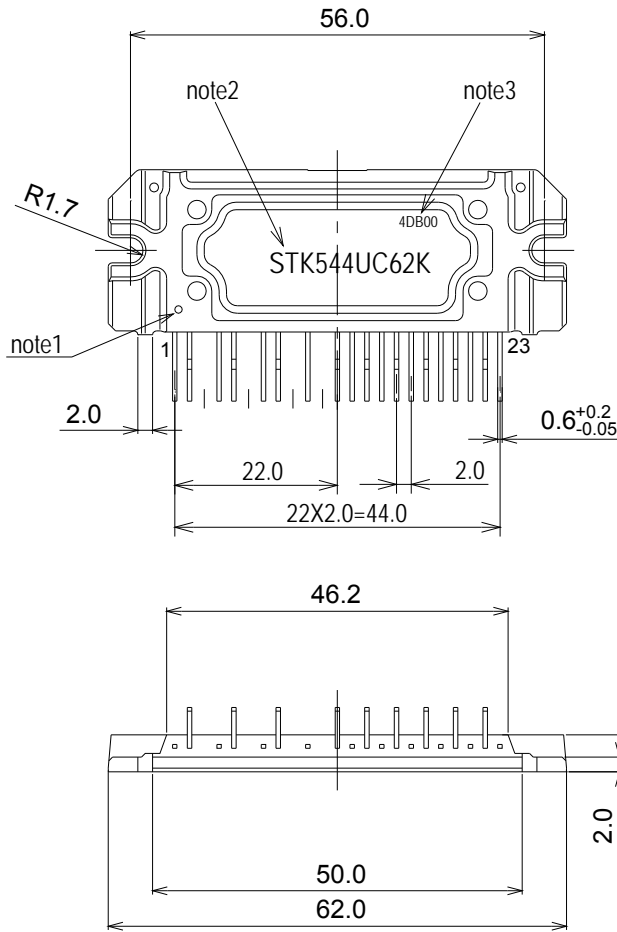


Fig. 19 Diode reverse recovery

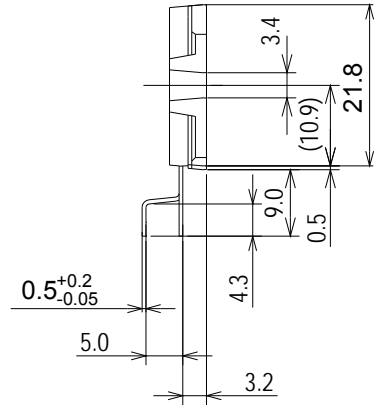
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PACKAGE DIMENSIONS

unit : mm



missing pin : 3,6,9,11



- note1 : Mark for No.1 pin identification.
- note2 : The form of a character in this drawing differs from that of IPM.
- note3 : This indicates the lot code.
The form of a character in this drawing differs from that of IPM.

The tolerances of length are +/- 0.5 mm unless otherwise specified.

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|--------------------|--------------------------|
| STK544UC62K-E | SIP23 (Pb-Free) | 8 / Tube |

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