ISL97678

8-Channel 45V, 50mA LED Driver

FN6998
Rev.3.00
Sep 8, 2017

The ISL97678 is an 8-channel PWM dimming LED driver for LCD backlight applications. The ISL97678 is capable of driving up to 96 pieces of 3.4V/50mA LEDs but larger numbers of LEDs are possible if the LED forward voltage combined is less than 45V. The ISL97678 has 8 channels of voltage controlled current sources with typical currents matching to ±1%, which compensate for the non-uniformity effect of forward voltages variance in the LED strings. To minimize the voltage headroom and power loss in the typical multi-string operation, the ISL97678 features dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for output regulation.

The ISL97678 features PWM dimming up to 30kHz with 0.4%~100% duty cycle and maintains ±1% current matching across all ranges. The PWM dimming frequency can be adjusted between 100Hz and 30kHz. The boost switching frequency can also be adjusted between 600kHz and 1.5MHz.

The ISL97678 features extensive protection functions that include string open and short circuit detections, OVP, and OTP.

The ISL97678 is available in the 32 Ld QFN 5mmx5mm and operate from -40°C to +85°C with input voltage ranges from 4.75V to 26V.

Related Literature

- For a full list of related documents, visit our website
  - ISL97678 product page

Features

- 8 channels
- 4.75V ~ 26V input
- 45V maximum output
- Drive typically 96 LEDs (3.4V/50mA each)
- External PWM input up to 20kHz dimming
- Dimming range 0.4%~100% up to 30kHz
- Current matching ±0.7% typical
- Protections
  - String open circuit and short circuit detections, OVP, and OTP
- Adjustable dimming frequency
- Adjustable switching frequency
- 32 Ld (5mmx5mm) QFN package

Applications

- Notebook displays WLED or RGB LED backlighting
- LCD monitor LED backlighting

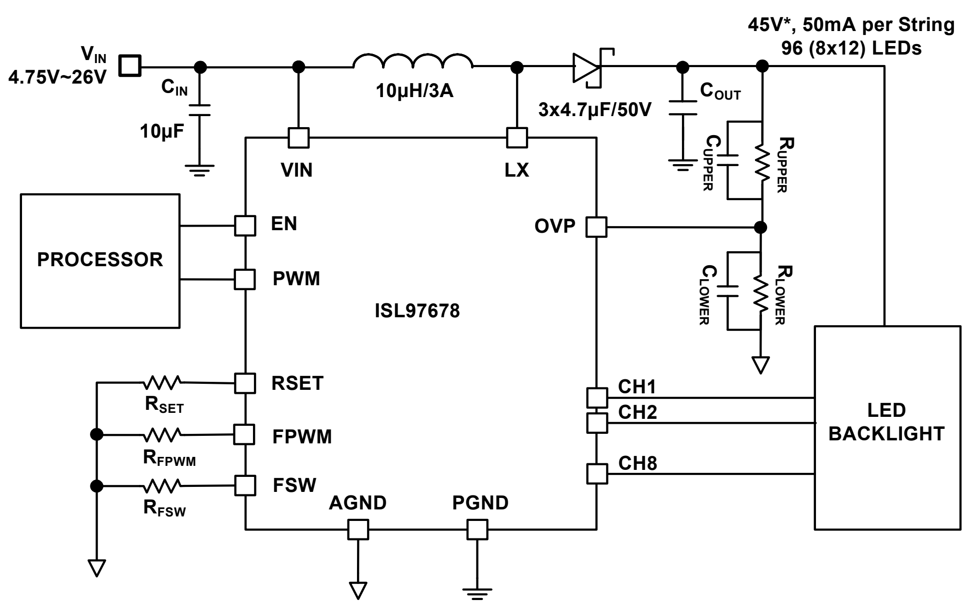


FIGURE 1. TYPICAL APPLICATION CIRCUIT: TFT-LCD NOTEBOOK DISPLAY

Typical Application Circuit

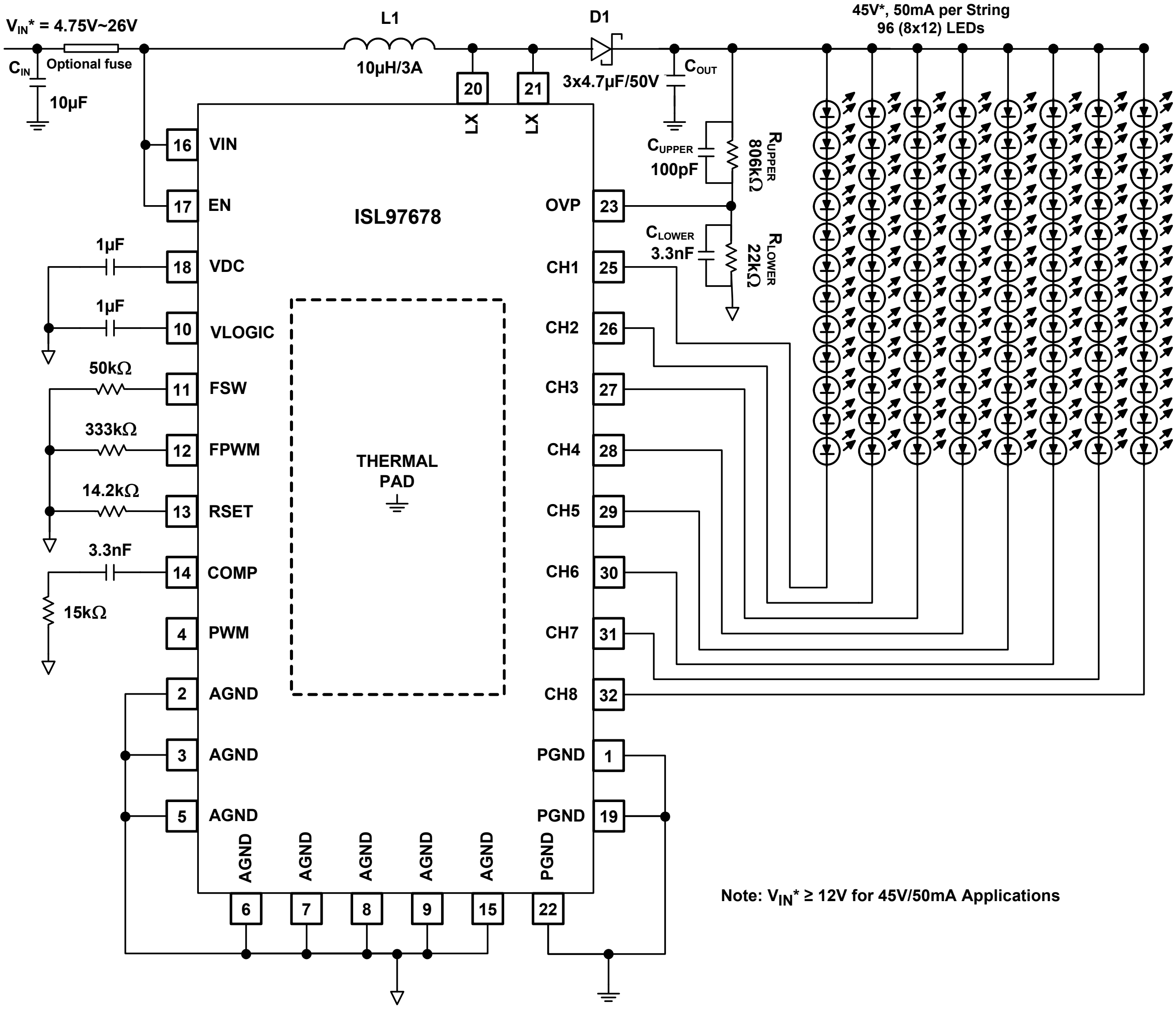


FIGURE 2. ISL97678 TYPICAL APPLICATION DIAGRAM

Block Diagram

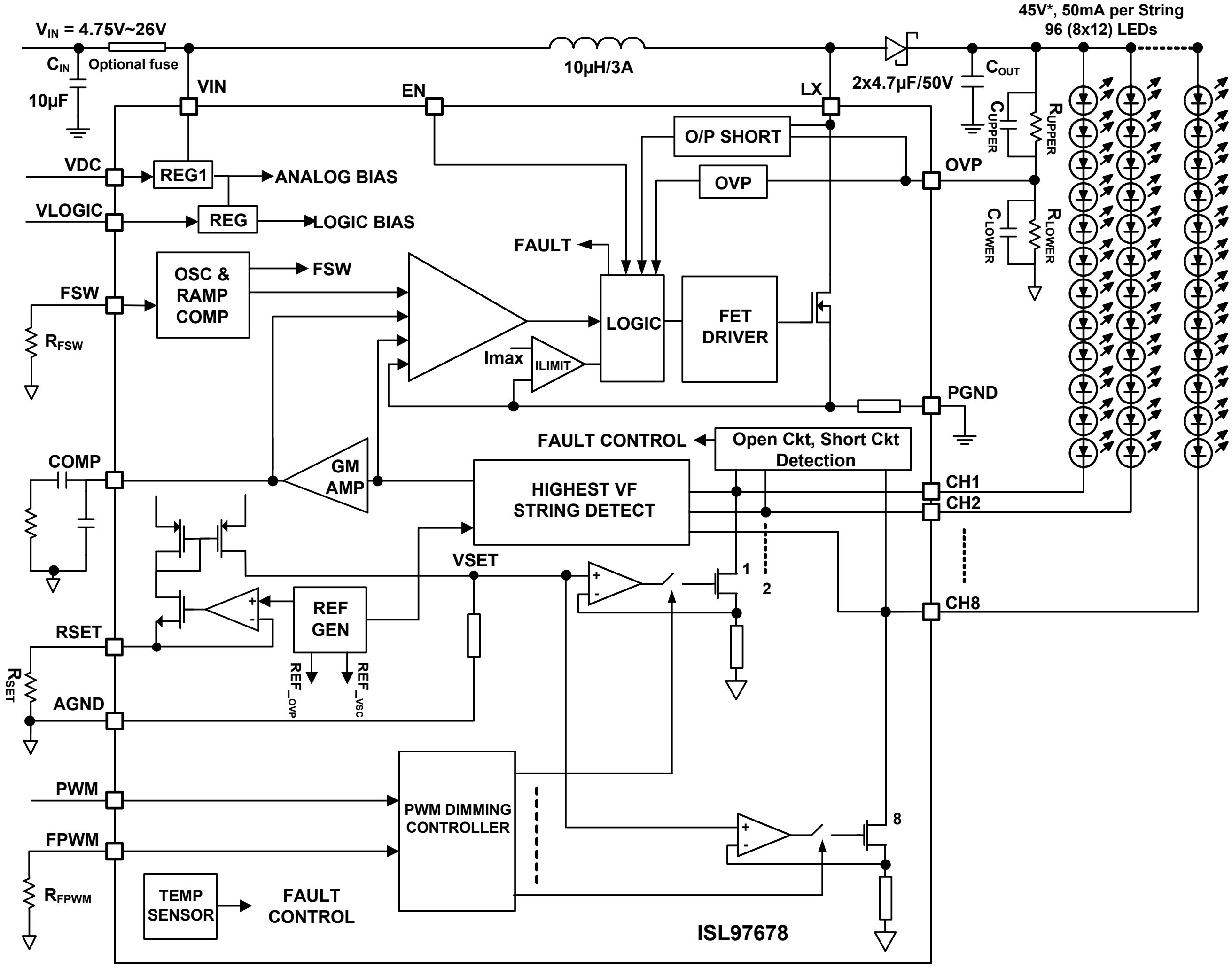


FIGURE 3. ISL97678 BLOCK DIAGRAM

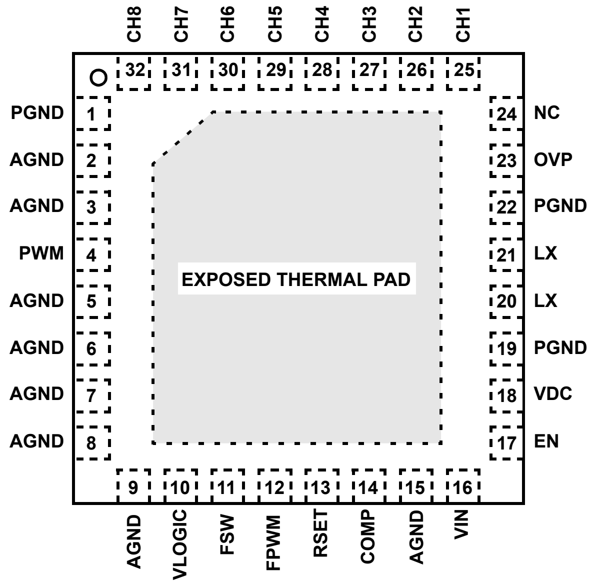
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL97678IRZ	ISL9767 8IRZ	32 Ld 5x5 QFN	L32.5x5B

NOTES:

1. Add “-T” suffix for 6k unit or “-TK” for 1k unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see the product information page for ISL97678. For more information on MSL, see TB363.

Pin Configuration



Pin Descriptions

(I = Input, O = Output, S = Supply)

PIN	NAME	TYPE	DESCRIPTION
1, 19, 22	PGND	S	Power Ground.
2, 3, 5, 6, 7, 8, 9, 15	AGND	S	Analog Ground.
4	PWM	I	PWM Brightness Control.
10	VLOGIC	O	Internal 2.5V Logic Bias Regulator. Need Decoupling Capacitor for Regulation.
11	FSW	I	When R_{FSW} is 100kΩ, f_{SW} is 500kHz. When R_{FSW} is 33kΩ, f_{SW} is 1.5MHz.
12	FPWM	I	When R_{FPWM} is 333kΩ, FPWM is 200Hz. When R_{FPWM} is 3.3kΩ, FPWM is 20kHz.
13	RSET	I	Resistor Connection for Setting LED Current.
14	COMP	O	Boost compensation.
16	VIN	S	Main Power.
17	EN	I	Enable
18	VDC	S	Internal 5V Analog Bias Regulator. Needs Decoupling Capacitor for Regulation.
20, 21	LX	O	Boost MOSFET Drain Terminal Switching Node.
23	OVP	I	Overvoltage Protection Input as well as Output Voltage FB Monitoring.
24	NC	I/O	No Connect
25 ~ 32	CH1 ~ CH8	I	LED Driver PWM Dimming Monitoring.

Absolute Maximum Ratings

Voltage ratings are all with respect to AGND pin
VIN . . . . -0.3V to 27V
EN . . . . -0.3V to 27V
VLOGIC . . . . -0.3V to 2.75V
VDC, PWM . . . . -0.3V to 5.75V
COMP, RSET, FPWM, FSW . . . . -0.3V to min
. . . . (VDC + 0.3V, 5.75V)
CH1 - CH8, LX, OVP. . . . . -0.3V to 45V
PGND, AGND . . . . -0.3V to +0.3V

Recommended Operating Conditions

Temperature Range . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN (Notes 4, 5)	31	3
Thermal Characterization (Typical, Note 6)		PSI_{JT} (°C/W)
32 Ld QFN		0.2

Maximum Continuous Junction Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C
Power Dissipation
T_A < +25°C 3.2W
T_A < +70°C 1.8W
T_A < +85°C 1.3W
T_A < +100°C 0.8W
Pb-Free Reflow Profile . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JA} and θ_{JC} thermal resistance ratings.

Electrical Specifications

All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 36kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
GENERAL						
V_{IN}	Backlight Supply Voltage		**4.75**		**26** (Note 8)	V
I_{VIN_SHDN}	VIN Shutdown Current	EN = 0			**5**	µA
V_{OUT}	Output Voltage				**45**	V
V_{UVLO}	Undervoltage Lockout Threshold		**2.9**		**3.3**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			300		mV
LINEAR REGULATOR						
V_{DC}	5V Analog Bias Regulator	V_{IN} > 6V	**4.8**	5	**5.1**	V
V_{DC_DROP}	VDC LDO Dropout Voltage	I_{VDC} = 30mA		71	**100**	mV
I_{VDC}	Active Current	EN = 5V, R = 33kΩ		10		mA
V_{LOGIC}	2.5V Logic Bias Regulator	V_{IN} > 6V	**2.3**	2.4	**2.5**	V
V_{LOGIC_DROP}	V_{LOGIC} LDO Dropout Voltage	I_{VLOGIC} = 30mA		31	**100**	mV
BOOST SWITCHING REGULATOR						
SS	Soft-Start			16		ms
SW_{ILimit}	Boost FET Current Limit	T_A = +25°C to +85°C	3.0		4.7	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance			130		mΩ
VFSW	f_{SW} Voltage	R_{FSW} = 33kΩ	**1.18**	1.21	**1.24**	V

Electrical Specifications All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 36kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Eff_peak	Peak Efficiency	V_{IN} = 24V, 96LEDs, 20mA each, L = 10µH with DCR ≤100mΩ, F_{SW} = 600kHz, T_A = +25°C		92.4		%
		V_{IN} = 12V, 96 LEDs, 20mA each, L = 10µH with DCR ≤100mΩ, F_{SW} = 600kHz, T_A = +25°C		91.5		%
		V_{IN} = 6V, 96 LEDs, 20mA each, L = 10µH with DCR ≤100mΩ, F_{SW} = 600kHz, T_A = +25°C		81.6		%
		V_{IN} = 24V, 80 LEDs, 40mA each, L = 10µH with DCR ≤100mΩ, F_{SW}=600kHz, T_A = +25°C		93.4		%
		V_{IN} = 12V, 80 LEDs, 40mA each, L = 10µH with DCR ≤100mΩ, F_{SW} = 600kHz, T_A = +25°C		90.7		%
D_{MAX}	Boost Maximum Duty Cycle	f_{SW} = 500kHz	**90**			%
D_{MIN}	Boost Minimum Duty Cycle	f_{SW} = 500kHz			**10**	%
f_{SW}	Boost Switching Frequency	R_{FSW} = 100kΩ	**0.45**	0.5	**0.55**	MHz
		R_{FSW} = 33kΩ	**1.35**	1.5	**1.65**	MHz
ILX_leakage	Lx Leakage Current	VLX = 45V, EN= 0V			**10**	µA
REFERENCE						
I_{MATCH}	Channel-to-Channel Current Matching	I_{LED} = 20mA	**-1.1**	±0.7	**+1.1**	%
I_{ACC}	Absolute Current Accuracy	R_{SET} = 36kΩ, T_A = +25°C	-1.5		+1.5	%
		R_{SET} = 36kΩ, T_A = -40°C to +80°C	-2		+2	%
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold		**3.3**		**4.6**	V
V_{temp}	Over-Temperature Threshold			150		°C
V_{temp_acc}	Over-Temperature Threshold Accuracy			5		°C
V_{OVP}	Overvoltage Limit on OVP Pin		**1.18**	1.22	**1.24**	V
DIGITAL INTERFACE						
V_{IL}	Logic Input Low Voltage				**0.8**	V
V_{IH}	Logic Input High Voltage		**1.5**		**5.5**	V
CURRENT SOURCES						
$V_{HEADROOM}$	Dominant Channel Current Source Headroom at CH Pin	I_{LED} = 50mA T_A = +25°C		1.0 (Note 10)		V
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at CHx Pin	I_{LED} = 50mA T_A = +25°C		90		mV
V_{RSET}	Voltage at RSET Pin		**1.18**	1.21	**1.24**	V

Electrical Specifications All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 36kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
ILEDmax	Maximum LED Current per Channel	LED config = 8P10S with VF = 3.4V and V_{IN} = 11V		50		mA
PWM GENERATOR						
FPWM	Generated PWM Frequency	R_{FPWM} = 330kΩ	**180**	200	**220**	Hz
		R_{FPWM} = 3.3kΩ	**18**	20	**22**	kHz
Dimming Range	PWM Dimming Duty Cycle Limits (Note 9)	f_{PWM} ≤ 30kHz	0.4		100	%
FPWMI	PWMI Input Frequency Range (Note 9)		200		20k	Hz
VFPWM	VFPWM Voltage	R_{FPWM} = 3.3kΩ	**1.18**	1.21	**1.25**	V

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. At maximum V_{IN} of 26V, minimum V_{OUT} is 28V. Minimum V_{OUT} can be lower at lower V_{IN}
9. Limits established by characterization and are not production tested.
10. Varies within range specified by $V_{HEADROOM\_RANGE}$.

Typical Performance Curves

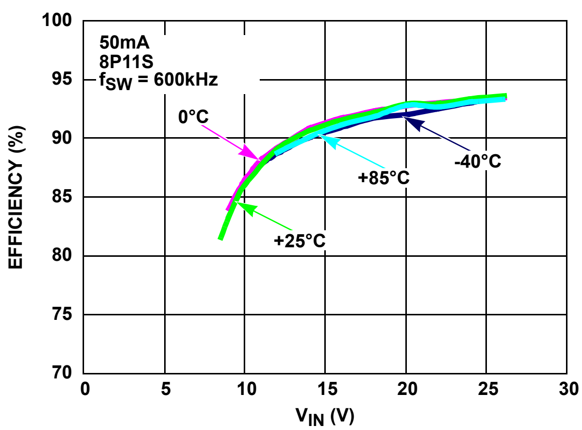


FIGURE 4. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 50mA

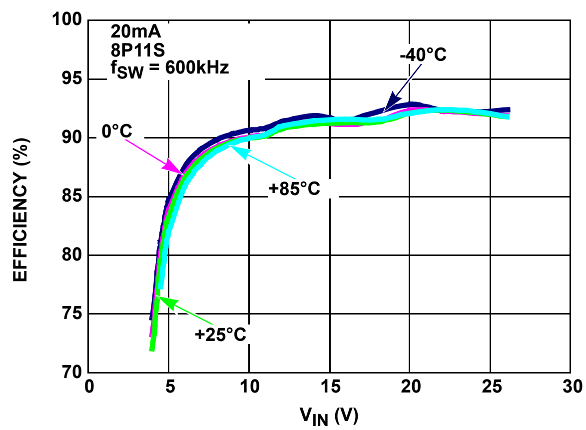


FIGURE 5. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA

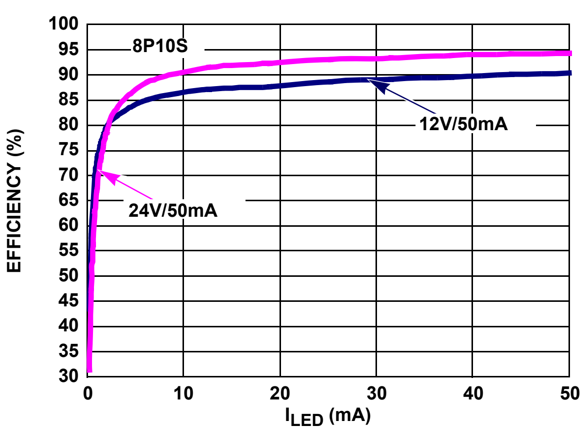


FIGURE 6. EFFICIENCY vs I_{LED}

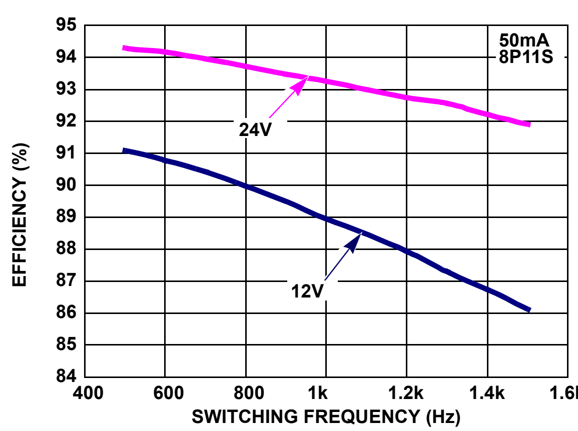


FIGURE 7. EFFICIENCY vs SWITCHING FREQUENCY

Typical Performance Curves (Continued)

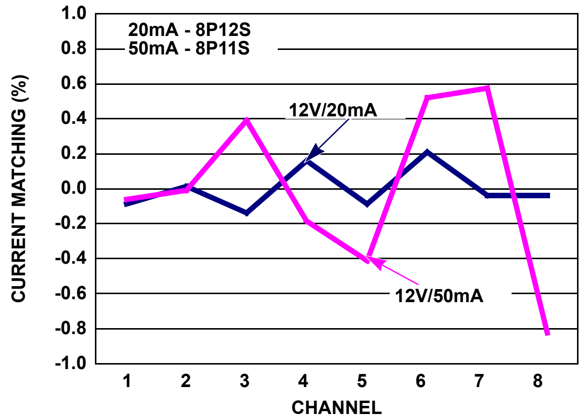


FIGURE 8. CHANNEL-TO-CHANNEL CURRENT MATCHING EXAMPLE

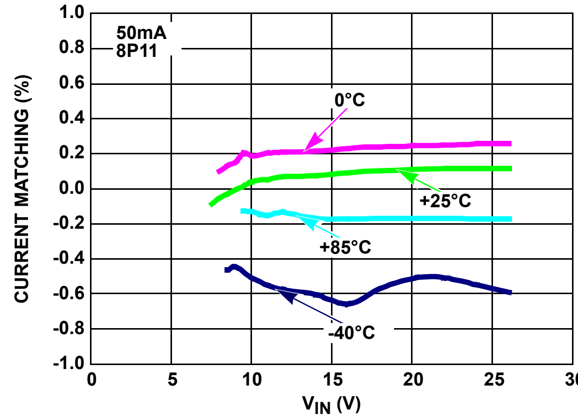


FIGURE 9. CURRENT MATCHING vs V_{IN} vs TEMPERATURE

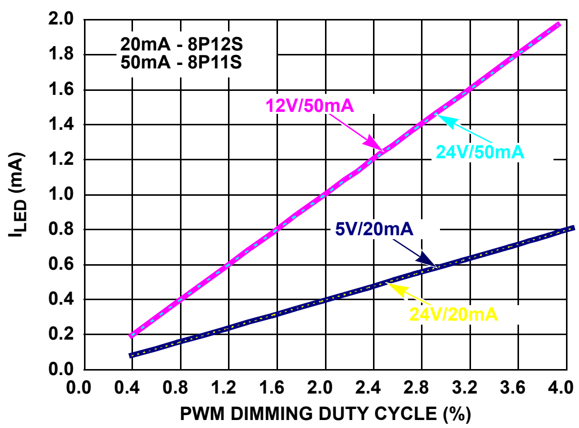


FIGURE 10. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE

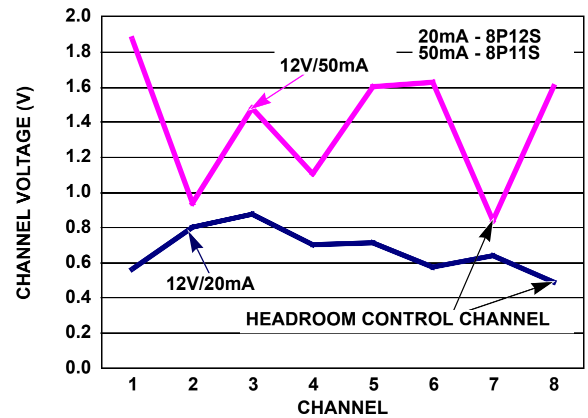


FIGURE 11. TYPICAL CHANNEL VOLTAGE EXAMPLE

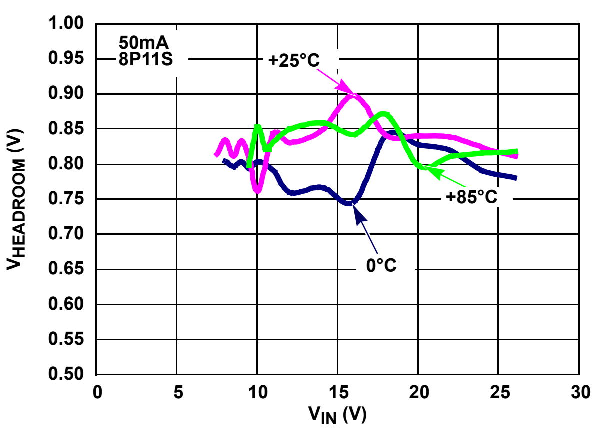


FIGURE 12. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 50mA

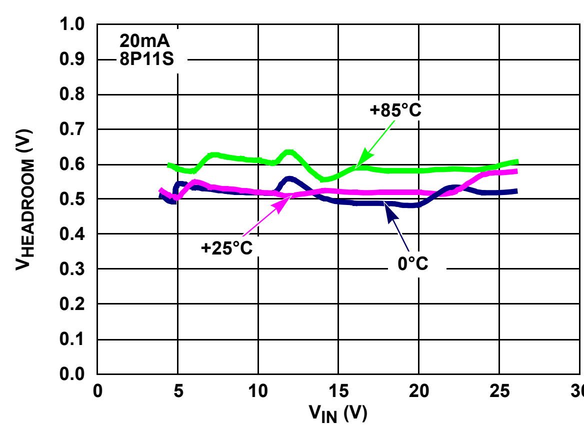


FIGURE 13. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 20mA

Typical Performance Curves (Continued)

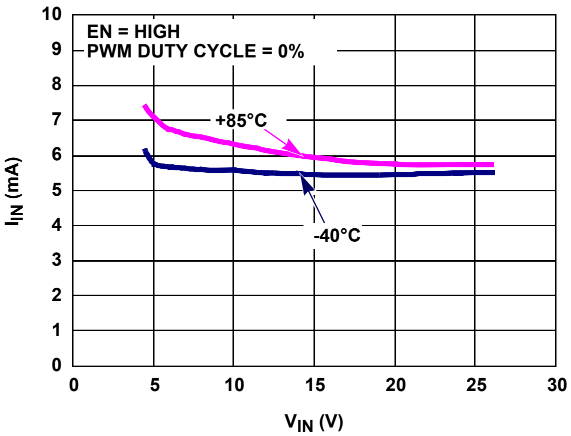


FIGURE 14. QUIESCENT CURRENT vs V_{IN} vs TEMPERATURE WITH ENABLE

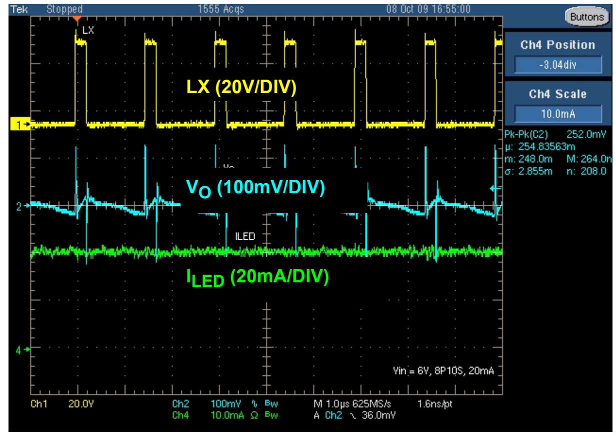


FIGURE 15. V_{OUT} RIPPLE VOLTAGE

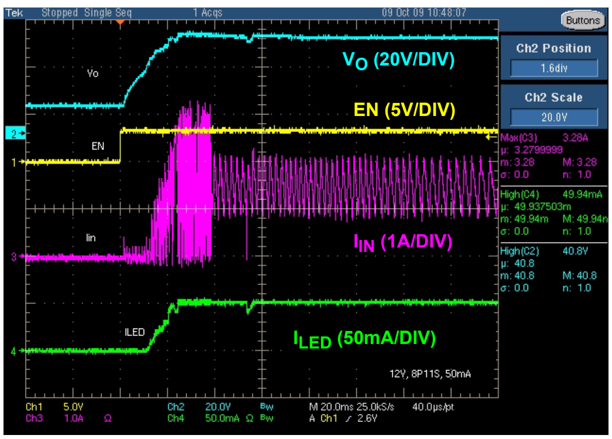


FIGURE 16. IN-RUSH CURRENT and LED CURRENT AT V_{IN} = 12V

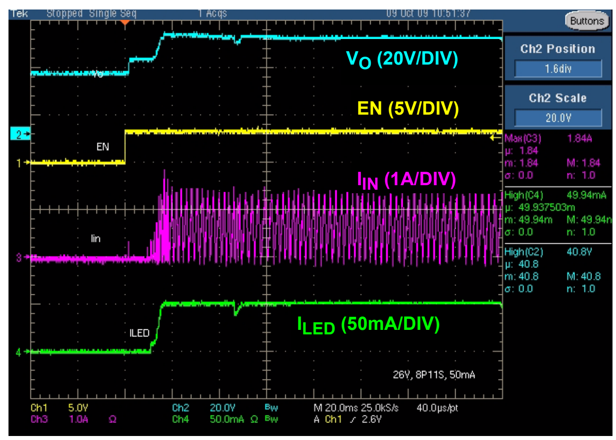


FIGURE 17. IN-RUSH CURRENT AND LED CURRENT AT V_{IN} = 26V

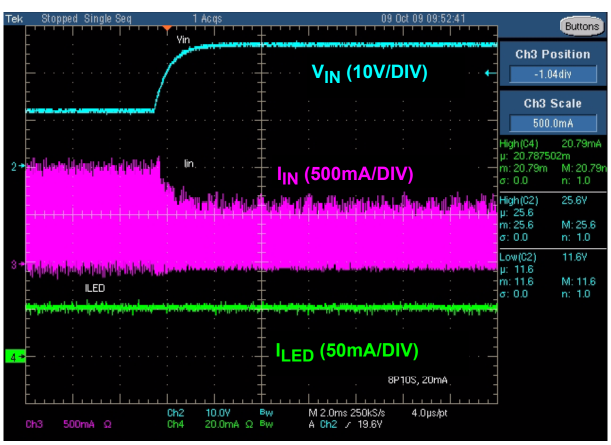


FIGURE 18. LINE REGULATION WITH V_{IN} CHANGES FROM 12V TO 26V DISABLE PROFILE

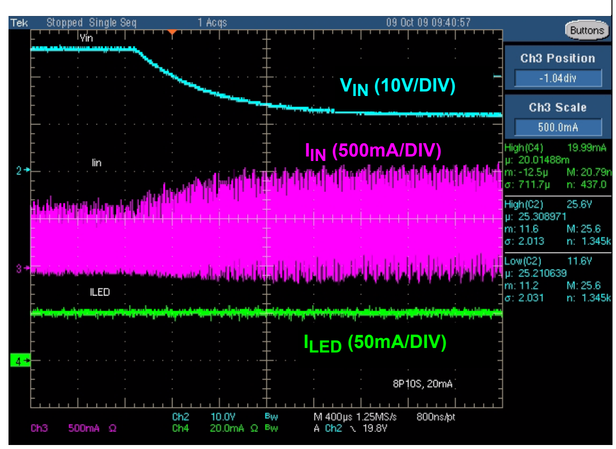


FIGURE 19. LINE REGULATION WITH V_{IN} CHANGES FROM 26V TO 12V

Typical Performance Curves (Continued)

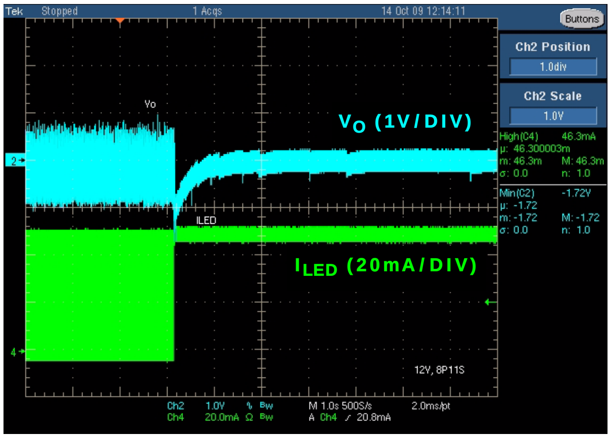


FIGURE 20. LOAD REGULATION WITH I_{LED} CHANGES FROM 0.4% TO 100% PWM DIMMING

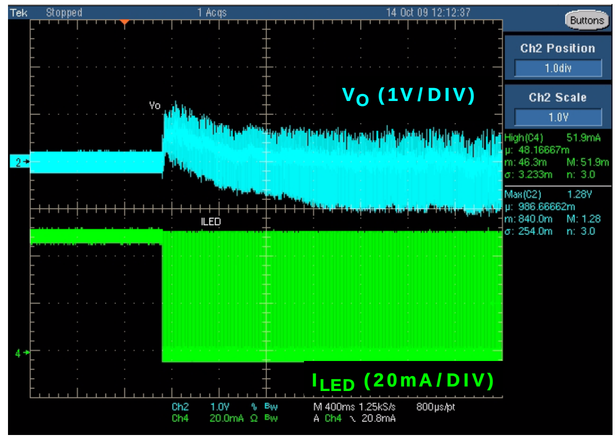


FIGURE 21. LOAD REGULATION WITH I_{LED} CHANGES FROM 100% TO 0.4% PWM DIMMING

FIGURE 22. LOAD REGULATION WITH I_{LED} CHANGES FROM 0% TO 100% PWM DIMMING

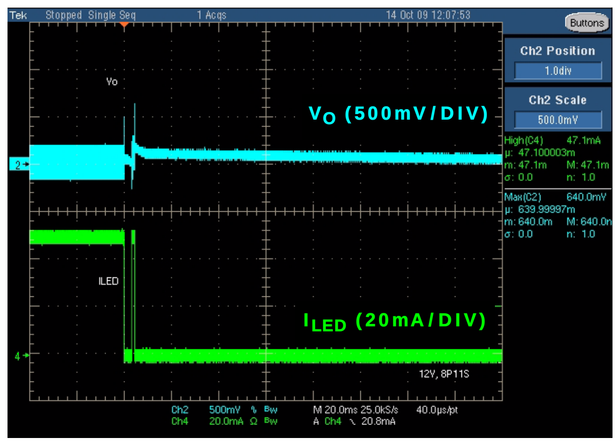


FIGURE 23. LOAD REGULATION WITH I_{LED} CHANGES FROM 100% to 0% PWM DIMMING

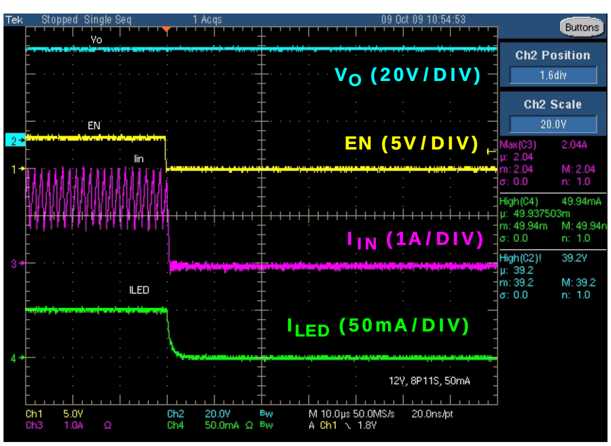


FIGURE 24. DISABLE PROFILE

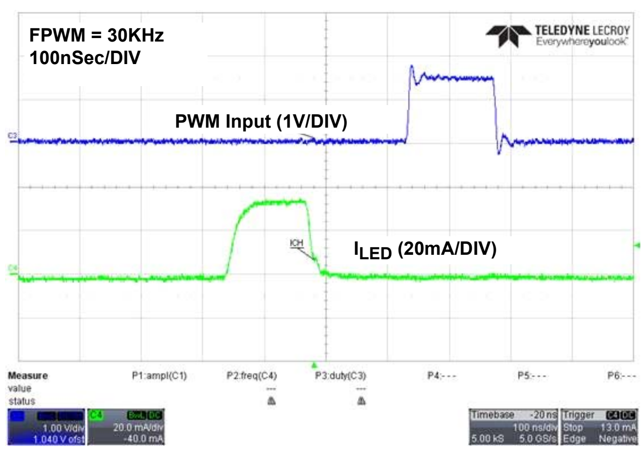


FIGURE 25. MINIMUM 0.4% PWM DIMMING DUTY CYCLE

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED string with the highest forward voltage drop to run at the programmed current. The ISL97678 employs current mode control boost architecture, which has a fast current sense loop and a slow voltage feedback loop. This architecture achieves a fast transient response that is essential for notebook backlight applications in which the power can be several Li-ion cell batteries that instantly change to an AC/DC adapter without rendering a noticeable visual nuisance. The number of LEDs that can be driven by the ISL97678 depends on the type of LED chosen in the application. The ISL97678 is capable of boosting up to 45V and drive eight channels of LEDs at a maximum of 45mA per channel.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 26.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $707.9/R_{SET}$. The sink terminals of the current source MOSFETs are designed to operate within a range at about 500mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amps offset, internal layout, reference, and current source resistors. These parameters are optimized for current matching and absolute current accuracy. However, the absolute accuracy is additionally determined by the external R_{SET}. A 0.1% tolerance resistor is recommended.

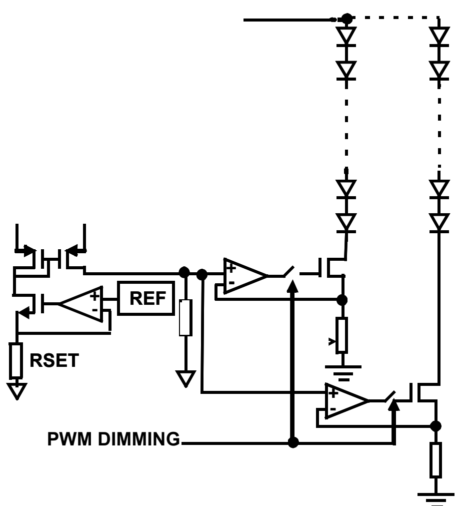


FIGURE 26. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97678 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CH pins. When this lowest I_{IN} voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest CH pin is at the target headroom voltage.

Because all LED strings are connected to the same output voltage, the other CH pins will have a higher voltage, but the regulated current source circuit on each channel ensures that each channel has the same programmed current. The output voltage regulates cycle-by-cycle and is always referenced to the highest forward voltage string in the architecture.

OVP and V_{OUT} Requirement

The Overvoltage Protection (OVP) pin sets the overvoltage trip level and limits the V_{OUT} regulation range.

The ISL97678 OVP threshold is set by R_{UPPER} and R_{LOWER} as shown in Equation 1:

$$V_{OUT\_OVP} = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 1)}$$

V_{OUT} can regulate only between 64% and 100% of the $V_{OUT-OVP}$ such that:

Allowable V_{OUT} = 64% to 100% of $V_{OUT-OVP}$

For example, if 10 LEDs are used with the worst case V_{OUT} of 35V. If R_{UPPER} and R_{LOWER} are chosen such that the OVP level is set at 40V, then the V_{OUT} is allowed to operate between 25.6V and 40V. If the requirement is changed to a 6 LEDs 21V V_{OUT} application, then the OVP level must be reduced and users should follow V_{OUT} = (64% ~100%) OVP requirement. Otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected and sometimes it can prevent the driver from operating properly.

The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER} = 1/33 with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF.

Dimming Controls

The ISL97678 provides two ways of controlling the LED current, and therefore the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

There are various ways to achieve DC or PWM current control, which will be described in the following.

In any dimming controls, the EN pin must be high. EN is a high voltage pin that can be applied with a digital signal or tied directly to V_{IN} for enable function.

MAXIMUM DC CURRENT SETTING

The initial brightness should be set by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{707.9}{R_{SET}} \quad \text{(EQ. 2)}$$

Alternatively, the R_{SET} can be replaced by a digital potentiometer for adjustable current.

PWM CONTROL

The ISL97678 provides PWM dimming by PWM chopping of the current in the LEDs for all eight channels. To achieve PWM dimming, the user must apply a PWM signal at the PWM pin. The PWM output follows the PWM input and the dimming frequency is set by R_{PWM}. During the On periods, the LED current is defined by the value of R_{SET}, as described in Equation 1.

PWM Dimming Frequency Adjustment

The dimming frequencies are set by an external resistor at the FPWM pin as shown by Equation 3:

$$f_{PWM} = \frac{6.66 \times 10^7}{R_{FPWM}} \qquad \text{(EQ. 3)}$$

where f_{PWM} is the desirable PWM dimming frequency and R_{FPWM} is the setting resistor. f_{PWM} range is from 100Hz to 30kHz.

Switching Frequency

The boost switching frequency can be adjusted by a resistor as shown in Equation 4:

$$f_{SW} = \frac{(5 \times 10^{10})}{R_{FSW}} \qquad \text{(EQ. 4)}$$

where f_{SW} is the desirable boost switching frequency and R_{FSW} is the setting resistor.

5V and 2.3V Low Dropout Regulators

A 5V LDO regulator is present at the VDC pin to develop the necessary low voltage supply, which is used by the chips internal control circuitry. Because VDC is an LDO pin, it requires a bypass capacitor of 1µF or more for the regulation. The VDC pin can be used for a coarse regulator or reference but does not pull more than a few mA from it.

Similarly, a 2.3V LDO regulator is present at the VLOGIC pin to develop the necessary low voltage supply for the chip's internal logic control circuitry. A 1µF bypass capacitor or more is needed for regulation. The VLOGIC pin can be used as a coarse regulator or reference but does not pull more than a few mA from it.

Soft-Start

The ISL97678 uses a digital soft-start in which the boost current limit is stepped up in eight steps. The initial current limit level is set to one ninth of the full current limit, with subsequent steps increasing this by a ninth every 2ms. If no LEDs are conducting during the interval since the last step (for example, if the LEDs are running at a low duty cycle at a low PWM frequency) then the step will be delayed until the LEDs are conducting. If the LEDs are disabled and re-enabled again then soft-start will be restarted when the LEDs are enabled.

Fault Protection and Monitoring

The ISL97678 features extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can take the form of either infinite resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97678 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED strings to fault out. See Table 1 for more details.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above the programmed short circuit threshold. When an LED becomes shorted, the action taken is described in Table 1. The short circuit threshold is 4V.

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97678 monitors the current in each channel such that any string which reaches the intended output current is considered "good". If the current subsequently falls below the target, the channel is considered an "open circuit". Furthermore, if the boost output of the ISL97678 reaches the OVP limit or if the lower over-temperature threshold is reached, all channels that are not "good" are immediately considered as "open circuit". Detection of an "open circuit" channel results in a time-out before disabling of the affected channel.

Some users employ LEDs that have zener diode structure in parallel with the LED for ESD enhancement, thus enabling open circuit operation. When this type of LED goes open circuit, the effect is as if the LED forward voltage has increased, but no light will be emitted. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, so as to make sure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channel look as if they have LED shorts. See Table 1 for details for responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as shown in Equation 5:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \qquad \text{(EQ. 5)}$$

These resistors should be large to minimize the power loss. For example, a 1MkΩ R_{UPPER} and 30kΩ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the

PWM Off time. Parallel capacitors should be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.8V, the device will stop switching and be reset. Operation will restart only if the device control interface re-enables it once the input voltage is back in the normal operating range. Also all digital settings will be reset to their default states.

Over-Temperature Protection (OTP)

The ISL97678 includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level significantly below the regulation target will be treated as “open circuit” and disabled after a time-out period. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off and stay off until the control driver is power off and re-enables it. For the extensive fault protection conditions, please refer to Figure 27 and Table 1 for details.

Shutdown

When the EN pin is low the entire chip is shut down to give close to zero shutdown current. The digital interfaces will not be active during this time.

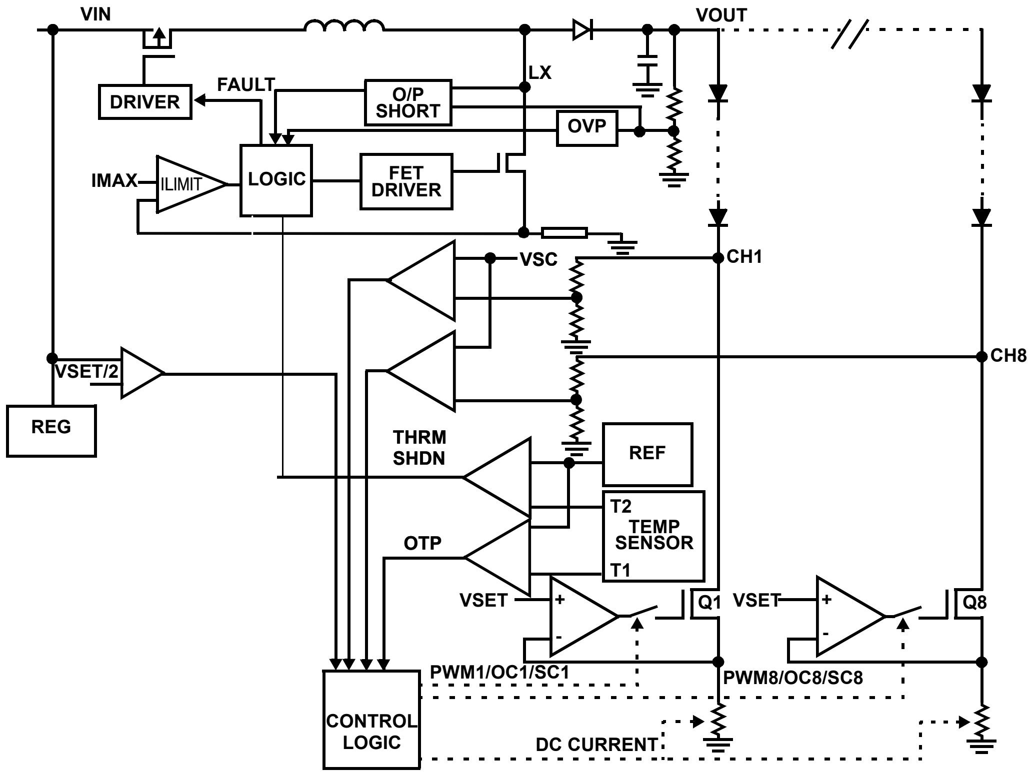


FIGURE 27. SIMPLIFIED FAULT PROTECTIONS

TABLE 1. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH1 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and VI_{IN0} < VSC	CH1 ON and burns power	CH2 through CH8 Normal	Highest VF of CH2 through CH8
2	CH1 Short Circuit	Upper OTP triggered but VI_{IN1} < VSC	CH1 goes off	Same as CH1	Highest VF of CH2 through CH8

TABLE 1. PROTECTIONS TABLE (Continued)

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
3	CH1 Short Circuit	Upper OTP not triggered but VI_{IN1} > VSC	CH1 disabled after 6 PWM cycles time-out.	If 3 channels are already shut down, all channels will be shut down. Otherwise CH2-8 will remain as normal	Highest VF of CH2 through CH8
4	CH1 Open Circuit with infinite resistance	Upper OTP not triggered and VI_{IN1} < VSC	V_{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V_{OUT} will drop to normal level.	CH2 through CH8 Normal	Highest VF of CH2 through CH8
5	CH1 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and VI_{IN1} < VSC	CH1 remains ON and has highest VF, thus V_{OUT} increases	CH2 through CH8 ON, Q2 through Q8 burn power	VF of CH1
6	CH1 LED Open Circuit but has paralleled Zener	Upper OTP triggered but VI_{IN1} < VSC	CH1 goes off	Same as CH1	VF of CH1
7	CH1 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but VI_{IN1} > VSC	CH1 OFF	CH2 through CH8 Normal	Highest VF of CH2 through CH8
		Upper OTP not triggered but VI_{INx} > VSC	CH1 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases then CH-X switches OFF. This is an unwanted shut off and can be prevented by setting OVP and/or VSC at an appropriate level.	VF of CH1
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but VI_{INx} < VSC	Any channel at below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest VF of CH1 through CH8
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but VI_{INx} < VSC	All channels switched off		Highest VF of CH1 through CH8
10	Output LED string voltage too high	V_{OUT} > VOVP	Driven with normal current. Any channel that is below the target current will time-out after 6 PWM cycles.		Highest VF of CH1 through CH8
11	V_{OUT}/LX shorted to GND		LX will not switch		

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On-time is equal to the change of inductor current during the switching regulator Off-time. The voltage across an inductor is as shown in Equation 6:

$$V_L = L \times \Delta I_L / \Delta t \qquad \text{(EQ. 6)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \qquad \text{(EQ. 7)}$$

where D is the switching duty cycle defined by the turn-on time over the switching periods. V_D is Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as Equations 8 and 9:

$$V_O/V_I = 1/(1 - D) \qquad \text{(EQ. 8)}$$

$$D = (V_O - V_I)/V_O \qquad \text{(EQ. 9)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum and saturation current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance, and stability.

The inductor's maximum current capability must be adequate enough to handle the peak current at the worst case condition. Additionally, if an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off-period, as expressed in Equation 10:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_{SW} \tag{EQ. 10}$$

The choice of 85% is an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and f_{SW} as a result, for a given switching.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
9/8/2017	FN6998.3	Added VHEADROOM_RANGE spec to the Electrical Specifications table. Added Note 11. In "Current Matching and Current Accuracy" on page 11, updated the second sentence in the second paragraph for clarification. Added Related Literature section. Applied new header/footer.
3/22/2014	FN6998.2	Changed PWM dimming "0.8%~100% duty cycle" to "0.4%~100% duty cycle" on the front page. Changed External PWM Input "25kHz" to "20kHz" in the Features section in order to be consistent with Electrical Specifications. Updated Application Circuit and Block Diagram drawings along with the resistor and capacitor names. Moved the VFSW specification to the BOOST SWITCHING REGULAR section of the Electrical Specifications table. Changed "/SHUT" to "EN" to be consistent with the Pin Descriptions table. Changed "I_{SET}" to "R_{SET}" for the LED current setting resistor to be consistent across the datasheet. Changed "V_{ISET}" to "V_{RSET}" to be consistent with the RSET pin name. Changed "R_{OSC}" to "R_{FSW}" to be consistent across the datasheet. Changed "R_1" and "R_2" to "R_{UPPER}" and "R_{LOWER}", respectively in OVP and V_{OUT} Requirement section. Added FIGURE 1. TYPICAL APPLICATION CIRCUIT: TFT-LCD NOTEBOOK DISPLAY. Added FIGURE 25. MINIMUM 0.4% PWM DIMMING DUTY CYCLE. Updated "Package Outline Drawing" on page 17 to the latest revision.
11/5/09	FN6998.1	Changed VSC spec from "3.3min, 4.4max" to "3.3min, 4.6max".
10/26/09	FN6998.0	Initial release

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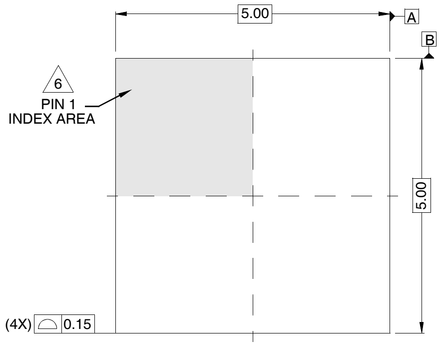
Package Outline Drawing

For the most recent package outline drawing, see L32.5x5B.

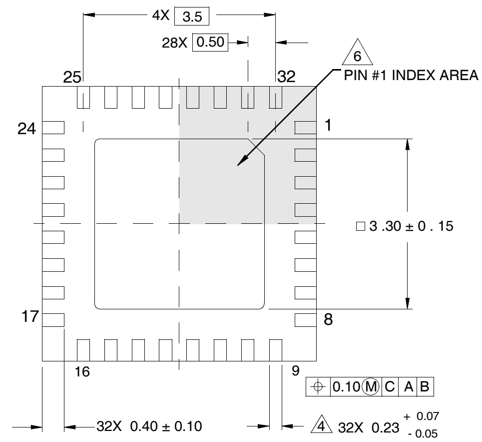
L32.5x5B

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

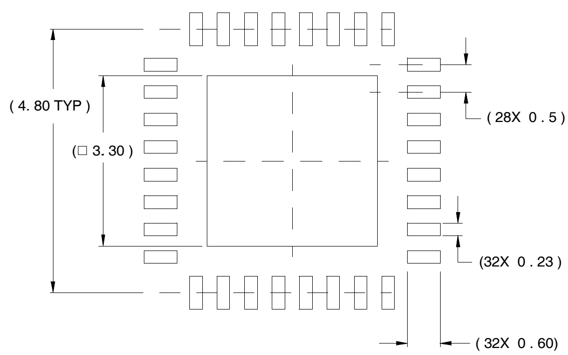
Rev 3, 5/10



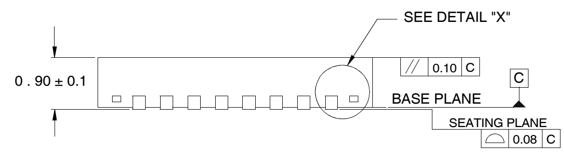
TOP VIEW



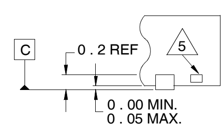
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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