

MC100LVEL17

3.3V ECL Quad Differential Receiver

Description

The MC100LVEL17 is a 3.3 V ECL, quad differential receiver. The device is functionally equivalent to the E116 device with the capability of operation from either a -3.3 V or $+3.3$ V supply voltage.

Under open input conditions, the \overline{D} input will be biased at $V_{CC}/2$ and the D input will be pulled down to V_{EE} . This operation will force the Q output LOW and ensure stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a $0.01 \mu\text{F}$ capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

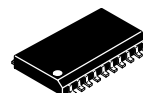
Features

- 325 ps Propagation Delay
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -3.8 V
- Internal Input Pulldown Resistors D Inputs; Pullup and Pulldown on \overline{D} Inputs
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Pb-Free Packages are Available*



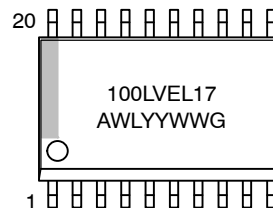
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**SO-20 WB
DW SUFFIX
CASE 751D**

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC100LVEL17

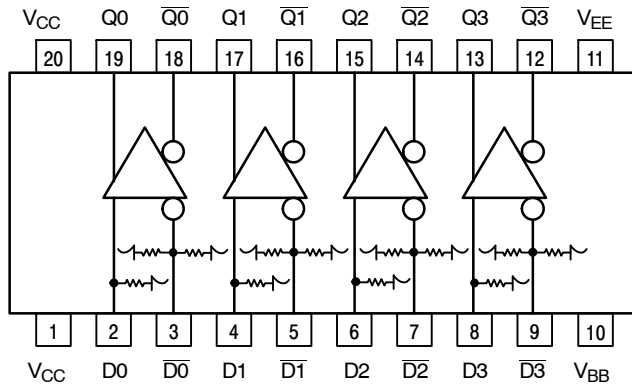


Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|---------------------|-------------------------------|
| Dn, \overline{Dn} | ECL Differential Data Inputs |
| Qn, \overline{Qn} | ECL Differential Data Outputs |
| V _{BB} | Reference Voltage Output |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |

* All V_{CC} pins are tied together on the die.
Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout: (Top View)

Table 2. ATTRIBUTES

| Characteristics | Value |
|--|---|
| Internal Input Pulldown Resistor | 75 k Ω |
| Internal Input Pullup Resistor | 75 k Ω |
| ESD Protection | Human Body Model Machine Model Charged Device Model |
| Moisture Sensitivity, (Note 1) | > 2 kV > 200 V > 4 kV |
| Pb (Indefinite Time Out of Drypack) Pb-Free | Level 1 Level 3 |
| Flammability Rating | Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in |
| Transistor Count | 141 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|-------------------|--------------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 8 to 0 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | –8 to 0 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 to 0 –6 to 0 | V V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I _{BB} | V _{BB} Sink/Source | | | ± 0.5 | mA |
| T _A | Operating Temperature Range | | | –40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | –65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction–to–Ambient) | 0 lfpm 500 lfpm | SO–20L SO–20L | 90 60 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction–to–Case) | Standard Board | SO–20L | 30 to 35 | °C/W |
| T _{sol} | Wave Solder Pb Pb–Free | <2 to 3 sec @ 248°C <2 to 3 sec @ 260°C | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 2)

| Symbol | Characteristic | –40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------|--|-------------|------|------|-------------|------|------|-------------|------|------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Power Supply Current | | 26 | 31 | | 26 | 31 | | 27 | 33 | mA |
| V _{OH} | Output HIGH Voltage (Note 3) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| V _{OL} | Output LOW Voltage (Note 3) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| V _{IH} | Input HIGH Voltage (Single–Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V _{IL} | Input LOW Voltage (Single–Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| V _{BB} | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| V _{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 4) | | | | | | | | | | |
| | V _{pp} < 500 mV | 1.3 | | 2.9 | 1.2 | | 2.9 | 1.2 | | 2.9 | V |
| | V _{pp} ≥ 500 mV | 1.5 | | 2.9 | 1.4 | | 2.9 | 1.4 | | 2.9 | V |
| I _{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I _{IL} | Input LOW Current | | | | | | | | | | |
| | Dn Dn | 0.5 –300 | | | 0.5 –300 | | | 0.5 –300 | | | μA μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
- Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.
- V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

MC100LEVEL17

Table 5. LVNECL DC CHARACTERISTICS $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 5)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 26 | 31 | | 26 | 31 | | 27 | 33 | mA |
| V_{OH} | Output HIGH Voltage (Note 6) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 6) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 7) | | | | | | | | | | |
| | $V_{pp} < 500\text{ mV}$ | -2.0 | | -0.4 | -2.1 | | -0.4 | -2.1 | | -0.4 | V |
| | $V_{pp} \geq 500\text{ mV}$ | -1.8 | | -0.4 | -1.9 | | -0.4 | -1.9 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | D_n | 0.5 | | 0.5 | | | 0.5 | | | μA |
| | | $\overline{D_n}$ | -300 | | -300 | | | -300 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.

6. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

7. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V .

Table 6. AC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 8)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|------------|-----|-----------------|------------|------|-----------------|------------|-----|-----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency | | | | | 1.75 | | | | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay D to Q Diff S.E. | 330 280 | | 530 580 | 350 300 | | 550 600 | 360 310 | | 560 610 | ps |
| t_{SKEW} | Skew Output-to-Output (Note 9) Part-to-Part (Diff) (Note 9) Duty Cycle (Diff) (Note 10) | | | 75 200 25 | | | 75 200 25 | | | 75 200 25 | ps |
| t_{JITTER} | Random Clock Jitter (RMS) | | | | | 0.7 | | | | | ps |
| V_{PP} | Input Swing (Note 11) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t_r t_f | Output Rise/Fall Times Q (20% – 80%) | 280 | | 550 | 280 | | 550 | 280 | | 550 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. V_{EE} can vary $\pm 0.3\text{ V}$.

9. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.

10. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

11. $V_{PP(min)}$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .

MC100LVEL17

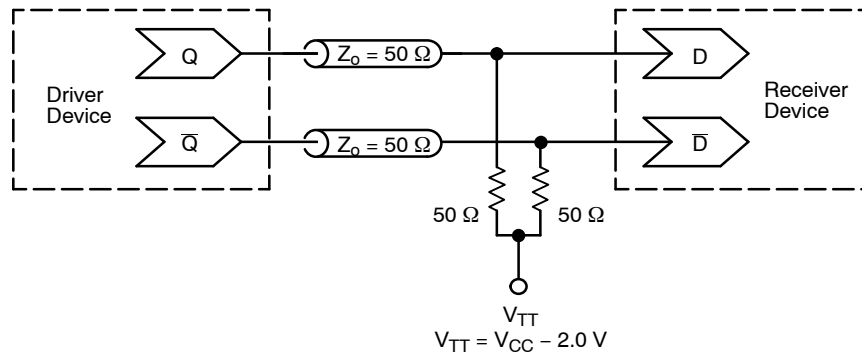


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|-----------------------|-----------------------|
| MC100LVEL17DW | SO-20 WB | 38 Units / Rail |
| MC100LVEL17DWG | SO-20 WB (Pb-Free) | 38 Units / Rail |
| MC100LVEL17DWR2 | SO-20 WB | 1000 / Tape & Reel |
| MC100LVEL17DWR2G | SO-20 WB (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

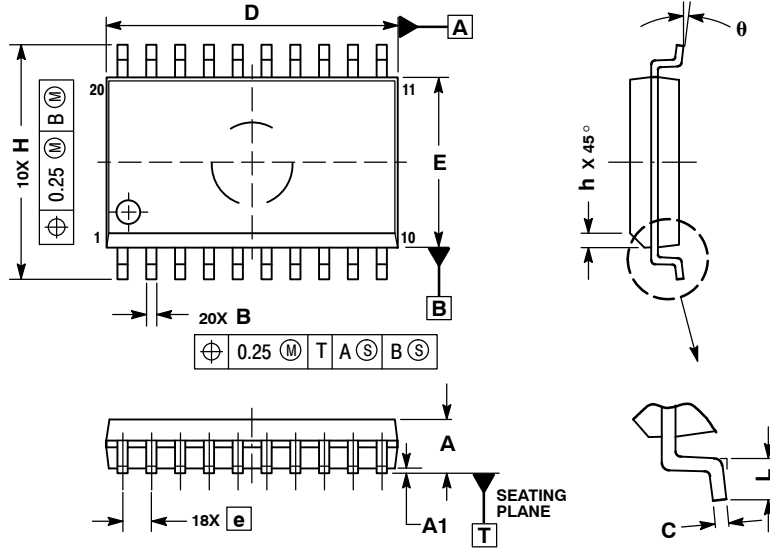
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC100LVEL17

PACKAGE DIMENSIONS

SO-20 WB
DW SUFFIX
CASE 751D-05
ISSUE G



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 | BSC |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| theta | 0 ° | 7 ° |

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