



Vishay Siliconix

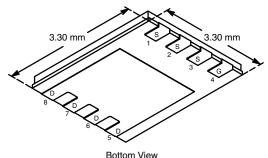
N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I _D (A) ^f	Q _g (Typ.)			
30	0.0033 at V _{GS} = 10 V	35 ^g	33.5 nC			
30	0.0043 at V _{GS} = 4.5 V	35 ^g	33.3110			

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % $\rm R_{\rm g}$ and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

HALOGEN FREE

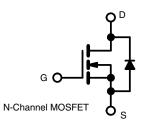


PowerPAK® 1212-8

Ordering Information: SiS444DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Motor Control
- Industrial
- Load Switch
- **ORing**



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	30	V	
Gate-Source Voltage		V_{GS}	± 20		
	T _C = 25 °C	I _D	35 ^g		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C		35 ^g		
Continuous Diain Current (1) = 150 °C)	T _A = 25 °C		24.9 ^{a, b}		
	T _A = 70 °C		20 ^{a, b}	A	
Pulsed Drain Current (t = 300 μs)		I _{DM}	70	7 ^	
Continuous Source-Drain Diode Current	T _C = 25 °C	1-	35 ^g		
Continuous Source-Drain Diode Current	T _A = 25 °C	'S	3.3 ^{a, b}		
Single Pulse Avalanche Current Single Pulse Avalanche Energy L = 0.1 mH		I _{AS}	20		
		E _{AS}	20	mJ	
	T _C = 25 °C		52		
Maximum Power Dissipation	T _C = 70 °C	P _D	43	w	
Maximum Power Dissipation	T _A = 25 °C		3.7 ^{a, b}	T **	
	T _A = 70 °C		3.1 ^{a, b}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{c, d}			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, e}	t ≤ 10 s	R _{thJA}	24	33	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4] 5/**	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. See solder profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- e. Maximum under steady state conditions is 81 °C/W. f. Based on $T_{\rm C}$ = 25 °C.
- g. Package limited.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					I.	ı	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			٧	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		30		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.6			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.2		2.3	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μΑ	
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a	` /	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		0.0026	0.0033	Ω	
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$		0.0034	0.0043		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A		65		S	
Dynamic ^b					<u> </u>	1	
Input Capacitance	C _{iss}			3065		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		406			
Reverse Transfer Capacitance	C _{rss}			360			
Tatal Cata Charma	Q _g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		68	102	nC	
Total Gate Charge				33.5	51		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		7.7			
Gate-Drain Charge	Q_{gd}			13.8			
Gate Resistance	R_{g}	f = 1 MHz	0.3	0.7	1.4	Ω	
Turn-On Delay Time	t _{d(on)}			24	45		
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω		24	45		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		32	60		
Fall Time	t _f			12	24		
Turn-On Delay Time	t _{d(on)}			14	28	ns	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω		13	26		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 10$ A, V_{GEN} = 10 V, R_g = 1 Ω		33	60		
Fall Time	t _f			8	16		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			35		
Pulse Diode Forward Current	I _{SM}				70	A	
Body Diode Voltage	V _{SD}	I _S = 3 A, V _{GS} = 0 V		0.7	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}			21	40	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 10 A, dl/dt = 100 A/μs, T _J = 25 °C		10	20	nC	
Reverse Recovery Fall Time	ta	i _F = 10 A, ui/uι = 100 A/μs, 1 _J = 25 °C		9			
Reverse Recovery Rise Time	t _b			12		ns	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

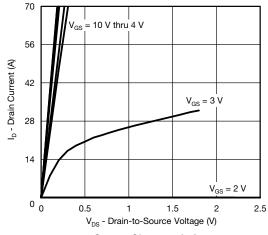
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing.

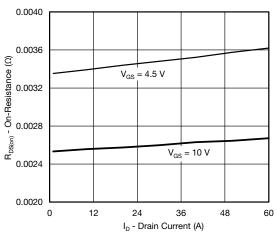


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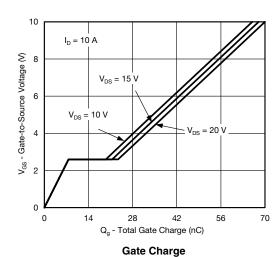
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Output Characteristics



On-Resistance vs. Drain Current and Gate Voltage



10
8

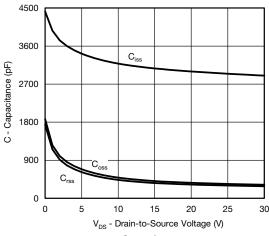
T_C = 25 °C

T_C = 125 °C

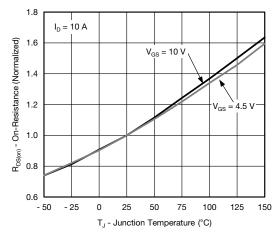
T_C = -55 °C

V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



Capacitance

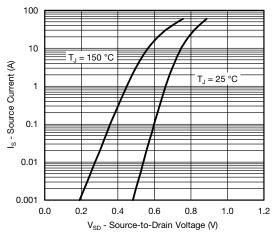


On-Resistance vs. Junction Temperature

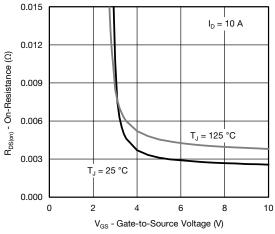
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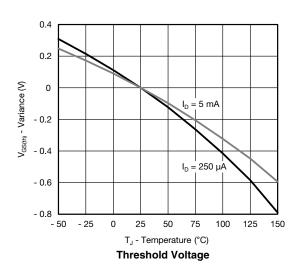
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

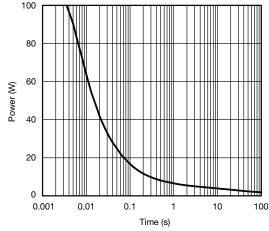


Source-Drain Diode Forward Voltage

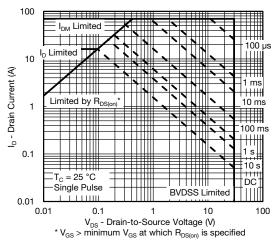


On-Resistance vs. Gate-to-Source Voltage





Single Pulse Power, Junction-to-Ambient

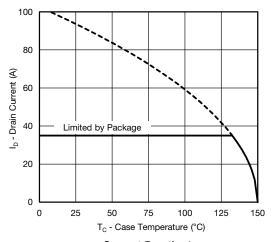


Safe Operating Area, Junction-to-Ambient

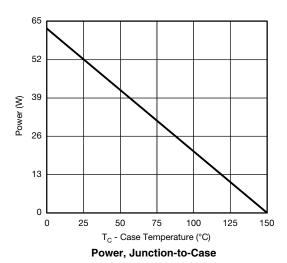


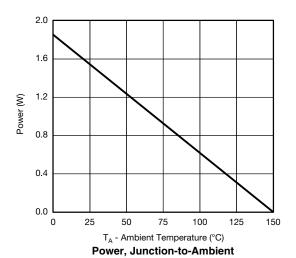
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*





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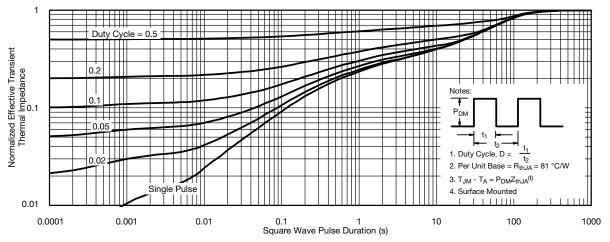
 $^{^*}$ The power dissipation P_D is based on $T_{J(max.)}$ = 150 $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiS444DN

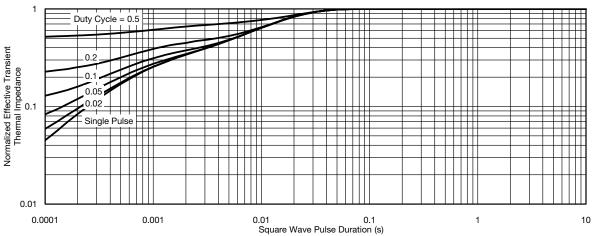
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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Revision: 11-Mar-11

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многоканальный

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