



**HIGH-SPEED 3.3V  
32/16K x 16  
SYNCHRONOUS  
DUAL-PORT STATIC RAM**

**IDT70V9279/69S/L**

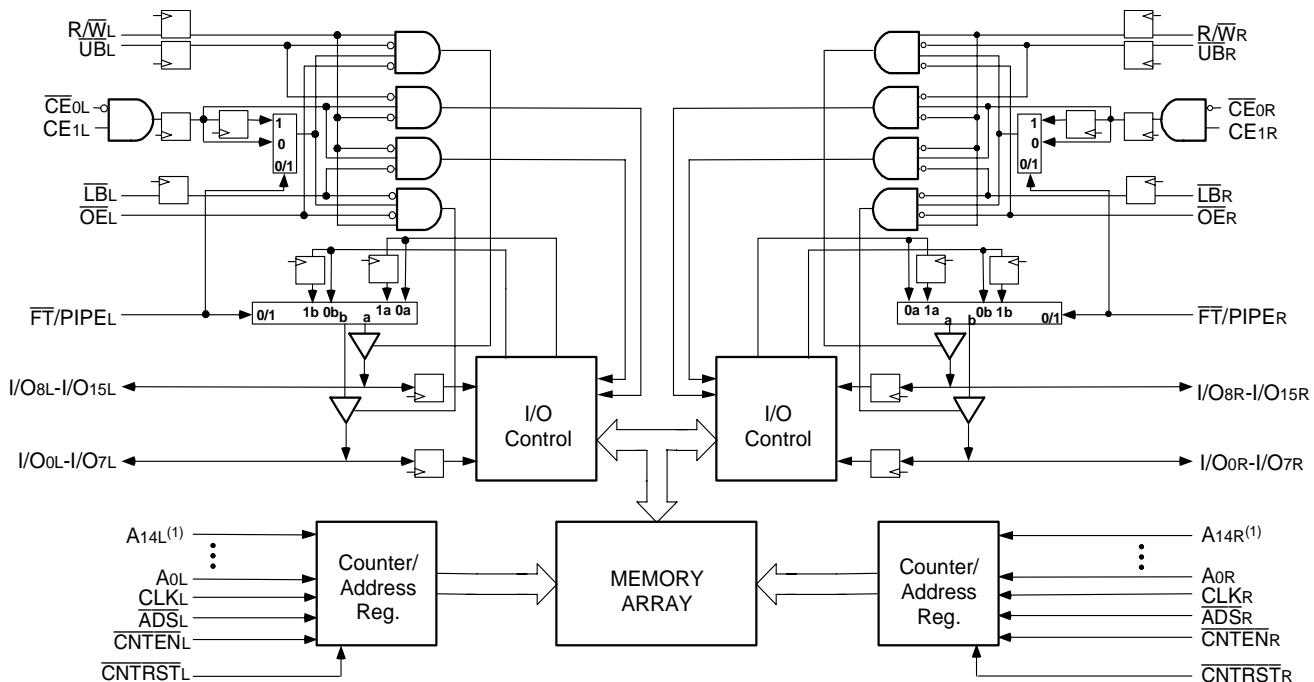
**LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018**

**Features:**

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - Commercial: 6.5/7.5/9/12/15ns (max.)
  - Industrial: 7.5ns (max.)
- Low-power operation
  - IDT70V9279/69S
    - Active: 429mW (typ.)
    - Standby: 3.3mW (typ.)
  - IDT70V9279/69L
    - Active: 429mW (typ.)
    - Standby: 1.32mW (typ.)
- Flow-through or Pipelined output mode on either port via the FT/PIPE pin
- Counter enable and reset features

- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - 4ns setup to clock and 1ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 6.5ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 10ns cycle time, 100MHz operation in Pipelined output mode
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- LVTTL- compatible, single 3.3V ( $\pm 0.3V$ ) power supply
- Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available for selected speeds
- Available in a 128-pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

**Functional Block Diagram**



**NOTE:**

1. A14x is a NC for IDT70V9269.

3743 drw 01

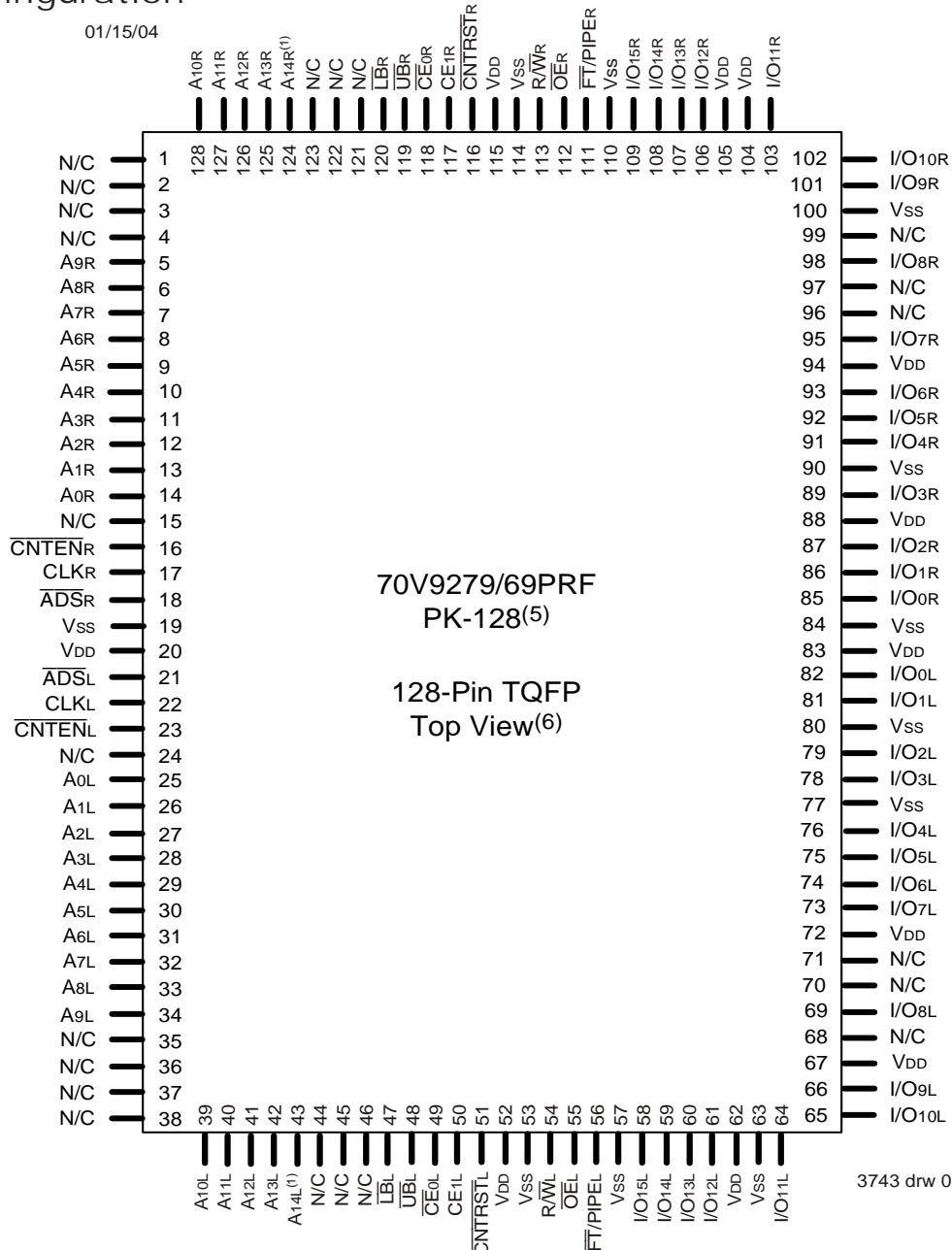
## Description:

The IDT70V9279/69 is a high-speed 32/16K x 16 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9279/69 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by  $\overline{CE}_0$  and  $CE_1$ , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 429mW of power.

## Pin Configuration<sup>(2,3,4)</sup>

01/15/04



### NOTES:

1. A14x is a NC for IDT70V9269.
2. All Vdd pins must be connected to power supply.
3. All Vss pins must be connected to ground.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$ , $CE_{1L}$	$\overline{CE}_{0R}$ , $CE_{1R}$	Chip Enables <sup>(3)</sup>
$\overline{R/W}_L$	$\overline{R/W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{14L}^{(1)}$	$A_{0R} - A_{14R}^{(1)}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
CLK <sub>L</sub>	CLK <sub>R</sub>	Clock
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select <sup>(2)</sup>
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select <sup>(2)</sup>
ADS <sub>L</sub>	$\overline{ADS}_R$	Address Strobe Enable
CNTEN <sub>L</sub>	CNTEN <sub>R</sub>	Counter Enable
CNTRST <sub>L</sub>	CNTRST <sub>R</sub>	Counter Reset
$\overline{FT/PIPE}_L$	$\overline{FT/PIPE}_R$	Flow-Through / Pipeline
V <sub>DD</sub>		Power (3.3V)
V <sub>SS</sub>		Ground (0V)

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## NOTES:

1. Address  $A_{14x}$  is a NC for IDT70V9269.
2.  $\overline{LB}$  and  $\overline{UB}$  are single buffered regardless of state of  $\overline{FT/PIPE}$ .
3.  $\overline{CE}_0$  and  $CE_1$  are single buffered when  $\overline{FT/PIPE} = V_{IL}$ ,  $\overline{CE}_0$  and  $CE_1$  are double buffered when  $\overline{FT/PIPE} = V_{IH}$ , i.e. the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control<sup>(1,2,3)</sup>

$\overline{OE}$	CLK	$\overline{CE}_0^{(5)}$	$CE_1^{(5)}$	$\overline{UB}^{(4)}$	$\overline{LB}^{(4)}$	R/W	Upper Byte I/O <sub>8-15</sub>	Lower Byte I/O <sub>0-7</sub>	MODE
X	$\uparrow$	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	$\uparrow$	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	$\uparrow$	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	$\uparrow$	L	H	L	H	L	D <sub>IN</sub>	High-Z	Write to Upper Byte Only
X	$\uparrow$	L	H	H	L	L	High-Z	DATA <sub>IN</sub>	Write to Lower Byte Only
X	$\uparrow$	L	H	L	L	L	DATA <sub>IN</sub>	DATA <sub>IN</sub>	Write to Both Bytes
L	$\uparrow$	L	H	L	H	H	DATA <sub>OUT</sub>	High-Z	Read Upper Byte Only
L	$\uparrow$	L	H	H	L	H	High-Z	DATA <sub>OUT</sub>	Read Lower Byte Only
L	$\uparrow$	L	H	L	L	H	DATA <sub>OUT</sub>	DATA <sub>OUT</sub>	Read Both Bytes
H	$\uparrow$	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

3743tbl02

## NOTES:

1. "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care.
2.  $\overline{ADS}$ ,  $CNTEN$ ,  $CNTRST$  = X.
3.  $\overline{OE}$  is an asynchronous input signal.
4.  $\overline{LB}$  and  $\overline{UB}$  are single buffered regardless of state of  $\overline{FT/PIPE}$ .
5.  $\overline{CE}_0$  and  $CE_1$  are single buffered when  $\overline{FT/PIPE} = V_{IL}$ .  $\overline{CE}_0$  and  $CE_1$  are double buffered when  $\overline{FT/PIPE} = V_{IH}$ , i.e. the signals take two cycles to deselect.

Truth Table II—Address Counter Control<sup>(1,2,3)</sup>

External Address	Previous Internal Address	Internal Address Used	CLK	<u>ADS</u>	<u>CNTEN</u>	<u>CNTRST</u>	I/O <sup>(3)</sup>	MODE
An	X	An	↑	L <sup>(4)</sup>	X	H	D/Io (n)	External Address Used
X	An	An + 1	↑	H	L <sup>(5)</sup>	H	D/Io(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	D/Io(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	A0	↑	X	X	L <sup>(4)</sup>	D/Io(0)	Counter Reset to Address 0

## NOTES:

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- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- CE<sub>0</sub>, LB, UB, and OE = V<sub>IL</sub>; CE1 and RW = V<sub>IH</sub>.
- Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
- ADS and CNTRST are independent of all other signals including CE<sub>0</sub>, CE1, UB and LB.
- The address counter advances if CNTEN = V<sub>IL</sub> on the rising edge of CLK, regardless of all other signals including CE<sub>0</sub>, CE1, UB and LB.

Recommended Operating Temperature and Supply Voltage<sup>(1,2)</sup>

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

## NOTES:

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- Industrial temperature: for specific speeds, packages and powers contact your sales office.
- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>DD</sub> +0.3V <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

3743 tbl 05

## NOTES:

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10 ns.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V.

Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub> <sup>(3)</sup>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>JN</sub>	Junction Temperature	+150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

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## NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>DD</sub> + 0.3V.
- Ambient Temperature Under DC Bias. No AC Conditions. Chip Deselected.

Capacitance<sup>(1)</sup>(T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	9	pF
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

3743 tbl 07

## NOTES:

- These parameters are determined by device characterization, but are not production tested.
- C<sub>OUT</sub> also references C<sub>IO</sub>.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V9279/69S		70V9279/69L		Unit
			Min.	Max.	Min.	Max.	
I <sub>U</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DD</sub> = 3.6V, V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	10	—	5	µA
I <sub>O</sub>	Output Leakage Current	CE <sub>0</sub> = V <sub>IH</sub> or CE <sub>1</sub> = V <sub>IL</sub> , V <sub>OUT</sub> = 0V to V <sub>DD</sub>	—	10	—	5	µA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +4mA	—	0.4	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	2.4	—	V

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## NOTE:

- At V<sub>DD</sub> ≤ 2.0V input leakages are undefined.

## DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range<sup>(3,6)</sup> (V<sub>DD</sub> = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version	70V9279/69X6 Com'l Only		70V9279/69X7 Com'l & Ind		70V9279/69X9 Com'l Only		Unit
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	
I <sub>DD</sub>	Dynamic Operating Current (Both Ports Active)	CE <sub>L</sub> and CE <sub>R</sub> = V <sub>IL</sub> , Outputs Disabled, f = f <sub>MAX</sub> <sup>(1)</sup>	COM'L	S 220 220	395 200	200 290	335 180	180 180	260 225	mA
			IND	S — —	— —	200 200	370 335	— —	— —	
I <sub>S81</sub>	Standby Current (Both Ports - TTL Level Inputs)	CE <sub>L</sub> = CE <sub>R</sub> = V <sub>IH</sub> f = f <sub>MAX</sub> <sup>(1)</sup>	COM'L	S 70 70	145 130	60 60	115 100	50 50	75 65	mA
			IND	S — —	— —	60 60	130 115	— —	— —	
I <sub>S82</sub>	Standby Current (One Port - TTL Level Inputs)	CE <sup>"A"</sup> = V <sub>IL</sub> and CE <sup>"B"</sup> = V <sub>IH</sub> <sup>(5)</sup> Active Port Outputs Disabled, f = f <sub>MAX</sub> <sup>(1)</sup>	COM'L	S 150 150	280 250	130 130	240 210	110 110	170 150	mA
			IND	S — —	— —	130 130	265 240	— —	— —	
I <sub>S83</sub>	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>DD</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0 <sup>(2)</sup>	COM'L	S 1.0 0.4	5 3	1.0 0.4	5 3	1.0 0.4	5 3	mA
			IND	S — —	— —	1.0 0.4	20 15	— —	— —	
I <sub>S84</sub>	Full Standby Current (One Port - CMOS Level Inputs)	CE <sup>"A"</sup> ≤ 0.2V and CE <sup>"B"</sup> ≥ V <sub>DD</sub> - 0.2V <sup>(5)</sup> VIN ≥ V <sub>DD</sub> - 0.2V or VIN ≤ 0.2V, Active Port, Outputs Disabled, f = f <sub>MAX</sub> <sup>(1)</sup>	COM'L	S 140 140	270 240	120 120	230 200	100 100	160 140	mA
			IND	S — —	— —	120 120	255 230	— —	— —	

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## NOTES:

- At f = f<sub>MAX</sub>, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t<sub>CYC</sub>, using "AC TEST CONDITIONS" at input levels of V<sub>SS</sub> to 3V.
- f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- V<sub>DD</sub> = 3.3V, TA = 25°C for Typ, and are not production tested. I<sub>DD</sub> DC(f=0) = 90mA (Typ).
- CE<sub>X</sub> = V<sub>IL</sub> means CE<sub>0X</sub> = V<sub>IL</sub> and CE<sub>1X</sub> = V<sub>IH</sub>  
CE<sub>X</sub> = V<sub>IH</sub> means CE<sub>0X</sub> = V<sub>IH</sub> or CE<sub>1X</sub> = V<sub>IL</sub>
- CE<sub>X</sub> ≤ 0.2V means CE<sub>0X</sub> ≤ 0.2V and CE<sub>1X</sub> ≥ V<sub>DD</sub> - 0.2V  
CE<sub>X</sub> ≥ V<sub>DD</sub> - 0.2V means CE<sub>0X</sub> ≥ V<sub>DD</sub> - 0.2V or CE<sub>1X</sub> ≤ 0.2V  
'X' represents "L" for left port or "R" for right port.
- 'X' in part numbers indicate power rating (S or L).

DC Electrical Characteristics Over the Operating  
Temperature Supply Voltage Range<sup>(3,6)</sup> (VDD = 3.3V ± 0.3V) (Cont'd)

Symbol	Parameter	Test Condition	Version	70V9279/69X12 Com'l Only		70V9279/69X15 Com'l Only		Unit
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S L	150 150	240 205	130 130	220 185
			IND	S L	— —	— —	— —	— —
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S L	40 40	65 50	30 30	55 35
			IND	S L	— —	— —	— —	— —
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_A = V_{IL}$ and $\overline{CE}_B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f=f_{MAX}^{(1)}$	COM'L	S L	100 100	160 140	90 90	150 130
			IND	S L	— —	— —	— —	— —
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L	S L	1.0 0.4	5 3	1.0 0.4	5 3
			IND	S L	— —	— —	— —	— —
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_A \leq 0.2V$ and $\overline{CE}_B \geq V_{DD} - 0.2V^{(5)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S L	90 90	150 130	80 80	140 120
			IND	S L	— —	— —	— —	— —

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## NOTES:

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cyc}$ , using "AC TEST CONDITIONS" at input levels of  $V_{SS}$  to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^{\circ}C$  for Typ, and are not production tested.  $IDD_{DC}(f=0) = 90mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DD} - 0.2V$   
 $\overline{CE}_X \geq V_{DD} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DD} - 0.2V$  or  $CE_{1X} \leq 0.2V$
- 'X' represents "L" for left port or "R" for right port.
- 'X' in part numbers indicate power rating (S or L).

## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

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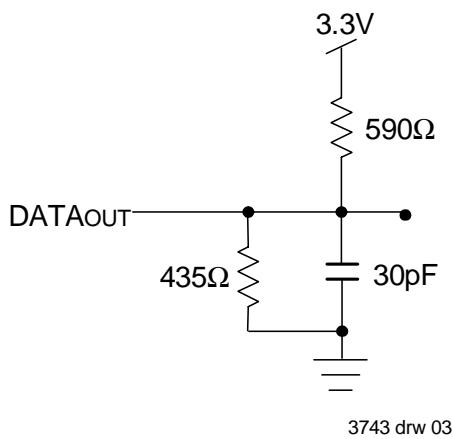


Figure 1. AC Output Test load.

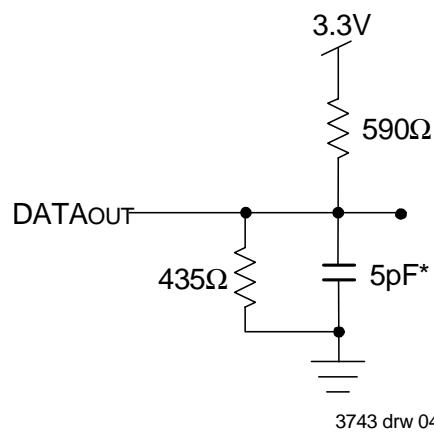
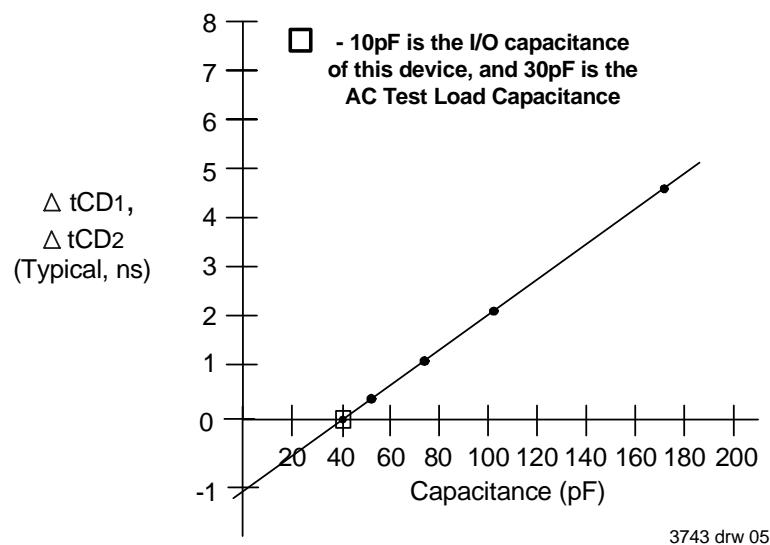
Figure 2. Output Test Load  
(For tCKLZ, tCKHZ, tolZ, and toHZ).  
\*Including scope and jig.

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range  
(Read and Write Cycle Timing)<sup>(3,4)</sup> (VDD = 3.3V ± 0.3V, TA = 0°C to +70°C)

		70V9279/69X6 Com'l Only		70V9279/69X7 Com'l & Ind		70V9279/69X9 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tCYC1	Clock Cycle Time (Flow-Through) <sup>(2)</sup>	19	—	22	—	25	—	ns
tCYC2	Clock Cycle Time (Pipelined) <sup>(2)</sup>	10	—	12	—	15	—	ns
tCH1	Clock High Time (Flow-Through) <sup>(2)</sup>	6.5	—	7.5	—	12	—	ns
tCL1	Clock Low Time (Flow-Through) <sup>(2)</sup>	6.5	—	7.5	—	12	—	ns
tCH2	Clock High Time (Pipelined) <sup>(2)</sup>	4	—	5	—	6	—	ns
tCL2	Clock Low Time (Pipelined) <sup>(2)</sup>	4	—	5	—	6	—	ns
tR	Clock Rise Time	—	3	—	3	—	3	ns
tF	Clock Fall Time	—	3	—	3	—	3	ns
tSA	Address Setup Time	3.5	—	4	—	4	—	ns
tHA	Address Hold Time	0	—	0	—	1	—	ns
tSC	Chip Enable Setup Time	3.5	—	4	—	4	—	ns
tHC	Chip Enable Hold Time	0	—	0	—	1	—	ns
tSW	R/W Setup Time	3.5	—	4	—	4	—	ns
tHW	R/W Hold Time	0	—	0	—	1	—	ns
tSD	Input Data Setup Time	3.5	—	4	—	4	—	ns
tHD	Input Data Hold Time	0	—	0	—	1	—	ns
tSAD	ADS Setup Time	3.5	—	4	—	4	—	ns
tHAD	ADS Hold Time	0	—	0	—	1	—	ns
tSCN	CNTEN Setup Time	3.5	—	4	—	4	—	ns
tHCN	CNTEN Hold Time	0	—	0	—	1	—	ns
tSRST	CNTRST Setup Time	3.5	—	4	—	4	—	ns
tHRST	CNTRST Hold Time	0	—	0	—	1	—	ns
toE	Output Enable to Data Valid	—	6.5	—	7.5	—	9	ns
tOLZ	Output Enable to Output Low-Z <sup>(1)</sup>	2	—	2	—	2	—	ns
tOHZ	Output Enable to Output High-Z <sup>(1)</sup>	1	7	1	7	1	7	ns
tCD1	Clock to Data Valid (Flow-Through) <sup>(2)</sup>	—	15	—	18	—	20	ns
tCD2	Clock to Data Valid (Pipelined) <sup>(2)</sup>	—	6.5	—	7.5	—	9	ns
tDC	Data Output Hold After Clock High	2	—	2	—	2	—	ns
tCKHZ	Clock High to Output High-Z <sup>(1)</sup>	2	9	2	9	2	9	ns
tCKLZ	Clock High to Output Low-Z <sup>(1)</sup>	2	—	2	—	2	—	ns
<b>Port-to-Port Delay</b>								
tcWDD	Write Port Clock High to Read Data Delay	—	24	—	28	—	35	ns
tccs	Clock-to-Clock Setup Time	—	9	—	10	—	15	ns

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (tCYC2, tCD2) apply to either or both left and right ports when  $\overline{FT}/PIPE = V_{IH}$ . Flow-through parameters (tCYC1, tCD1) apply when  $\overline{FT}/PIPE = V_{IL}$  for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPE$ .  $\overline{FT}/PIPE$  should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

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AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(3,4)</sup> (VDD = 3.3V ± 0.3V, TA = 0°C to +70°C)(Cont'd)

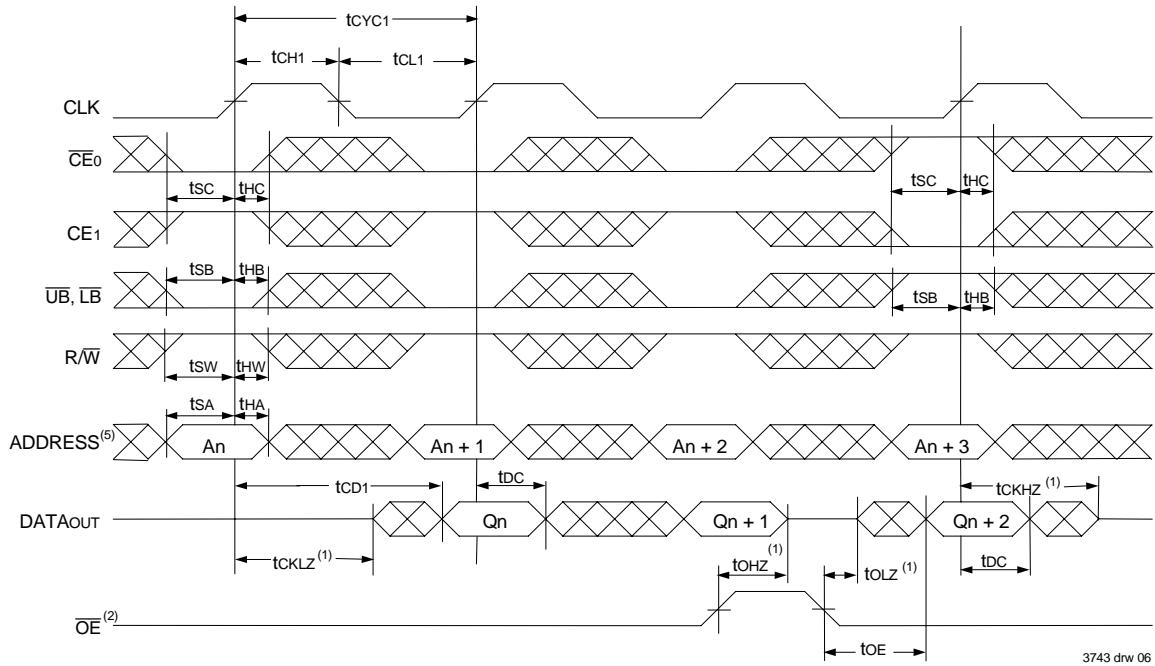
		70V9279/69X12 Com'l Only	70V9279/69X15 Com'l Only			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tCyc1	Clock Cycle Time (Flow-Through) <sup>(2)</sup>	30	—	35	—	ns
tCyc2	Clock Cycle Time (Pipelined) <sup>(2)</sup>	20	—	25	—	ns
tCh1	Clock High Time (Flow-Through) <sup>(2)</sup>	12	—	12	—	ns
tCl1	Clock Low Time (Flow-Through) <sup>(2)</sup>	12	—	12	—	ns
tCh2	Clock High Time (Pipelined) <sup>(2)</sup>	8	—	10	—	ns
tCl2	Clock Low Time (Pipelined) <sup>(2)</sup>	8	—	10	—	ns
tR	Clock Rise Time	—	3	—	3	ns
tF	Clock Fall Time	—	3	—	3	ns
tSA	Address Setup Time	4	—	4	—	ns
tHA	Address Hold Time	1	—	1	—	ns
tSC	Chip Enable Setup Time	4	—	4	—	ns
tHC	Chip Enable Hold Time	1	—	1	—	ns
tSW	R/W Setup Time	4	—	4	—	ns
tHW	R/W Hold Time	1	—	1	—	ns
tSD	Input Data Setup Time	4	—	4	—	ns
tHD	Input Data Hold Time	1	—	1	—	ns
tSAD	ADS Setup Time	4	—	4	—	ns
tHAD	ADS Hold Time	1	—	1	—	ns
tSCN	CNTEN Setup Time	4	—	4	—	ns
tHCN	CNTEN Hold Time	1	—	1	—	ns
tSRST	CNTRST Setup Time	4	—	4	—	ns
tHRST	CNTRST Hold Time	1	—	1	—	ns
tOE	Output Enable to Data Valid	—	12	—	15	ns
tOLZ	Output Enable to Output Low-Z <sup>(1)</sup>	2	—	2	—	ns
tOHZ	Output Enable to Output High-Z <sup>(1)</sup>	1	7	1	7	ns
tCD1	Clock to Data Valid (Flow-Through) <sup>(2)</sup>	—	25	—	30	ns
tCD2	Clock to Data Valid (Pipelined) <sup>(2)</sup>	—	12	—	15	ns
tDC	Data Output Hold After Clock High	2	—	2	—	ns
tCKHZ	Clock High to Output High-Z <sup>(1)</sup>	2	9	2	9	ns
tCKLZ	Clock High to Output Low-Z <sup>(1)</sup>	2	—	2	—	ns
<b>Port-to-Port Delay</b>						
tCWDD	Write Port Clock High to Read Data Delay	—	40	—	50	ns
tCCS	Clock-to-Clock Setup Time	—	15	—	20	ns

3743 tbl 11b

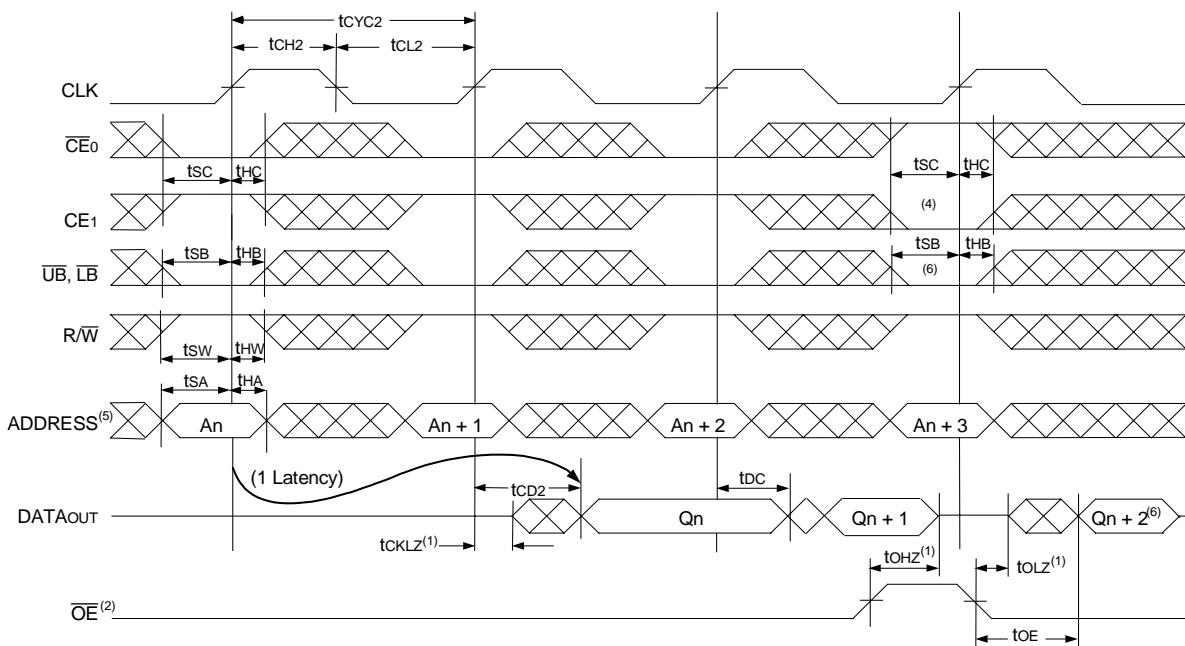
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (tCyc2, tCD2) apply to either or both left and right ports when  $\overline{FT}/PIPE = V_{IH}$ . Flow-through parameters (tCyc1, tCD1) apply when  $\overline{FT}/PIPE = V_{IL}$  for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPE$ .  $\overline{FT}/PIPE$  should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

## Timing Waveform of Read Cycle for Flow-through Output ( $\overline{FT}/PIPE$ "x" = $V_{IL}$ )<sup>(3,7)</sup>

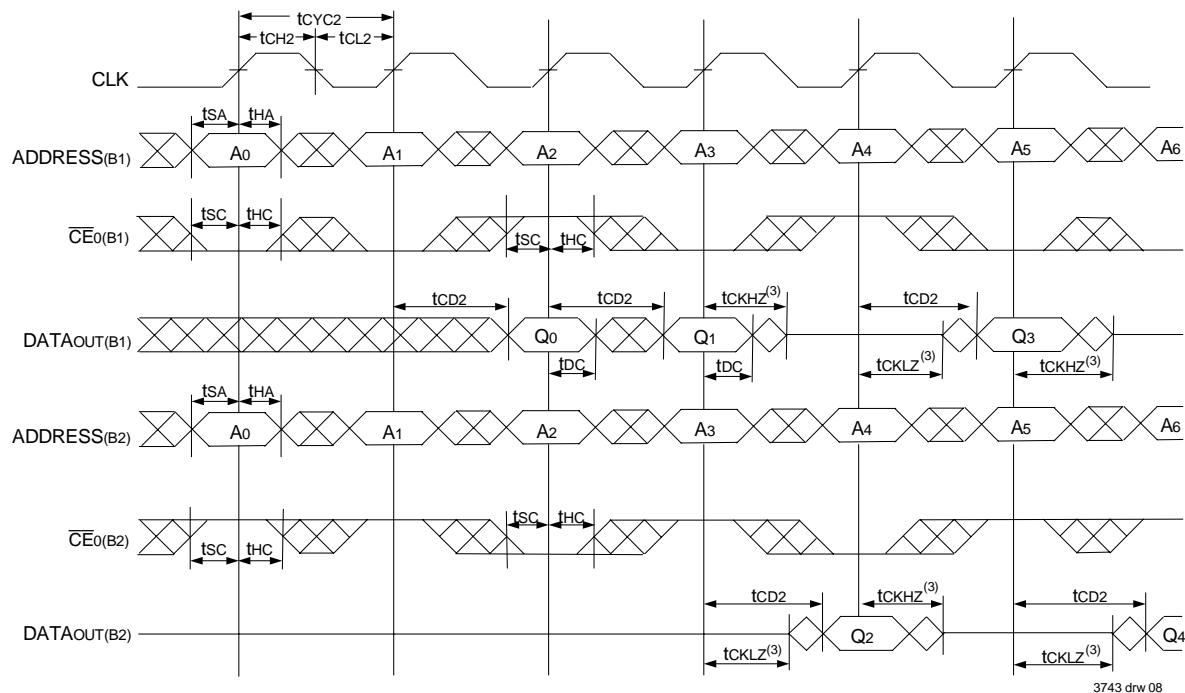
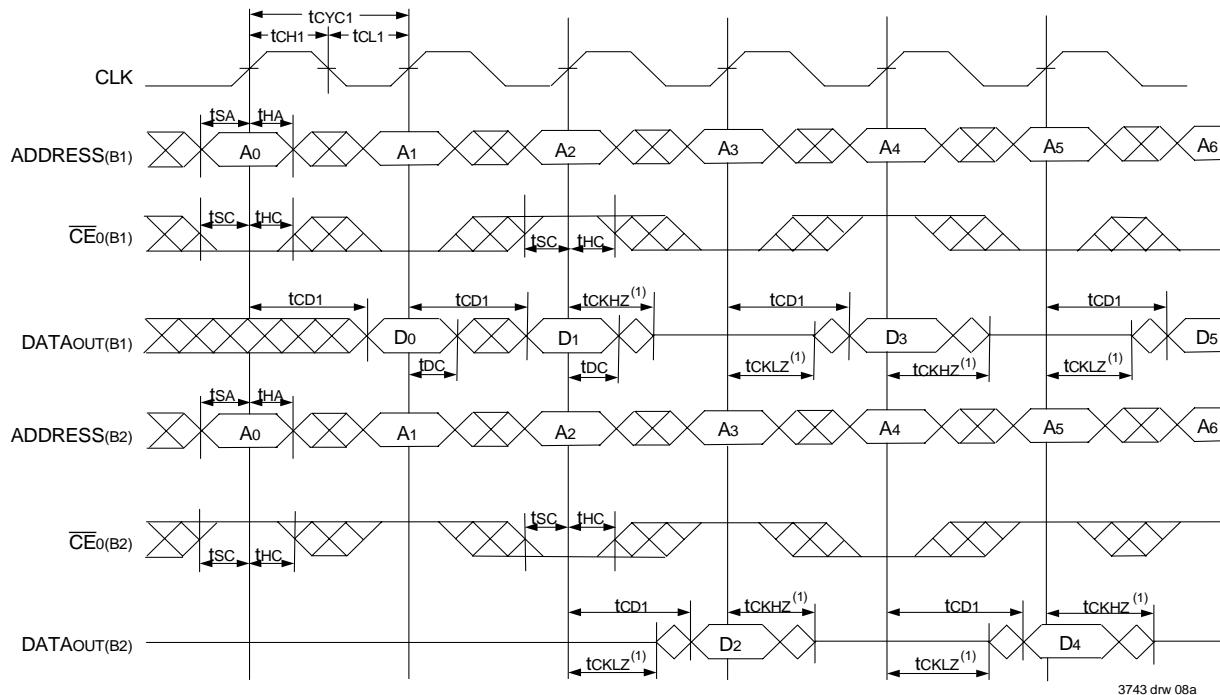


## Timing Waveform of Read Cycle for Pipelined Output ( $\overline{FT}/PIPE$ "x" = $V_{IH}$ )<sup>(3,7)</sup>



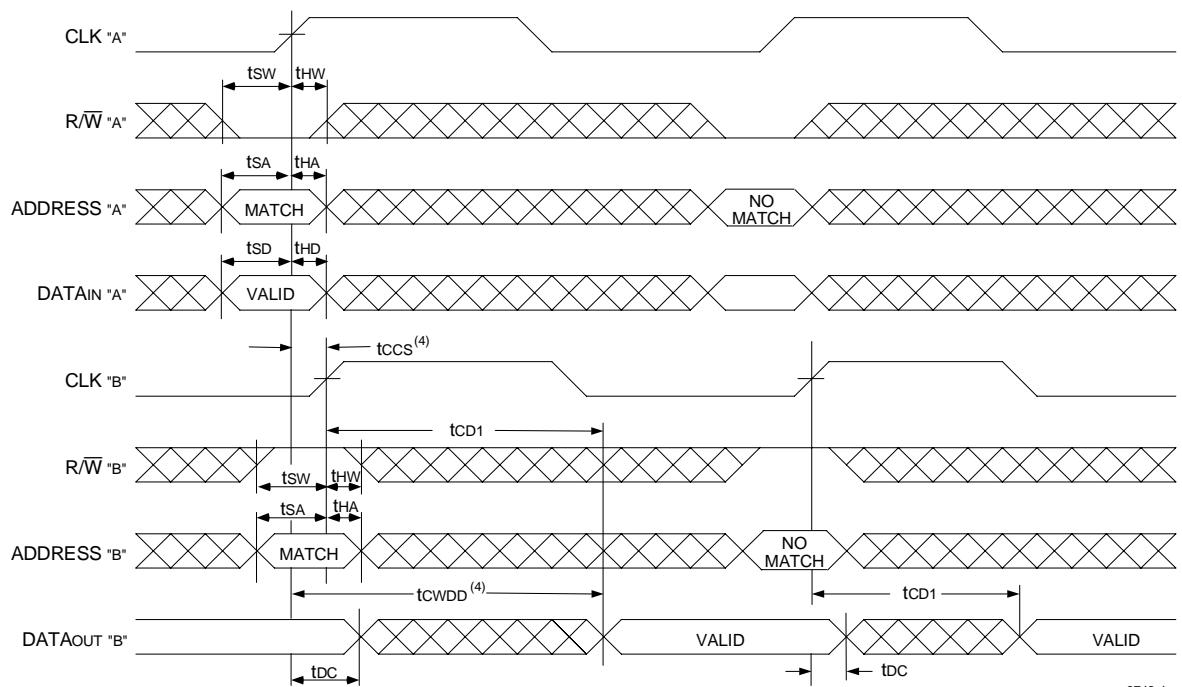
### NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3.  $ADS = V_{IL}$ ,  $CNTEN$  and  $CNTRST = V_{IH}$ .
4. The output is disabled (High-Impedance state) by  $\overline{CE}_0 = V_{IH}$  or  $CE_1 = V_{IL}$  following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since  $ADS = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If  $\overline{UB}$  or  $LB$  was HIGH, then the Upper Byte and/or Lower Byte of DATAout for  $Qn + 2$  would be disabled (High-Impedance state).
7. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read<sup>(1,2)</sup>Timing Waveform of a Bank Select Flow-Through Read<sup>(6)</sup>

## NOTES:

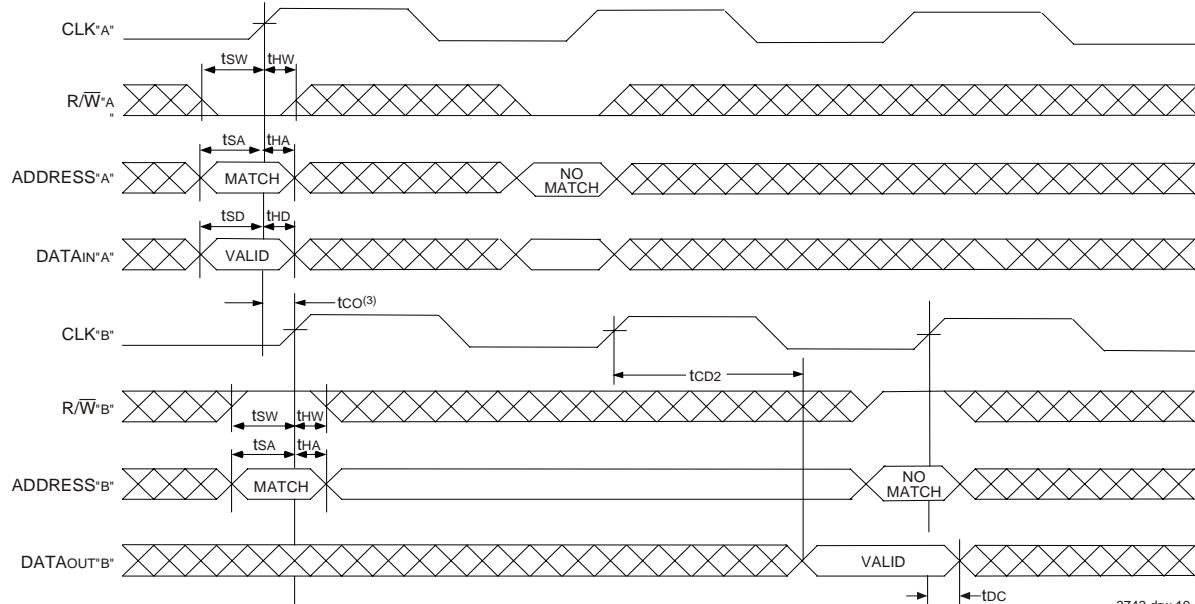
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9279/69 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2.  $\overline{UB}$ ,  $\overline{LB}$ ,  $\overline{OE}$ , and  $\overline{ADS}$  =  $V_{IL}$ ;  $CE1(B1)$ ,  $CE1(B2)$ ,  $R/W$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST}$  =  $V_{IH}$ .
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS}$  =  $V_{IL}$ ;  $CE1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST}$  =  $V_{IH}$ .
5.  $\overline{OE}$  =  $V_{IL}$  for the Right Port, which is being read from.  $\overline{OE}$  =  $V_{IH}$  for the Left Port, which is being written to.
6. If  $t_{CCS} \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for  $t_{CWD}$ . If  $t_{CCS} >$  maximum specified, then data from right port READ is not valid until  $t_{CCS} + t_{CD1}$ .  $t_{CWD}$  does not apply in this case.

Timing Waveform with Port-to-Port Flow-Through Read<sup>(1,2,3,5)</sup>

3743 drw 09

## NOTES:

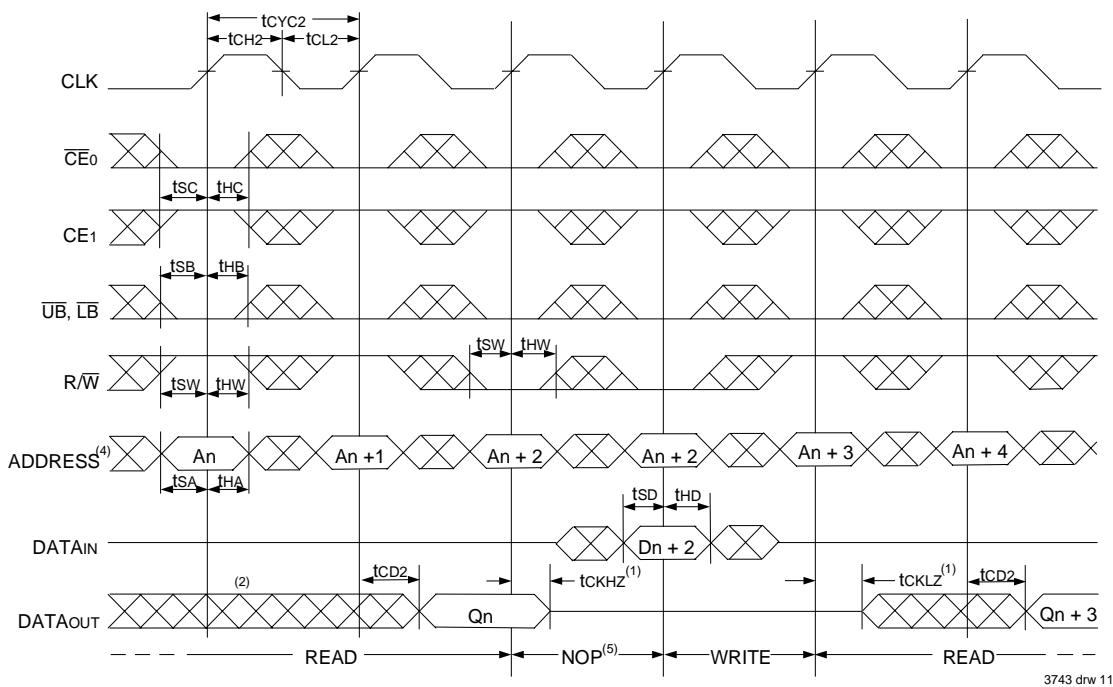
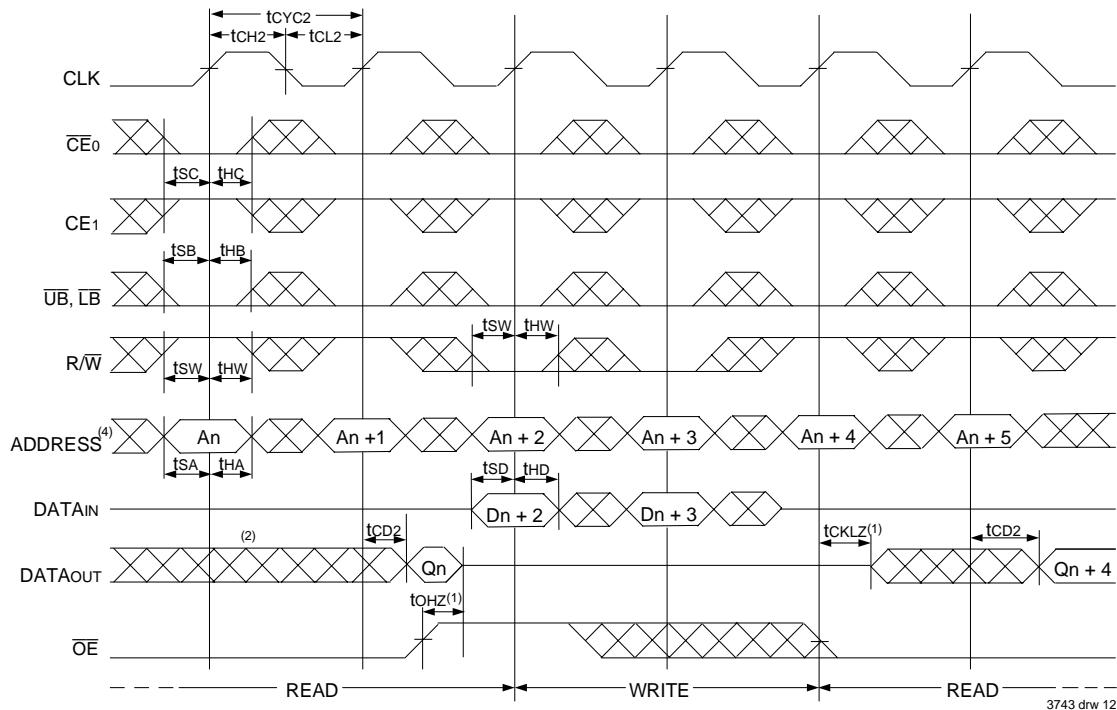
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
3.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
4. If  $tccs \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for tcwdd. If  $tccs >$  maximum specified, then data from right port READ is not valid until  $tccs + tcd1$ . tcwdd does not apply in this case.
5. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

Timing Waveform of Left Port Write to Pipelined Right Port Read<sup>(1,2,4)</sup>

3743 drw 10

## NOTES:

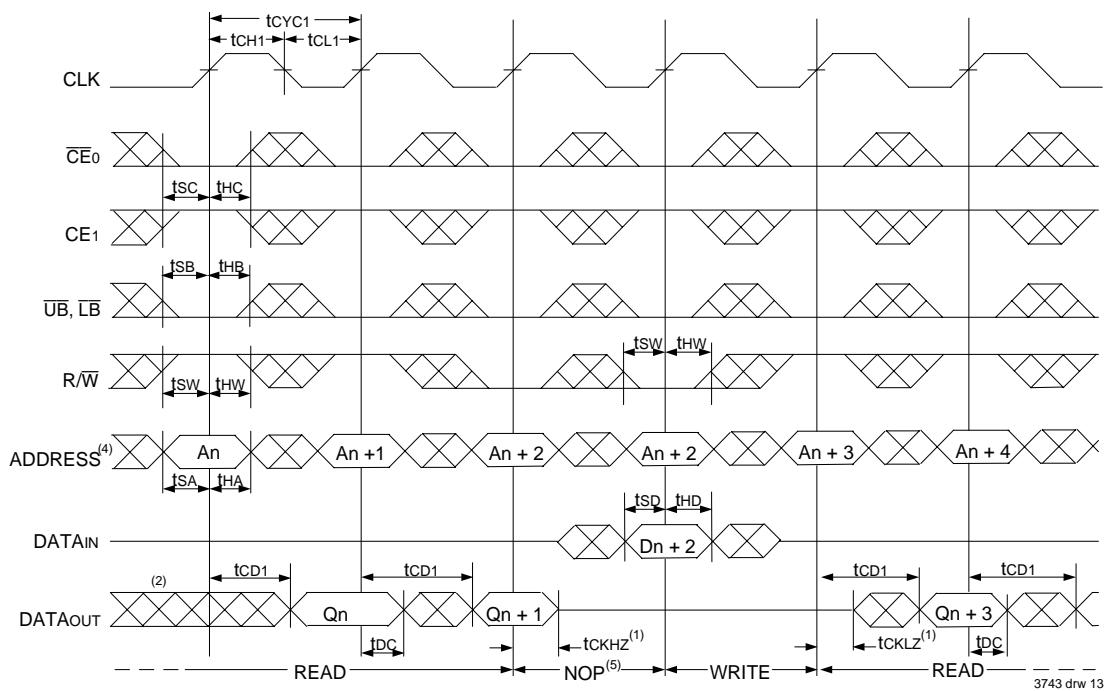
1.  $\overline{CE}_0$ ,  $\overline{BE}_n$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for Port "B", which is being read from.  $\overline{OE} = V_{IH}$  for Port "A", which is being written to.
3. If  $tco \leq$  minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be  $tco + 2 tcy2 + tcd2$ ). If  $tco >$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be  $tco + tcy2 + tcd2$ ).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(3)</sup>

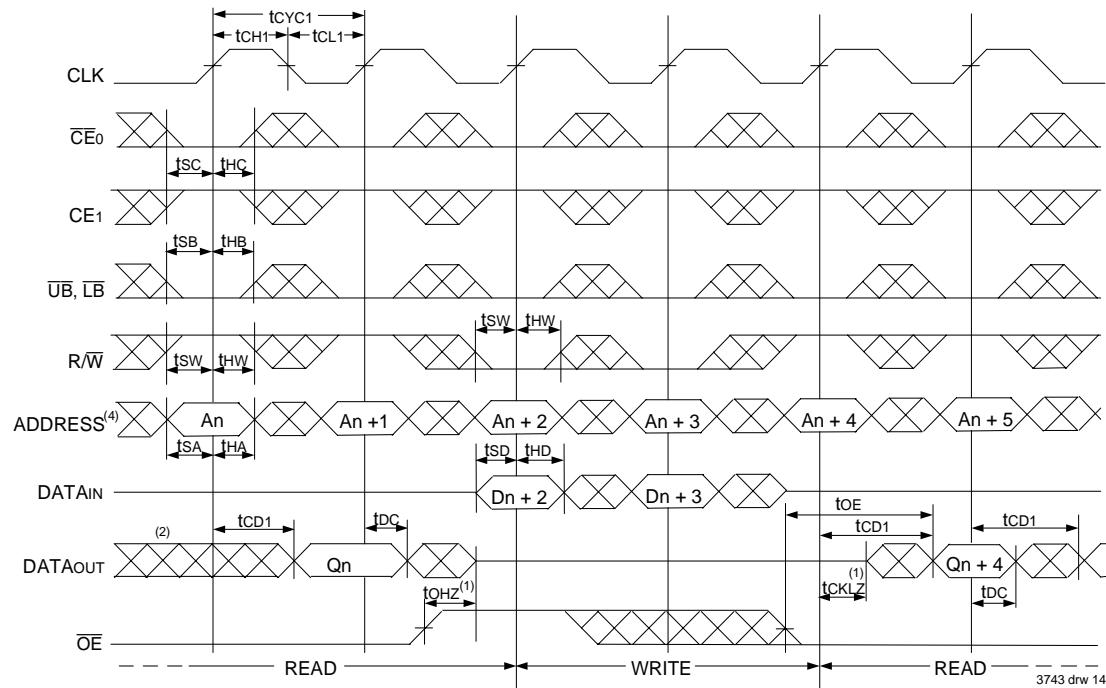
## NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $ADS = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $\overline{CNTRST} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $ADS = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>

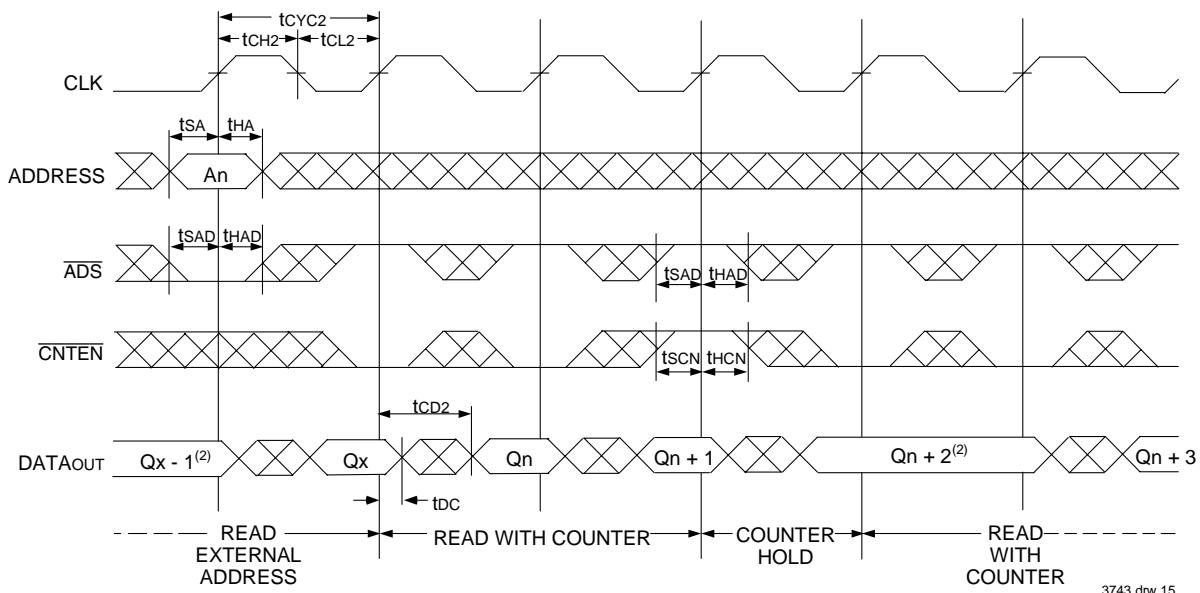


Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(3)</sup>

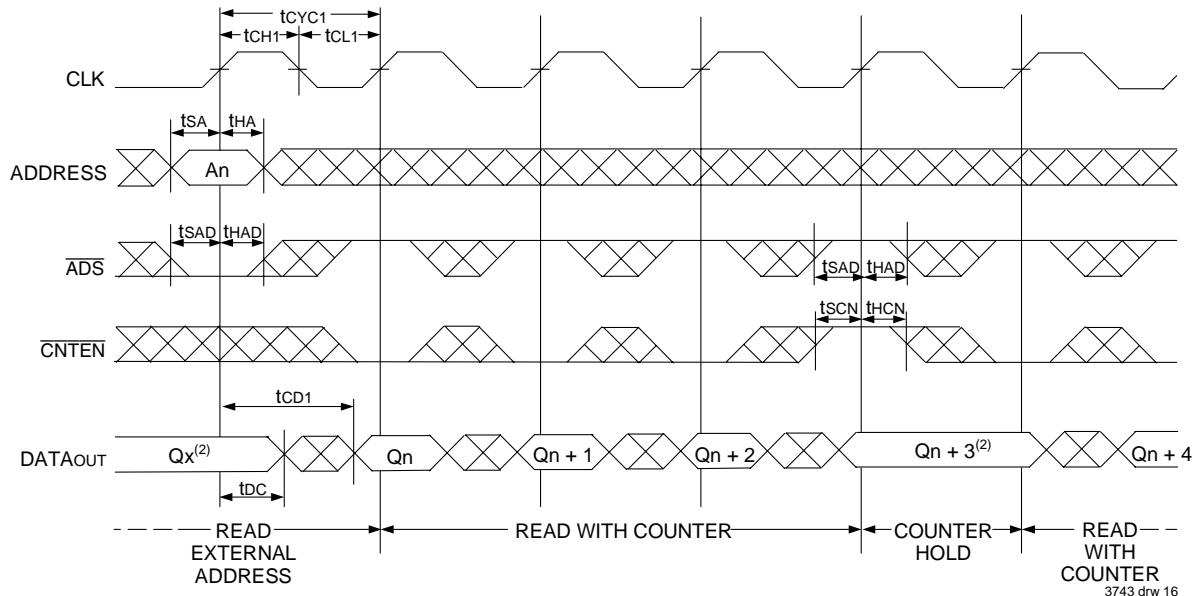


NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>

3743 drw 15

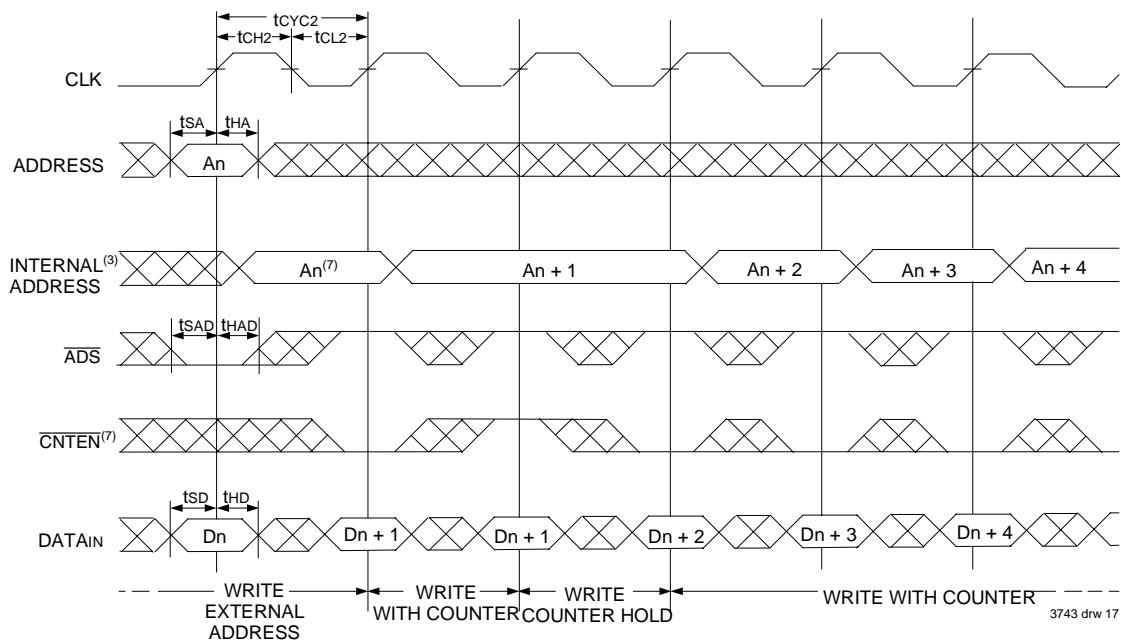
Timing Waveform of Flow-Through Read with Address Counter Advance<sup>(1)</sup>

3743 drw 16

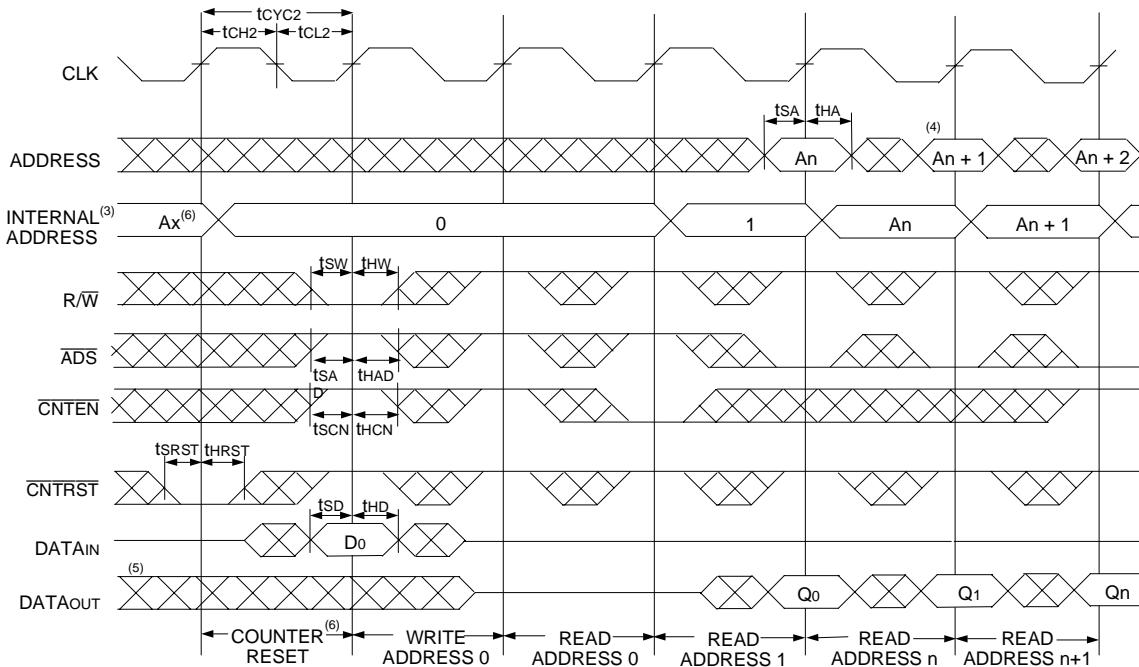
## NOTES:

1.  $\overline{CE}_0$ ,  $\overline{OE}$ ,  $\overline{UB}$ , and  $\overline{LB}$  =  $V_{IL}$ ;  $CE_1$ ,  $R\overline{W}$ , and  $\overline{CNTRST}$  =  $V_{IH}$ .
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)<sup>(1)</sup>



## Timing Waveform of Counter Reset (Pipelined Outputs)<sup>(2)</sup>



### NOTES:

1.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $R/W = V_{IL}$ ;  $CE_1$  and  $CNTRST = V_{IH}$ .
2.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB} = V_{IL}$ ;  $CE_1 = V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. ADDR<sub>0</sub> will be accessed. Extra cycles are shown here simply for clarification.
7.  $CNTEN = V_{IL}$  advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

## Functional Description

The IDT70V9279/69 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to staff the operation of the address counters for fast interleaved memory applications.

A HIGH on  $\overline{CE}_0$  or a LOW on  $CE_1$  for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9279/69's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with  $\overline{CE}_0$  LOW and  $CE_1$  HIGH to re-activate the outputs.

## Depth and Width Expansion

The IDT70V9279/69 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9279/69 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.

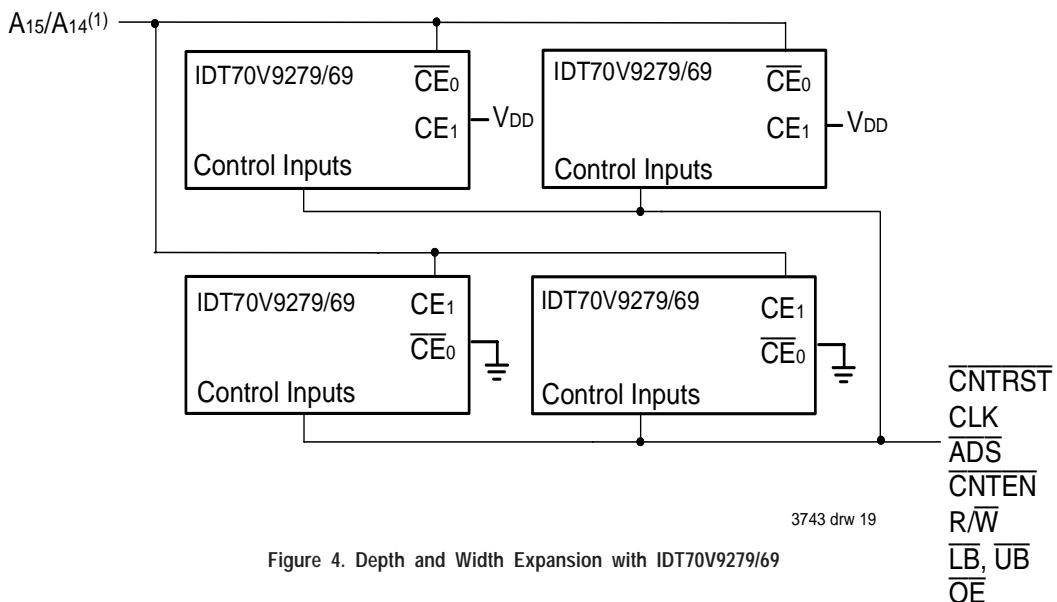
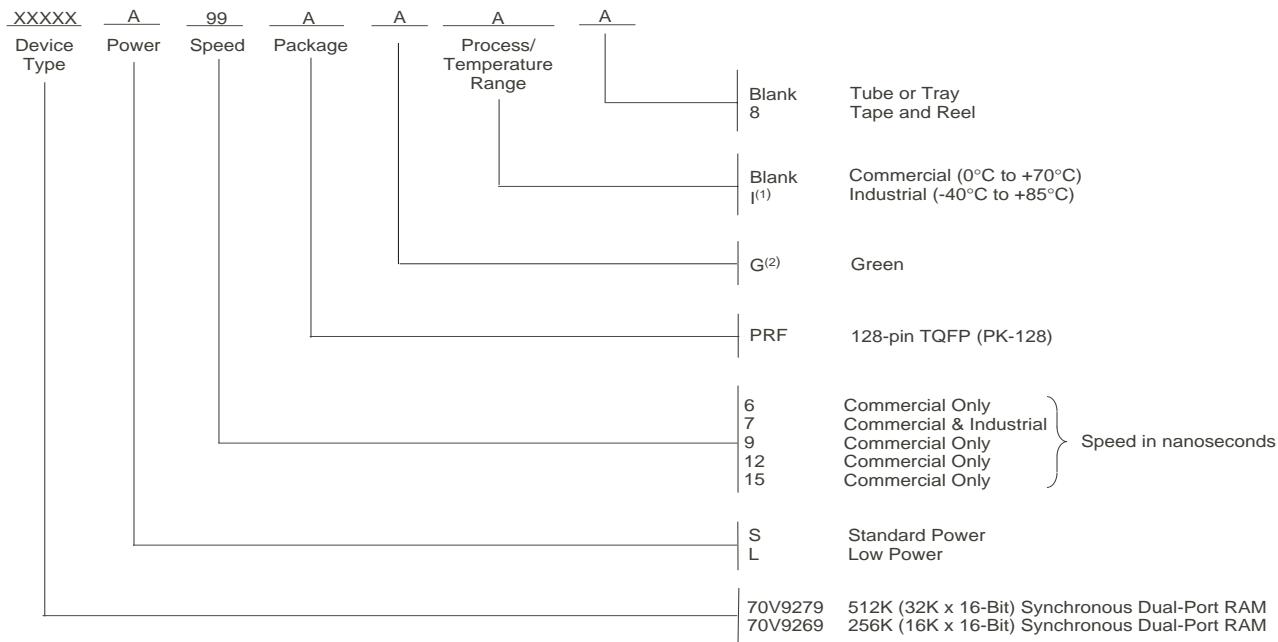


Figure 4. Depth and Width Expansion with IDT70V9279/69

**NOTE:**

1. A15 is for IDT70V9279. A14 is for IDT70V9269.

## Ordering Information



3743 drw 20

### NOTE:

1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

**LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02**

## Ordering Information for Flow-through Devices

Old Flow-through Part	New Combined Part
70V927S/L25	70V9279S/L12
70V927S/L30	70V9279S/L15

3743 tbl 12

## IDT Clock Solution for IDT70V9279/69 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70V9279/69	3.3	LVTTL	9pF	40%	100	150ps	2305 2308 2309	49FCT3805 49FCT3805D/E 74FCT3807 74FCT3807D/E

3743 tbl 13

## Datasheet Document History

01/12/99:		Initiated datasheet document history Converted to new format Cosmetic and typographical corrections Added additional notes to pin configurations
	Page 14	Added Depth & Width Expansion section
06/15/99:	Page 4	Deleted note 6 for Table II
09/29/99:	Page 7	Corrected typo in heading
11/10/99:		Replaced IDT logo
03/31/00:		Combined Pipelined 70V9279/69 family and Flow-through 70V927 family offerings into one data sheet Changed $\pm 200\text{mV}$ in waveform notes to 0mV Added corresponding part chart with ordering information
01/017/01:	Page 4	Changed information in Truth Table II Increased storage temperature parameters Clarified TA parameter
	Page 5	DC Electrical parameters—changed wording from "open" to "disabled" Removed Preliminary status
02/25/04:		Consolidated multiple devices into one datasheet Changed naming conventions from Vcc to Vdd and from GND to Vss Page 2 Added date revision for pin configuration Page 3 Added footnotes for $\overline{\text{UB}}$ , $\overline{\text{LB}}$ , $\overline{\text{CE0}}$ and $\text{CE1}$ buffer conditions when $\overline{\text{FT}}$ or PIPE Page 4 Added junction temperature to Absolute Maximum Ratings Table Added Ambient Temperature footnote Page 5 Added I-temp numbers for 9ns speed to DC Electrical Characteristics Table Added 6ns speed DC power numbers to the DC Electrical Characteristics Table Page 7 Added I-temp for 9ns speed to AC Electrical Characteristics Table Added 6ns speed AC timing numbers to the AC Electrical Characteristics Table Page 18 Added 6ns speed grade and 9ns I-temp to ordering information Added IDT Clock Solution Table Page 1 & 19 Updated IDT logo, replaced IDT™ logo with IDT® logo
05/04/04:	Page 1 & 18	Added 7ns speed grade to ordering information Page 5 Added 7ns speed DC power numbers to the DC Electrical Characteristics Table Page 8 Added 7ns speed AC timing numbers to the AC Electrical Characteristics Table
10/11/04:	Page 4	Updated Capacitance table
	Page 5	Added 7ns I-temp and removed 9ns I-temp DC power numbers from the DC Electrical Characteristics table
	Page 8	Added 7ns I-temp and removed 9ns I-temp from the AC Electrical Characteristics table
	Page 12	Added Timing Waveform of Left Port Write to Pipelined Right Port Read
	Page 18	Added 7ns I-temp and removed 9ns I-temp from ordering information
01/19/06:	Page 1	Added green availability to features
	Page 18	Added green indicator to ordering information
10/23/08:	Page 18	Removed "IDT" from orderable part number
06/25/18:		Added Tape & Reel to Ordering Information Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018



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70V9269S7PRFI 70V9279S6PRF8 70V9269S6PRF8 70V9279L6PRF 70V9269L15PRF8 70V9279S9PRF  
70V9269S9PRF 70V9279S12PRF 70V9269S12PRF 70V9279S7PRF8 70V9269S7PRF8 70V9269L12PRF8  
70V9279L12PRF8 70V9279L7PRFI8 70V9279L7PRFG8 70V9269L9PRF8 70V9279L9PRF8 70V9269L15PRF  
70V9279L7PRFGI8 70V9279L7PRFG 70V9279L7PRFI 70V9269S12PRFGI 70V9269L12PRFGI 70V9279L6PRF8  
70V9279S12PRF8 70V9269S12PRF8 70V9269L12PRFI 70V9279L7PRF 70V9279L7PRFGI 70V9269S7PRFI8  
70V9269S12PRFGI8 70V9269L12PRFGI8 70V9279S6PRF 70V9269S6PRF 70V9269S15PRF 70V9279S9PRFI8  
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