

74ALVC244

Octal buffer/line driver; 3-state

Rev. 4 — 10 October 2017

Product data sheet

1 General description

The 74ALVC244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

2 Features and benefits

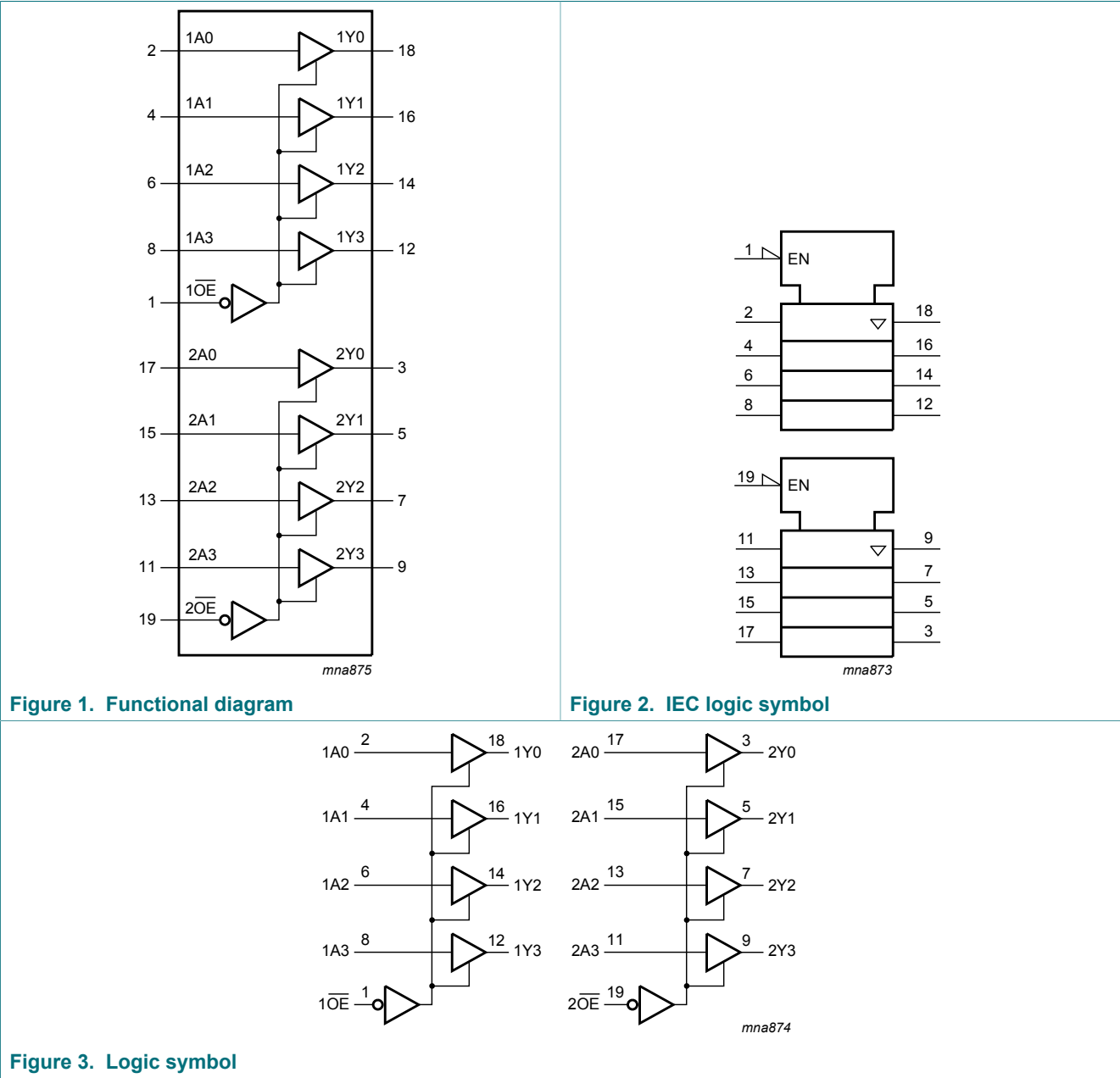
- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3 Ordering information

Table 1. Ordering information

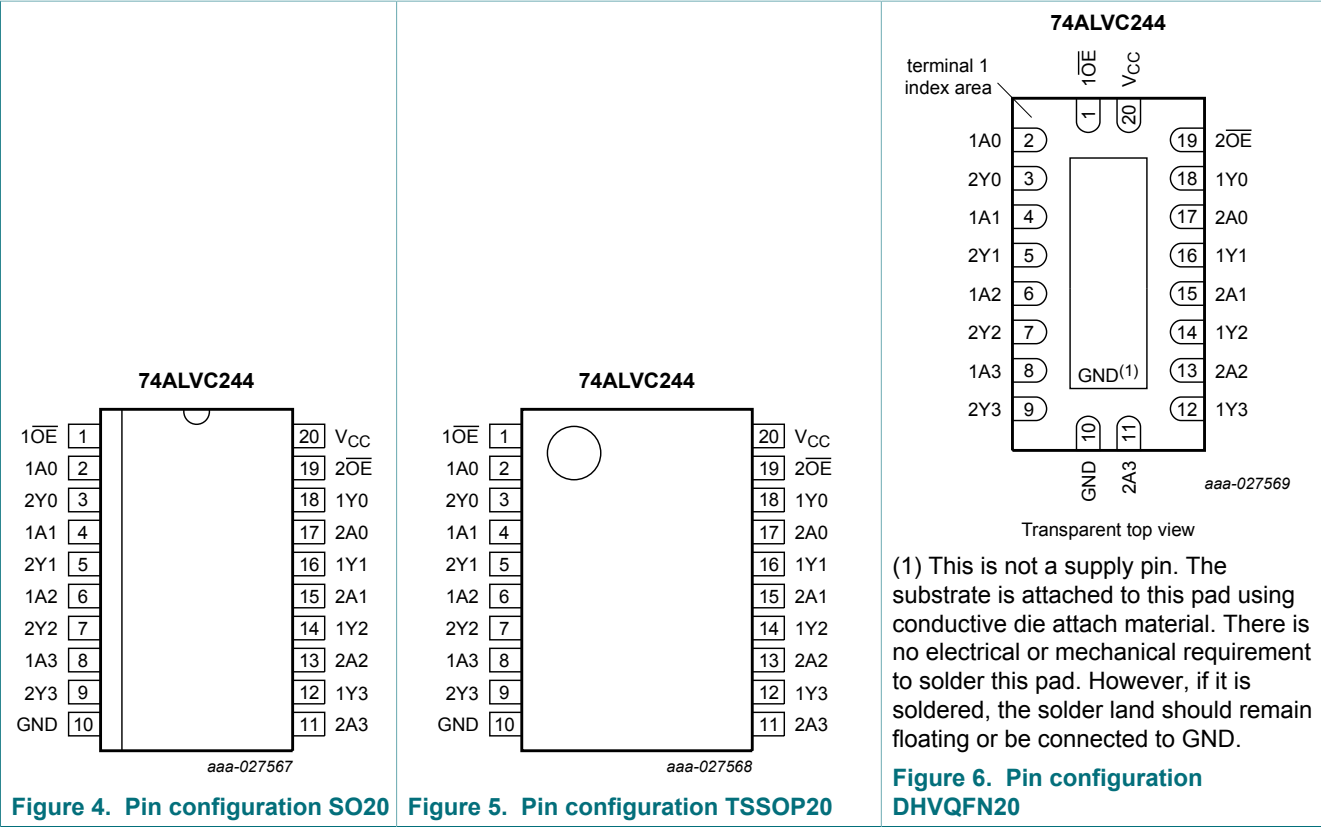
Type number	Package			
	Temperature range	Name	Description	Version
74ALVC244D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC244PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC244BQ	-40 °C to +85 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4 Functional diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
VCC	20	supply voltage

6 Functional description

Table 3. Function table ^[1]

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+4.6	V
V _O	output voltage	output HIGH or LOW state [1]	-0.5	V _{CC} + 0.5	V
		output OFF-state	-0.5	+4.6	V
		power-down mode, V _{CC} = 0 V [2]	-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-	-50	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C [3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.

For TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	$V_{CC} = 1.65$ to 3.6 V; output HIGH or LOW state	0	V_{CC}	V
		$V_{CC} = 1.65$ to 3.6 V; output OFF-state	0	3.6	V
		$V_{CC} = 0$ V; power-down mode	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\text{ }\mu\text{A}$; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6\text{ mA}$; $V_{CC} = 1.65$ V	1.25	-	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.3$ V	1.8	-	-	V
		$I_O = -18\text{ mA}$; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.7$ V	2.2	-	-	V
		$I_O = -18\text{ mA}$; $V_{CC} = 3.0$ V	2.4	-	-	V
		$I_O = -24\text{ mA}$; $V_{CC} = 3.0$ V	2.2	-	-	V

Symbol	Parameter	Conditions	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
V_{OL}	LOW-level output voltage	$V_{\text{I}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$				
		$I_{\text{O}} = 100\text{ }\mu\text{A}; V_{\text{CC}} = 1.65\text{ V to }3.6\text{ V}$	-	-	0.2	V
		$I_{\text{O}} = 6\text{ mA}; V_{\text{CC}} = 1.65\text{ V}$	-	-	0.3	V
		$I_{\text{O}} = 12\text{ mA}; V_{\text{CC}} = 2.3\text{ V}$	-	-	0.4	V
		$I_{\text{O}} = 18\text{ mA}; V_{\text{CC}} = 2.3\text{ V}$	-	-	0.6	V
		$I_{\text{O}} = 12\text{ mA}; V_{\text{CC}} = 2.7\text{ V}$	-	-	0.4	V
		$I_{\text{O}} = 18\text{ mA}; V_{\text{CC}} = 3.0\text{ V}$	-	-	0.4	V
		$I_{\text{O}} = 24\text{ mA}; V_{\text{CC}} = 3.0\text{ V}$	-	-	0.55	V
I_{I}	input leakage current	$V_{\text{CC}} = 3.6\text{ V}; V_{\text{I}} = 3.6\text{ V or GND}$	-	± 0.1	± 5	μA
I_{OZ}	OFF-state output current	$V_{\text{CC}} = 3.6\text{ V}; V_{\text{I}} = V_{\text{IH}} \text{ or } V_{\text{IL}};$ $V_{\text{O}} = 3.6\text{ V or GND}$	-	0.1	± 10	μA
I_{OFF}	power-off leakage current	$V_{\text{CC}} = 0\text{ V}; V_{\text{I}} \text{ or } V_{\text{O}} = 3.6\text{ V}$	-	± 0.1	± 10	μA
I_{CC}	supply current	$V_{\text{CC}} = 3.6\text{ V}; V_{\text{I}} = V_{\text{CC}} \text{ or GND}; I_{\text{O}} = 0\text{ A}$	-	0.2	20	μA
ΔI_{CC}	additional supply current	per input pin; $V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V};$ $V_{\text{I}} = V_{\text{CC}} - 0.6\text{ V}; I_{\text{O}} = 0\text{ A}$	-	5	750	μA
C_{I}	input capacitance		-	3.5	-	pF

[1] All typical values are measured at $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 9](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t _{pd}	propagation delay	nAn to nYn; see Figure 7 ^[2]				
		V _{CC} = 1.65 V to 1.95 V	1.0	2.7	4.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.0	3.1	ns
		V _{CC} = 2.7 V	1.0	2.3	3.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.2	2.8	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nYn; see Figure 8 ^[3]				
		V _{CC} = 1.65 V to 1.95 V	1.0	3.4	6.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	5.4	ns
		V _{CC} = 2.7 V	1.0	3.2	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	4.5	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nYn; see Figure 8 ^[4]				
		V _{CC} = 1.65 V to 1.95 V	1.0	3.8	5.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.2	4.1	ns
		V _{CC} = 2.7 V	1.0	3.0	4.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.9	4.2	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[5]	-	20	-	pF

[1] Typical values are measured at T_{amb} = 25 °C

Typical values for V_{CC} = 1.65 V to 1.95 V are measured at V_{CC} = 1.8 V

Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V

Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz

f_o = output frequency in MHz

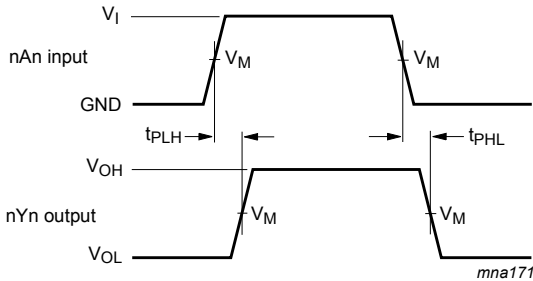
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volt

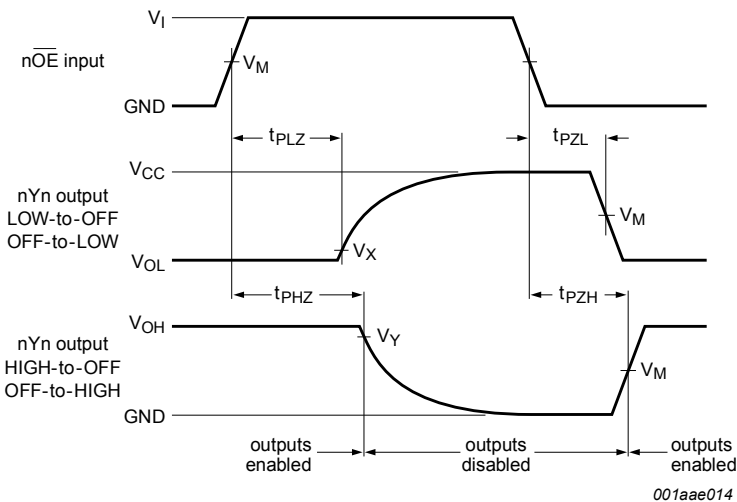
N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

10.1 Waveforms and test circuit



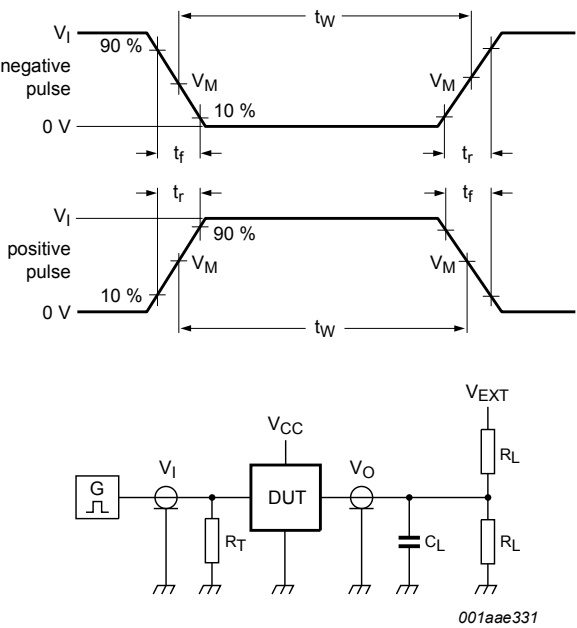
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.
Figure 7. Inputs nAn to output nYn propagation delays



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.
Figure 8. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Figure 9. Test circuit for measuring switching times

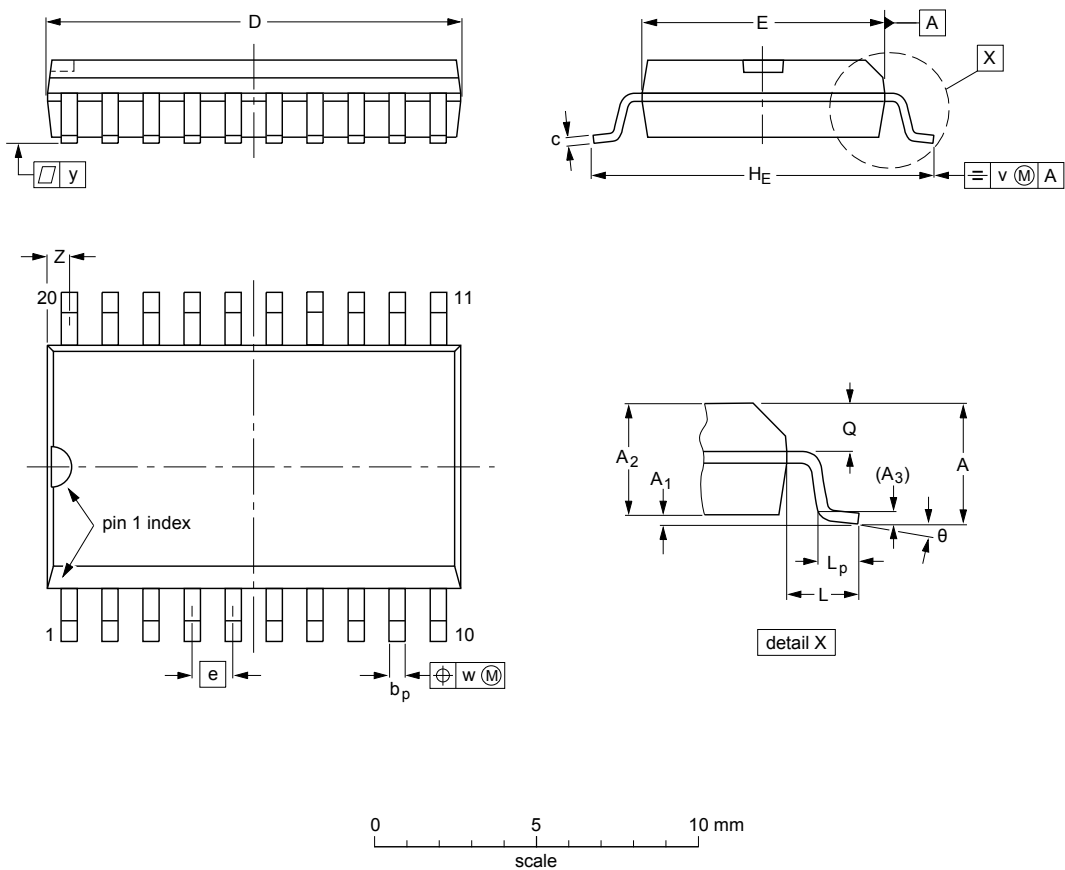
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

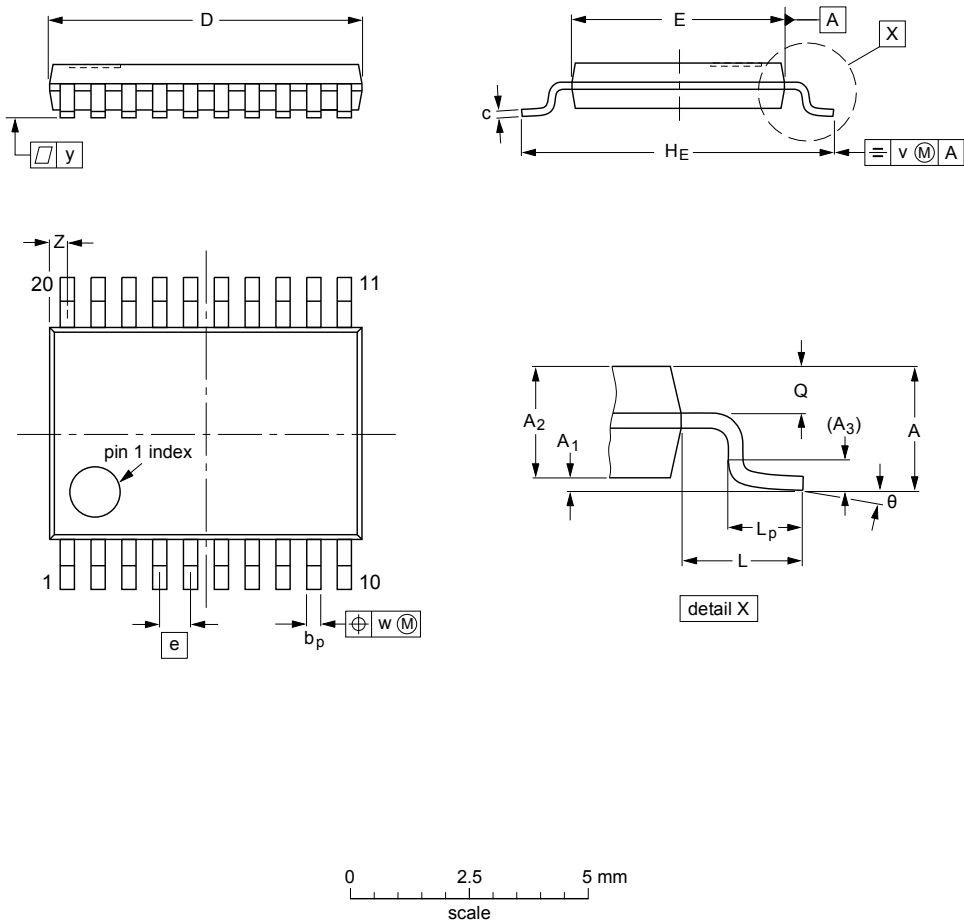
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Figure 10. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

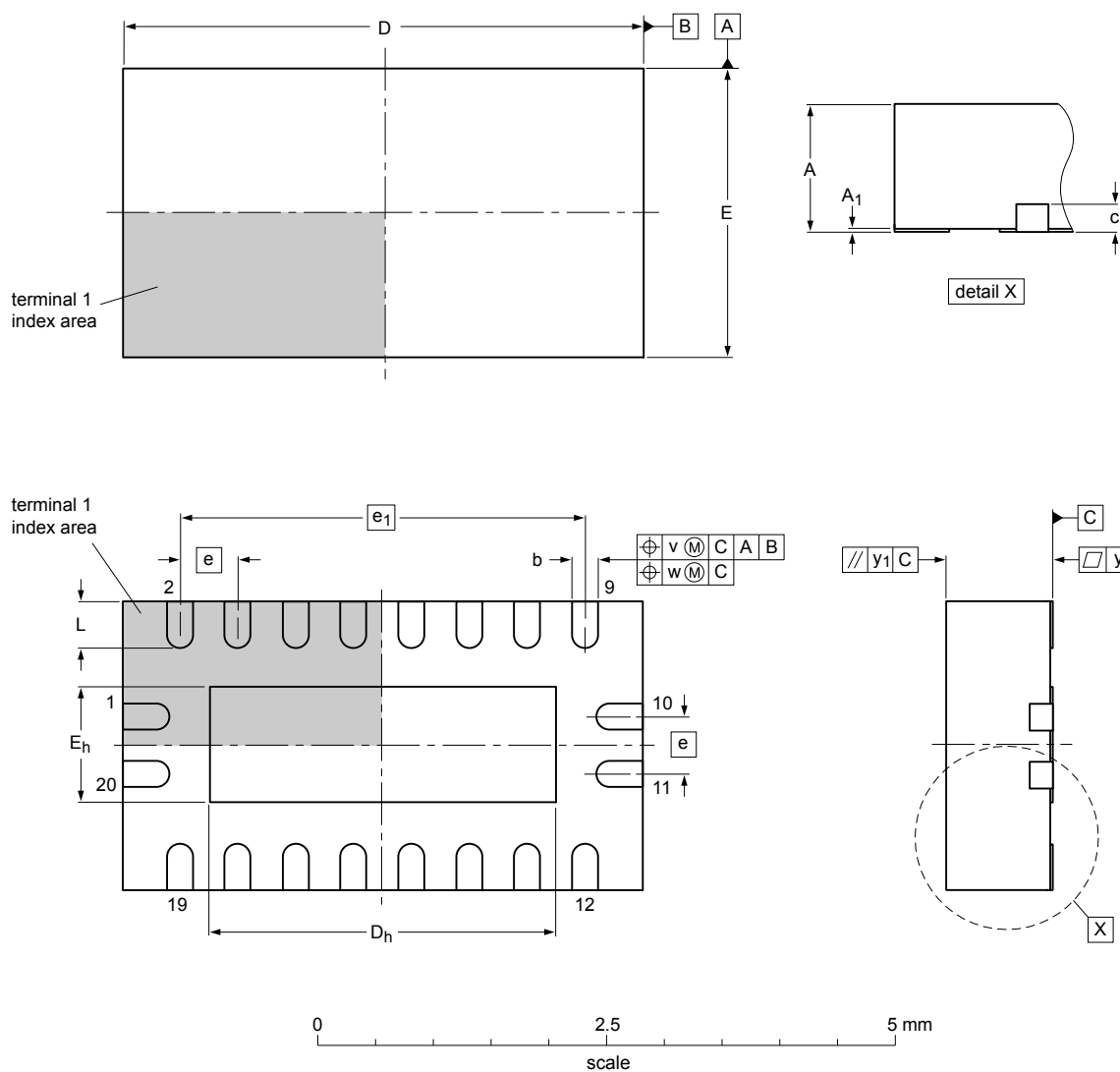
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				-99-12-27- 03-02-19

Figure 11. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	---	MO-241	---			03-01-27 14-12-12

Figure 12. Package outline SOT764-1 (DHVQFN20)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC244 v.4	20171010	Product data sheet	-	74ALVC244 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74ALVC244 v.3	20030908	Product specification	-	74ALVC244 v.2
74ALVC244 v.2	20030811	Product specification	-	74ALVC244 v.1
74ALVC244 v.1	20011030	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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