

## SPI/Digital or I<sup>2</sup>C μModule Isolator with Fixed ±5V and Adjustable 5V Regulated Power

### FEATURES

- 6-Channel Logic Isolator: 2500V<sub>RMS</sub> for 1 Minute
- UL-CSA Recognized cULus File #E151738
- Isolated DC Power:
  - 3V to 5V Adjustable at Up to 100mA
  - ±5V Fixed at Up to 100mA
- No External Components Required
- SPI/Digital (LTM2886-S) or I<sup>2</sup>C (LTM2886-I) Options
- High Common Mode Transient Immunity: 30kV/μs
- High Speed Operation:
  - 10MHz Digital Isolation
  - 4MHz/8MHz SPI Isolation
  - 400kHz I<sup>2</sup>C Isolation
- 3.3V (LTM2886-3) or 5V (LTM2886-5) Operation
- 1.62V to 5.5V Logic Supply
- ±10kV ESD HBM Across the Isolation Barrier
- Maximum Continuous Working Voltage: 560V<sub>PEAK</sub>
- Low Current Shutdown Mode (<10μA)
- Low Profile (15mm × 11.25mm × 3.42mm) BGA Package

### APPLICATIONS

- Isolated SPI or I<sup>2</sup>C Interfaces
- Industrial Systems
- Test and Measurement Equipment
- Breaking Ground Loops

### DESCRIPTION

The LTM<sup>®</sup>2886 is a complete galvanic digital μModule<sup>®</sup> (micromodule) isolator. No external components are required. A single 3.3V or 5V supply powers both sides of the interface through an integrated, isolated DC/DC converter. A logic supply pin allows easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

Available options are compliant with SPI and I<sup>2</sup>C (master mode only) specifications.

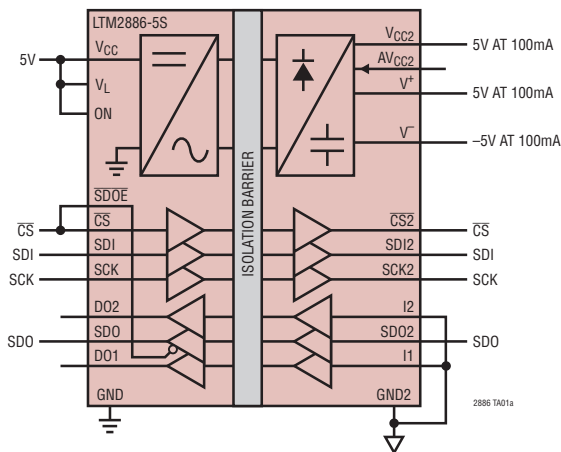
The isolated side includes fixed ±5V and 5V adjustable power supplies, each capable of providing more than 100mA of load current. The 5V adjustable supply may be programmed via an external voltage divider.

Coupled inductors and an isolation power transformer provide 2500V<sub>RMS</sub> of isolation between the input and output logic interface. This device is ideal for systems where the ground loop is broken, allowing for a large common mode voltage range. Communication is uninterrupted for common mode transients greater than 30kV/μs.

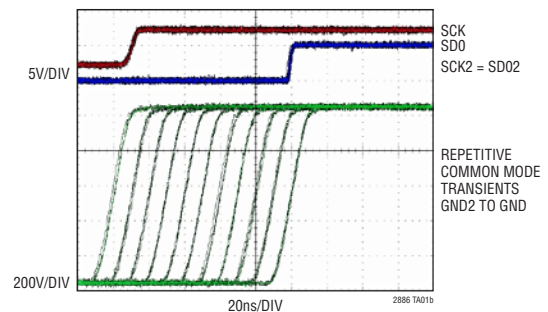
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### TYPICAL APPLICATION

Isolated 4MHz SPI Interface



LTM2886 Operating Through 50kV/μs CM Transients



# LTM2886

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CC}$ to GND	-0.3V to 6V
$V_L$ to GND	-0.3V to 6V
$V_{CC2}$ , $AV_{CC2}$ to GND2	-0.3V to 6V
$V^+$ to GND2	-0.3V to 6V
$V^-$ to GND2	0.3V to -6V
Logic Inputs	
DI1, SCK, SDI, $\overline{CS}$ , SCL, SDA, $\overline{SDOE}$ , ON to GND	-0.3V to ( $V_L + 0.3V$ )
I1, I2, SDA2, SDO2 to GND2	-0.3V to ( $V_{CC2} + 0.3V$ )

Logic Outputs

DO1, DO2, SDO to GND	-0.3V to ( $V_L + 0.3V$ )
O1, SCK2, SDI2, $\overline{CS2}$ , SCL2 to GND2	-0.3V to ( $V_{CC2} + 0.3V$ )

Operating Temperature Range (Note 4)

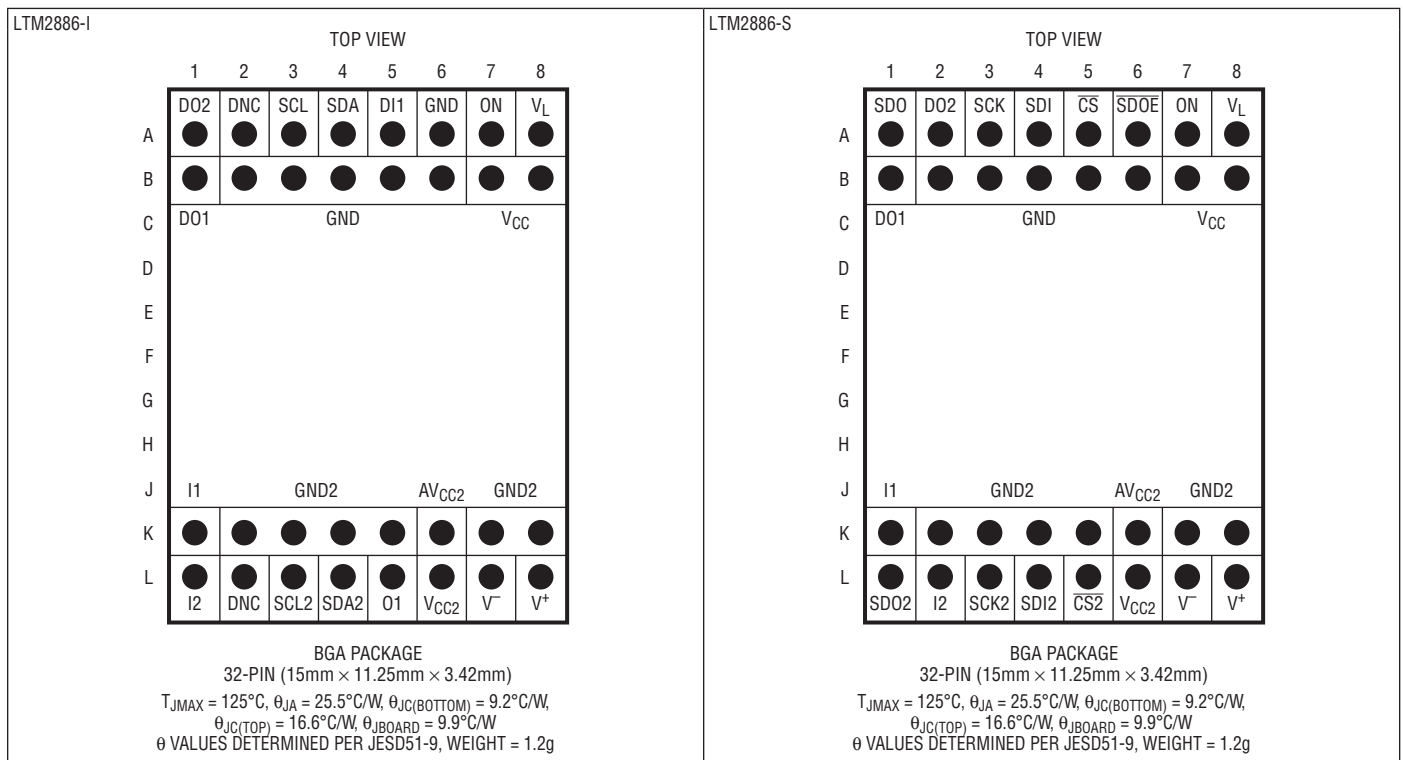
LTM2886C	0°C to 70°C
LTM2886I	-40°C to 85°C
LTM2886H	-40°C to 125°C

Maximum Internal Operating Temperature..... 125°C

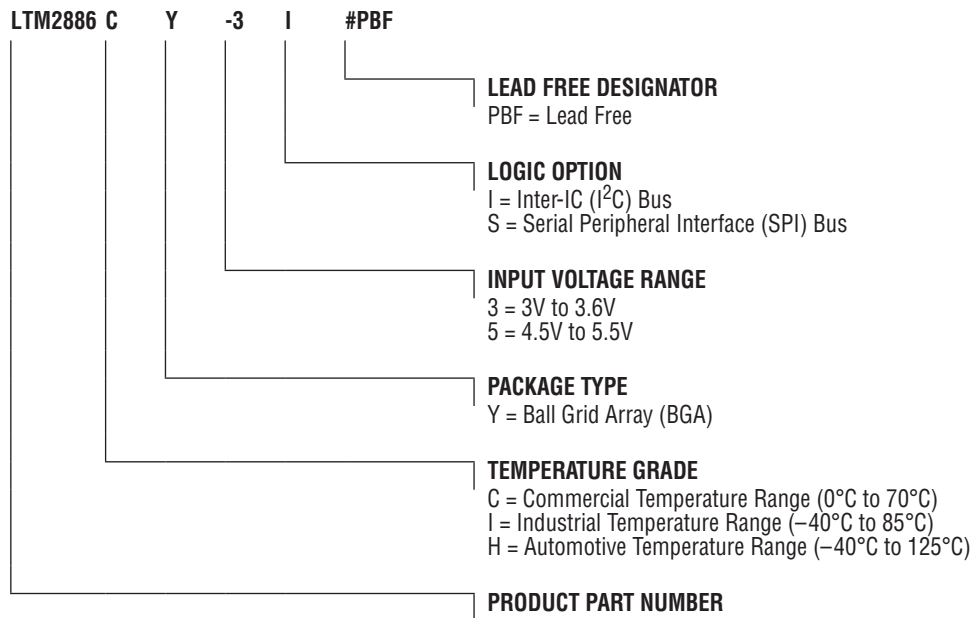
Storage Temperature Range ..... -55°C to 125°C

Peak Body Reflow Temperature ..... 245°C

## PIN CONFIGURATION



## PRODUCT SELECTION GUIDE



## ORDER INFORMATION <http://www.linear.com/product/LTM2886#orderinfo>

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	INPUT VOLTAGE RANGE	LOGIC OPTION	TEMPERATURE RANGE			
		DEVICE	FINISH CODE								
LTM2886CY-3I#PBF	SAC305 (RoHS)	LTM2886Y-3I	e1	BGA	3	3V to 3.6V	I <sup>2</sup> C	0°C to 70°C			
LTM2886IY-3I#PBF								-40°C to 85°C			
LTM2886HY-3I#PBF								-40°C to 125°C			
LTM2886CY-3S#PBF							SPI	0°C to 70°C			
LTM2886IY-3S#PBF								-40°C to 85°C			
LTM2886HY-3S#PBF								-40°C to 125°C			
LTM2886CY-5I#PBF		LTM2886Y-5I				e1	BGA	3	4.5V to 5.5V	I <sup>2</sup> C	0°C to 70°C
LTM2886IY-5I#PBF											-40°C to 85°C
LTM2886HY-5I#PBF											-40°C to 125°C
LTM2886CY-5S#PBF										SPI	0°C to 70°C
LTM2886IY-5S#PBF											-40°C to 85°C
LTM2886HY-5S#PBF											-40°C to 125°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: [www.linear.com/leadfree](http://www.linear.com/leadfree)
- This product is not recommended for second side reflow. For more information, go to [www.linear.com/BGA-assy](http://www.linear.com/BGA-assy)
- Recommended BGA PCB Assembly and Manufacturing Procedures: [www.linear.com/BGA-assy](http://www.linear.com/BGA-assy)
- BGA Package and Tray Drawings: [www.linear.com/packaging](http://www.linear.com/packaging)
- This product is moisture sensitive. For more information, go to: [www.linear.com/BGA-assy](http://www.linear.com/BGA-assy)

# LTM2886

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . LTM2886-3  $V_{CC} = 3.3\text{V}$ , LTM2886-5  $V_{CC} = 5\text{V}$ ,  $V_L = 3.3\text{V}$ , and  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Input Supplies</b>							
$V_{CC}$	Input Supply Range	LTM2886-3	●	3	3.3	3.6	V
		LTM2886-5	●	4.5	5	5.5	V
$V_L$	Logic Supply Range	LTM2886-S	●	1.62		5.5	V
		LTM2886-I	●	3	5	5.5	V
$I_{CC}$	Input Supply Current	ON = 0V	●		0	10	$\mu\text{A}$
		LTM2886-3, No Load	●		25	37	mA
		LTM2886-5, No Load	●		19	27	mA
$I_L$	Logic Supply Current	ON = 0V	●		0	10	$\mu\text{A}$
		LTM2886-S, ON = $V_L$			10		$\mu\text{A}$
		LTM2886-I, ON = $V_L$				150	$\mu\text{A}$
<b>Output Supplies</b>							
$V_{CC2}$	Regulated Output Voltage	No Load, $\text{AV}_{CC2}$ OPEN	●	4.75	5	5.25	V
	Output Voltage Operating Range	(Note 2)		3		5.5	V
	Line Regulation	$I_{LOAD} = 1\text{mA}$ , $\text{MIN} \leq V_{CC} \leq \text{MAX}$	●		2	7.5	mV
	Load Regulation	$I_{LOAD} = 1\text{mA}$ to 100mA	●		15	100	mV
	ADJ Pin Voltage	$I_{LOAD} = 1\text{mA}$ to 100mA	●	1.15	1.220	1.27	V
	Voltage Ripple	$I_{LOAD} = 100\text{mA}$ (Note 2)			1		mV <sub>RMS</sub>
	Efficiency	LTM2886-5, $I_{LOAD} = 100\text{mA}$ (Note 2)			61		%
$I_{CC2}$	Output Short Circuit Current	$V_{CC2} = 0\text{V}$			150		mA
	Current Limit	$\Delta V_{CC2} = -5\%$	●	90			mA
$V^+$	Regulated Output Voltage	No Load	●	4.8	5	5.2	V
	Line Regulation	$I_{LOAD} = 1\text{mA}$ , $\text{MIN} \leq V_{CC} \leq \text{MAX}$	●		2	7.5	mV
	Load Regulation	$I_{LOAD} = 1\text{mA}$ to 100mA	●		35	150	mV
	Voltage Ripple	$I_{LOAD} = 100\text{mA}$ (Note 2)			1		mV <sub>RMS</sub>
	Efficiency	LTM2886-5, $I_{LOAD} = 100\text{mA}$ (Note 2)			61		%
$I^+$	Output Short Circuit Current	$V^+ = 0\text{V}$			150		mA
	Current Limit	$\Delta V^+ = -5\%$	●	90			mA
$V^-$	Regulated Output Voltage	No Load	●	-4.8	-5	-5.2	V
	Line Regulation	$I_{LOAD} = -1\text{mA}$ , $\text{MIN} \leq V_{CC} \leq \text{MAX}$	●		5	15	mV
	Load Regulation	$I_{LOAD} = 1\text{mA}$ to 100mA	●		35	150	mV
	Voltage Ripple	$I_{LOAD} = 100\text{mA}$ (Note 2)			1		mV <sub>RMS</sub>
	Efficiency	LTM2886-5, $I_{LOAD} = 100\text{mA}$ (Note 2)			61		%
$I^-$	Output Short-Circuit Current	$V^- = 0\text{V}$			150		mA
	Current Limit	$\Delta V^- = 5\%$	●	90			mA

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . LTM2886-3  $V_{CC} = 3.3\text{V}$ , LTM2886-5  $V_{CC} = 5\text{V}$ ,  $V_L = 3.3\text{V}$ , and  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Logic/SPI</b>						
$V_{\text{ITH}}$	Input Threshold Voltage	ON, DI1, $\overline{\text{SDOE}}$ , SCK, SDI, $\overline{\text{CS}}$ : $1.62\text{V} \leq V_L < 2.35\text{V}$ ON, DI1, $\overline{\text{SDOE}}$ , SCK, SDI, $\overline{\text{CS}}$ : $2.35\text{V} \leq V_L$ I1, I2, SDO2	● ● ●	$0.25 \cdot V_L$ $0.33 \cdot V_L$ $0.33 \cdot V_{\text{CC2}}$	$0.75 \cdot V_L$ $0.67 \cdot V_L$ $0.67 \cdot V_{\text{CC2}}$	V V V
$I_{\text{INL}}$	Input Current		●		$\pm 1$	$\mu\text{A}$
$V_{\text{HYS}}$	Input Hysteresis			150		mV
$V_{\text{OH}}$	Output High Voltage	DO1, DO2, SDO, $I_{\text{LOAD}} = -1\text{mA}$ , $1.62\text{V} \leq V_L < 3\text{V}$ , $I_{\text{LOAD}} = -4\text{mA}$ , $3\text{V} \leq V_L \leq 5.5\text{V}$	●	$V_L - 0.4$		V
		O1, SCK2, SDI2, $\overline{\text{CS2}}$ , $I_{\text{LOAD}} = -4\text{mA}$	●	$V_{\text{CC2}} - 0.4$		V
$V_{\text{OL}}$	Output Low Voltage	DO1, DO2, SDO, $I_{\text{LOAD}} = 1\text{mA}$ , $1.62\text{V} \leq V_L < 3\text{V}$ , $I_{\text{LOAD}} = 4\text{mA}$ , $3\text{V} \leq V_L \leq 5.5\text{V}$	●		0.4	V
		O1, SCK2, SDI2, $\overline{\text{CS2}}$ , $I_{\text{LOAD}} = 4\text{mA}$	●		0.4	V
$I_{\text{SC}}$	Short-Circuit Current	$0\text{V} \leq (\text{DO1}, \text{DO2}, \text{SDO}) \leq V_L$ $0\text{V} \leq (\text{O1}, \text{SCK2}, \text{SDI2}, \overline{\text{CS2}}) \leq V_{\text{CC2}}$	●	$\pm 60$	$\pm 85$	mA mA
<b>I<sup>2</sup>C</b>						
$V_{\text{IL}}$	Low Level Input Voltage	SCL, SDA SDA2	● ●		$0.3 \cdot V_L$ $0.3 \cdot V_{\text{CC2}}$	V V
$V_{\text{IH}}$	High Level Input Voltage	SCL, SDA SDA2	● ●	$0.7 \cdot V_L$ $0.7 \cdot V_{\text{CC2}}$		V V
$I_{\text{INL}}$	Input Current	SCL, SDA = $V_L$ or $0\text{V}$ SDA2 = $V_{\text{CC2}}$ , SDA2 = $V_{\text{CC2}} = 0\text{V}$	● ●		$\pm 1$ $\pm 1$	$\mu\text{A}$ $\mu\text{A}$
$V_{\text{HYS}}$	Input Hysteresis	SCL, SDA SDA2		$0.05 \cdot V_L$ $0.05 \cdot V_{\text{CC2}}$		V V
$V_{\text{OH}}$	Output High Voltage	SCL2, $I_{\text{LOAD}} = -2\text{mA}$ DO2, $I_{\text{LOAD}} = -2\text{mA}$	● ●	$V_{\text{CC2}} - 0.4$ $V_L - 0.4$		V V
$V_{\text{OL}}$	Output Low Voltage	SDA, $I_{\text{LOAD}} = 3\text{mA}$ DO2, $I_{\text{LOAD}} = 2\text{mA}$ SCL2, $I_{\text{LOAD}} = 2\text{mA}$ SDA2, No Load, SDA = $0\text{V}$ , $4.5\text{V} \leq V_{\text{CC2}} < 5.5\text{V}$ SDA2, No Load, SDA = $0\text{V}$ , $3\text{V} \leq V_{\text{CC2}} < 4.5\text{V}$	● ● ● ● ●		0.4 0.4 0.4 0.45 0.55	V V V V V
$C_{\text{IN}}$	Input Pin Capacitance	SCL, SDA, SDA2 (Note 2)	●		10	pF
$C_{\text{B}}$	Bus Capacitive Load	SCL2, Standard Speed (Note 2) SCL2, Fast Speed SDA, SDA2, $\text{SR} \geq 1\text{V}/\mu\text{s}$ , Standard Speed (Note 2) SDA, SDA2, $\text{SR} \geq 1\text{V}/\mu\text{s}$ , Fast Speed	● ● ● ●		400 200 400 200	pF pF pF pF
	Minimum Bus Slew Rate	SDA, SDA2	●	1		V/ $\mu\text{s}$
$I_{\text{SC}}$	Short-Circuit Current	SDA2 = $0$ , SDA = $V_L$ $0\text{V} \leq \text{SCL2} \leq V_{\text{CC2}}$ $0\text{V} \leq \text{DO2} \leq V_L$ SDA = $0$ , SDA2 = $V_{\text{CC2}}$ SDA = $V_L$ , SDA2 = $0$	●	$\pm 30$ $\pm 30$ 6 -1.8	100	mA mA mA mA
<b>ESD (HBM) (Note 2)</b>						
	Isolation Boundary	( $V_{\text{CC2}}$ , $V^+$ , $V^-$ , GND2) to ( $V_{\text{CC}}$ , $V_L$ , GND)			$\pm 10$	kV

**SWITCHING CHARACTERISTICS** The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . LTM2886-3  $V_{CC} = 3.3\text{V}$ , LTM2886-5  $V_{CC} = 5\text{V}$ ,  $V_L = 3.3\text{V}$ , and  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted. Specifications apply to all options unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Logic</b>							
	Maximum Data Rate	D11 → O1, Ix → DOx, $C_L = 15\text{pF}$ (Note 3)	●	10		MHz	
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay	$C_L = 15\text{pF}$ (Figure 1)	●	35	60	100	ns
$t_{\text{R}}$	Rise Time	$C_L = 15\text{pF}$ (Figure 1) LTM2886-I, DO2, $C_L = 15\text{pF}$ (Figure 1)	● ●		3 20	12.5 35	ns ns
$t_{\text{F}}$	Fall Time	$C_L = 15\text{pF}$ (Figure 1) LTM2886-I, DO2, $C_L = 15\text{pF}$ (Figure 1)	● ●		3 20	12.5 35	ns ns
<b>SPI</b>							
	Maximum Data Rate	Bidirectional Communication (Note 3) Unidirectional Communication (Note 3)	● ●	4 8			MHz MHz
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay	$C_L = 15\text{pF}$ (Figure 1)	●	35	60	100	ns
$t_{\text{PWU}}$	Output Pulse Width Uncertainty	SDO, SDI2, $\overline{\text{CS2}}$ (Note 2)				±50	ns
$t_{\text{R}}$	Rise Time	$C_L = 15\text{pF}$ (Figure 1)	●		3	12.5	ns
$t_{\text{F}}$	Fall Time	$C_L = 15\text{pF}$ (Figure 1)	●		3	12.5	ns
$t_{\text{PZH}}, t_{\text{PZL}}$	Output Enable Time	$\overline{\text{SDOE}} = \downarrow$ , $R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ (Figure 2)	●			50	ns
$t_{\text{PHZ}}, t_{\text{PLZ}}$	Output Disable Time	$\overline{\text{SDOE}} = \uparrow$ , $R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ (Figure 2)	●			50	ns
<b>I<sup>2</sup>C</b>							
	Maximum Data Rate	(Note 3)	●	400			kHz
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay	SCL → SCL2, $C_L = 15\text{pF}$ (Figure 1) SDA → SDA2, $R_L = \text{Open}$ , $C_L = 15\text{pF}$ (Figure 3) SDA2 → SDA, $R_L = 1.1\text{k}\Omega$ , $C_L = 15\text{pF}$ (Figure 3)	● ● ●		150 150 300	225 250 500	ns ns ns
$t_{\text{PWU}}$	Output Pulse Width Uncertainty	SDA, SDA2 (Note 2)				±50	ns
$t_{\text{HD, DAT}}$	Data Hold Time	(Note 2)			600		ns
$t_{\text{R}}$	Rise Time	SDA2, $C_L = 200\text{pF}$ (Figure 3) SDA, $R_L = 1.1\text{k}\Omega$ , $C_L = 200\text{pF}$ (Figure 3) SCL2, $C_L = 200\text{pF}$ (Figure 1)	● ● ●	40 40		300 250 250	ns ns ns
$t_{\text{F}}$	Fall Time	SDA2, $C_L = 200\text{pF}$ (Figure 3) SDA, $R_L = 1.1\text{k}\Omega$ , $C_L = 200\text{pF}$ (Figure 3) SCL2, $C_L = 200\text{pF}$ (Figure 1)	● ● ●	40 40		250 250 250	ns ns ns
$t_{\text{SP}}$	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
<b>Power Supply</b>							
	Power-Up Time	ON = ↑ to $V_{CC2}$ (Min) ON = ↑ to $V^+$ (Min) ON = ↑ to $V^-$ (Min)	● ● ●		0.6 0.6 0.6	5 5 5	ms ms ms

## ISOLATION CHARACTERISTICS $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{ISO}$	Rated Dielectric Insulation Voltage	1 Minute, Derived from 1 Second Test 1 Second (Notes 5, 6)	2500 3000			$V_{RMS}$ $V_{RMS}$
	Common Mode Transient Immunity	LTM2886-3 $V_{CC} = 3.3\text{V}$ , LTM2885-5 $V_{CC} = 5\text{V}$ , $V_L = ON = 3.3\text{V}$ , $V_{CM} = 1\text{kV}$ , $\Delta t = 33\text{ns}$ (Note 2)	30			$\text{kV}/\mu\text{s}$
$V_{IORM}$	Maximum Continuous Working Voltage	(Notes 2, 5)	560 400			$V_{PEAK}$ $V_{DC}$ $V_{RMS}$
	Partial Discharge	$V_{PD} = 750V_{RMS}$ (Note 5)			5	$\text{pC}$
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			$V_{RMS}$
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.06		mm
	Input to Output Resistance	(Notes 2, 5)	$10^9$			$\Omega$
	Input to Output Capacitance	(Notes 2, 5)		6		$\text{pF}$
	Creepage Distance	(Note 2)		9.5		mm

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Guaranteed by design and not subject to production test.

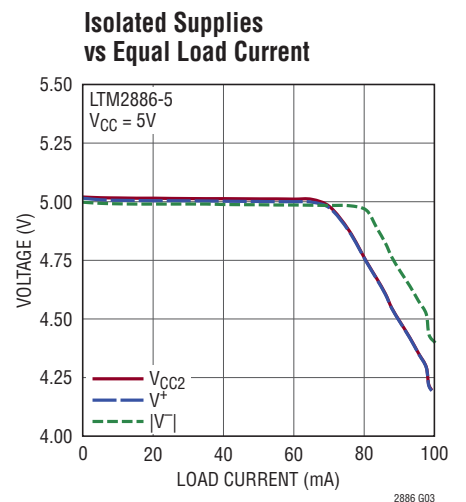
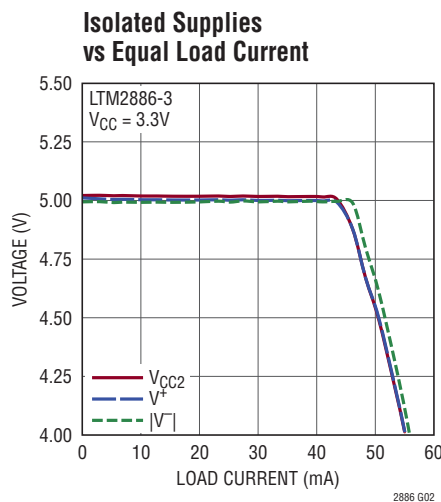
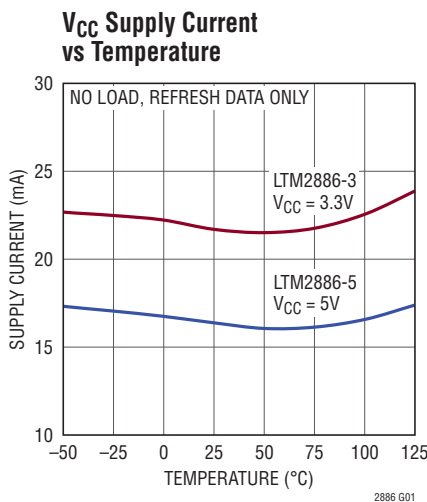
**Note 3:** Maximum Data rate is guaranteed by other measured parameters and is not tested directly.

**Note 4:** This Module includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

**Note 5:** Device considered a 2-terminal device. Pin group A1 through B8 shorted together and pin group K1 through L8 shorted together.

**Note 6:** The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , LTM2886-3 $V_{CC} = 3.3\text{V}$ , LTM2886-5 $V_{CC} = 5\text{V}$ , $V_L = 3.3\text{V}$ , $\text{GND} = \text{GND2} = 0\text{V}$ , $\text{ON} = V_L$ unless otherwise noted.



# LTM2886

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , LTM2886-3 $V_{CC} = 3.3\text{V}$ , LTM2886-5 $V_{CC} = 5\text{V}$ , $V_L = 3.3\text{V}$ , $\text{GND} = \text{GND2} = 0\text{V}$ , $\text{ON} = V_L$ unless otherwise noted.

**$V_{CC2}$  Line Regulation vs Load Current**



**$V^+$  Line Regulation vs Load Current**



**$V^-$  Line Regulation vs Load Current**



**$V_{CC2}$  Line Regulation vs Load Current**



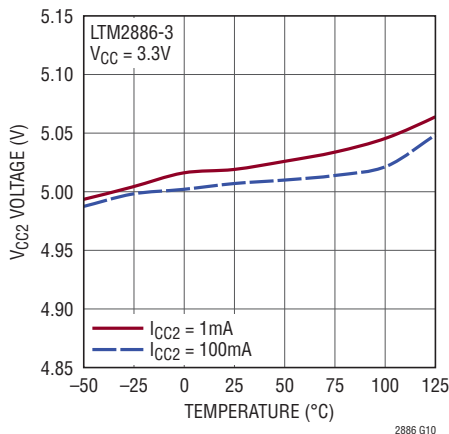
**$V^+$  Line Regulation vs Load Current**



**$V^-$  Line Regulation vs Load Current**



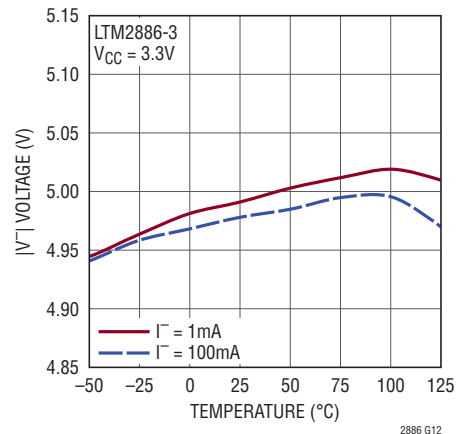
**$V_{CC2}$  Load Regulation vs Temperature**



**$V^+$  Load Regulation vs Temperature**



**$V^-$  Load Regulation vs Temperature**



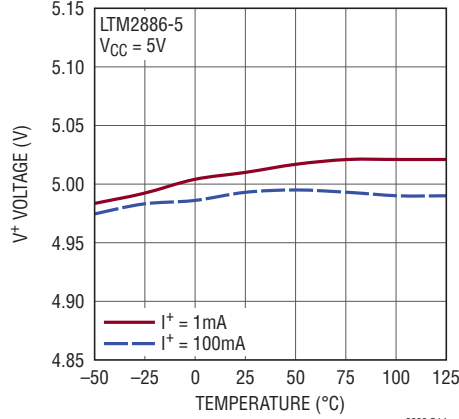


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , LTM2886-3  $V_{CC} = 3.3\text{V}$ , LTM2886-5  $V_{CC} = 5\text{V}$ ,  $V_L = 3.3\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted.

**$V_{CC2}$  Load Regulation vs Temperature**



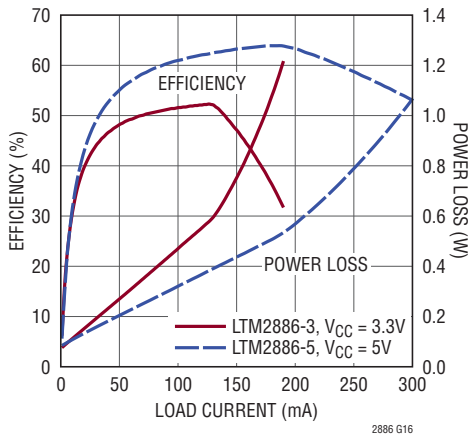
**$V^+$  Load Regulation vs Temperature**



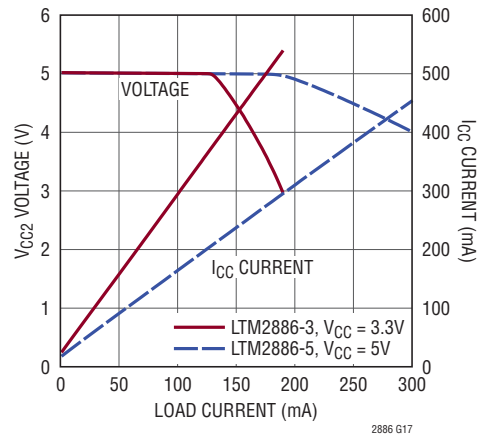
**$V^-$  Load Regulation vs Temperature**



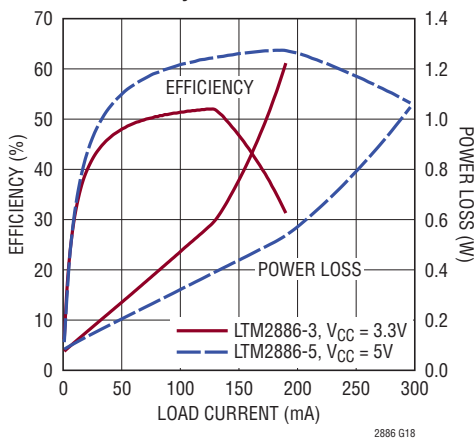
**$V_{CC2}$  Efficiency**



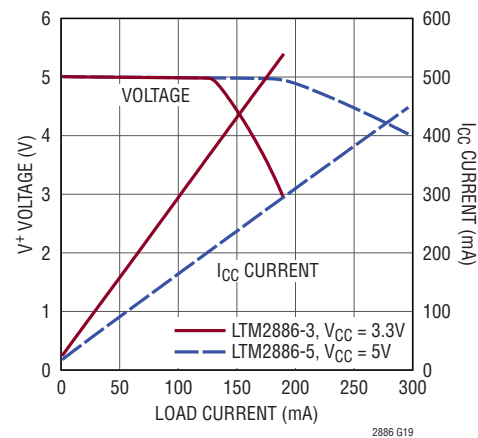
**$V_{CC2}$  Voltage and  $I_{CC}$  Current vs Load Current**



**$V^+$  Efficiency**

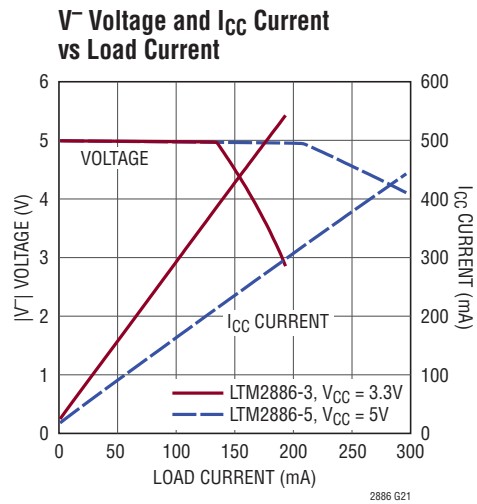
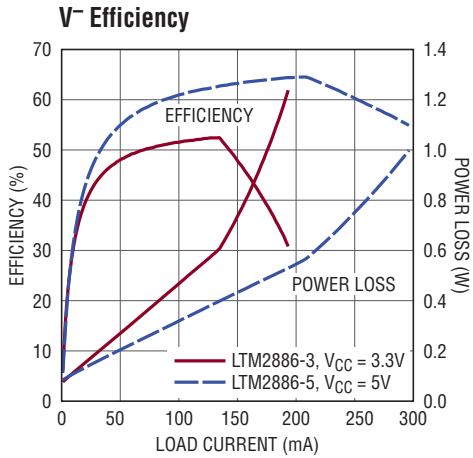


**$V^+$  Voltage and  $I_{CC}$  Current vs Load Current**



# LTM2886

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , LTM2886-3 $V_{CC} = 3.3\text{V}$ , LTM2886-5 $V_{CC} = 5\text{V}$ , $V_L = 3.3\text{V}$ , $\text{GND} = \text{GND2} = 0\text{V}$ , $\text{ON} = V_L$ unless otherwise noted.



### V<sub>CC2</sub> Transient Response 100mA Load Step



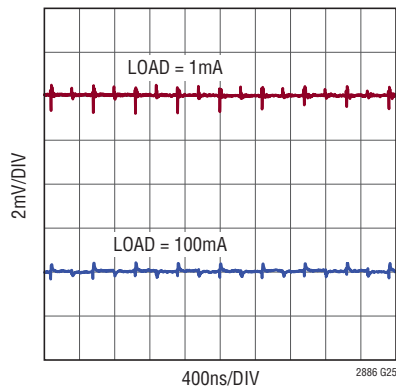
### V<sup>+</sup> Transient Response 100mA Load Step



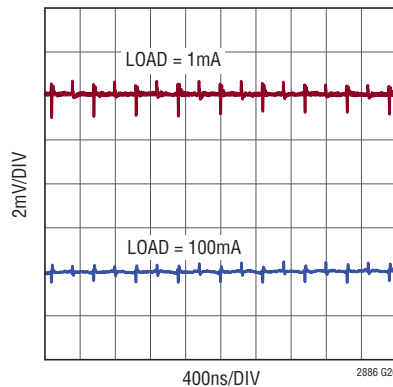
### V<sup>-</sup> Transient Response 100mA Load Step



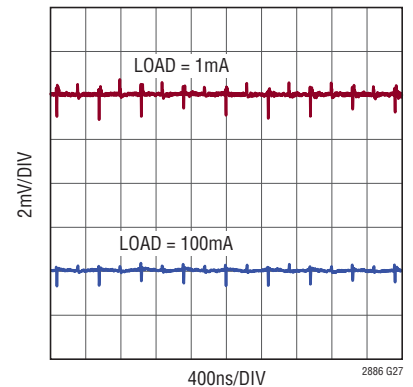
### V<sub>CC2</sub> Ripple



### V<sup>+</sup> Ripple



### V<sup>-</sup> Ripple



**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , LTM2886-3  $V_{CC} = 3.3\text{V}$ , LTM2886-5  $V_{CC} = 5\text{V}$ ,  $V_L = 3.3\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted.

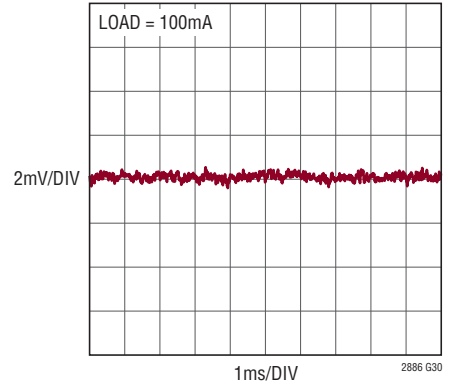
**$V_{CC2}$  Noise**



**$V^+$  Noise**



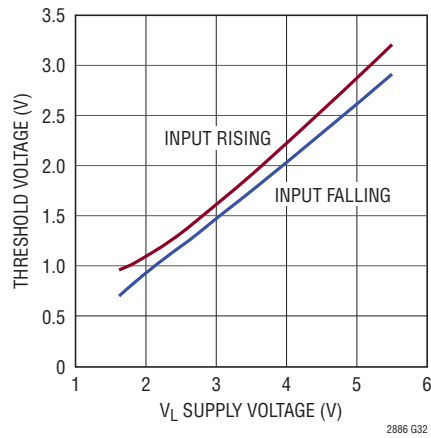
**$V^-$  Noise**



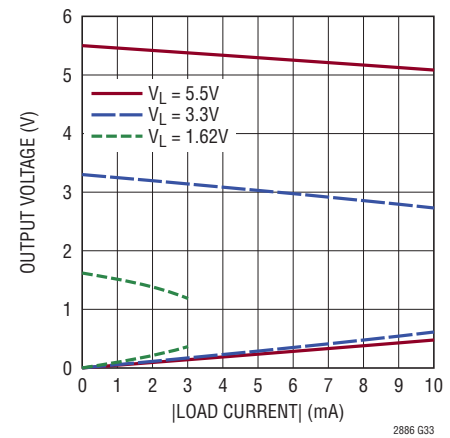
**$V_{CC}$  Supply Current vs Single Channel Data Rate**



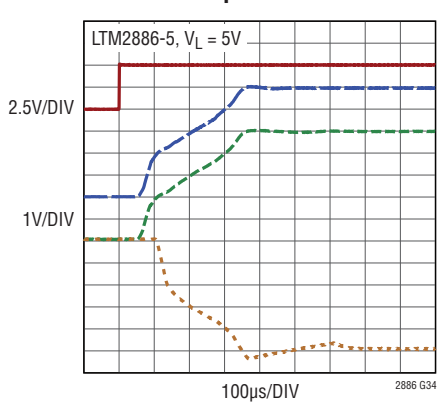
**Logic Input Threshold vs  $V_L$  Supply Voltage**



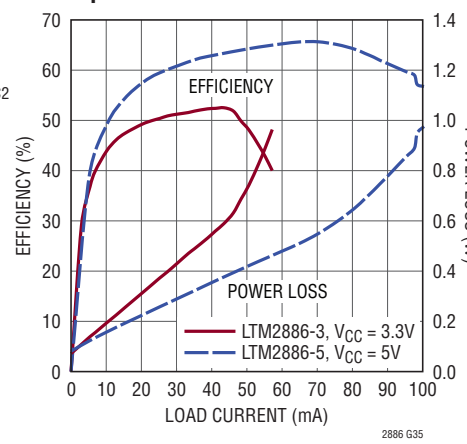
**Logic Output Voltage vs Load Current**



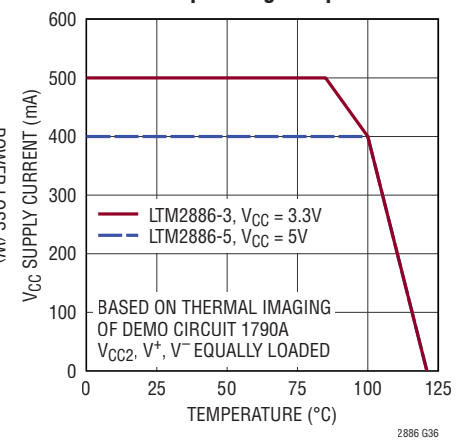
**Power On Sequence**



**Isolated Supply Efficiency with Equal Load Current**



**Derating for 125°C Maximum Internal Operating Temperature**



**PIN FUNCTIONS** (LTM2886-1)**Logic Side**

**DO2 (A1):** Digital Output, Referenced to  $V_L$  and GND. Logic output connected to I2 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

**DNC (A2):** Do Not Connect. Pin connected internally.

**SCL (A3):** Serial I<sup>2</sup>C Clock Input, Referenced to  $V_L$  and GND. Logic input connected to isolated side SCL2 pin through isolation barrier. Clock is unidirectional from logic to isolated side. Do not float.

**SDA (A4):** Serial I<sup>2</sup>C Data Pin, Referenced to  $V_L$  and GND. Bidirectional logic pin connected to isolated side SDA2 pin through isolation barrier. Under the condition of an isolation communication failure this pin is in a high impedance state. Do not float.

**DI1 (A5):** Digital Input, Referenced to  $V_L$  and GND. Logic input connected to O1 through isolation barrier. The logic state on DI1 translates to the same logic state on O1. Do not float.

**GND (A6, B2 to B6):** Circuit Ground.

**ON (A7):** Enable, Referenced to  $V_L$  and GND. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state, and the isolated side is unpowered. Do not float.

**$V_L$  (A8):** Logic Supply. Interface supply voltage for pins DI1, SCL, SDA, DO1, DO2, and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed with 1 $\mu$ F.

**DO1 (B1):** Digital Output, Referenced to  $V_L$  and GND. Logic output connected to I1 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

**$V_{CC}$  (B7 to B8):** Supply Voltage. Operating voltage is 3V to 3.6V for LTM2886-3 and 4.5V to 5.5V for LTM2886-5. Internally bypassed with 2.2 $\mu$ F.

**Isolated Side**

**I2 (L1):** Digital Input, Referenced to  $V_{CC2}$  and GND2. Logic input connected to DO2 through isolation barrier.

The logic state on I2 translates to the same logic state on DO2. Do not float.

**DNC (L2):** Do Not Connect. Pin connected internally.

**SCL2 (L3):** Serial I<sup>2</sup>C Clock Output, Referenced to  $V_{CC2}$  and GND2. Logic output connected to logic side SCL pin through isolation barrier. Clock is unidirectional from logic to isolated side. SCL2 has a push-pull output stage, do not connect an external pull-up device. Under the condition of an isolation communication failure this output defaults to a high state.

**SDA2 (L4):** Serial I<sup>2</sup>C Data Pin, Referenced to  $V_{CC2}$  and GND2. Bidirectional logic pin connected to logic side SDA pin through isolation barrier. Output is biased high by a 1.8mA current source. Do not connect an external pull-up device to SDA2. Under the condition of an isolation communication failure this output defaults to a high state.

**O1 (L5):** Digital Output, Referenced to  $V_{CC2}$  and GND2. Logic output connected to DI1 through isolation barrier. Under the condition of an isolation communication failure O1 defaults to a high state.

**$V_{CC2}$  (L6):** 3V to 5.5V Adjustable Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to 5V with no external components. Internally bypassed with 2.2 $\mu$ F.

**$V^-$  (L7):** -5V Nominal Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to -5V with no external components. Internally bypassed with 2.2 $\mu$ F.

**$V^+$  (L8):** 5V Nominal Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to 5V with no external components. Internally bypassed with 2.2 $\mu$ F.

**I1 (K1):** Digital Input, Referenced to  $V_{CC2}$  and GND2. Logic input connected to DO1 through isolation barrier. The logic state on I1 translates to the same logic state on DO1. Do not float.

**GND2 (K2 to K5, K7, K8):** Isolated Ground.

**$AV_{CC2}$  (K6):** 5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is 1.22V referenced to GND2. See Applications Information section for details.

## PIN FUNCTIONS (LTM2886-S)

### Logic Side

**SDO (A1):** Serial SPI Digital Output, Referenced to  $V_L$  and GND. Logic output connected to isolated side SDO2 pin through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

**DO2 (A2):** Digital Output, Referenced to  $V_L$  and GND. Logic output connected to I2 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

**SCK (A3):** Serial SPI Clock Input, Referenced to  $V_L$  and GND. Logic input connected to isolated side SCK2 pin through isolation barrier. Do not float.

**SDI (A4):** Serial SPI Data Input, Referenced to  $V_L$  and GND. Logic input connected to isolated side SDI2 pin through isolation barrier. Do not float.

**$\overline{CS}$  (A5):** Serial SPI Chip Select, Referenced to  $V_L$  and GND. Logic input connected to isolated side  $\overline{CS2}$  pin through isolation barrier. Do not float.

**$\overline{SDOE}$  (A6):** Serial SPI Data Output Enable, Referenced to  $V_L$  and GND. A logic high on  $\overline{SDOE}$  places the logic side SDO pin in a high impedance state, a logic low enables the output. Do not float.

**ON (A7):** Enable, Referenced to  $V_L$  and GND. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset, all digital outputs are in a high impedance state, and the isolated side is unpowered. Do not float.

**$V_L$  (A8):** Logic Supply. Interface supply voltage for pins SDI, SCK, SDO,  $\overline{SDOE}$ , DO1, DO2,  $\overline{CS}$ , and ON. Operating voltage is 1.62V to 5.5V. Internally bypassed with 1 $\mu$ F.

**DO1 (B1):** Digital Output, Referenced to  $V_L$  and GND. Logic output connected to I1 through isolation barrier. Under the condition of an isolation communication failure this output is in a high impedance state.

**GND (B2 to B6):** Circuit Ground.

**$V_{CC}$  (B7 to B8):** Supply Voltage. Operating voltage is 3V to 3.6V for LTM2886-3 and 4.5V to 5.5V for LTM2886-5. Internally bypassed with 2.2 $\mu$ F.

### Isolated Side

**SDO2 (L1):** Serial SPI Digital Input, Referenced to  $V_{CC2}$  and GND2. Logic input connected to logic side SDO pin through isolation barrier. Do not float.

**I2 (L2):** Digital Input, Referenced to  $V_{CC2}$  and GND2. Logic input connected to DO2 through isolation barrier. The logic state on I2 translates to the same logic state on DO2. Do not float.

**SCK2 (L3):** Serial SPI Clock Output, Referenced to  $V_{CC2}$  and GND2. Logic output connected to logic side SCK pin through isolation barrier. Under the condition of an isolation communication failure this output defaults to a low state.

**SDI2 (L4):** Serial SPI Data Output, Referenced to  $V_{CC2}$  and GND2. Logic output connected to logic side SDI pin through isolation barrier. Under the condition of an isolation communication failure this output defaults to a low state.

**$\overline{CS2}$  (L5):** Serial SPI Chip Select, Referenced to  $V_{CC2}$  and GND2. Logic output connected to logic side  $\overline{CS}$  pin through isolation barrier. Under the condition of an isolation communication failure this output defaults to a high state.

**$V_{CC2}$  (L6):** 3V to 5.5V Adjustable Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to 5V with no external components. Internally bypassed with 2.2 $\mu$ F.

**$V^-$  (L7):** -5V Nominal Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to -5V with no external components. Internally bypassed with 2.2 $\mu$ F.

**$V^+$  (L8):** 5V Nominal Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to 5V with no external components. Internally bypassed with 2.2 $\mu$ F.

**I1 (K1):** Digital Input, Referenced to  $V_{CC2}$  and GND2. Logic input connected to DO1 through isolation barrier. The logic state on I1 translates to the same logic state on DO1. Do not float.

**GND2 (K2 to K5, K7, K8):** Isolated Ground.

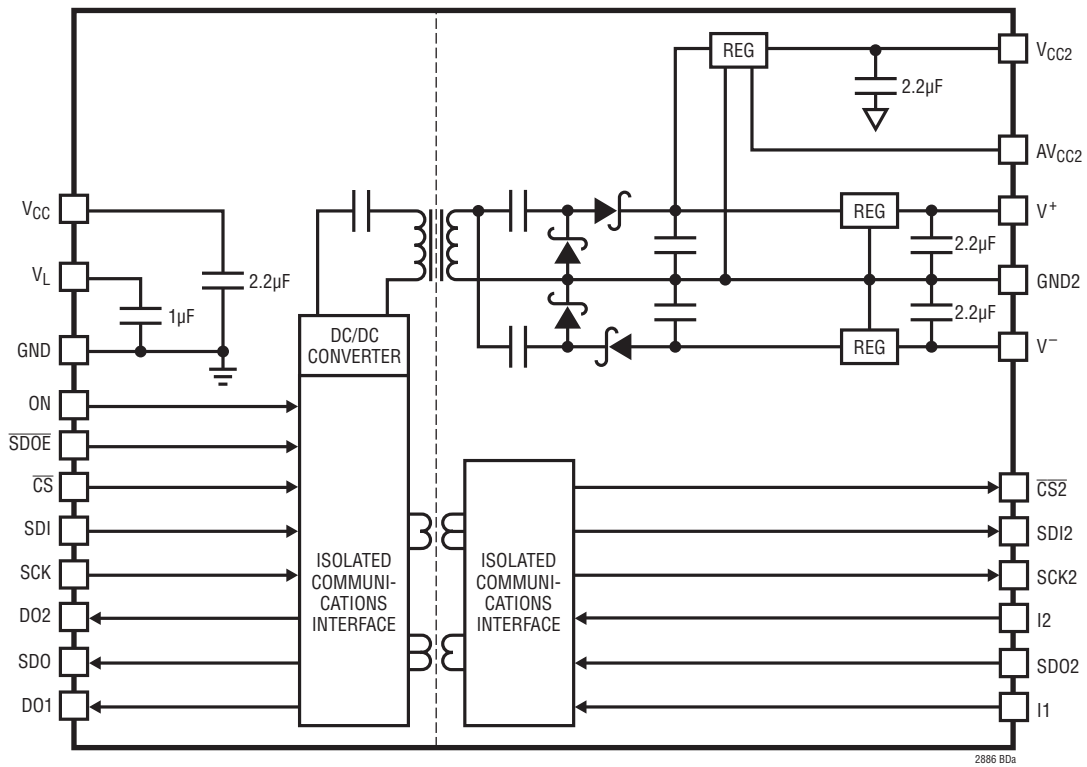
**$AV_{CC2}$  (K6):** 5V Nominal Isolated Supply Voltage Adjust. The adjust pin voltage is 1.22V Referenced to GND2. See Applications Information section for details.

**BLOCK DIAGRAMS**

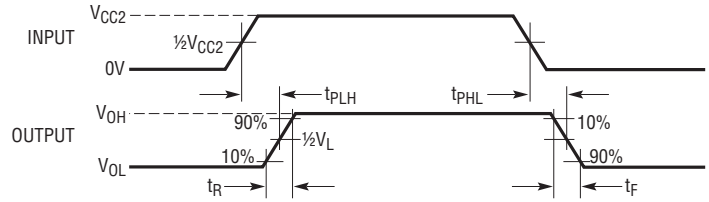
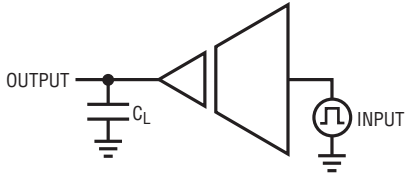
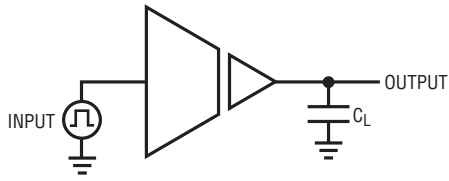
(LTM2886-1)



(LTM2886-S)

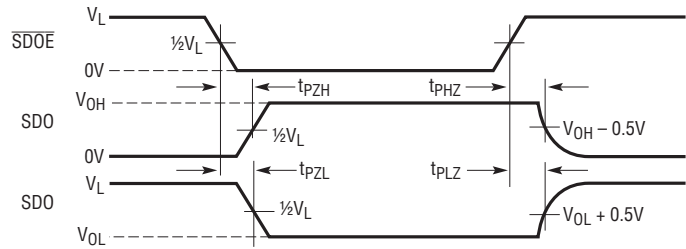
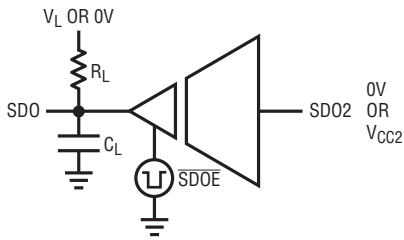


TEST CIRCUITS



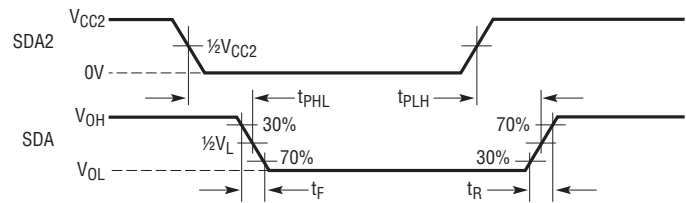
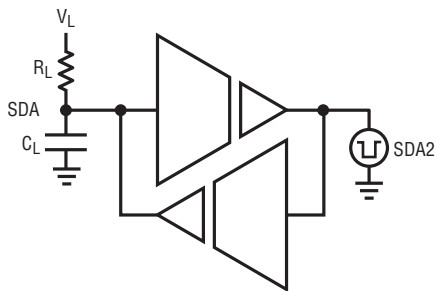
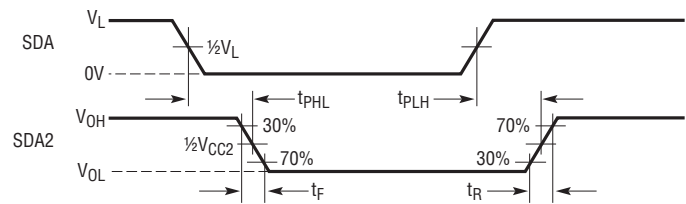
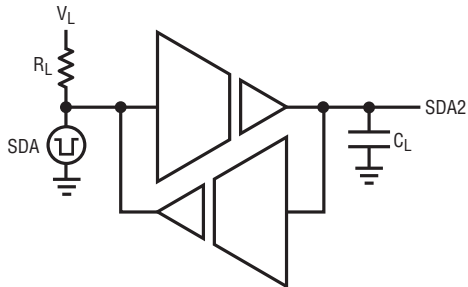
2886 F01

Figure 1. Logic Timing Measurements



2886 F02

Figure 2. Logic Enable/Disable Time



2886 F03

Figure 3. I<sup>2</sup>C Timing Measurements



## APPLICATIONS INFORMATION

### Overview

The LTM2886 digital  $\mu$ Module isolator provides a galvanically-isolated robust logic interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. The LTM2886 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2886 blocks high voltage differences, eliminates ground loops and is extremely tolerant of common mode transients between ground planes. Error-free operation is maintained through common mode events greater than  $30\text{kV}/\mu\text{s}$  providing excellent noise isolation.

### Isolator $\mu$ Module Technology

The LTM2886 utilizes isolator  $\mu$ Module technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the  $\mu$ Module substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The  $\mu$ Module technology provides the means to combine the isolated signaling with multiple regulators and a powerful isolated DC/DC converter in one small package.

### DC/DC Converter

The LTM2886 contains a fully integrated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running at 1.6MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a voltage quadrupler. This topology eliminates transformer saturation caused by secondary imbalances.

The quadrupler is grounded in the middle producing symmetrical positive and negative voltage rails. The positive rail is post regulated with two low dropout regulators (LDOs) producing  $V_{CC2}$  and  $V^+$ , the negative rail also has an LDO producing  $V^-$ .

Each voltage rail is capable of producing 100mA of output current, total output power capability is approximately 1W. All voltage rails are bypassed with  $2.2\mu\text{F}$  ceramic capacitors.

### $V_L$ Logic Supply

A separate logic supply pin  $V_L$  allows the LTM2886 to interface with any logic signal from 1.62V to 5.5V as shown in Figure 4. Simply connect the desired logic supply to  $V_L$ .

There is no interdependency between  $V_{CC}$  and  $V_L$ ; they may simultaneously operate at any voltage within their specified operating ranges and sequence in any order.  $V_L$  is bypassed internally by a  $1\mu\text{F}$  capacitor.

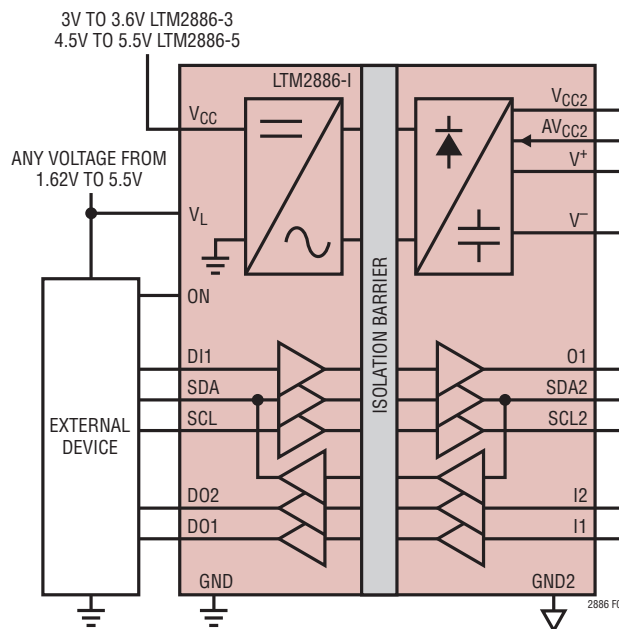


Figure 4.  $V_{CC}$  and  $V_L$  Are Independent

### Hot-Plugging Safely

Caution must be exercised in applications where power is plugged into the LTM2886's power supplies,  $V_{CC}$  or  $V_L$ , due to the integrated ceramic decoupling capacitors. The parasitic cable inductance along with the high Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTM2886. Refer to Linear Technology Application Note 88, entitled Ceramic Input Capacitors Can Cause Overvoltage Transients for a detailed discussion and mitigation of this phenomenon.

## APPLICATIONS INFORMATION

### Isolated Supply Adjustable Operation

The  $V_{CC2}$  isolated power rail is nominally 5V, but may be overdriven by adding two external resistors. The unadjusted output voltage represents the maximum for guaranteed performance. Figure 5 illustrates configuration for  $V_{CC2} = 3.3V$ ,  $V^+$  and  $V^-$  are fixed at 5V and  $-5V$  respectively.

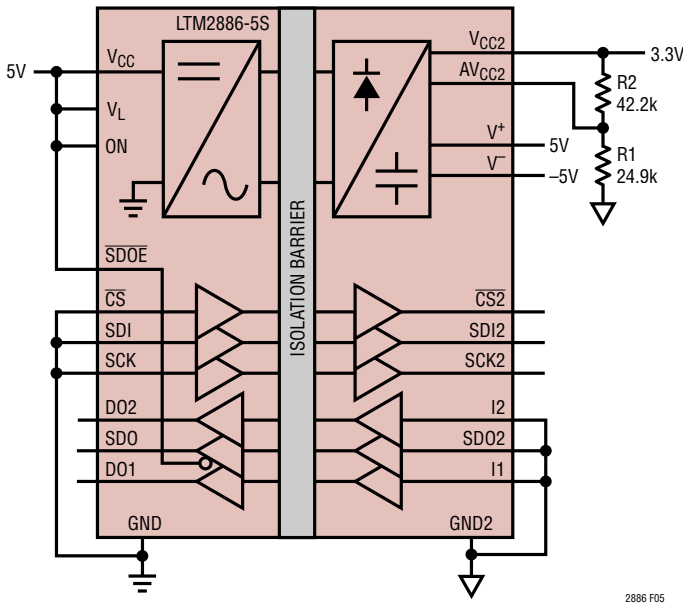


Figure 5. Adjustable Voltage Rails

The output adjustment range for  $V_{CC2}$  is 3V to 5.5V.  $V_{CC2}$  output voltage is calculated by:

$$V_{CC2} = 1.22V(1 + R2/R1)$$

The value of R1 should be no greater than 24.9k to minimize errors in the output voltage caused by the  $AV_{CC2}$  pin bias current.

Operation at low output voltages may result in thermal shutdown due to low dropout regulator power dissipation.

### Channel Timing Uncertainty

Multiple channels are supported across the isolation boundary by encoding and decoding of the inputs and outputs. Up to three signals in each direction are assembled as a packet and transferred across the isolation barrier. The time required to transfer all 3 bits is 100ns maximum, and sets the limit for how often a signal can change on the opposite side of the barrier. Encoding transmission is independent for each data direction. The technique used assigns SCK or SCL on the logic side, and SDO2 or I2 on the isolated side, the highest priority such that there is no jitter on the associated output channels, only delay. This preemptive scheme will produce a certain amount of uncertainty on the other isolation channels. The resulting pulse width uncertainty on these low priority channels is typically  $\pm 6ns$ , but may vary up to  $\pm 50ns$  if the low priority channels are not encoded within the same high priority serial packet.

### Serial Peripheral Interface (SPI) Bus

The LTM2886-S provides a SPI compatible isolated interface. The maximum data rate is a function of the inherent channel propagation delays, channel to channel pulse width uncertainty, and data direction requirements. Channel timing is detailed in Figures 6 through 9 and Tables 2 and 3. The SPI protocol supports four unique timing configurations defined by the clock polarity (CPOL) and clock phase (CPHA) summarized in Table 1.

Table 1. SPI Mode

CPOL	CPHA	DATA TO (CLOCK) RELATIONSHIP	
0	0	Sample (Rising)	Set-Up (Falling)
0	1	Set-Up (Rising)	Sample (Falling)
1	0	Sample (Falling)	Set-Up (Rising)
1	1	Set-Up (Falling)	Sample (Rising)

The maximum data rate for bidirectional communication is 4MHz, based on a synchronous system, as detailed in the timing waveforms. Slightly higher data rates may be achieved by skewing the clock duty cycle and minimizing the SDO to SCK set-up time, however the clock rate is still dominated by the system propagation delays. A discussion of the critical timing paths relative to Figures 6 and 7 follows.

## APPLICATIONS INFORMATION

- $\overline{CS}$  to SCK (master sample SDO, 1st SDO valid)
  - $t_0 \rightarrow t_1$   $\approx 50\text{ns}$ ,  $\overline{CS}$  to  $\overline{CS2}$  propagation delay
  - $t_1 \rightarrow t_{1+}$  Isolated slave device propagation (response time), asserts SDO2
  - $t_1 \rightarrow t_3$   $\approx 50\text{ns}$ , SDO2 to SDO propagation delay
  - $t_3 \rightarrow t_5$  Set-up time for master SDO to SCK
- SDI to SCK (master data write to slave)
  - $t_2 \rightarrow t_4$   $\approx 50\text{ns}$ , SDI to SDI2 propagation delay
  - $t_5 \rightarrow t_6$   $\approx 50\text{ns}$ , SCK to SCK2 propagation delay
  - $t_2 \rightarrow t_5$   $\geq 50\text{ns}$ , SDI to SCK, separate packet non-zero set-up time
  - $t_4 \rightarrow t_6$   $\geq 50\text{ns}$ , SDI2 to SCK2, separate packet non-zero set-up time
- SDO to SCK (master sample SDO, subsequent SDO valid)
  - $t_8$  set-up data transition SDI and SCK
  - $t_8 \rightarrow t_{10}$   $\approx 50\text{ns}$ , SDI to SDI2 and SCK to SCK2 propagation delay

- $t_{10}$  SDO2 data transition in response to SCK2
- $t_{10} \rightarrow t_{11}$   $\approx 50\text{ns}$ , SDO2 to SDO propagation delay
- $t_{11} \rightarrow t_{12}$  Set-up time for master SDO to SCK

Maximum data rate for single direction communication, master to slave, is 8MHz, limited by the systems encoding/decoding scheme or propagation delay. Timing details for both variations of clock phase are shown in Figures 8 and 9 and Table 3.

Additional requirements to insure maximum data rate are:

- $\overline{CS}$  is transmitted prior to (asynchronous) or within the same (synchronous) data packet as SDI
- SDI and SCK set-up data transition occur within the same data packet. Referencing Figure 6, SDI can precede SCK by up to 13ns ( $t_7 \rightarrow t_8$ ) or lag SCK by 3ns ( $t_8 \rightarrow t_9$ ) and not violate this requirement. Similarly in Figure 8, SDI can precede SCK by up to 13ns ( $t_4 \rightarrow t_5$ ) or lag SCK by 3ns ( $t_5 \rightarrow t_6$ ).

APPLICATIONS INFORMATION

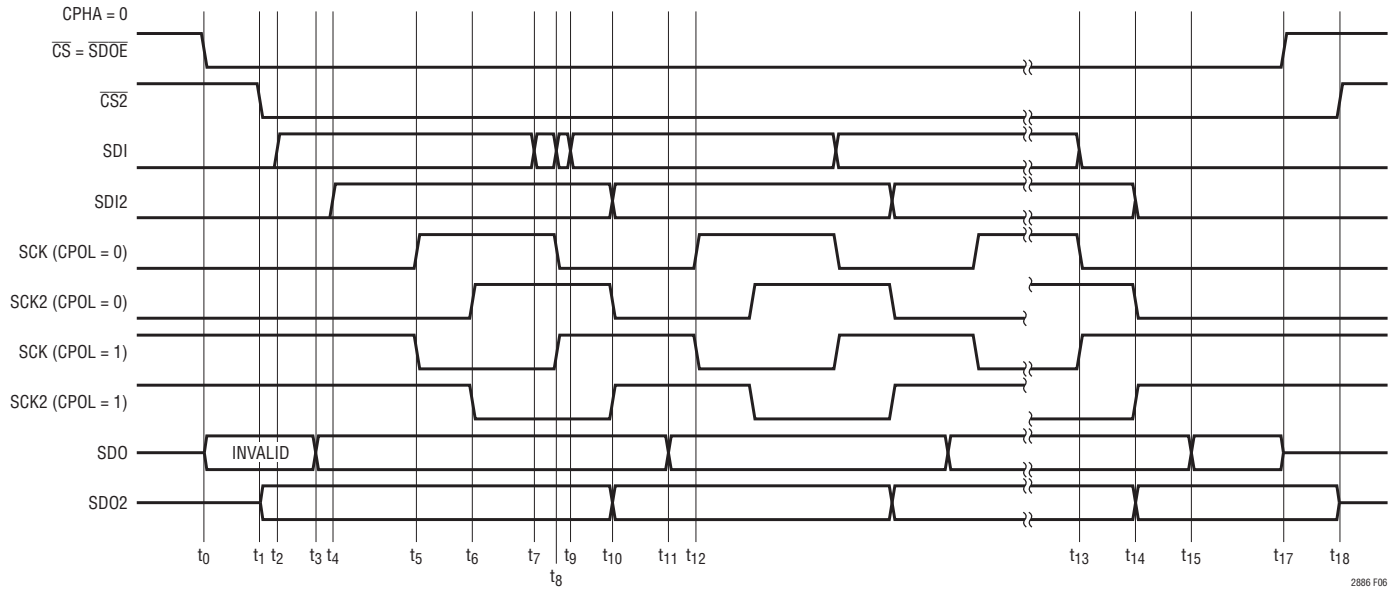


Figure 6. SPI Timing, Bidirectional, CPHA = 0

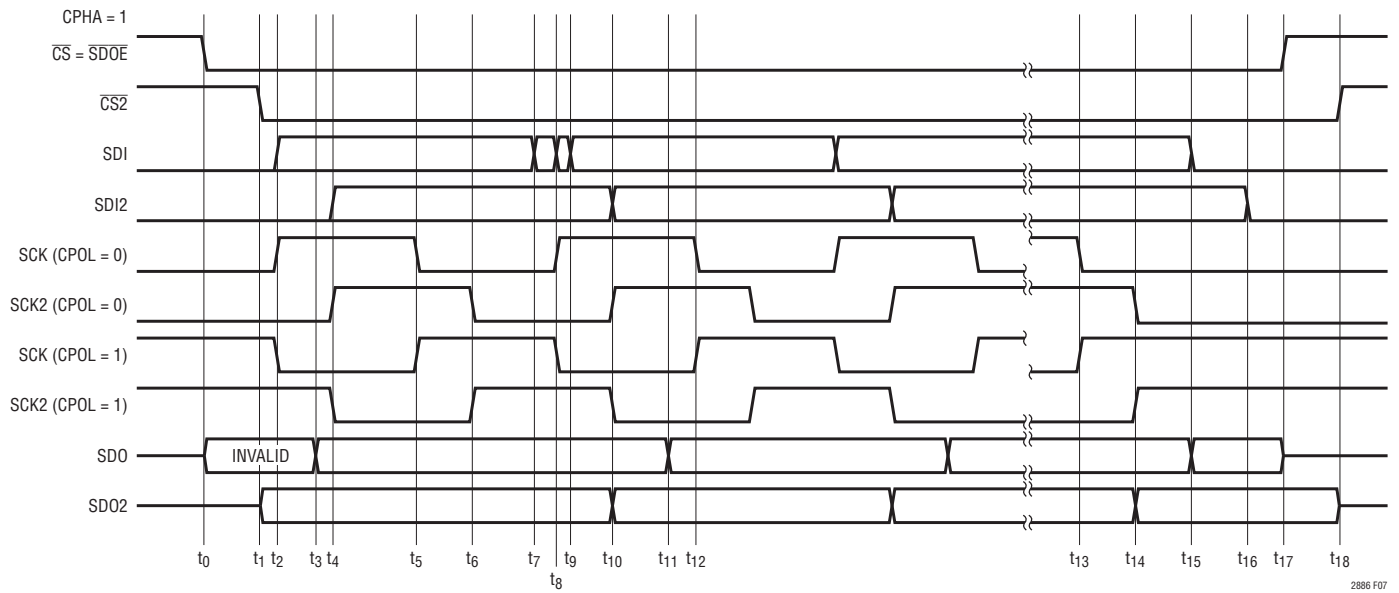


Figure 7. SPI Timing, Bidirectional, CPHA = 1

# APPLICATIONS INFORMATION

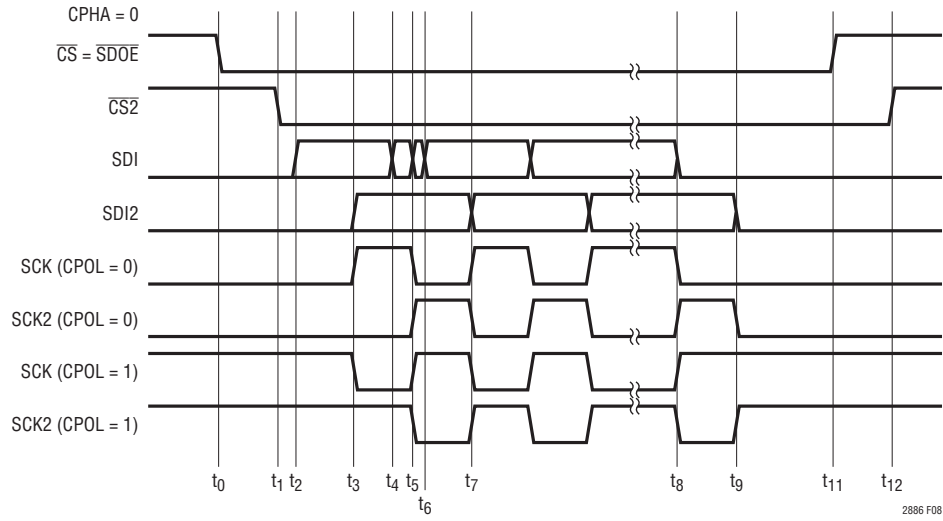


Figure 8. SPI Timing, Unidirectional, CPHA = 0

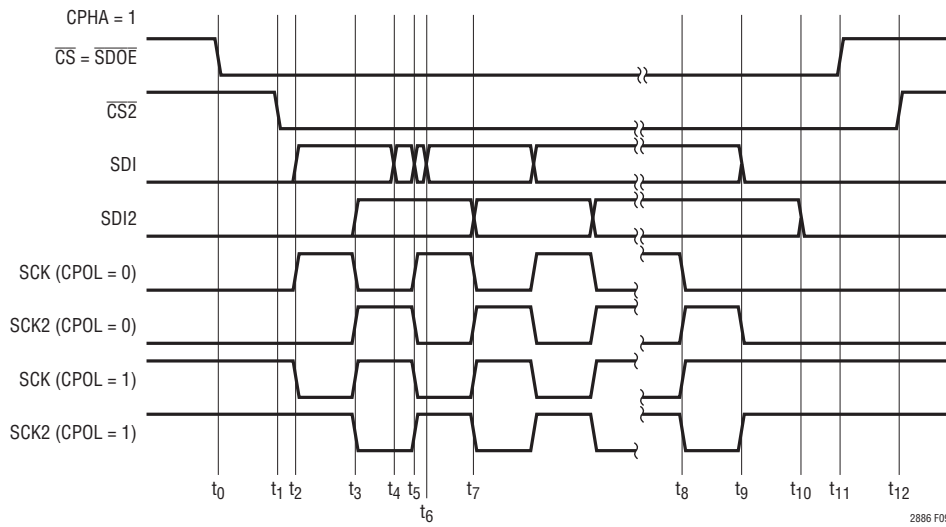


Figure 9. SPI Timing, Unidirectional, CPHA = 1

## APPLICATIONS INFORMATION

**Table 2. Bidirectional SPI Timing Event Description**

TIME	CPHA	EVENT DESCRIPTION
$t_0$	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns. Logic side slave data output enabled, initial data is not equivalent to slave device data output
$t_0$ to $t_1$ , $t_{17}$ to $t_{18}$	0, 1	Propagation delay chip select, logic to isolated side, 50ns typical
$t_1$	0, 1	Slave device chip select output data enable
$t_2$	0	Start of data transmission, data set-up
	1	Start of transmission, data and clock set-up. Data transition must be within -13ns to 3ns of clock edge
$t_1$ to $t_3$	0, 1	Propagation delay of slave data, isolated to logic side, 50ns typical
$t_3$	0, 1	Slave data output valid, logic side
$t_2$ to $t_4$	0	Propagation delay of data, logic side to isolated side
	1	Propagation delay of data and clock, logic side to isolated side
$t_5$	0, 1	Logic side data sample time, half clock period delay from data set-up transition
$t_5$ to $t_6$	0, 1	Propagation delay of clock, logic to isolated side
$t_6$	0, 1	Isolated side data sample time
$t_8$	0, 1	Synchronous data and clock transition, logic side
$t_7$ to $t_8$	0, 1	Data to clock delay, must be $\leq 13$ ns
$t_8$ to $t_9$	0, 1	Clock to data delay, must be $\leq 3$ ns
$t_8$ to $t_{10}$	0, 1	Propagation delay clock and data, logic to isolated side
$t_{10}$ , $t_{14}$	0, 1	Slave device data transition
$t_{10}$ to $t_{11}$ , $t_{14}$ to $t_{15}$	0, 1	Propagation delay slave data, isolated to logic side
$t_{11}$ to $t_{12}$	0, 1	Slave data output to sample clock set-up time
$t_{13}$	0	Last data and clock transition logic side
	1	Last sample clock transition logic side
$t_{13}$ to $t_{14}$	0	Propagation delay data and clock, logic to isolated side
	1	Propagation delay clock, logic to isolated side
$t_{15}$	0	Last slave data output transition logic side
	1	Last slave data output and data transition, logic side
$t_{15}$ to $t_{16}$	1	Propagation delay data, logic to isolated side
$t_{17}$	0, 1	Asynchronous chip select transition, end of transmission. Disable slave data output logic side
$t_{18}$	0, 1	Chip select transition isolated side, slave data output disabled

### Inter-IC Communication (I<sup>2</sup>C) Bus

The LTM2886-I provides an I<sup>2</sup>C compatible isolated interface. Clock (SCL) is unidirectional, supporting master mode only, and data (SDA) is bidirectional. The maximum data rate is 400kHz which supports fast-mode I<sup>2</sup>C. Timing is detailed in Figure 10. The data rate is limited by the slave acknowledge setup time ( $t_{SU;ACK}$ ), consisting of the I<sup>2</sup>C standard minimum setup time ( $t_{SU;DAT}$ ) of 100ns, maximum clock propagation delay of 225ns, glitch filter and isolated data delay of 500ns maximum, and the combined isolated and logic data fall time of 300ns at maximum bus loading.

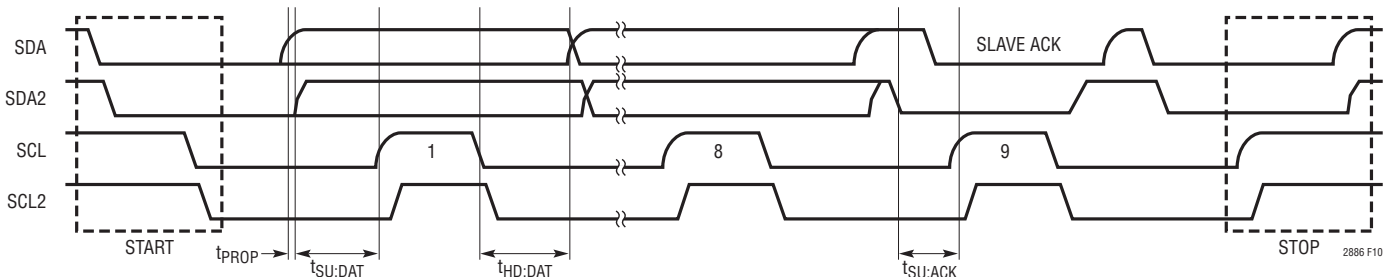
The total setup time reduces the I<sup>2</sup>C data hold time ( $t_{HD;DAT}$ ) to a maximum of 175ns, guaranteeing sufficient data setup time ( $t_{SU;ACK}$ ).

The isolated side bidirectional serial data pin, SDA2, simplified schematic is shown in Figure 11. An internal 1.8mA current source provides a pull-up for SDA2. Do not connect any other pull-up device to SDA2. This current source is sufficient to satisfy the system requirements for bus capacitances greater than 200pF in FAST mode and greater than 400pF in STANDARD mode.

## APPLICATIONS INFORMATION

**Table 3. Unidirectional SPI Timing Event Description**

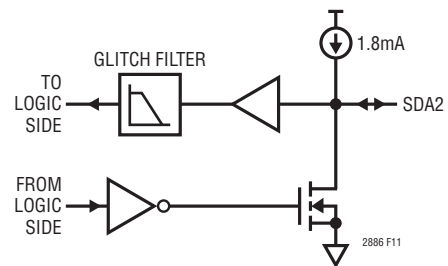
TIME	CPHA	EVENT DESCRIPTION
$t_0$	0, 1	Asynchronous chip select, may be synchronous to SDI but may not lag by more than 3ns
$t_0$ to $t_1$	0, 1	Propagation delay chip select, logic to isolated side
$t_2$	0	Start of data transmission, data set-up
	1	Start of transmission, data and clock set-up. Data transition must be within $-13\text{ns}$ to $3\text{ns}$ of clock edge
$t_2$ to $t_3$	0	Propagation delay of data, logic side to isolated side
	1	Propagation delay of data and clock, logic side to isolated side
$t_3$	0, 1	Logic side data sample time, half clock period delay from data set-up transition
$t_3$ to $t_5$	0, 1	Clock propagation delay, clock and data transition
$t_4$ to $t_5$	0, 1	Data to clock delay, must be $\leq 13\text{ns}$
$t_5$ to $t_6$	0, 1	Clock to data delay, must be $\leq 3\text{ns}$
$t_5$ to $t_7$	0, 1	Data and clock propagation delay
$t_8$	0	Last clock and data transition
	1	Last clock transition
$t_8$ to $t_9$	0	Clock and data propagation delay
	1	Clock propagation delay
$t_9$ to $t_{10}$	1	Data propagation delay
$t_{11}$	0, 1	Asynchronous chip select transition, end of transmission
$t_{12}$	0, 1	Chip select transition isolated side



**Figure 10. I<sup>2</sup>C Timing Diagram**

Additional proprietary circuitry monitors the slew rate on the SDA and SDA2 signals to manage directional control across the isolation barrier. Slew rates on both pins must be greater than  $1\text{V}/\mu\text{s}$  for proper operation.

The logic side bidirectional serial data pin, SDA, requires a pull-up resistor or current source connected to  $V_L$ . Follow the requirements in Figures 12 and 13 for the appropriate pull-up resistor on SDA that satisfies the desired rise time specifications and  $V_{OL}$  maximum limits for FAST and STANDARD modes. The resistance curves represent the maximum resistance boundary; any value may be used to the left of the appropriate curve.



**Figure 11. Isolated SDA2 Pin Schematic**

APPLICATIONS INFORMATION



Figure 12. Maximum Standard Speed Pull-Up Resistance on SDA



Figure 13. Maximum Fast Speed Pull-Up Resistance on SDA

The isolated side clock pin, SCL2, has a weak push-pull output driver; do not connect an external pull-up device. SCL2 is compatible with I<sup>2</sup>C devices without clock stretching. On lightly loaded connections, a 100pF capacitor from SCL2 to GND2 or RC lowpass filter (R = 500Ω, C = 100pF) can be used to increase the rise and fall times and minimize noise.

Some consideration must be given to signal coupling between SCL2 and SDA2. Separate these signals on a printed circuit board or route with ground between.

If these signals are wired off board, twist SCL2 with V<sub>CC2</sub> and/or GND2 and SDA2 with GND2 and/or V<sub>CC2</sub>, do not twist SCL2 and SDA2 together. If coupling between SCL2 and SDA2 is unavoidable, place the aforementioned RC filter at the SCL2 pin to reduce noise injection onto SDA2.

Low Noise Applications

For precision analog applications the V<sup>+</sup> and V<sup>-</sup> power rails may be filtered to improve the noise performance. Figure 14 shows the recommended component values to reduce noise at high frequencies. The selected inductor should be chosen such that the parasitic capacitance is low enough to keep the self resonant frequency greater than 10MHz. The plots of Figures 15 and 16 show the high frequency noise improvement for the V<sup>+</sup> rail, the improvement on the V<sup>-</sup> rail will be nearly equivalent.

Some applications may require the noise performance be improved in the 100Hz to 10kHz region. An additional LC filter stage may be added between the LTM2886 and the high frequency filter to lower the noise corner frequency. Using an inductance of 330μH and capacitance of 680μF reduces the noise corner to approximately 340Hz. The RMS noise at a bandwidth of 340Hz is approximately 22μV.



Figure 14. Filtered Voltage Rails for Low Noise Applications



## APPLICATIONS INFORMATION

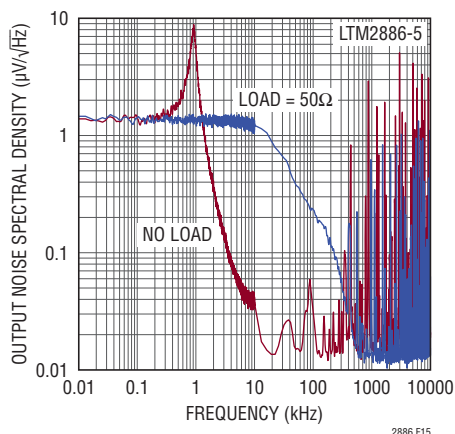


Figure 15.  $V^+$  Output Noise Spectral Density Without Filter

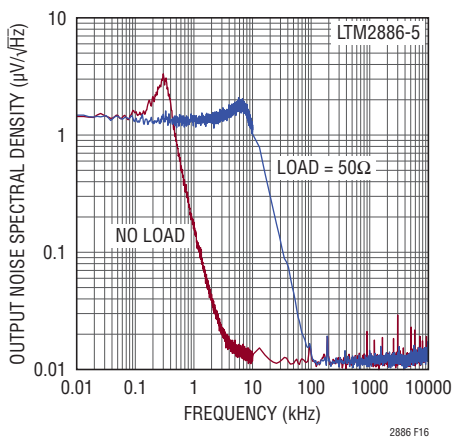


Figure 16.  $V^+$  Output Noise Spectral Density With Filter

### RF, Magnetic Field Immunity

The isolator  $\mu$ Module technology used within the LTM2886 has been independently evaluated, and successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3	Radiated, Radio-Frequency, Electromagnetic Field Immunity
EN 61000-4-8	Power Frequency Magnetic Field Immunity
EN 61000-4-9	Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 5.

Table 4. EMC Immunity Tests

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3 Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8 Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8 Level 5	60Hz	100A/m*
EN 61000-4-9 Level 5	Pulse	1000A/m

\*non IEC method

### PCB Layout

The high integration of the LTM2886 makes PCB layout very simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- Under heavily loaded conditions  $V_{CC}$  and GND current can exceed 300mA. Sufficient copper must be used on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level. Similarly, the  $V_{CC2}$  and GND2 conductors must be sized to support any external load current. These heavy copper traces will also help to reduce thermal stress and improve the thermal conductivity.
- Input and output supply decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8 $\mu$ F to 22 $\mu$ F is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1 $\mu$ F to 4.7 $\mu$ F, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace

2886fb

## APPLICATIONS INFORMATION

conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.

- For large ground planes a small capacitance ( $\leq 330\text{pF}$ ) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be four layers. Care must be exercised in applying either technique to ensure the voltage rating of the barrier is not compromised.
- In applications without an embedded PCB substrate capacitance a slot may be added between the logic side and isolated side device pins. The slot extends the creepage path between terminals on the PCB side, and may reduce leakage caused by PCB contamination. The slot should be placed in the middle of the device and extend beyond the package perimeter.

The PCB layout in Figures 17 and 18 shows the low EMI demo board for the LTM2886. The demo board uses a combination of EMI mitigation techniques, including both embedded PCB bridge capacitance and discrete GND to GND2 capacitors. Two safety rated type Y2 capacitors are used in series, manufactured by MuRata, part number GA342QR7GF471KW01L. The embedded capacitor effectively suppresses emissions above 400MHz, whereas the discrete capacitors are more effective below 400MHz.

EMI performance is shown in Figure 19, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides.

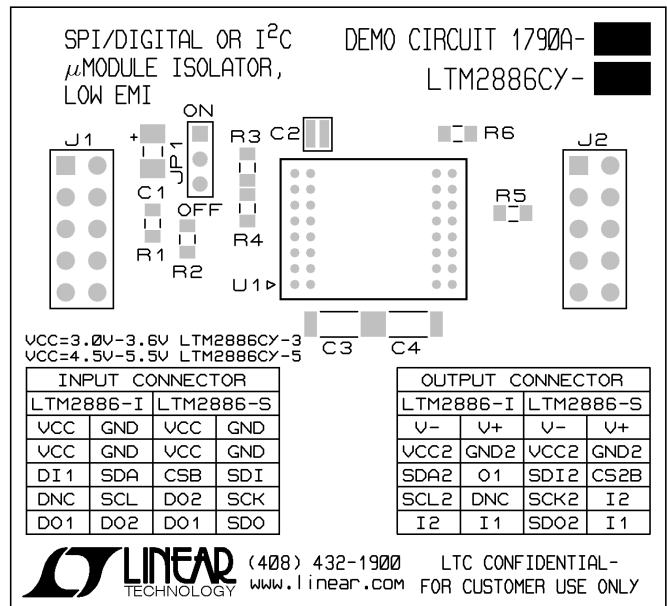
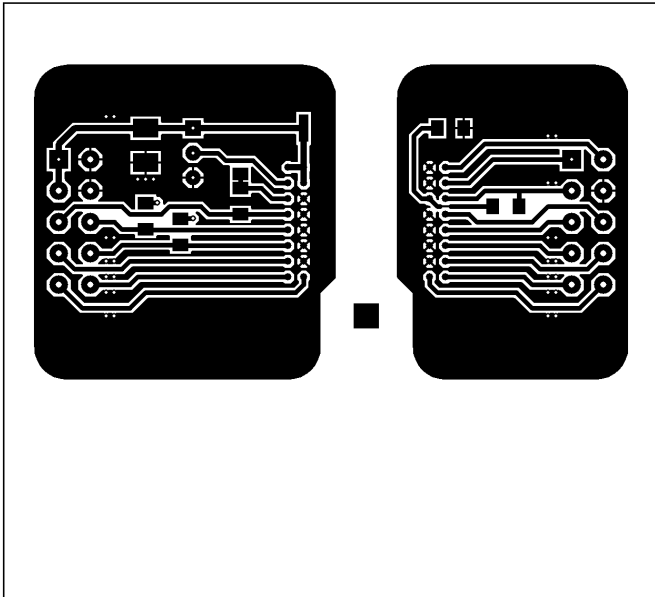


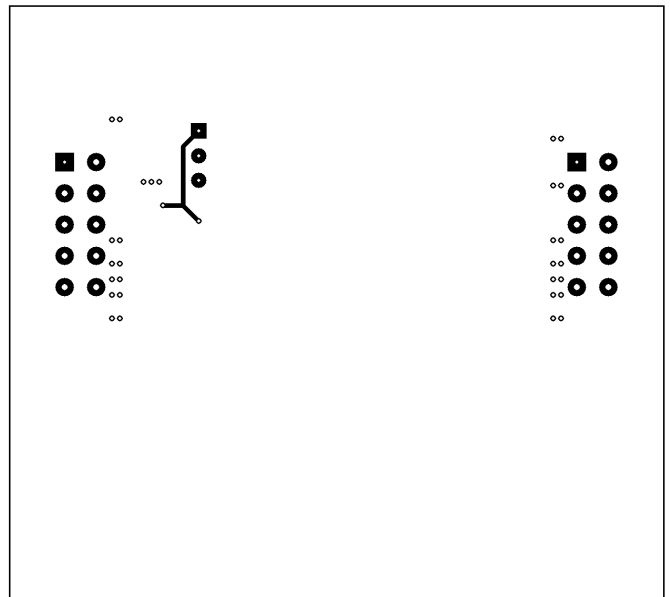
Figure 17. LTM2886 Low EMI Demo Board Layout

# APPLICATIONS INFORMATION

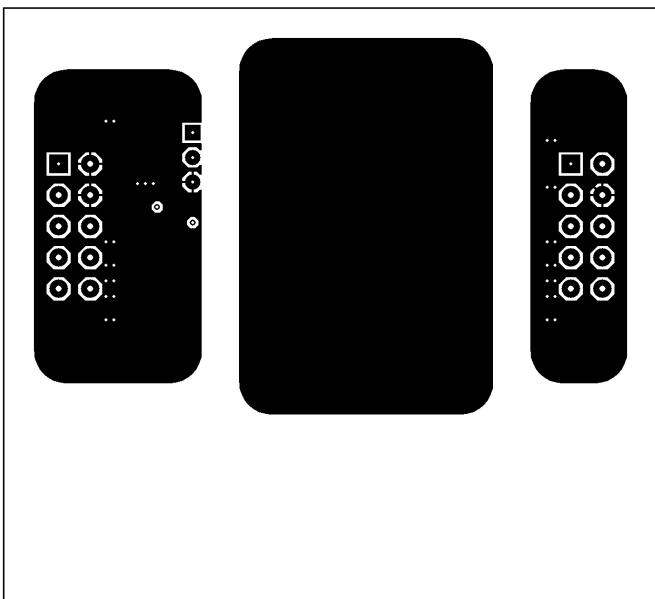
Top Layer



Inner Layer 2



Inner Layer 1



Bottom Layer

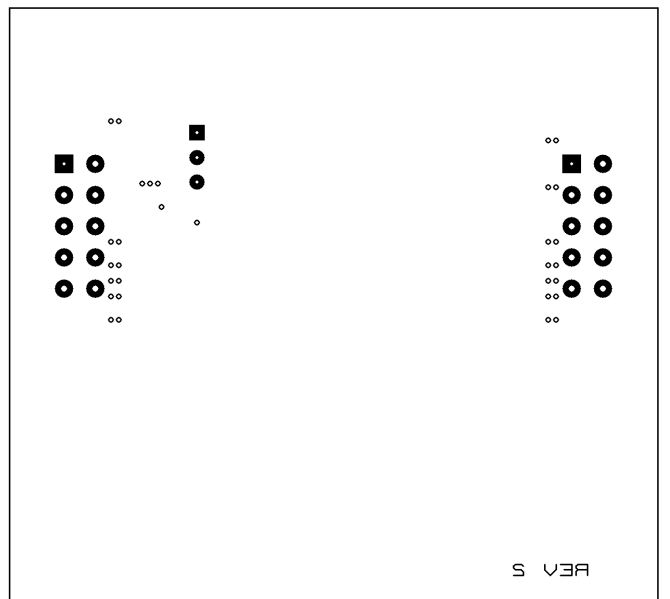


Figure 18. LTM2886 Low EMI Demo Board Layout (DC1790A)

## APPLICATIONS INFORMATION

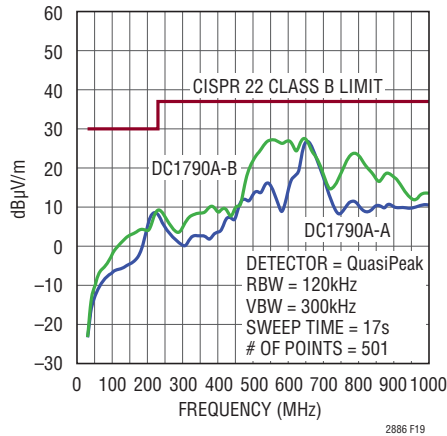


Figure 19. LTM2886 Low EMI Demo Board Emissions

## TYPICAL APPLICATIONS

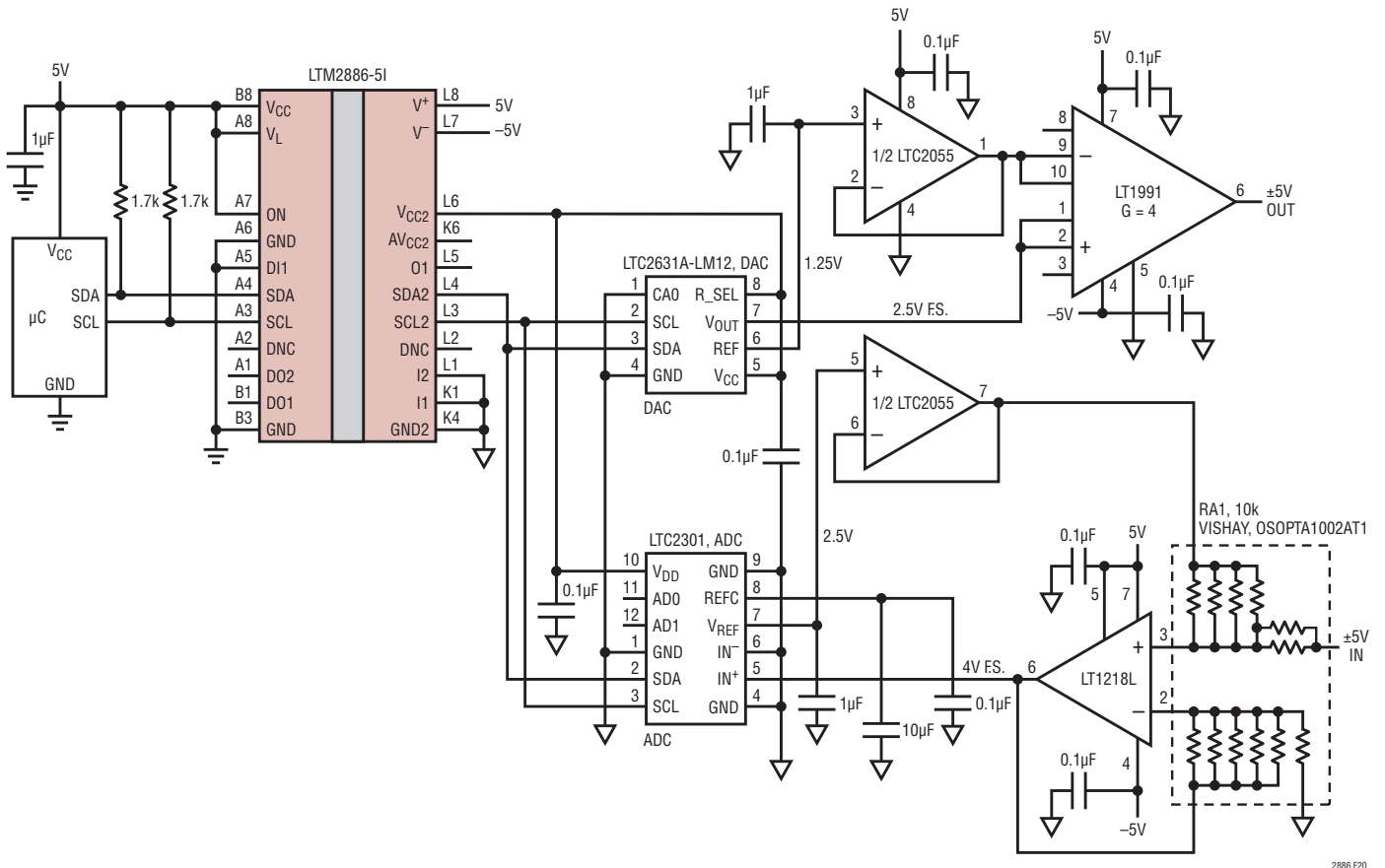


Figure 20. Isolated I<sup>2</sup>C 12-Bit, ±5V Analog Input and Output

# TYPICAL APPLICATIONS

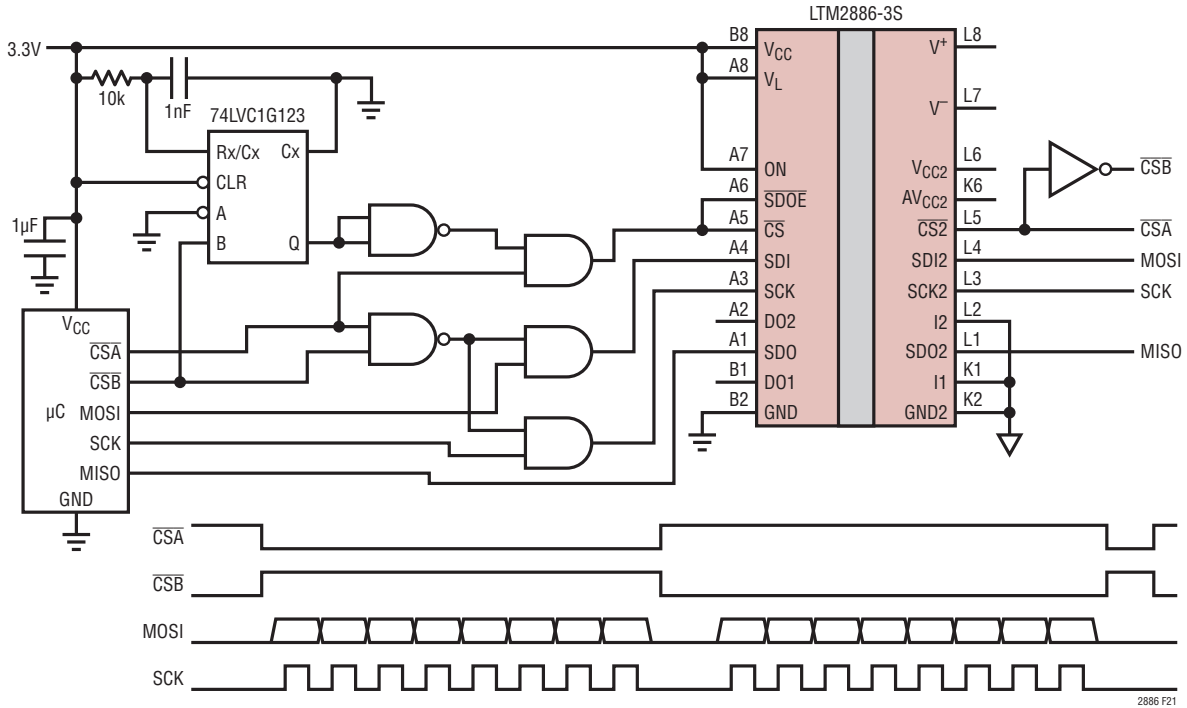


Figure 21. Isolated SPI Device Expansion

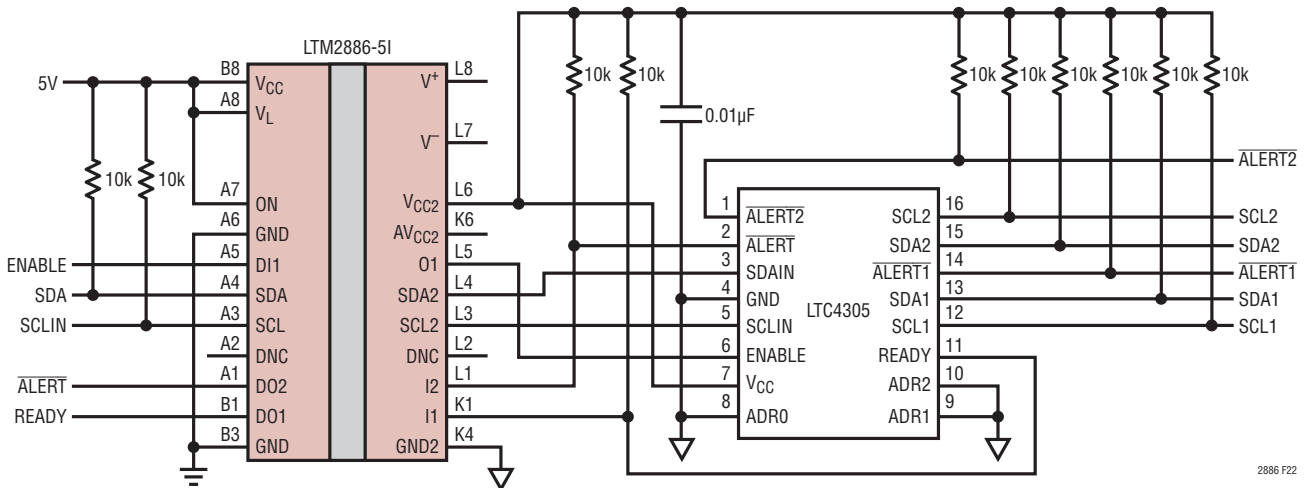


Figure 22. Isolated I<sup>2</sup>C Buffer with Dual Outputs

## TYPICAL APPLICATIONS



Figure 23. 16-Channel Isolated Temperature to Frequency Converter

TYPICAL APPLICATIONS

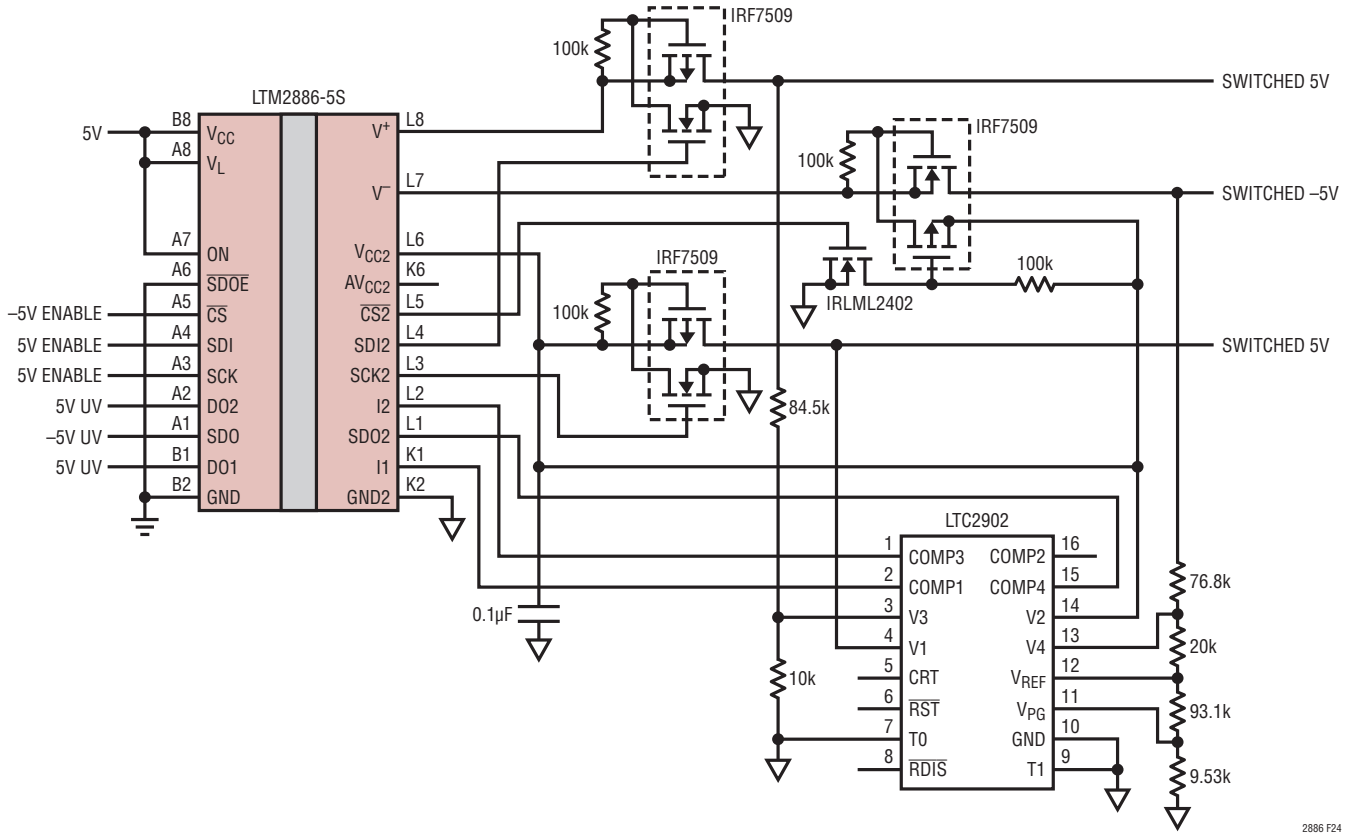


Figure 24. Digitally Switched Triple Power Supply with Undervoltage Monitor

2886 F24

## TYPICAL APPLICATIONS



Figure 25. Quad 16-Bit  $\pm 5V$  Output Range DAC

2886 F25



TYPICAL APPLICATIONS

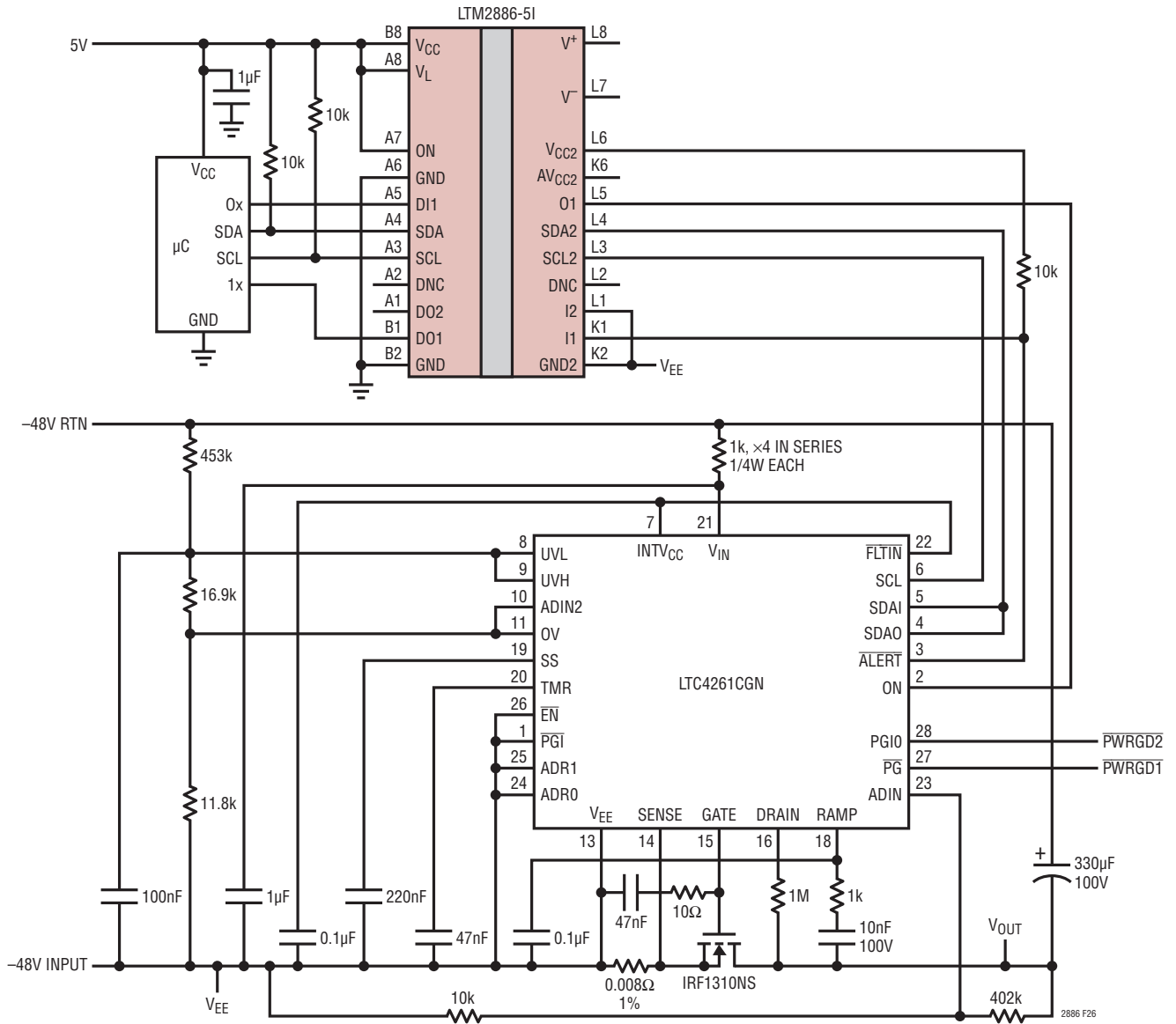


Figure 26. -48V, 200W Hot Swap Controller with Isolated I<sup>2</sup>C Interface

## TYPICAL APPLICATIONS

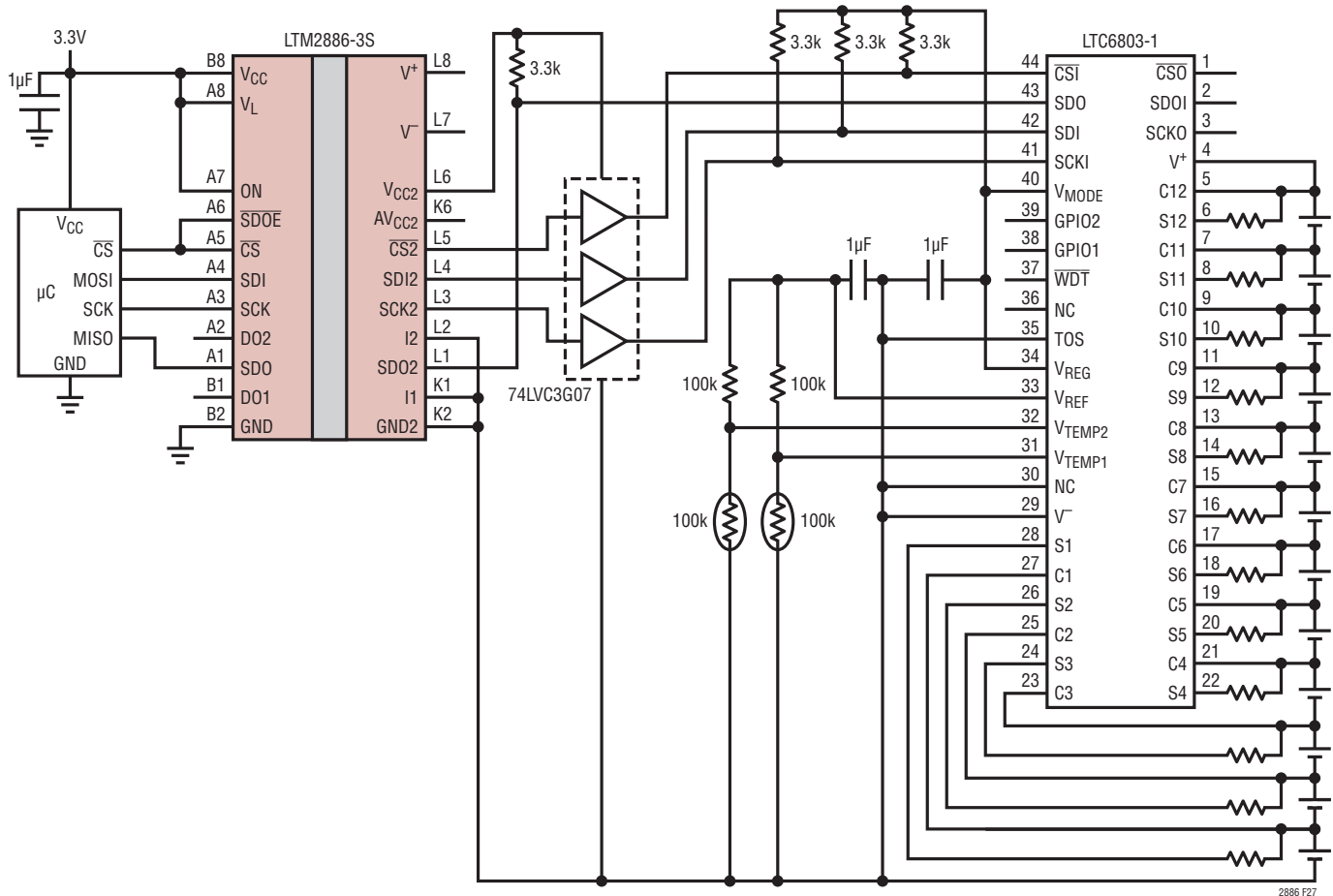
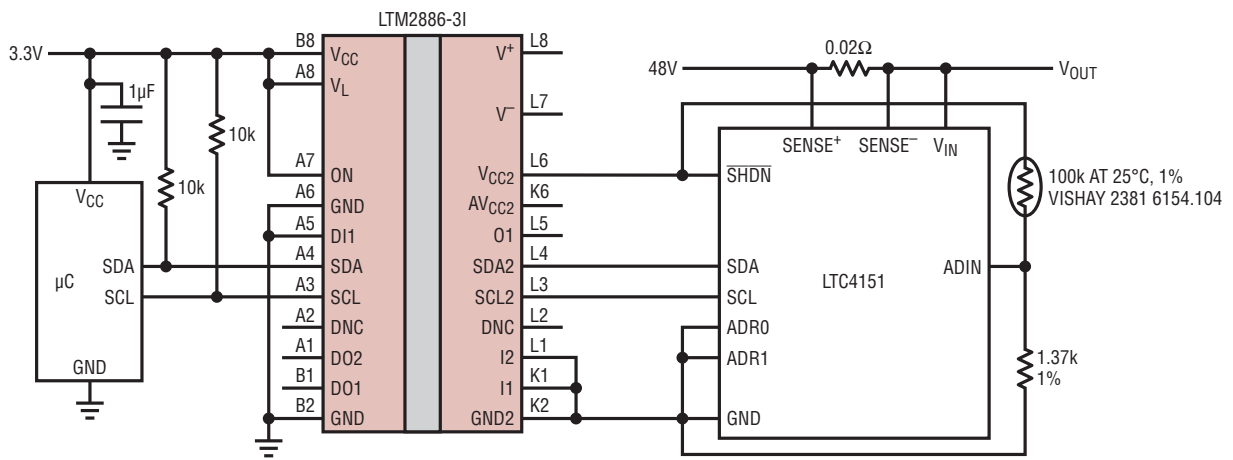


Figure 27. 12-Cell Battery Stack Monitor with Isolated SPI Interface and Low Power Shutdown



$$T(^{\circ}\text{C}) = \frac{3950}{8.965 + \text{LN}\left(\frac{1000}{N_{\text{ADIN}}} - 1\right)} - 273, -40^{\circ}\text{C} < T < 150^{\circ}\text{C}$$

$N_{\text{ADIN}}$  IS THE DIGITAL CODE MEASURED BY THE ADC AT THE ADIN PIN

Figure 28. Isolated I<sup>2</sup>C Voltage, Current and Temperature Power Supply Monitor

TYPICAL APPLICATIONS

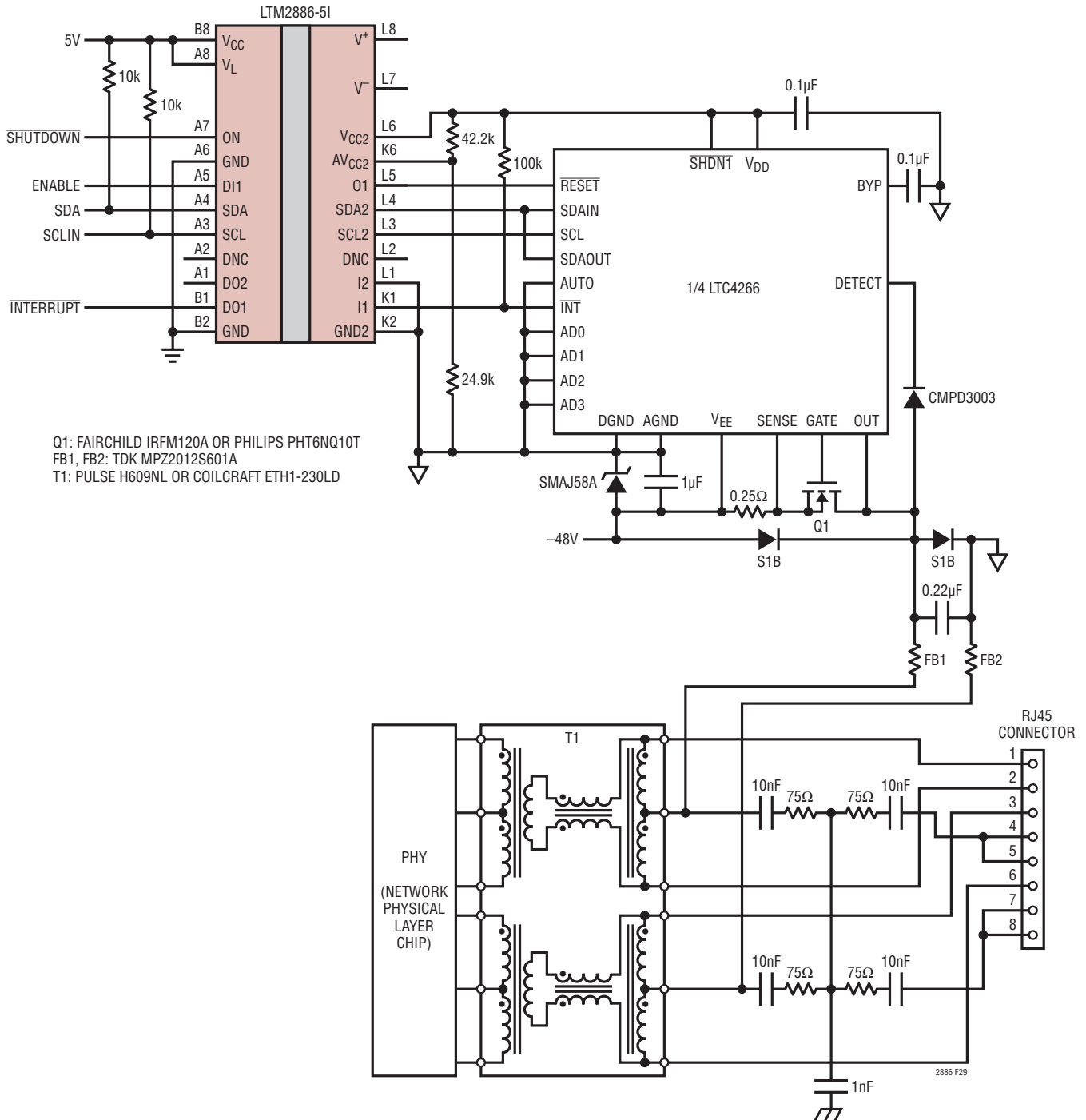
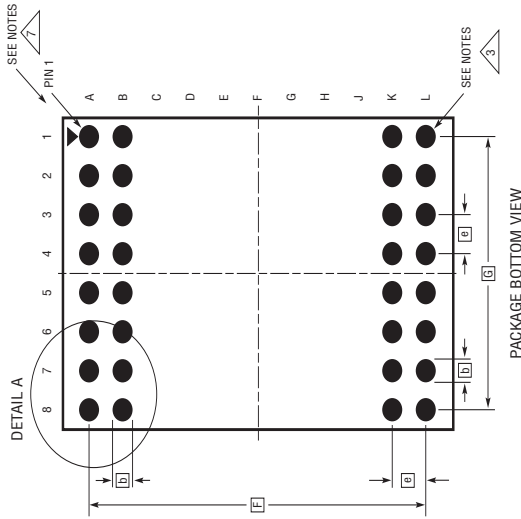


Figure 29. One Complete Isolated Powered Ethernet Port

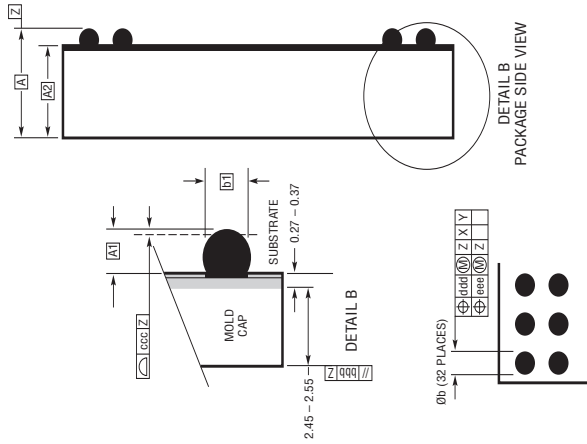
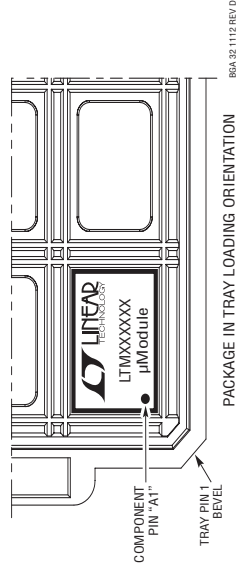
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTM2886#packaging> for the most recent package drawings.

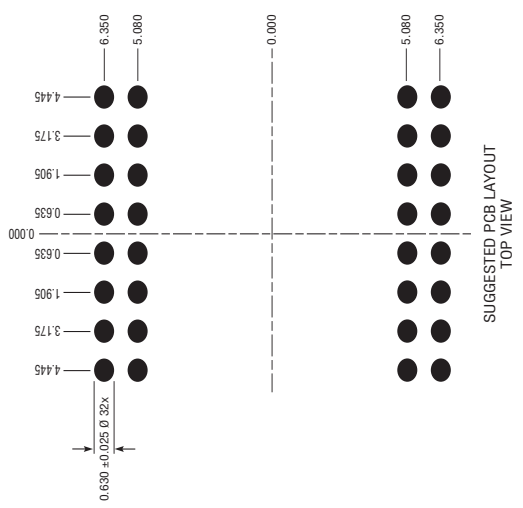
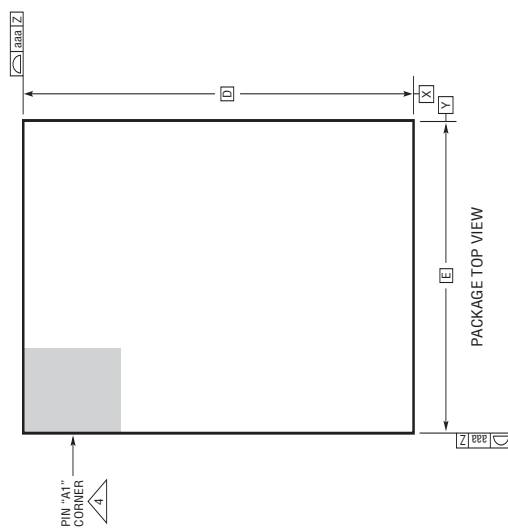
**BGA Package**  
**32-Lead (15mm × 11.25mm × 3.42mm)**  
 (Reference LIC DWG # 05-08-1851 Rev D)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
  7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ MODULE PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	3.22	3.42	3.62
A1	0.50	0.60	0.70
A2	2.72	2.82	2.92
b	0.60	0.75	0.90
b1	0.60	0.63	0.66
D		15.0	
E		11.25	
e		1.27	
F		12.70	
G		8.89	
aaa			0.15
bbb			0.10
ccc			0.20
ddd			0.30
eee			0.15
TOTAL NUMBER OF BALLS: 32			



## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/17	Added UL-CSA File Number	1
B	07/17	Changed MIN limits for $t_{PWU}$ (SPI and I <sup>2</sup> C) Changed MAX limits for Power-Up Time	6 6



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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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