# ±0.5% Accurate Quad Configurable Supervisor

## FEATURES

- **Simultaneously Monitor Four Power Supplies**
- **±0.5% Threshold Accuracy Over Temperature**
- **Selectable –4% and –6% Thresholds per Supply: 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1V and ±ADJ**
- Adjustable Reset ($\overline{RST}$) Timeout
- Overvoltage and Negative Voltage Monitoring
- Push-Pull or Open-Drain $\overline{RST}$ Output
- Margin Pin $\overline{RDIS}$ for Reset Disable
- H-Grade Temperature Range
- LTC2963
  - Non-Windowed (–1) Watchdog
  - Adjustable Watchdog Timer
  - Watchdog Status Output $\overline{WDO}$
  - Selectable Initial Watchdog Timeout
- LTC2964
  - Individual Comparator Open-drain Outputs
- 16-Lead 3mm × 3mm QFN (LTC2962)
- 20-Lead 3mm × 4mm QFN (LTC2963, LTC2964)

## APPLICATIONS

- High Reliability Systems
- Network, Telecom and Server Systems
- Automotive Control Systems

## DESCRIPTION

The LTC®2962 series of configurable power supply monitors can supervise systems with up to four supply voltages. One of 16 preset or adjustable voltage monitor thresholds per channel can be selected using external 1% resistors connected to the programming (PG) inputs. The preset voltage thresholds are accurate to ±0.5% over temperature. Positive (+ADJ) and negative (–ADJ) adjustable inputs with a 0.5V threshold allow undervoltage, negative voltage and overvoltage monitoring.

The watchdog (LTC2963 only) and reset timeout periods are adjustable using external capacitors. Accurate voltage thresholds and comparator glitch immunity ensure reliable reset operation without false triggering. The $\overline{RST}$ output is guaranteed to be in the correct state for $V_{CC}$ input voltage down to 1V.

The flexibility of the LTC2962 family provides the ability to monitor a wide variety of power supply combinations, including multiple supplies of the same voltage, with ±0.5% accuracy.

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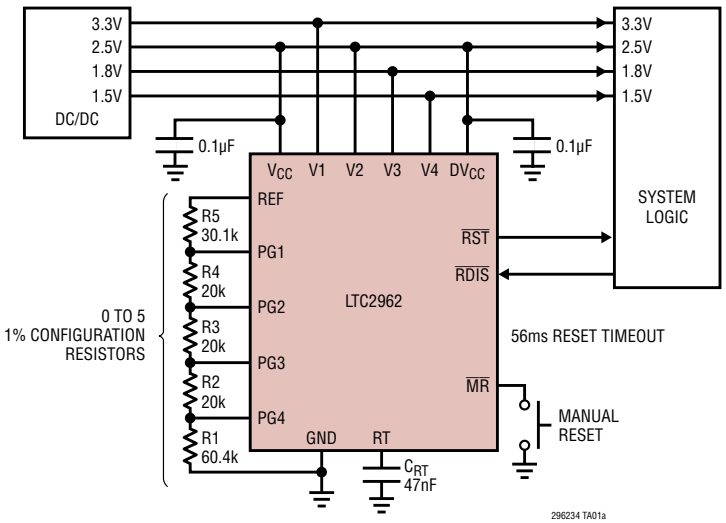
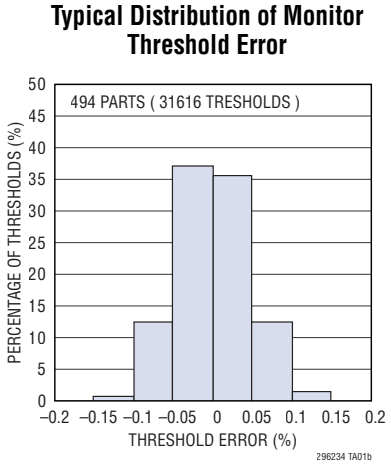
## TYPICAL APPLICATION




Rev 0

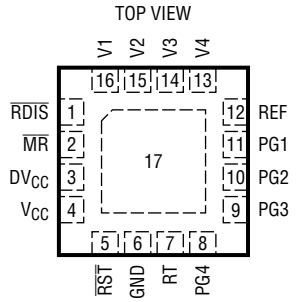
## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

V1 - V4, $\overline{MR}$, $\overline{RDIS}$, WDI, $DV_{CC}$, $V_{CC}$ ..... –0.3V to 6V
PG1 - PG4, REF..... –0.3V to 1.5V
OUT1 - OUT4..... –0.3V to 6V
RT, WT, WDS .....–0.3V to ($V_{CC}$ + 0.3V)
$\overline{RST}$, $\overline{WDO}$ ($DV_{CC} \geq 1.6V$) ..... –0.3V to ($DV_{CC}$ + 0.3V)
$\overline{RST}$, $\overline{WDO}$ ($DV_{CC}$ = GND) ..... –0.3V to 6V
Reference Load Current ($I_{REF}$) ..... ±1mA
$\overline{RST}$, $\overline{WDO}$, OUT1 - OUT4 Currents..... ±10mA
Operating Temperature Range
C-Grade ..... 0°C to 70°C
I-Grade..... –40°C to 85°C
H-Grade ..... –40°C to 125°C
Storage Temperature Range .....–65 to 150°C

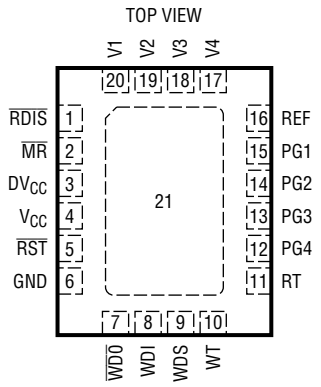
## PIN CONFIGURATION

LTC2962



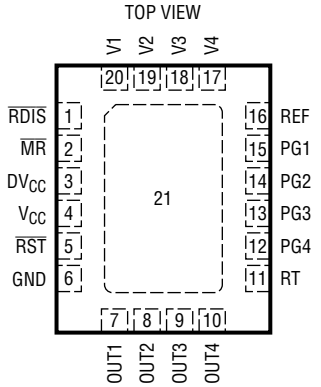

UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 68°C/W, $\theta_{JC}$ = 7.5°C/W
EXPOSED PAD (PIN 17) PCB GND CONNECTION OPTIONAL

LTC2963




UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 52°C/W, $\theta_{JC}$ = 6.8°C/W
EXPOSED PAD (PIN 21) PCB GND CONNECTION OPTIONAL

LTC2964




UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 52°C/W, $\theta_{JC}$ = 6.8°C/W
EXPOSED PAD (PIN 21) PCB GND CONNECTION OPTIONAL

## ORDER INFORMATION

| TUBE | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2962CUD#PBF | LTC2962CUD#TRPBF | LGZZ | 16-Lead (3mm × 3mm) Plastic QFN | 0°C to 70°C |
| LTC2962IUD#PBF | LTC2962IUD#TRPBF | LGZZ | 16-Lead (3mm × 3mm) Plastic QFN | –40°C to 85°C |
| LTC2962HUD#PBF | LTC2962HUD#TRPBF | LGZZ | 16-Lead (3mm × 3mm) Plastic QFN | –40°C to 125°C |
| LTC2963CUDC-1#PBF | LTC2963CUDC-1#TRPBF | LHBC | 20-Lead (3mm × 4mm) Plastic QFN | 0°C to 70°C |
| LTC2963IUDC-1#PBF | LTC2963IUDC-1#TRPBF | LHBC | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 85°C |
| LTC2963HUDC-1#PBF | LTC2963HUDC-1#TRPBF | LHBC | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 125°C |
| LTC2964CUDC#PBF | LTC2964CUDC#TRPBF | LHBB | 20-Lead (3mm × 4mm) Plastic QFN | 0°C to 70°C |
| LTC2964IUDC#PBF | LTC2964IUDC#TRPBF | LHBB | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 85°C |
| LTC2964HUDC#PBF | LTC2964HUDC#TRPBF | LHBB | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3.3V, $DV_{CC}$ = 0V, $\overline{MR}$ = $\overline{RDIS}$ = $V_{CC}$, unless otherwise specified. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| | $V_{CC}$ Operating Range | | ● | 2.25 | | 5.5 | V |
| | Guaranteed $\overline{RST}$ Output Low | $V_{CC}$ Rising | ● | | | 1 | V |
| $V_{CCMINC}$ | Minimum Required for Configuration | $V_{CC}$ Rising | ● | | | 2.2 | V |
| $I_{VCC}$ | $V_{CC}$ Input Supply Current | | ● | 80 | 140 | 210 | µA |
| | $DV_{CC}$ Operating Range | | ● | 1.6 | | 5.5 | V |
| | $DV_{CC}$ Input Supply Current | $I_{RST}$ = 0, $I_{WDO}$ = 0 | ● | | 25 | 500 | nA |
| $V_{RT50}$ | 5V, –4% Reset Threshold<br>5V, –6% Reset Threshold | | ●<br>● | 4.775<br>4.675 | 4.8<br>4.7 | 4.825<br>4.725 | V<br>V |
| $V_{RT33}$ | 3.3V, –4% Reset Threshold<br>3.3V, –6% Reset Threshold | | ●<br>● | 3.152<br>3.087 | 3.168<br>3.102 | 3.185<br>3.119 | V<br>V |
| $V_{RT25}$ | 2.5V, –4% Reset Threshold<br>2.5V, –6% Reset Threshold | | ●<br>● | 2.388<br>2.338 | 2.4<br>2.35 | 2.413<br>2.363 | V<br>V |
| $V_{RT18}$ | 1.8V, –4% Reset Threshold<br>1.8V, –6% Reset Threshold | | ●<br>● | 1.719<br>1.683 | 1.728<br>1.692 | 1.737<br>1.701 | V<br>V |
| $V_{RT15}$ | 1.5V, –4% Reset Threshold<br>1.5V, –6% Reset Threshold | | ●<br>● | 1.433<br>1.403 | 1.44<br>1.41 | 1.448<br>1.418 | V<br>V |
| $V_{RT12}$ | 1.2V, –4% Reset Threshold<br>1.2V, –6% Reset Threshold | | ●<br>● | 1.146<br>1.122 | 1.152<br>1.128 | 1.158<br>1.134 | V<br>V |
| $V_{RT10}$ | 1.0V, –4% Reset Threshold<br>1.0V, –6% Reset Threshold | | ●<br>● | 0.955<br>0.935 | 0.96<br>0.94 | 0.965<br>0.945 | V<br>V |
| $V_{RTA}$ | ±ADJ Reset Threshold | | ● | 497.5 | 500 | 502.5 | mV |
| $V_{REF}$ | Reference Voltage | $V_{CC}$ = 2.25V to 5.5V, $I_{REF}$ = ±1mA, $C_{REF}$ ≤ 1000pF | ● | 1.183 | 1.195 | 1.207 | V |
| $V_{PG}$ | PG1 to PG4 Configuration Voltage Range | $V_{CC}$ > $V_{CCMINC}$ | ● | 0 | | $V_{REF}$ | V |
| $I_{MON}$ | Monitor Input Current for V1 - V4 | ±ADJ Modes (Vn = 0.5V) | ● | | | ±15 | nA |
| $R_{MON}$ | Monitor Input Resistance for V1 - V4 | All Modes Except ±ADJ | | 0.8 | 1.2 | 1.6 | MΩ |
| $t_{UV}$ | Comparator Propagation Delay to $\overline{RST}$ or OUTn Falling Edge | Overdrive = 10% | ● | | 20 | 40 | µs |
| | RT and WT Pull-Up Current | V = GND | ● | –1.5 | –2 | –2.5 | µA |
| | RT and WT Pull-Down Current | V = 1.3V | ● | 1.5 | 2 | 2.5 | µA |
| $t_{RST}$ | Reset Timeout Period | $C_{RT}$ = 1500pF<br>$V_{RT}$ = $V_{CC}$ | ●<br>● | 12<br>160 | 18<br>200 | 24<br>240 | ms<br>ms |
| | Internal Timer Select Level (WT and RT) | | ● | $V_{CC}$ – 0.1 | | | V |
| | $V_{CC}$-Detect Current in Internal Timer Mode (WT and RT) | V = $V_{CC}$ | ● | | 1 | 2 | µA |
| **LTC2963 Watchdog** | | | | | | | |
| $t_{WDU}$ | Watchdog Upper Timeout Period | $C_{WT}$ = 1500pF<br>WT Tied to $V_{CC}$ | ●<br>● | 100<br>1.3 | 150<br>1.6 | 200<br>2 | ms<br>s |
| $t_{WD(INIT)}$ | Initial Watchdog Timeout Period | WDS = Logic Low<br>WDS = Open<br>WDS = Logic High | ●<br>●<br>● | | $t_{WDU}$<br>8 • $t_{WDU}$<br>64 • $t_{WDU}$ | | |
| $V_{WDS}$ | WDS Input Level<br>($V_{CC}$ = 2.25 to 5.5V) | Logic Low<br>Open<br>Logic High | ●<br>●<br>● | <br>0.7<br>$V_{CC}$ – 0.3 | <br>1.3 | 0.4<br>$V_{CC}$ – 0.7 | V<br>V<br>V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3.3V, $DV_{CC}$ = 0V, $\overline{MR}$ = $\overline{RDIS}$ = $V_{CC}$, unless otherwise specified. (Note 2)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{WDS}$ | WDS Input Current | $V_{WDS}$ = GND<br>$V_{WDS}$ = $V_{CC}$ | ●<br>● | –4 | –2.6<br>2.6 | <br>4 | µA<br>µA |
| $I_{WDS(HZ)}$ | Allowable WDS Leakage in Open State | | ● | | | ±1 | µA |
| $t_{WDI,MAX}$ | Rise/Fall Time of WDI Edge | | | | | 2 | µs |
| $t_{WP}$ | WDI Input Pulse Width | $V_{CC}$ = 2.25V to 5.5V | ● | 2 | | | µs |
| $t_{WD}$ | WDI to WDO Propagation Delay | | ● | | | 0.5 | µs |
| **Logic I/O** | | | | | | | |
| $V_{OL}$ | Voltage Output Low $\overline{RST}$, $\overline{WDO}$ (Note 3) | $I_{SINK}$ = 3mA, $V_{CC}$ = 2.25V to 5.5V | ● | | 40 | 150 | mV |
| | $\overline{RST}$ Only | $I_{SINK}$ = 100µA, $V_{CC}$ = 1.1V | ● | | 10 | 60 | mV |
| | Voltage Output Low OUTn (LTC2964, Note 4) | $I_{SINK}$ = 5mA, $V_{CC}$ = 2.25V to 5.5V | ● | | 50 | 300 | mV |
| $V_{OH}$ | Voltage Output High $\overline{RST}$, $\overline{WDO}$ (Note 3) | $I_{SOURCE}$ = –200µA; $DV_{CC}$ = 3.3V | ● | 0.7 • $DV_{CC}$ | | | V |
| | Voltage Output High, OUTn (LTC2964, Note 4) | $I_{SOURCE}$ = –1µA | ● | $V_{CC}$ – 1 | | | V |
| $I_{OH}$ | $\overline{RST}$, $\overline{WDO}$ Output Voltage High Leakage | V = 5.5V, $V_{CC}$ = 5.5V or $V_{CC}$ = GND | ● | | | 100 | nA |
| $I_{OPU}$ | $\overline{RST}$, $\overline{WDO}$ and OUTn Internal Pull-Up Current | V = GND | ● | –4 | –6 | -10 | µA |
| $V_{IL}$ | $\overline{RDIS}$, $\overline{MR}$ and $\overline{WDI}$ Input Level Low | $V_{CC}$ = 2.25 to 5.5V | ● | 0.4 | | | V |
| $V_{IH}$ | $\overline{RDIS}$, $\overline{MR}$ and $\overline{WDI}$ Input Level High | $V_{CC}$ = 2.25 to 5.5V | ● | | | 1.6 | V |
| $I_{IL}$ | $\overline{RDIS}$, $\overline{MR}$ and $\overline{WDI}$ Internal Pull-up Current | V = GND | ● | –16 | –10 | –4 | µA |
| $t_{MP}$ | $\overline{MR}$ Input Pulse Width | | ● | 150 | | | ns |
| $t_{MD}$ | $\overline{MR}$ Input Propagation Delay | $\overline{MR}$ Falling to $\overline{RST}$ Falling | ● | | 0.1 | 1 | µs |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

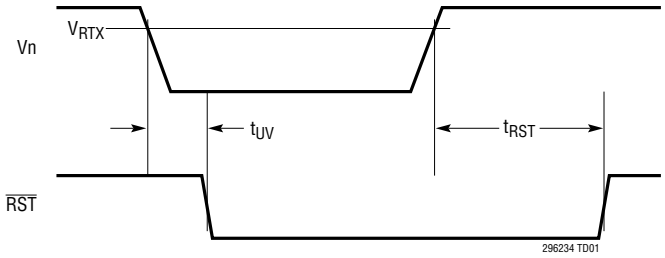
**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

**Note 3:** The $\overline{RST}$ and $\overline{WDO}$ pins are push-pull outputs that swing to $DV_{CC}$ when $DV_{CC}$ is greater than 1.6V.

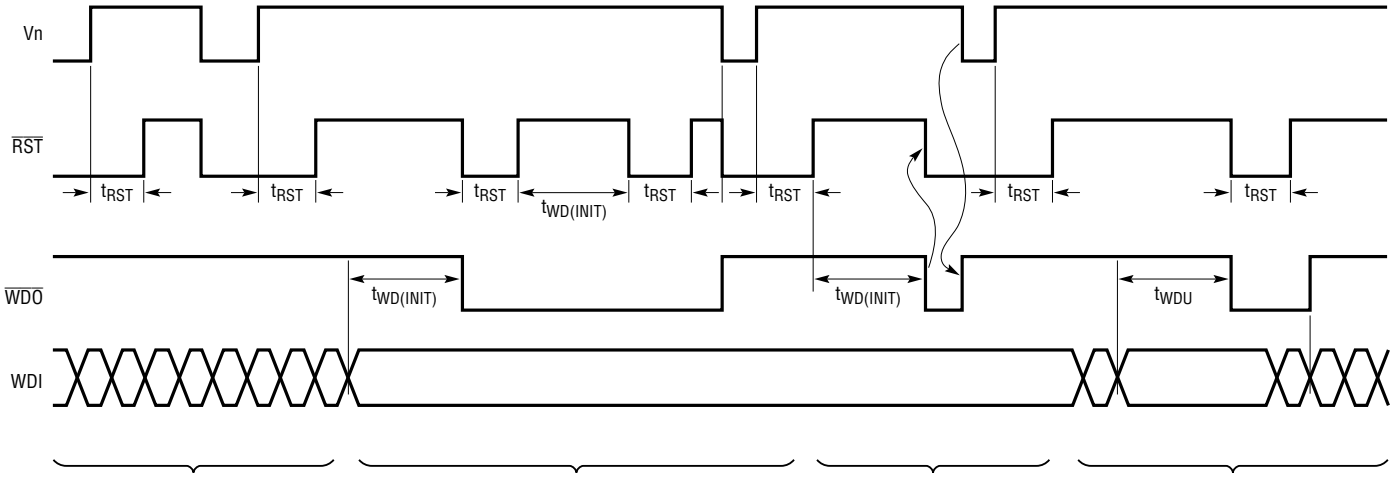
**Note 4:** The output pins, OUT1 - OUT4, have internal pull-ups to $V_{CC}$ of typically 6µA. However, external pull-up resistors may be used when faster rise times are required or for $V_{OH}$ voltages greater than $V_{CC}$.

# TIMING DIAGRAMS

### Vn Monitor Timing




### Reset and Watchdog Timing (LTC2963)




POWER-ON RESET FOLLOWED BY RESET CAUSED BY UNDERVOLTAGE EVENT.

WATCHDOG OUTPUT SET HIGH, WATCHDOG INPUT = DON'T CARE.

WATCHDOG INPUT NOT TOGGLED, INITIAL WATCHDOG TIMER EXPIRES, WATCHDOG OUTPUT PULLS LOW. RESET OUTPUT PULLS LOW FOR ONE RESET TIMEOUT PERIOD.

WATCHDOG INPUT REMAINS UNTOGGLED, WATCHDOG OUTPUT REMAINS LOW, RESET OUTPUT PULLS LOW AGAIN AFTER ONE INITIAL WATCHDOG TIMEOUT PERIOD. WATCHDOG OUTPUT CLEARED BY UNDERVOLTAGE EVENT.

WATCHDOG INPUT NOT TOGGLED, INITIAL WATCHDOG TIMER EXPIRES, WATCHDOG OUTPUT PULLS LOW. RESET OUTPUT PULLS LOW.

WATCHDOG OUTPUT LOW TIME SHORTENED BY UNDERVOLTAGE EVENT DURING RESET TIMEOUT.

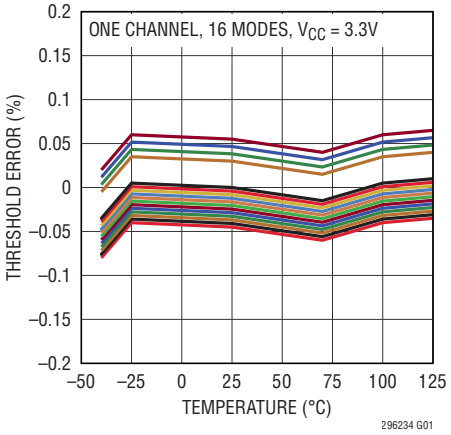
WATCHDOG INPUT TOGGLED, INITIAL WATCHDOG TIMER CLEARED. WATCHDOG INPUT NOT TOGGLED, WATCHDOG TIMER EXPIRES, WATCHDOG OUTPUT PULLS LOW. RESET OUTPUT PULLS LOW.

WATCHDOG OUTPUT NOT CLEARED BY WATCHDOG INPUT DURING RESET TIMEOUT. AFTER RESET COMPLETED, WATCHDOG INPUT CLEARS WATCHDOG OUTPUT.

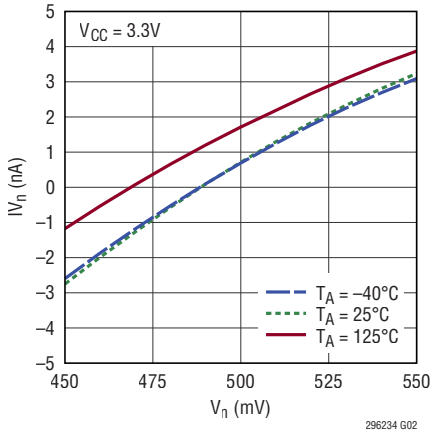
296234 TD02

## TYPICAL PERFORMANCE CHARACTERISTICS

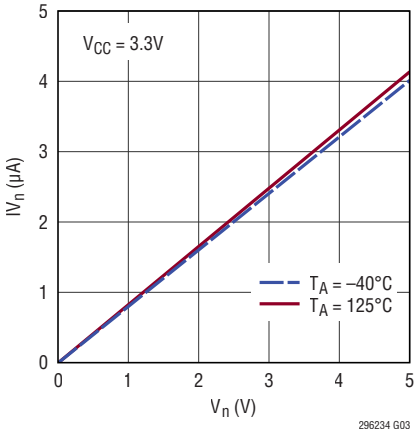
### Normalized Threshold Error vs Temperature



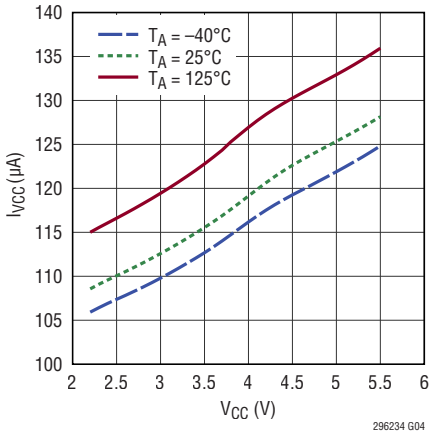

### $V_n$ Input Current vs Voltage: ±ADJ Mode



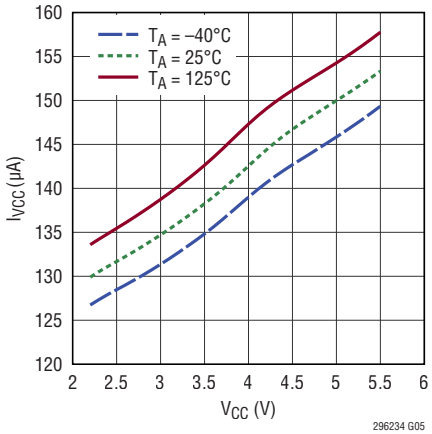

### $V_n$ Input Current vs Voltage: All Modes Except ±ADJ



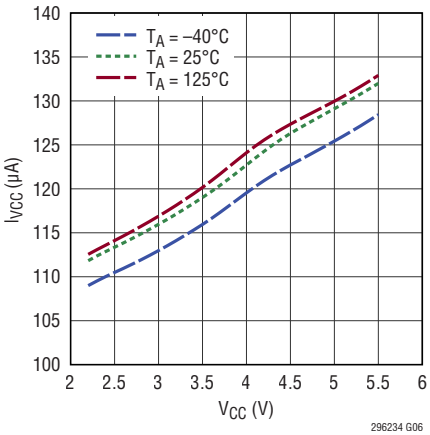

### $I_{VCC}$ vs $V_{CC}$ (LTC2962)



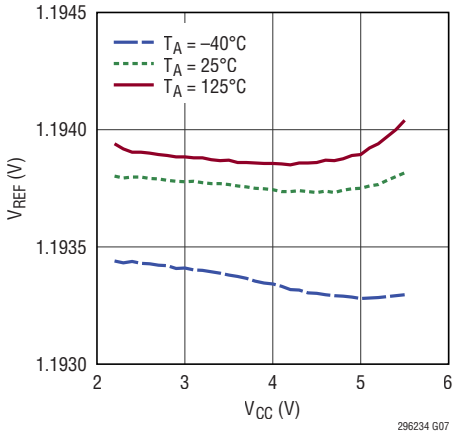

### $I_{VCC}$ vs $V_{CC}$ (LTC2963)



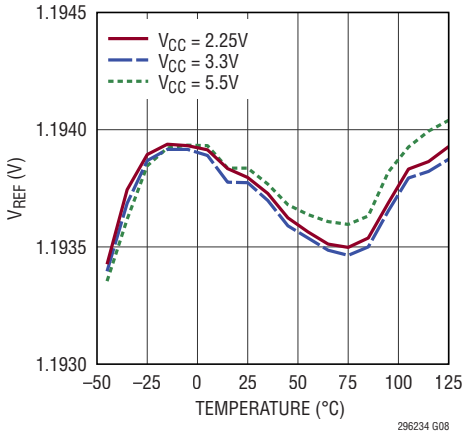

### $I_{VCC}$ vs $V_{CC}$ (LTC2964)



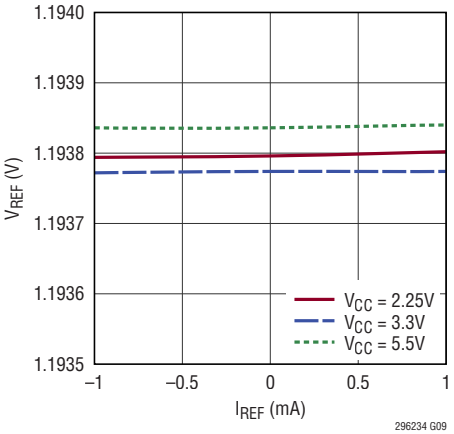

### $V_{REF}$ vs $V_{CC}$




### $V_{REF}$ vs Temperature

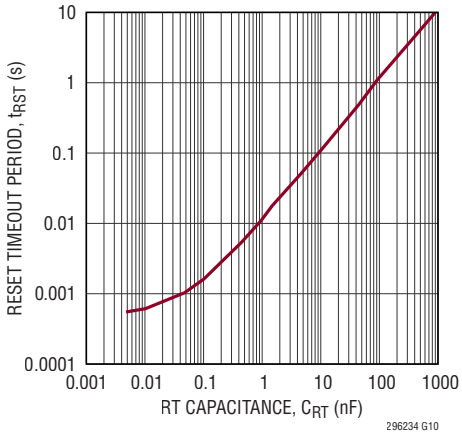



### $V_{REF}$ vs $I_{REF}$

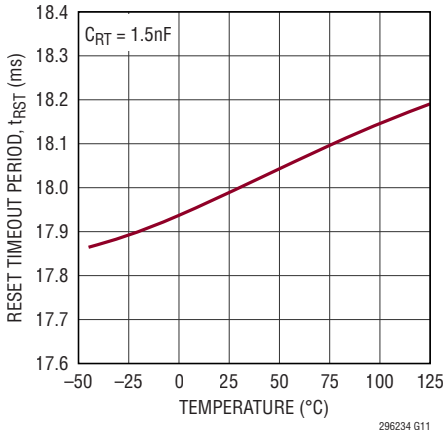


# TYPICAL PERFORMANCE CHARACTERISTICS

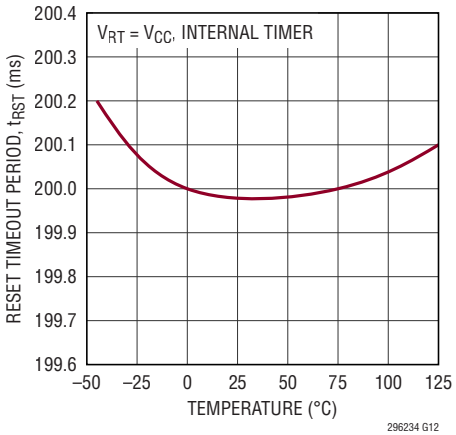
### Reset Timeout Period vs Capacitance



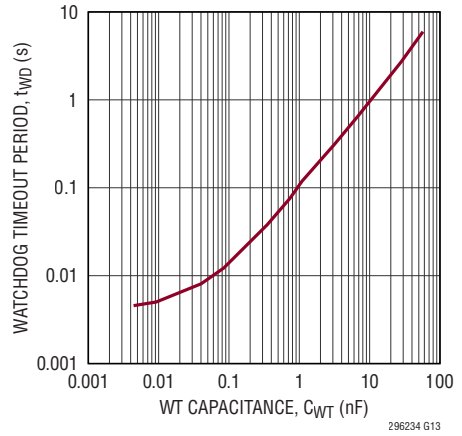

### Reset Timeout Period vs Temperature



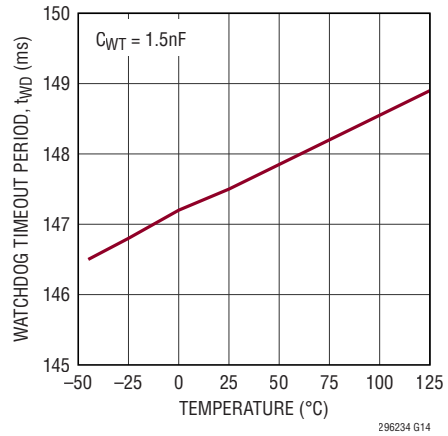

### Reset Timeout Period vs Temperature



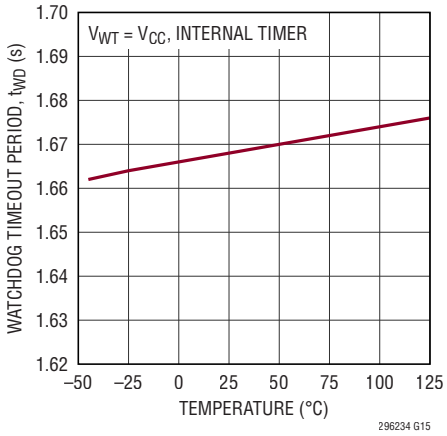

### Watchdog Timeout Period vs Capacitance



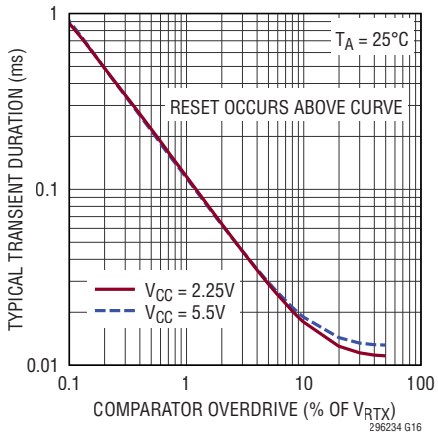

### Watchdog Timeout Period vs Temperature



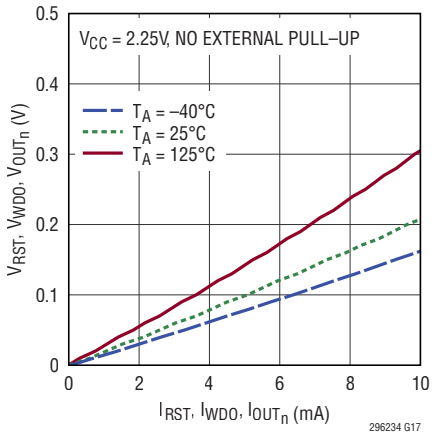

### Watchdog Timeout Period vs Temperature



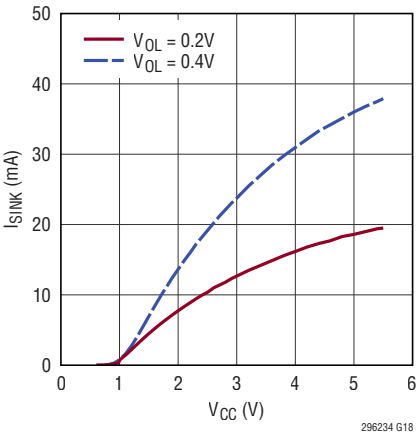

### Transient Duration vs Comparator Overdrive




### $\overline{RST}$, $\overline{WDO}$, $OUT_n$ $V_{OL}$ vs Pull-Down Current

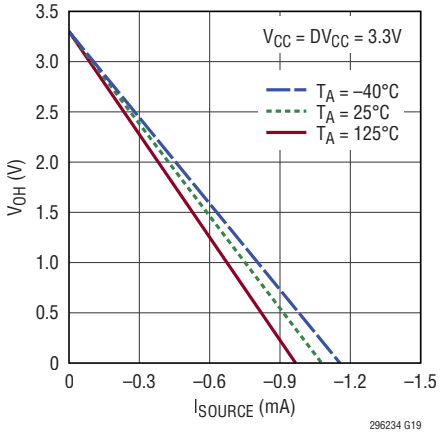



### Output Logic Low, $I_{SINK}$ vs $V_{CC}$ $\overline{RST}$, $\overline{WDO}$, $OUT_n$

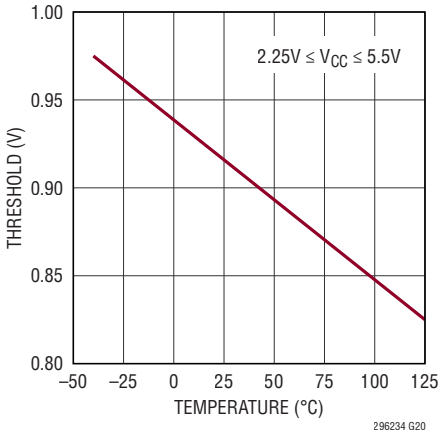


## TYPICAL PERFORMANCE CHARACTERISTICS

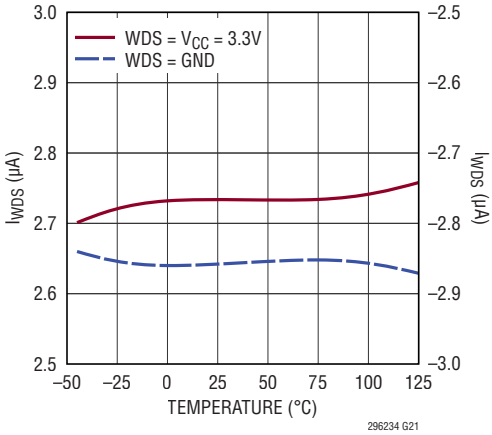
**$\overline{RST}$, $\overline{WDO}$ $V_{OH}$ vs Source Current**




**$\overline{MR}$, $\overline{RDIS}$, WDI Input vs Temperature**




**$I_{WDS}$ vs Temperature**




## PIN FUNCTIONS

**$DV_{CC}$:** Digital Logic Supply. $DV_{CC}$ is used for setting the logic swing at the $\overline{RST}$ and $\overline{WDO}$ (LTC2963 only) outputs. Tying $DV_{CC}$ to a voltage greater than 1.6V allows the $\overline{RST}$ and $\overline{WDO}$ to act as active push-pull outputs. When $DV_{CC}$ is applied above 1.6V, a 0.1µF (or greater) bypass capacitor is recommended. Ground the $DV_{CC}$ pin to configure the $\overline{RST}$ and $\overline{WDO}$ as open drain outputs. Do not leave $DV_{CC}$ open.

**Exposed Pad:** Exposed pad internally connected to ground. PCB connection is optional.

**GND:** Device Ground.

**$\overline{MR}$:** Manual Reset Input. A logic low on this input pulls $\overline{RST}$ low. When $\overline{MR}$ returns high, $\overline{RST}$ returns high after the configured reset timeout assuming all four Vn inputs are above their respective thresholds. The manual reset input is pulled up to $V_{CC}$ by an internal 10µA current source. Drive the input with a mechanical switch or logic signal. Leave the input open or tied to $V_{CC}$ if unused.

**OUT1 - OUT4 (LTC2964 only):** Individual Comparator Outputs. These four pins are real-time open drain logic outputs of the monitor comparators. Each output is released when the corresponding input is above its reset threshold, and pulls low when its input is below the reset threshold (except in –ADJ mode). A weak internal 6µA pulls these pins up to $V_{CC}$. Connect an external pull up resistor to an external logic supply to ensure that the output high of each pin is above $V_{IH}$ of the external detector and/or for faster rise times. Leave open if unused.

**PG1 - PG4:** Threshold Select Inputs. Connect an external 1% resistive divider between REF and GND to select one of sixteen possible voltage thresholds for each channel. Do not add capacitance to PG1 through PG4 inputs. See the Monitor Configuration section for more information. Connect to REF if unused.

**$\overline{RDIS}$:** Reset Disable Input. Pulling this input to GND prevents the $\overline{RST}$ output from being pulled low. This function allows supply margining without issuing a reset command to the processor. A weak internal 10µA pull-up to $V_{CC}$ allows this pin to be left open for normal operation.

**REF:** Buffered Reference Voltage Output. A 1.195V nominal reference is used for the mode selection voltage and for level shifting in negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

## PIN FUNCTIONS

**$\overline{RST}$:** Reset Output. An internal 6µA current pulls this open drain output to $V_{CC}$. Pulls low when any voltage monitor input is below the reset threshold and held low for the configured reset delay time after all voltage inputs are above their threshold. Leave open if unused.

**RT:** Reset Timeout Capacitor Input. Attach an external capacitor ($C_{RT}$) to GND to set a reset timeout of 12ms/nF. Tie RT to $V_{CC}$ to activate the internal 200ms reset timeout.

**V1 - V4:** Voltage Monitor Inputs. Select from 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1V or ±ADJ monitor thresholds as determined by the threshold selection inputs PG1 - PG4. See Applications Information for details. Connect to $V_{CC}$ and set to +ADJ mode if unused.

**$V_{CC}$:** Power Supply Input. $V_{CC}$ powers the part. Bypass this input to ground with a 0.1µF (or greater) capacitor. All status outputs are weakly pulled up to $V_{CC}$.

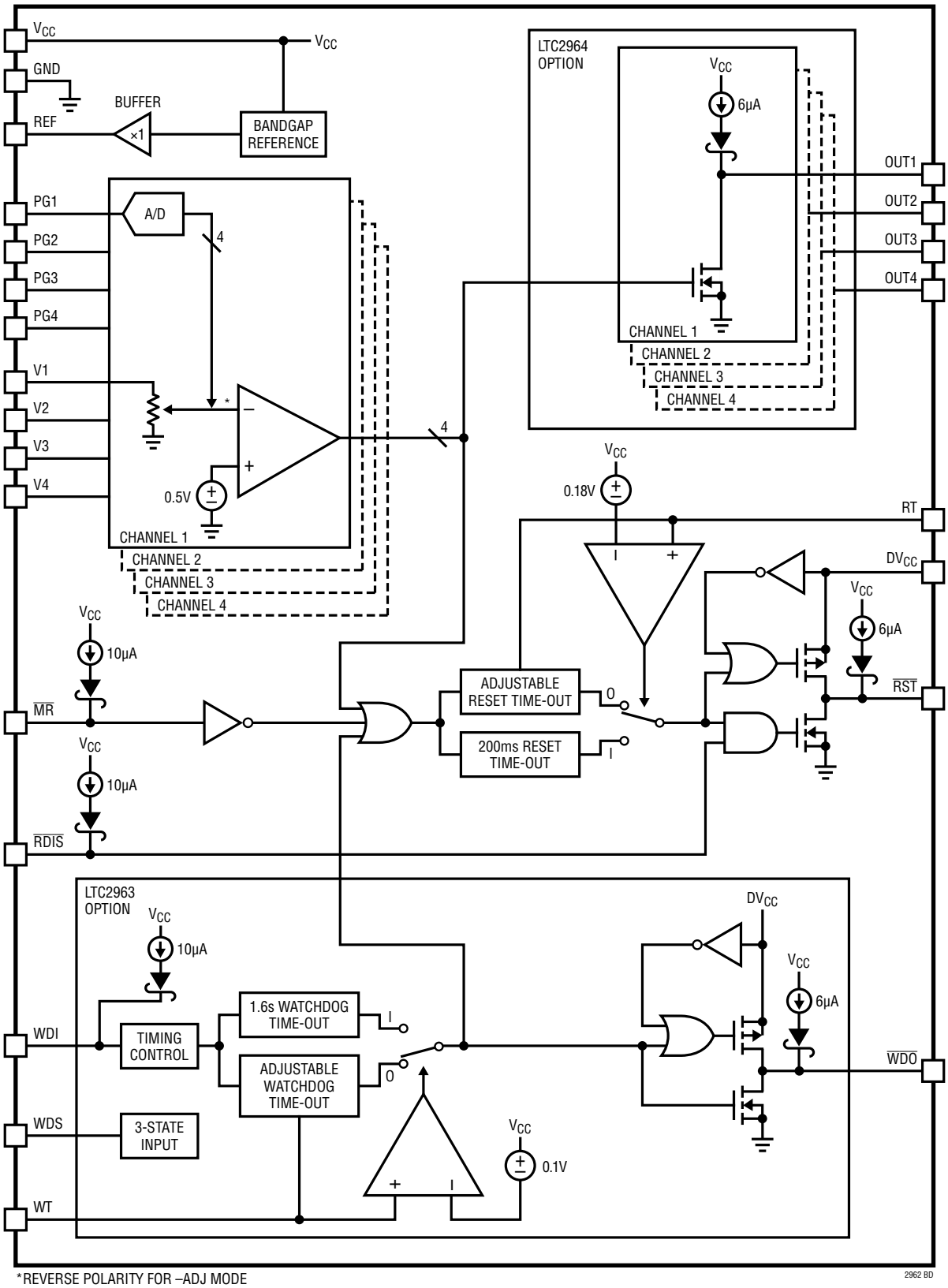
**WDI (LTC2963 only):** Watchdog Input. It controls the operation of the watchdog timer. While $\overline{RST}$ is high, a valid WDI transition during the watchdog timeout period is required to inhibit $\overline{WDO}$ and $\overline{RST}$ from pulling low and initiating a watchdog reset. In LTC2963, both rising and falling edges are valid WDI inputs. A capacitor attached to WT sets the watchdog timeout period. A valid WDI edge clears the internal counter driven by a clock signal based on $C_{WT}$, preventing $\overline{WDO}$ from going low. Once the watchdog timer expires and $\overline{WDO}$ is latched low, WDI must transition between low and high logic levels to clear $\overline{WDO}$. See the Watchdog Timer section for more information.

**$\overline{WDO}$ (LTC2963 only):** Watchdog Output. Open drain output weakly pulled to $V_{CC}$. The watchdog timer is enabled when $\overline{RST}$ is high. The $\overline{WDO}$ output pulls low if the watchdog timer expires, and it remains low until the next valid WDI transition during the watchdog timer period or if a channel undervoltage condition occurs. A watchdog failure also triggers a reset event, and the $\overline{RST}$ output pulls low. Leave open if unused. See the Watchdog Timer section for more information.

**WDS (LTC2963 only):** Initial watchdog timeout select input. A three-state input controls the duration of the initial watchdog timeout immediately following any reset event. Extending the timeout for the first period gives extra time for the system logic to initialize before generating watchdog input pulses. A logic low sets the timeout to its nominal time period (equal to the watchdog upper timeout). Leaving the WDS input open sets the timeout to eight times the watchdog upper timeout, while a logic high selects sixty-four times the watchdog upper timeout. See the Initial Watchdog Timeout discussion for more details.

**WT (LTC2963 only):** Watchdog Timeout Capacitor Input. Attach a capacitor $C_{WT}$ between WT and GND to set a watchdog timeout period of 100ms/nF. Leaving WT open generates a minimum timeout period of approximately 2ms, which may vary depending on parasitic capacitance on the pin. Tie WT to GND in order to disable the watchdog function. Tie WT to $V_{CC}$ to activate the internal 1.6s watchdog timer.

## BLOCK DIAGRAM




Rev 0

## OPERATION

The LTC2962 family monitors up to four power supplies (or channels) with industry leading ±0.5% accuracy over a wide temperature range. While primarily intended for monitoring undervoltage (UV) events, the LTC2962 family has a mode allowing for overvoltage (OV) monitoring. In typical operation, if any of the monitored supplies fall below a predetermined threshold, the reset output, $\overline{RST}$, pulls low immediately. When all four supplies rise above their threshold (or below, in the case of –ADJ mode), the reset output is released after a timeout period. The reset timeout can be a fixed 200ms or it can be adjusted using an external capacitor. The reset output is held low during power-up, power-down and brownout conditions on any channel.

±ADJ modes and fourteen UV thresholds can be configured for each channel individually. Each of the four program (PG) inputs select one of sixteen voltage monitor thresholds for each input respectively. During power-up, a 4-bit ADC converts the voltage on each PG input. The resultant digital value is decoded into one of the sixteen threshold options (see Table 1). This technique allows for 1% standard resistors to be used to configure the PG inputs while maintaining tight ±0.5% accuracy for each threshold. 65,536 different threshold combinations can be selected with the LTC2962 family, including the ability to monitor the same voltage on more than one channel. The +ADJ and –ADJ modes compare the channel inputs to 0.5V. With an external resistive divider, +ADJ can be used to monitor any voltage greater than 0.5V. –ADJ can be used as an overvoltage monitor for positive supplies or an undervoltage monitor for negative supplies.

The reset disable function, $\overline{RDIS}$, eases system voltage margining by forcing $\overline{RST}$ high. During normal operation, $\overline{RST}$ will go low when the monitored voltage (e.g. V1, V2, etc.) falls below its threshold (or above, in the case of –ADJ mode). By disabling the reset function with $\overline{RDIS}$, a microprocessor voltage limit can be tested through margining without issuing a system reset. In addition to being able to ignore valid reset outputs, a manual reset can also be commanded with the $\overline{MR}$ input. This input has an internal pull-up and debounce circuitry making it well suited for a pushbutton input. When $\overline{MR}$ goes low, $\overline{RST}$ pulls low immediately. When $\overline{MR}$ goes high, $\overline{RST}$ is released after the configured reset timeout delay – assuming that all four monitored voltages are above their configured threshold.

With $DV_{CC}$ grounded, $\overline{RST}$ is an open-drain output weakly pulled up internally to $V_{CC}$ by 6µA through a Schottky diode. However, if $DV_{CC}$ is externally connected to a voltage greater than 1.6V, then $\overline{RST}$ will be driven as an active push-pull output to $DV_{CC}$.

### LTC2963 Watchdog Functionality

In addition to the common LTC2962 family functionality discussed above, the LTC2963 offers a watchdog function. In the LTC2963, the WDI input must receive an edge (rising or falling) at least as often as the configured watchdog upper timeout period. This time can be fixed to 1.6s by connecting WT to $V_{CC}$ or it can be adjusted using an external capacitor on WT. If WDI does not receive a signal quickly enough, then $\overline{WDO}$ (watchdog status) and $\overline{RST}$ outputs will both pull low. $\overline{RST}$ returns high after a single reset timeout period. Like the $\overline{RST}$ output, the $\overline{WDO}$ output has a weak internal pull-up to $V_{CC}$, but can be used as an active push-pull if $DV_{CC}$ is greater than 1.6V. The details of $\overline{WDO}$ functionality can be found in the Watchdog Timer section.

Following a reset event, the microprocessor under supervision may require more time than usual to send valid watchdog edge transitions. The 3-state WDS input provides a way to choose three different initial watchdog timeout periods immediately following a reset.

### LTC2964 Individual Outputs

The LTC2964 provides individual comparator outputs for each voltage input. These outputs could serve as a status indicator, e.g. power good, or be part of a power supply sequencer circuit. OUT1 through OUT4 provide the outputs of each of the four channel comparators without the adjustable reset timeout delay.

## APPLICATIONS INFORMATION

### Threshold Accuracy

The LTC2962 family features outstanding accuracy. To better understand the importance and implication of the monitor accuracy, we provide the following example. Consider a system device whose operation requires 1V ± 4.5% tolerance. In other words, to guarantee proper operation, the manufacturer states that the voltage presented to the device remain between 0.955V and 1.045V. In an ideal world, the power supply providing voltage to this device could vary over that entire range, and an ideal undervoltage supervisor for the supply would generate a reset at exactly 0.955V. However, no supervisor is perfect. The actual reset threshold of a supervisor varies over a specified range; the LTC2962 family varies ±0.5% around its nominal threshold voltage over temperature (see Figure 1).

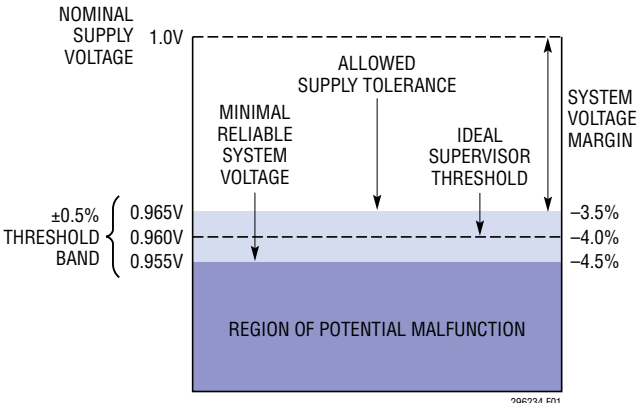



**Figure 1. Threshold Diagram**

The monitor reset threshold range and the power supply tolerance range should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance range.

The LTC2962 family has ±0.5% reset threshold accuracy, so a system load requiring ±4.5% tolerance requires the supervisor threshold to be set 4% below the nominal supply voltage. Using the 1V system described, the nominal –4% monitor threshold would be 0.96V. The monitor threshold is guaranteed to be between 0.955V and 0.965V over temperature. The powered system must work reliably down to the low end of the threshold range, 0.955V, or risk malfunction before a reset signal is properly issued. Furthermore, the power supply must be guaranteed to provide a voltage greater than 0.965V to avoid a false or nuisance reset.

An extremely accurate supervisor, like the LTC2962 family, has reduced monitor threshold spread, which increases system voltage margin and reduces the probability of system malfunction. By providing increased system margin the demands of the power supply are relaxed. For example, with a ±1% supervisor, the nominal supervisor threshold would need to be increased from –4% to –3.5%, and the lower limit of the power supply tolerance would be at –2.5%, 0.975V as opposed to 0.965V. In other words, the power supply would need to be more precise by 1%. Because of the accuracy of the LTC2962 family, it may be possible to use a smaller capacitor or a smaller inductor in the power supply. The system may be more tolerant of transient excursions. The additional margin may even allow a lower nominal supply voltage, which can dramatically reduce power consumption. Hence, the best-in-class ±0.5% accuracy of the LTC2962 family provides many benefits.

### Power-Up

Upon initial application of voltage, $V_{CC}$ will power the drive circuits for the $\overline{RST}$ output. This ensures that the $\overline{RST}$ output will be low as soon as $V_{CC}$ reaches 1V. The $\overline{RST}$ output remains low until the part is configured. See Monitor Configuration for details about configuration. After configuration, if any one of the supply monitor inputs falls below (or rises above, in –ADJ mode) its configured threshold, $\overline{RST}$ will continue to remain low. Once all monitor inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after the configured delay time, $t_{RST}$.

### Monitor Configuration

Configure the monitor threshold for each channel input by placing the recommended resistive divider from REF to GND and connect the tap point to the appropriate PG input, as shown in Figure 2. Table 1 specifies optimum $V_{PG}/V_{REF}$ ratios when configuring with a resistive divider or a ratiometric DAC.

As one may want to share the resistive divider for all four PG inputs, the following procedure is recommended.

## APPLICATIONS INFORMATION

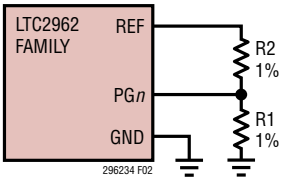



**Figure 2. Monitor Configuration**

First, create a resistive divider between REF and GND composed of fifteen ideal 10k resistors. For a specific input threshold combination, locate the optimal tap point for each PG input following the ratio provided in Table 1. Second, merge all resistors between any two adjacent tap points into one single resistor and choose the standard value using Table 2. Note the actual resistors in Table 2 are standard 1% values. Despite the difference between the actual and the calculated resistance value as well as the 1% tolerance, the LTC2962 family is guaranteed to select the proper configuration.

**Table 1. Voltage Configuration Table**

| SUPPLY VOLTAGE | OPTIMAL RATIO $V_{PG}/V_{REF}$ |
|---|---|
| +ADJ | 1 |
| 5.0V, –4% | 14/15 |
| 5.0V, –6% | 13/15 |
| 3.3V, –4% | 12/15 |
| 3.3V, –6% | 11/15 |
| 2.5V, –4% | 10/15 |
| 2.5V, –6% | 9/15 |
| 1.8V, –4% | 8/15 |
| 1.8V, –6% | 7/15 |
| 1.5V, –4% | 6/15 |
| 1.5V, –6% | 5/15 |
| 1.2V, –4% | 4/15 |
| 1.2V, –6% | 3/15 |
| 1.0V, –4% | 2/15 |
| 1.0V, –6% | 1/15 |
| –ADJ | 0 |

Figure 3 shows an example of choosing PG resistors using the above procedure. In the example, the V1 monitor threshold is 5V –4% (4.8V), V2 is 3.3V –6% (3.102V), V3 is 1.2V –4% (1.152V) and V4 is set to –ADJ mode, respectively.

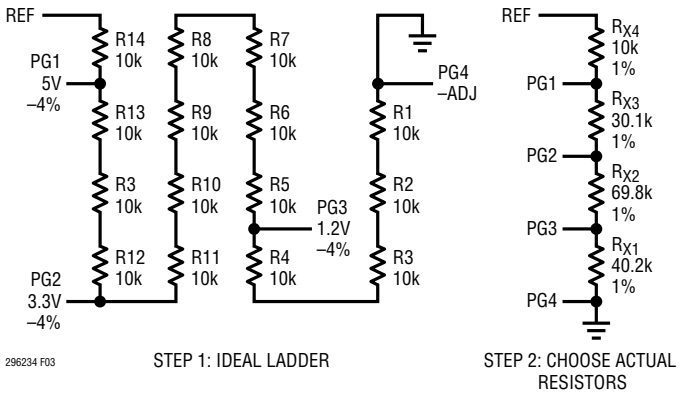



**Figure 3. Programming (PG) Pin Bias Example**

When a DAC is used to drive the PG inputs, the LTC2962 family is guaranteed to operate properly for bias voltage within ±1.5% of $V_{REF}$ relative to the optimal value.

During power-up, once $V_{CC}$ reaches $V_{CCMINC}$ (2.2V max), the LTC2962 family enters a configuration period of approximately 500µs during which the voltage on each of the four PG inputs are sampled and the monitor is configured to the desired threshold. Immediately after configuration, the comparators are enabled and supply monitoring will begin. Note once the part is configured, it cannot be reconfigured without powering down. Do not add capacitance to the PG inputs. It is always beneficial to Kelvin connect the resistive divider ground to the LTC2962 family GND.

**Table 2. Recommended 1% Resistors for Programming**

| CALCULATED RESISTOR VALUE (kΩ) | ACTUAL RESISTOR VALUE (kΩ) |
|---|---|
| 10 | 10 |
| 20 | 20 |
| 30 | 30.1 |
| 40 | 40.2 |
| 50 | 49.9 |
| 60 | 60.4 |
| 70 | 69.8 |
| 80 | 80.6 |
| 90 | 90.9 |
| 100 | 100 |
| 110 | 110 |
| 120 | 121 |
| 130 | 130 |
| 140 | 140 |

## APPLICATIONS INFORMATION

### Supply Monitoring – Fixed Thresholds

With the exception of the +ADJ and –ADJ modes, the remaining fourteen configuration settings for each channel set a fixed monitor threshold for that channel. In these settings, the input impedance of each of the four channel voltage inputs (V1 ~ V4) is a fixed 1.2MΩ to ground. As shown in the block diagram, the 4-bit programming ADC selects an attenuation factor between the channel voltage input and the channel comparator input corresponding to the configured fixed monitor threshold. These settings require the fewest external components and provide the ability to monitor any of the preselected thresholds with ±0.5% accuracy using, at most, five external 1% PG resistors.

### Supply Monitoring – Adjustable Thresholds

In the two Adjustable modes (+ADJ and –ADJ), the channel voltage inputs become high impedance. Normally these modes require the use of an additional external resistive divider, but provide the ability to monitor any supply voltage threshold.

In positive adjustable (+ADJ) mode, the comparator reference input (inverting) is set to 0.5V as shown in Figure 4. An external resistive divider connected between the positive voltage being sensed and ground is connected to the channel voltage input (V1 ~ V4). Calculate the channel threshold voltage from:

$$V_{TH} = 0.5V \bullet \left(1 + \frac{R4}{R3}\right)$$

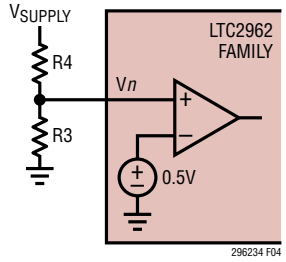



**Figure 4. Setting the Positive Adjustable (+ADJ) Threshold**

In the negative adjustable (–ADJ) mode, the comparator polarity is reversed as shown in Figure 5. The internal 0.5V reference is connected to the non-inverting comparator input. An external resistive divider connected between the negative voltage being sensed and the REF output is connected to the channel voltage input (V1 ~ V4). $V_{REF}$ provides the necessary level shift required to operate the comparator. Calculate the negative threshold voltage from:

$$V_{TH} = 0.5V \bullet \left(1 + \frac{R3}{R4}\right) - V_{REF} \bullet \frac{R3}{R4}$$

where $V_{REF}$ = 1.195V Nominal

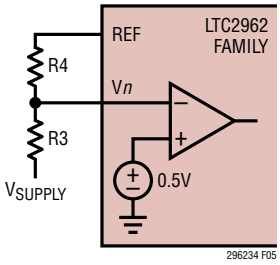



**Figure 5. Setting the Negative Adjustable (–ADJ) Threshold**

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of REF (1mA). With no other load on REF, R4 (minimum) is:

$$R4(min) = \frac{1.195V - 0.5V}{1mA} = 695\Omega$$

Tables 3 and 4 offer suggested 0.1% resistor values for various adjustable applications.

**Table 3. Suggested 0.1% Resistor Values for +ADJ Inputs (Figure 4)**

| $V_{SUPPLY}$ (V) | $V_{TH}$ (V) | R4 (kΩ) | R3 (kΩ) |
|---|---|---|---|
| 12 | 11.25 | 2150 | 100 |
| 10 | 9.4 | 1780 | 100 |
| 8 | 7.5 | 1400 | 100 |
| 7.5 | 7 | 1300 | 100 |
| 6 | 5.6 | 1020 | 100 |

## APPLICATIONS INFORMATION

**Table 4. Suggested 0.1% Resistor Values for –ADJ Inputs (Figure 5)**

| $V_{SUPPLY}$ (V) | $V_{TH}$ (V) | R3 (kΩ) | R4 (kΩ) |
|---|---|---|---|
| –2 | –1.866 | 412 | 121 |
| –5 | –4.721 | 909 | 121 |
| –5.2 | –4.847 | 931 | 121 |
| –10 | –9.494 | 1740 | 121 |
| –12 | –11.28 | 2050 | 121 |

### Supply Monitoring – Overvoltage Thresholds

Because the comparator polarity is reversed for the –ADJ mode, this mode can also be used for overvoltage monitoring. Implementing undervoltage and overvoltage (UV/OV) monitoring of a single supply is as simple as dedicating two channels in ±ADJ mode as shown in Figure 6. The threshold voltages are:

$$V_{OVTH} = 0.5 \bullet \left(1 + \frac{R5+R4}{R3}\right)$$

$$V_{UVTH} = 0.5 \bullet \left(1 + \frac{R5}{R4+R3}\right)$$

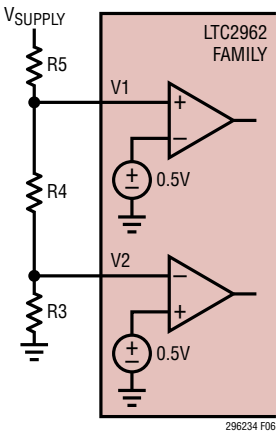



**Figure 6. 3-Resistor Positive UV/OV Monitoring Configuration (V1 in +ADJ, V2 in –ADJ)**

### Power-Down

On power-down, once any of the monitor inputs drop below its threshold, $\overline{RST}$ is held at a logic low. A logic low of 0.4V is guaranteed until $V_{CC}$ drops below 1V. If $V_{CC}$ drops below the minimum voltage required for configuration ($V_{CCMINC}$, guaranteed to be below 2.2V), then the device may reconfigure when $V_{CC}$ rises above $V_{CCMINC}$.

### Selecting the Reset Timing Capacitor

The reset timeout period is adjustable in order to accommodate a variety of applications. The reset timeout period, $t_{RST}$, is adjusted by connecting a capacitor, $C_{RT}$, between RT and ground. The value of this capacitor is determined by:

$$C_{RT} = t_{RST} \bullet 83 \text{ [pF/ms]}$$

A graph of reset timeout period as a function of the RT capacitor can be found in the Typical Performance Characteristics section.

Leaving RT open generates a minimum reset timeout period of approximately 250µs. Maximum reset timeout period is limited by the largest available low leakage capacitor. The accuracy of the timeout period is affected by capacitor tolerance, temperature coefficienct and leakage (the nominal RT charging current is 2µA). A low leakage ceramic capacitor is recommended.

Connect RT to $V_{CC}$ generates a fixed reset timeout of approximately 200ms.

### Glitch Immunity

In any supervisor application, noise on the monitored DC voltage could cause spurious undesirable resets. Two techniques are used to combat the spurious resets without sacrificing threshold accuracy. First, the reset timeout period helps prevent high-frequency supply variation whose frequency is above $1/t_{RST}$ from appearing at the output $\overline{RST}$.

When the voltage input goes below the threshold, the $\overline{RST}$ output goes low. When it recovers beyond the threshold, the reset timer starts (assuming it is not disabled by $\overline{RDIS}$), and $\overline{RST}$ does not go high until the timeout completes. If the monitored supply becomes invalid during the timeout period, the timer resets. The timer will restart when the supply becomes valid again.

While the reset timeout is useful at preventing $\overline{RST}$ toggling in most cases, it is not effective at preventing nuisance resets due to short glitches (due to load transients

## APPLICATIONS INFORMATION

or other effects) on a valid supply. Hysteresis is traditionally used to solve this problem, but it causes additional error in the threshold voltage. In order to reduce sensitivity to these short glitches without introducing hysteresis, the LTC2962 family low-pass filters the output of the first stage in the comparator. This filter integrates the output of the comparator before pulling the reset output low, dramatically reducing the effect of instantaneous glitches or noise. Only a transient with sufficient magnitude and duration at the input of the comparator will trigger the output logic. The Typical Performance Characteristics section shows a graph of the Transient Duration vs Comparator Overdrive. Unlike some other supply monitors, LTC2962 family transient duration is not sensitive to supply voltage $V_{CC}$ and thus leads to better predictability. The combination of the reset timeout and anti-glitch circuitry prevents spurious changes in output state without sacrificing threshold accuracy.

### Watchdog Timer (LTC2963)

Watchdog circuitry is used to ensure that the system is functioning properly by continuously monitoring microprocessor activity. The microprocessor is required to change the logic state of the WDI input periodically to clear the watchdog timer. The $C_{WT}$ timing capacitor adjusts the watchdog timeout period depending on the application and microprocessor requirements. If the software malfunctions and the state of WDI does not change properly, the watchdog times out and the $\overline{WDO}$ output is latched low. Simultaneously, $\overline{RST}$ is pulled low to reset the microprocessor. While $\overline{RST}$ is low, the WDI input does not affect $\overline{RST}$ or $\overline{WDO}$. The system therefore resets for at least $t_{RST}$.

After the configured reset timeout period, $t_{RST}$, $\overline{RST}$ goes back high and the microprocessor can poll the state of the $\overline{WDO}$ output to determine if the reset was caused by a voltage-based comparator event or by a watchdog fault. Following the rising edge of $\overline{RST}$, if $\overline{WDO}$ output is high, then the reset was caused by a voltage-based comparator event. If $\overline{WDO}$ output is low, then the system reset was caused by a watchdog fault. The rising edge of $\overline{RST}$ resets the watchdog timer, and the microprocessor can then issue a valid WDI input to clear the $\overline{WDO}$ latch. Please see the Initial Watchdog Timeout section for details on a valid WDI input following a reset. If the microprocessor fails to issue a valid WDI, the watchdog will timeout and behave as described above with the exception that the $\overline{WDO}$ output will already be low. Note manual reset has the same effect on watchdog function as comparator event.

The $\overline{RST}$ and $\overline{WDO}$ outputs should not be tied together to generate the master reset signal since a watchdog timeout forces $\overline{RST}$ low together with $\overline{WDO}$ and the master reset signal will remain low indefinitely.

LTC2963 provides traditional watchdog functionality with a constraint on the lower bound of the WDI input frequency.

### Selecting the Watchdog Timing Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog upper timeout, $t_{WDU}$, can be adjusted by connecting a capacitor, $C_{WT}$, between WT and ground. Given a specified watchdog timeout period, the capacitor is determined by:

$$C_{WT} = t_{WDU} \bullet 10\ [pF/ms]$$

The accuracy of the timeout period will be affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended. Leaving WT open will generate a minimum watchdog timeout of approximately 2ms. Connecting WT to $V_{CC}$ generates a fixed watchdog timeout of 1.6s.

### Initial Watchdog Timeout

Following a reset event, the microprocessor under supervision may require more time than usual to send valid watchdog edge transitions. In order for the microprocessor to have sufficient setup time to issue valid WDI inputs and avoid an unnecessary reset, the LTC2963 offers flexible adjustability for the initial watchdog timeout using the WDS input. The 3-state WDS input provides three different initial watchdog timeout periods immediately following a reset. Connecting the WDS input to ground sets the initial watchdog timeout, $t_{WD(INIT)}$ equal to the watchdog

## APPLICATIONS INFORMATION

upper timeout, $t_{WDU}$. Leaving WDS open sets the initial watchdog timeout to eight times the upper timeout, while connecting WDS to $V_{CC}$ sets it to sixty-four times the upper timeout.

**Table 6. Initial Watchdog Timeout Options with WDS**

| WDS | INITIAL WATCHDOG TIMEOUT $t_{WD(INIT)}$ |
|---|---|
| GND | $t_{WDU}$ |
| Open | $8 \cdot t_{WDU}$ |
| $V_{CC}$ | $64 \cdot t_{WDU}$ |

The rising edge of the $\overline{RST}$ output resets the watchdog timer and starts the initial watchdog timeout, $t_{WD(INIT)}$, and is the upper limit for a valid WDI input immediately following a rising edge of the $\overline{RST}$ output. If there is no valid WDI edge before $t_{WD(INIT)}$ expires, a typical watchdog fault occurs as described above in the Watchdog Timer section. When the initial watchdog timer is properly cleared by a valid WDI edge, the LTC2963 starts using the normal watchdog timer limits ($t_{WDU}$ for LTC2963).

### PCB Layout

The LTC2962 family is a precision device whose comparator thresholds are factory trimmed to ±0.5% accuracy as shown in the Typical Performance Characteristics section. The mechanical stress caused by soldering parts to a printed circuit board may cause the threshold to shift and the temperature coefficient to change. While every situation is different, expected errors due to these effects are likely to be on the order of 0.05%. To reduce the effects of stress-related shifts, mount the device near the short edge of a printed circuit board or in a corner. In addition, slots can be cut into the board on two sides of the device to reduce mechanical stress. A thicker and smaller board is stiffer and less prone to bend. Finally, use stress relief, such as flexible standoffs, when mounting the board.

To prevent interference, try to place the LTC2962 close to the device it monitors. For best accuracy, connect the channel voltage inputs (V1 ~ V4) directly to the supply pin of the device it monitors. This avoids possible voltage drop between the output of the power supply and the input supply of the device under supervision.

Careful attention to grounding is also important, especially when LTC2962 is sinking significant current through logic outputs or the REF output. The return load current can produce ground potential differences between LTC2962 and the device under supervision. This voltage difference may manifest as threshold hysteresis. Use a star ground connection and minimize the ground metal resistance, especially for applications where multiple devices are monitored. Figure 7 gives an example of the optimal layout practice for good voltage monitoring.

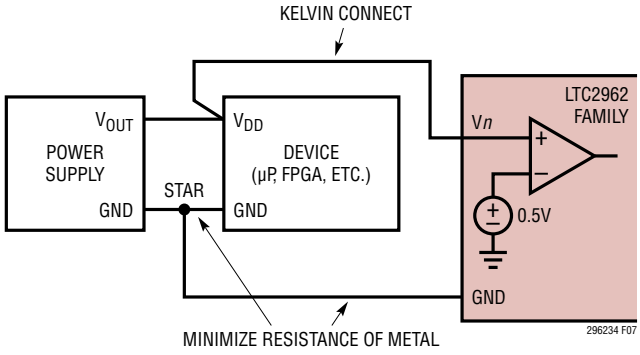
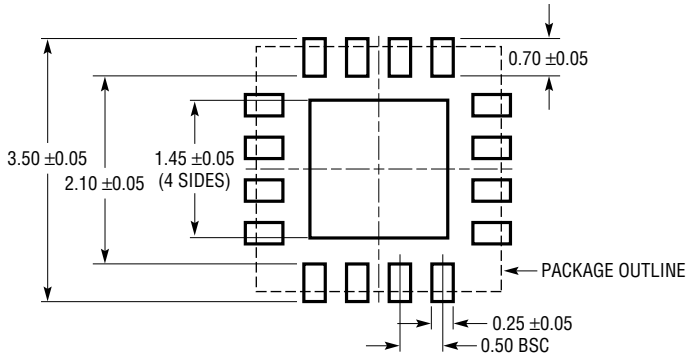


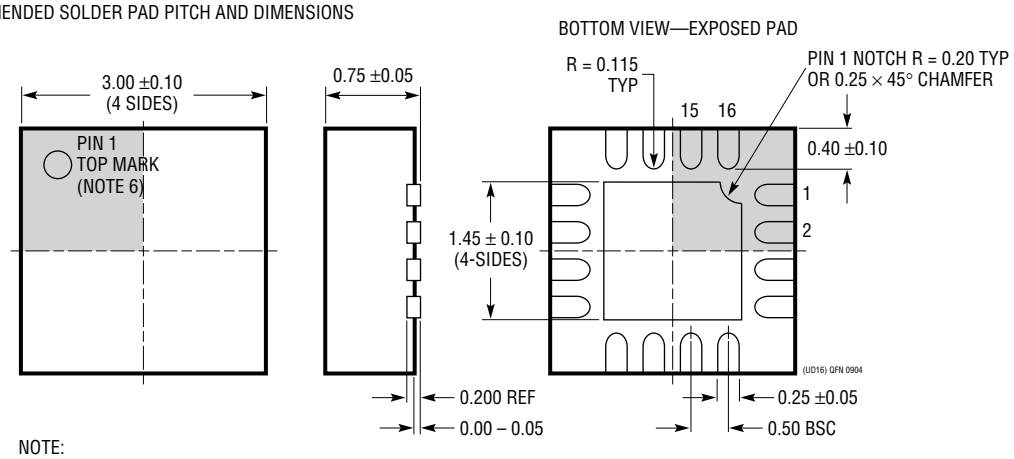

**Figure 7. Kelvin Connection for Good Voltage Monitoring**

# PACKAGE DESCRIPTION

**UD Package**
**16-Lead Plastic QFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1691 Rev Ø)



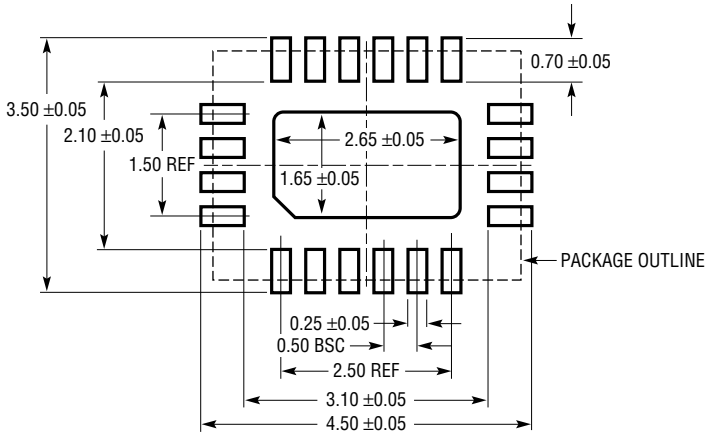

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



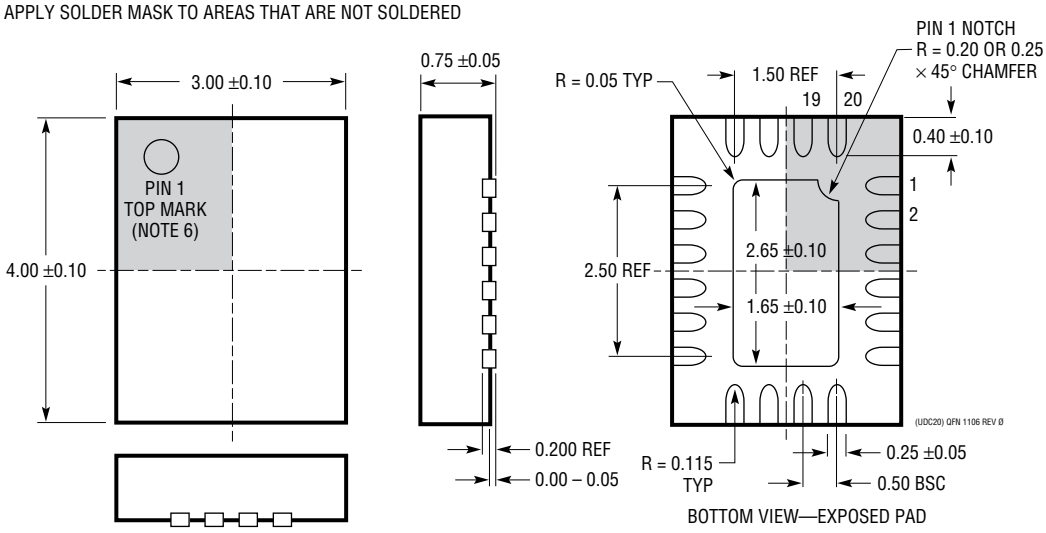

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**UDC Package**
**20-Lead Plastic QFN (3mm × 4mm)**
(Reference LTC DWG # 05-08-1742 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



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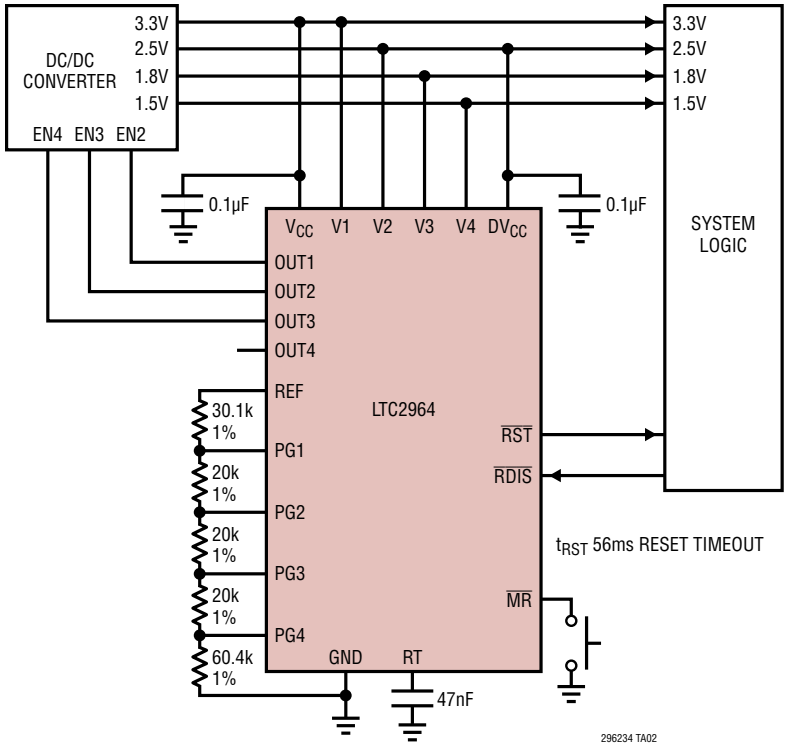
## TYPICAL APPLICATION

**Supervisor with Power-Up Sequence Function**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC2900/LTC2902 | Programmable Quad Supply Monitor | Adjustable Reset and Watchdog Timer, 10-Lead MSOP and DFN Packages |
| LTC2903-1 | Precision Quad Supply Monitor | 6-Lead SOT-23 Package |
| LTC2904/LTC2907 | Three-State Programmable Precision Dual Supply Monitor | 8-Lead SOT-23 and DFN Packages |
| LTC2908 | Precision Six Supply Monitor (Four Fixed and Two Adjustable) | 8-Lead TSOT-23 and DFN Packages |
| LTC2909 | Precision Triple/Dual Input UV, OV and Negative Voltage Monitor | Shunt Regulated $V_{CC}$ Pin, Adjustable Threshold and Reset, 8-Lead SOT-23 and DFN Packages |
| LTC2910 | Precision Octal Positive/Negative Voltage Supply Monitor | 16-Lead SSOP and 5mm × 3mm DFN Packages, H-Grade Temperature Range |
| LTC2912/LTC2914 | Single/Dual/Quad UV and OV Voltage Monitors | Separate $V_{CC}$ Pin, Adjustable Reset Timer, H-Grade Temperature Range |
| LTC2915/LTC2918 | Single Supply Monitor with 27 Pin-Selectable Thresholds | Manual Reset, Watchdog, TSOT-8/MSOP-10 and 3mm × 2mm DFN Packages, H-Grade Temperature Range |
| LTC2928 | Quad Power Supply Sequencer and Supervisor | Easily Configure Power Management without Software, 36-Lead |
| LTC2932 | Configurable Six Supply Monitor with Adjustable Reset Timer and Supply Tolerance | Selectable Supply Tolerance, 20-Lead TSSOP Package |
| LTC2938 | Configurable 4-Supply Monitors with Watchdog Timer | Adjustable Reset and Watchdog Timeout, 12-Lead MSOP and DFN Packages |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**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9