MICRF007

QwikRadio® Low-Power UHF Receiver

General Description

The MICRF007 is a single chip, ON-OFF Keyed (ASK/OOK) Receiver for remote wireless applications, employing Micrel's latest QwikRadio® technology. This device is a true "antenna-in to data-out" monolithic device. All RF and IF tuning is accomplished automatically within the IC, which eliminates manual tuning, and reduces production costs. The result is a highly reliable yet extremely low cost solution. The MICRF007 is an enhanced version of the MICRF002 and MICRF011.

The MICRF007 is a conventional superhetrodyne receiver, with an (internal) Local oscillator fixed at a single frequency based on an external reference crystal or clock. As with any conventional superhetrodyne receiver, the companion transmitter's frequency must be accurately controlled, generally with a crystal or SAW (surface acoustic wave) resonator.

The MICRF007 provides two enhancements over the MICRF001/011: (1) a Shutdown Mode, which may be used for duty-cycle operation, and (2) reduced current consumption. The MICRF007 requires a mere 2.3mA at 315MHz (3.8mA at 433.92MHz) when fully operational. These features make the MICRF007 ideal for low and ultra-low power applications, such as RKE and RFID.

All post-detection (demodulator) data filtering is provided on the MICRF007, so no external baseband filters are required. The demodulator filter bandwidth is fixed at 2.5kHz. Data rates up to 3.2kbps NRZ may be used.

All support documentation can be found on Micrel's web site at www.micrel.com.

QwikRadio®

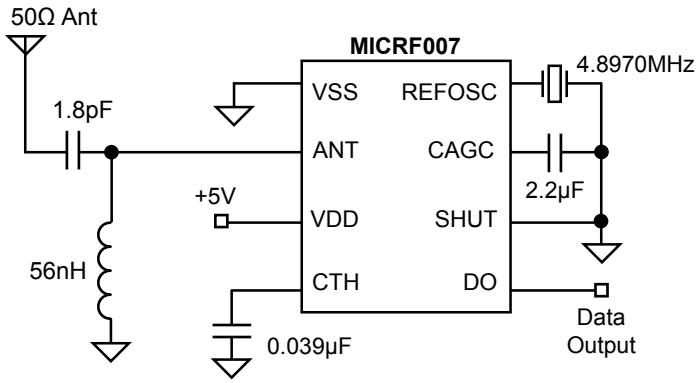
Features

- Complete UHF receiver on a monolithic chip
- 300MHz to 440MHz
- Data rates up to 3.2kbps NRZ
- Automatic tuning, no manual adjustment
- Low power consumption
  - 315MHz:
    - 2.3 mA fully operational
    - 0.5µA shutdown
    - 230µA polled at a 10:1 duty cycle ratio
  - 433.92MHz:
    - 3.8mA fully operational
    - 0.5µA shutdown
    - 380µA polled at a 10:1 duty cycle ratio
- Virtually no RF re-radiation at the antenna
- CMOS logic interface to standard decoder and microprocessor ICs
- Extremely low external part count
- No filters or inductors required

Applications

- Automotive remote keyless entry (RKE)
- Long range RF identification
- Remote fan and light control
- Garage door and gate openers

Typical Application



315MHz 1200b/s On-Off Keyed Receiver

QwikRadio is a trademark of Micrel, Inc. The QwikRadio ICs were developed under a partnership agreement with AIT of Orlando, Florida.

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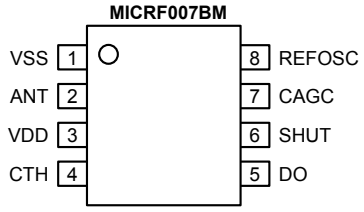
Ordering Information

Part Number		Junction Temp. Range	Package
Standard	Pb-Free		
MICRF007BM	MICRF007YM	–40°C to +85°C	8-pin SOIC

Pin Configuration



8-Pin SOIC (M)

Pin Description

Pin Number	Pin Name	Pin Function
1	VSS	Ground: Signal and power ground.
2	ANT	Antenna (Analog Input): High-impedance, internally AC-coupled receiver input. For optimal performance, the ANT pin should be impedance matched to the antenna.
3	VDD	Power Supply (Input): Positive supply input. Connect a low ESL, low ESR de-coupling capacitor from this pin to VSS. Lead lengths should be as short as possible.
4	CTH	Data Slicing Threshold Capacitor (Analog I/O): Capacitor connected to this pin extracts the DC average value from the demodulated waveform which becomes the reference for the internal data slicing comparator.
5	DO	Data Output (Digital Output): CMOS-level compatible data output signal.
6	SHUT	Shutdown (Digital Input): Shutdown-mode logic-level control input. Pull low to enable the receiver. Internally pulled-up to VDD.
7	CAGC	Automatic Gain Control (Analog I/O): Connect an external capacitor to set the attack/decay ratio of the on-chip automatic gain control.
8	REFOSC	Reference Oscillator: Timing reference, sets the RF receive frequency.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +7V
Input/Output Voltage ($V_{I/O}$) ..... V_{SS}–0.3 to V_{DD}+0.3
Junction Temperature (T_J) ..... +150°C
Storage Temperature Range (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +260°C
ESD Rating[3]

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... +4.75V to +5.5V
RF Frequency Range ..... 300MHz to 440MHz
Data Duty-Cycle ..... 20% to 80%
Reference Oscillator Input range ..... 0.1V_{PP} to 1.5V_{PP}
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
8-pin SOIC (θ_{JA}) ..... 120°C/W

Electrical Characteristics[4]

Power supply: +4.75V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V; C_{AGC} = 4.7µF, C_{TH} = 0.047µF; f_T = 6.7458MHz (equivalent of f_{RF} = 433.92MHz); data-rate = 600bps (Manchester encoded). T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; current flow into device pins is positive; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OP}	Operating Current at 315.0MHz	continuous operation		2.3	**3.5**	**mA**
		polled with 10:1 duty cycle		230		µA
	Operating Current at 433.92MHz	continuous operation		3.8	**5.7**	**mA**
		polled with 10:1 duty cycle		470		µA
I_{STBY}	Standby Current	V_{SHUT} = V_{DD}		0.9	**2**	µA
RF Section, IF Section						
	Receiver Sensitivity	f_{RF} = 433.92MHz, 1.2kbps		–99		dBm
f_{IF}	IF Center Frequency	**Note 7**		1.18		MHz
f_{BW}	IF Bandwidth	**Notes 6, 7**	0.4	0.70		MHz
	Maximum Receiver Input	Ref. Impedance = 50Ω		–20		dBm
	Spurious Reverse Isolation	ANT pin, Ref. Impedance = 50Ω[8]		30		µVrms
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$		10		
	AGC Leakage Current	T_A = +85°C		±50		nA
Reference Oscillator[9]						
	Reference Oscillator Stabilization Time	to 1% of final value		2.5		ms
Z_{REFOSC}	Reference Oscillator Input Impedance			290		kΩ
	Reference Oscillator Source Current			5.2		µA
Demodulator						
Z_{CTH}	C_{TH} Source Impedance	**Note 10**		110		kΩ
ΔZ_{CTH}	C_{TH} Source Impedance Variation		**–15**		**+15**	%
$I_{ZCTH(leak)}$	C_{TH} Leakage Current	T_A = +85°C		±50		nA
	Demodulator Filter Bandwidth	**Note 7**		2.5		kHz
Digital/Control Section						
$I_{IN(pu)}$	Input Pull-Up Current	V_{SHUT} = V_{SS}		8		µA
V_{IH}	Input High Voltage	V_{SHUT} = V_{SS}	**0.8V_{DD}**			V
V_{IL}	Input Low Voltage	V_{SHUT} = V_{SS}			**0.2V_{DD}**	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OH}	Output High Current			**20.8**		µA
I_{OL}	Output Low Current			**17.6**		µA
V_{OH}	Output High Voltage	DO, I_{OUT} = –1µA	**$0.9V_{DD}$**			V
V_{OL}	Output Low Voltage	DO, I_{OUT} = +1µA			**$0.1V_{DD}$**	V
t_R, t_F	Output Rise and Fall Times	DO, C_{LOAD} = 15pF		10		µs

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are E
   MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.
4. Specification for packaged product only.
5. Sensitivity is defined as the average signal level, measured at the input, necessary to achieve 10^{-2} BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded data) at a data rate of 600bps. The RF input is assumed to be matched into 50Ω.
6. Sensitivity, a commonly specified receiver parameter, provides an indication of the receiver's input referred noise, generally input thermal noise. However, it is possibl
   noise is appreciab

   A better indicator of achievable receiver range performance is usually given by its selectivity, often stated as intermediate frequency (IF) or radio frequency (RF) bandwidth, depending on receiver topology. Selectivity is a measure of the rejection by the receiver of ambient noise. More selective receivers will almost inva -
   ally thermal will the receiver demonstrate sensitivity-limited performance.
7. Parameter scales linearly with reference oscillator frequency f_T. For any reference oscillator frequency other than 6.7458MHz, compute the parameter value as the ratio:

   $$\frac{f_T MHz}{6.7458} \times (\text{parameter value at 6.7458MHz})$$

   Example: For reference oscillator freqency f_T = 6.00MHz:

   $$(\text{parameter value at 6.00MHz}) = \frac{6.7458}{6.00} \times (\text{parameter value at 6.7458MHz})$$
8. Spurious reve -
   ing network.
9. Series resistance
   resistance is too great, the oscillator may oscillate at a diminished peak-to-peak level, or may fail to oscillate entirely. Micrel recommends that series resistances for ceramic resonators and crystals not exceed 50Ω and 100Ω respectively. Refer to "Application Hint 35" for crystal recommendations.
10. **Parameter scales inversely with reference oscillator frequency f_T**. For any reference oscillator frequency other than 6.7458MHz, compute the parameter value as the ratio:

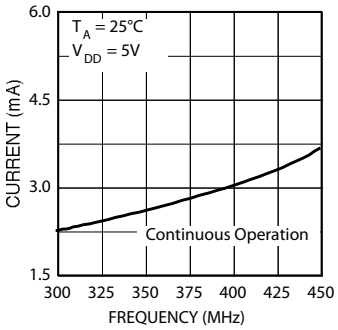
    $$\frac{6.7458}{f_T MHZ} \times (\text{parameter value at 6.7458MHz})$$

    Example: For reference oscillator frequency f_T = 6.00MHz:

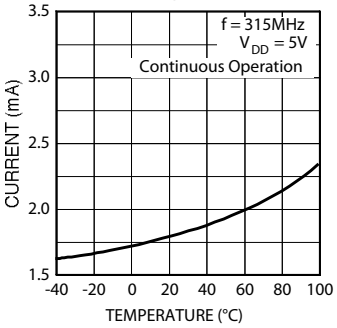
    $$(\text{parameter value at 6.00MHz}) = \frac{6.7458}{6.00} \times (\text{parameter value at 6.7458MHz})$$

Typical Characteristics

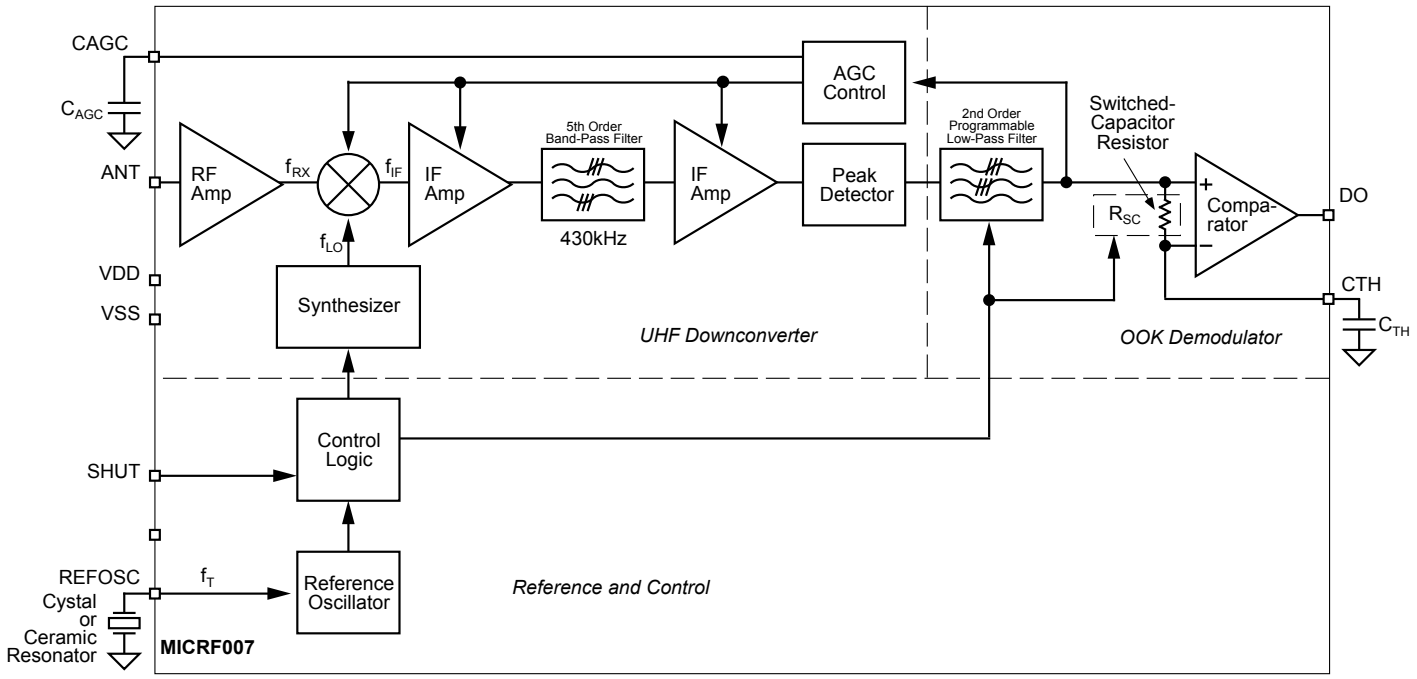
Supply Current
vs. Frequency



Supply Current
vs. Temperature



Functional Diagram



MICRF007 Block Diagram

Applications Information and Functional Description

Refer to the functional diagram. Three sections of the IC are identified: UHF Down-converter, OOK Demodulator and Reference and Control. Also shown are two capacitors (CTH, CAGC) and one timing component (Y1), usually a crystal. With the exception of a supply decoupling capacitor, these are the only external components needed by the MICRF007 to assemble a complete UHF receiver.

For optimal performance, MICRF007 input impedance must be matched to the antenna impedance. The matching network will add an additional two or three components.

There is one control input, SHUT pin. The SHUT function is used to enable the receiver. This input is CMOS compatible, and is pulled-up on the IC.

Roll-off response of the IF Band-Pass Filter is 5th order, while the demodulator data filter exhibits a 2nd order response.

The MICRF007 is a standard super-heterodyne receiver with a narrow IF filter bandwidth of 700kHz. It is less susceptible to interfering RF signals. The MICRF007 RF center frequency is controlled by an integrated PLL/VCO frequency synthesizer, which is locked to the reference oscillator frequency, typically set by a crystal. A tight tolerance transmitter such as SAW or crystal-based transmitters must be used for the system.

The MICRF007 has a fully integrated base-band demodulator filter. The filter has a fixed 2.5kHz bandwidth and exhibits a 2nd order response. This filter limits the receiver raw data rate to 3.2Kbps NRZ.

Design Steps

The following steps are the basic design steps for using the MICRF007 receiver:

1. Select the reference oscillator
2. Select the C_{TH} capacitor
3. Select the C_{AGC} capacitor

Step 1: Selecting Reference Oscillator

All timing and tuning operations on the MICRF007 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of two ways:

1. Connect a crystal.
2. Drive this pin with an external timing signal.

The specific reference frequency required is related to the system transmit frequency.

Crystal Selection

Care should be taken to ensure low ESR crystals are selected. “Application Hint 35” provides additional information and recommended sources for crystals.

When a crystal is used, the minimum voltage is $300mV_{PP}$. If using an externally applied signal, it should be AC-coupled and limited to the operating range of $0.1V_{PP}$ to $1.5V_{PP}$.

Selecting Reference Oscillator Frequency f_T

As with any super-heterodyne receiver, the difference between the internal local oscillator (LO) frequency f_{LO} and

the incoming transmit frequency f_{TX} should equal the IF center frequency. Equation 1 may be used to compute the

appropriate f_{LO} for a given f_{TX}:

$$f_{LO} = f_{TX} \pm \left(1.18 \frac{f_{TX}}{433.92}\right) \quad (1)$$

Frequencies f_{TX} and f_{LO} are in MHz. Note that two values of f_{LO} exist for any given f_{TX}, distinguished as "high-side mixing" and "low-side mixing." High-side mixing results in an image frequency above the frequency of interest and low-side mixing results in a frequency below. There is generally no preference of one over the other.

After choosing one of the two acceptable values of f_{LO}, use Equation 2 to compute the reference oscillator frequency f_T:

$$f_T = \frac{f_{LO}}{64.5} \quad (2)$$

Frequency f_T is in MHz. Connect a crystal of frequency f_T to REFOSC on the MICRF007. Four-decimal-place accuracy on the frequency is generally adequate. The following table identifies f_T for some common transmit frequencies.

Transmit Frequency f_{TX}	Reference Oscillator Frequency f_T
315MHz	4.8970MHz
390MHz	6.0630MHz
418MHz	6.4983MHz
433.92MHz	6.7458MHz

Table 2. Recommended Reference Oscillator Values for Typical Transmit Frequencies (high-side mixing)

Step 2: Selecting C_{TH} Capacitor

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip switched capacitor "resistor" RSC, shown in the block diagram.

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms.This issue is covered in more detail in "Application Note 22." Optimization of the value of C_{TH} is required to maximize range.

τ of 5x the bit-rate is recommended. The effective resistance of RSC is listed in the electrical characteristics table as 110kΩ at 433.92MHz, This value scales inversely with frequency. Source impedance of the C_{TH} pin at other frequencies is given by equation (3), where f_T is in MHz:

$$RSC = 110k\Omega \frac{6.7458}{f_T} \quad (3)$$

Since slicing level time constant τ has been established as 5 times bit rate, capacitor C_{TH} may be computed using equation (4),

$$C_{TH} = \frac{\tau}{R_{SC}} \quad (4)$$

A standard ±20% X7R ceramic capacitor is generally sufficient. Refer to "Application Hint 42" for C_{TH} and C_{AGC} selection examples.

Step 3: Selecting C_{AGC} Capacitor

The signal path has automatic gain control (AGC) to increase input dynamic range. The attack time constant of the AGC is set externally by the value of the C_{AGC} capacitor connected to the C_{AGC} pin of the device. To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under $10mV_{PP}$ once the control voltage has attained its quiescent value. For this reason, capacitor values of at least 0.47µF are recommended.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF007. When the device is placed into shutdown mode (SHUT pin is pulled high), the AGC capacitor floats to retain the voltage. When operation is resumed, only the voltage droop due to capacitor leakage must be replenished. A relatively low-leakage capacitor is recommended when the devices are used in duty-cycled operation.

To further enhance duty-cycled operation, the AGC push and pull currents are boosted for approximately 10ms immediately after the device is taken out of shutdown. This compensates for AGC capacitor voltage droop and reduces the time to restore the correct AGC voltage. The current is boosted by a factor of 45.

Selecting C_{AGC} Capacitor in Continuous Mode

A C_{AGC} capacitor in the range of 0.47µF to 4.7µF is typically recommended. **Caution! If the capacitor is too large, the AGC may react too slowly to incoming signals. AGC settling time from a completely discharged (zero-volt) state is given approximately by this equation:**

$$\Delta t = 1.333 \times C_{AGC} - 0.44 \quad (5)$$

where:

C_{AGC} is in µF, and Δt is in seconds.

Selecting C_{AGC} Capacitor in Duty-Cycle Mode

Voltage droop across the C_{AGC} capacitor during shutdown should be replenished as quickly as possible after the IC is enabled. As mentioned above, the MICRF007 boosts the push-pull current by a factor of 45 immediately after start-up. This fixed time period is based on the reference oscillator frequency f_T. The time is 10.9ms for f_T = 6.00MHz, and varies inversely with f_T. The value of C_{AGC} capacitor and the duration of the shutdown time period should be selected such that the droop can be replenished within this 10ms period.

Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. The worst-case from a recovery standpoint is downward droop, since the AGC pull-up current is 1/10th magnitude of the pull-down current. The downward droop is replenished according to the Equation 6:

$$C_{AGC} = \frac{I\Delta t}{\Delta V} \quad (6)$$

where:

I = AGC pull-up current for the initial 10ms (67.5µA)
CAGC = AGC capacitor value
Δt = droop recovery time

ΔV = droop voltage

For example, if user desires Δt = 10ms and chooses a 4.7µF C_{AGC}, then the allowable droop is about 144mV. Using the same equation with 200nA, the worst case pin leakage, and assuming 1µA of capacitor leakage in the same direction, the maximum allowable Δt (shutdown time) is about 0.56s for droop recovery in 10ms.

The ratio of decay-to-attack time-constant is fixed at 1:10 (that is, the attack time constant is 10 times of the delay time constant). Generally, the design value of 1:10 is adequate for the vast majority of applications. If adjustment is required, adding a resistor in parallel of the C_{AGC} capacitor may vary the ratio. The value of the resistor must be determined on a case by case basis.

Additional Applications Information

In addition to the basic operation of the MICRF007, the following enhancements can be made. In particular, it is strongly recommended that the antenna impedance is matched to the input of the IC.

Antenna Impedance Matching

As shown in Figure 2 and Table 3, the antenna pin input impedance is frequency dependent.

The ANT pin can be matched to 50Ω with a high pass circuit as shown in Figure 3. That is, a shunt inductor from the antenna input to ground and a capacitor in series from the antenna input to the ANT pin.

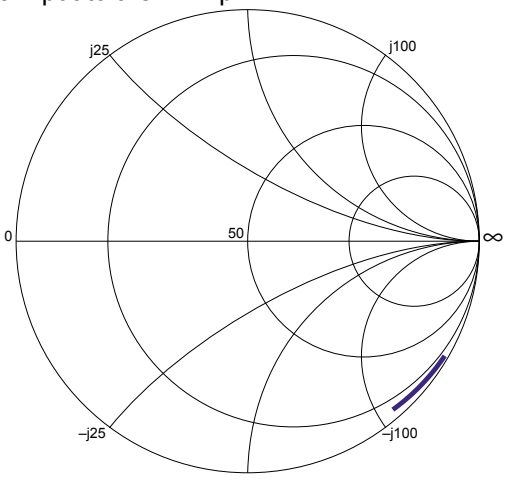


Figure 2. Impedance Looking into Antenna Pin

Frequency (MHz)	Z_{IN}(Ω) Z11	S11	C_{SERIES} (pF)	L_{SHUNT} (nH)
300	12– j166	0.803– j0.529	1.5	62
305	12– j165	0.800– j0.530	1.4	62
310	12 – j163	0.796– j0.536	1.6	56
315	13 – j162	0.791– j0.536	1.5	56
320	12 – j160	0.789– j0.543	1.4	56
325	12 – j157	0.782– j0.550	1.7	51
330	12 - j155	0.778– j0.556	1.5	51
335	12 – j152	0.770– j0.564	1.4	51
340	11 - j150	0.767– j0.572	1.6	47
345	11 – j148	0.762– j0.578	1.5	47
350	11 – j145	0.753– j0.586	1.4	47
355	11 – j143	0.748– j0.592	1.6	43
360	11 – j141	0.742– j0.597	1.5	43
365	11 – j139	0.735– j0.603	1.4	43
370	10 – j137	0.732– j0.61	1.3	43
375	10 – j135	0.725– j0.619	1.6	39
380	10 – j133	0.718– j0.625	1.4	39
385	10 – j131	0.711– j0.631	1.3	39
390	10 – j130	0.707– j0.634	1.2	39
395	10 – j128	0.700– j0.641	1.5	36
400	10 – j126	0.692– j0.647	1.4	36
405	10 – j124	0.684– j0.653	1.2	36
410	10 – j122	0.675– j0.660	1.5	33
415	10 – j120	0.667– j0.667	1.4	33
420	10 – j118	0.658– j0.673	1.3	33
425	10 – j117	0.653– j0.677	1.6	30
430	10 – j115	0.643– j0.684	1.5	30
435	10 – j114	0.638– j0.687	1.4	30
440	8 – j112	0.635– j0.704	1.2	30

Table 4. Input Impedance vs. Frequency

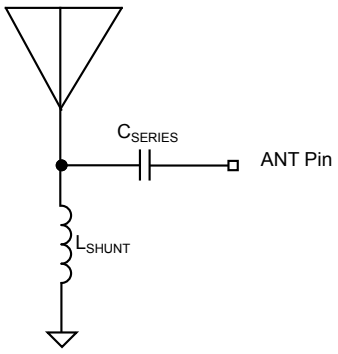


Figure 3. Antenna Impedance Matching Network

Inductor values may be different from Table 4, depending on PCB material, PCB thickness, ground configuration, and how long the traces are in the layout. Values shown were charac-terized for a 0.031 inch thickness, FR4 board, solid ground plane on bottom layer, and very short traces. Murata and Coilcraft wire-wound 0603 or 0805 surface mount inductors were tested, however, any wire-wound inductor with high SRF (self-resonance frequency) should do the job.

Shutdown Function

Duty-cycled operation of the MICRF007 (often referred to as polling) is achieved by turning the MICRF007 on and off via the SHUT pin. The shutdown function is controlled by a logic state applied to the SHUT pin. When V_{SHUT} is high, the device goes into low-power standby mode. This pin is pulled high internally, it must be externally pulled low to enable the receiver. It is recommended to connect this pin through a 100kΩ resistor to ground

Power Supply Bypass Capacitors

Power supply bypass capacitor(s) connected to V_{DD} should have the shortest possible lead lengths to V_{SS}.

Increasing Selectivity with Optional Band-Pass Filter

For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and V_{SS} to provide additional receiver selectivity and input overload protection. A minimum input configuration is included in Figure 10. It provides some filtering and necessary overload protection.

Data Squelching

During quiet periods (no signal), the data output (DO pin) transitions randomly with noise. Most decoders can discriminate between this random noise and actual data. But for some system, it does present a problem. There are three possible approaches to reduce this output noise:

1. Analog squelch to raise the demodulator threshold
2. Digital squelch to disable the output when data is not present
3. Output filter to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is to add analog squelch by introducing a small offset, or squelch voltage, on the C_{TH} pin so that noise does not trigger the internal comparator. Usually 20mV to 30mV is sufficient, and may be achieved by connecting a several-meg-ohm resistor from the C_{TH} pin to either V_{SS} or V_{DD}, depending on the desired offset polarity. Since MICRF007's receiver AGC noise at the internal comparator input is always the same (set by the AGC), the squelch offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce sensitivity and also reduce range. Only introduce an amount of offset sufficient to quiet the output. Typical squelch resistor values range from 10MΩ to 6.8MΩ for low to high squelch strength.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF007 are diagrammed in Figures 4 through 9. The ESD protection diodes at all input and output pins are not shown.

ANT Pin

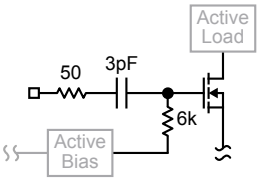


Figure 4. ANT Pin

The ANT pin is internally AC-coupled via a 3pF capacitor to an RF N-Channel MOSFET, as shown in Figure 4. Im-pedance on this pin to VSS is quite high at low frequencies, and decreases as frequency increases. In the UHF fre-quency range, the device input can be modeled as 6.3k. in parallel with 2pF (pin capacitance) to V_{SS}.

C_{TH} Pin

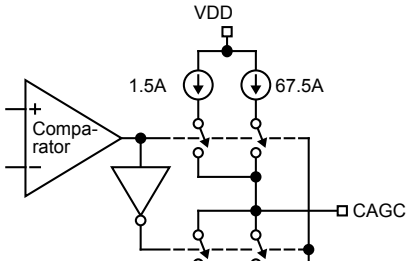


Figure 5. C_{TH} Pin

Figure 5 illustrates the C_{TH}-pin interface circuit. The C_{TH} pin is driven from a P-Channel MOSFET source-follower with approximately 10µA of bias. Transmission gates TG1 and TG2 isolate the 6.9pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a "resistance" of approximately 110kΩ. The DC potential at the C_{TH} pin is approximately 1.6V

C_{AGC} Pin

Figure 6 illustrates the C_{AGC} pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor C_{AGC}. The attack current is nominally 1.5µA, while the decay current is a 10 times scaling of this, approximately 15µA. Signal gain of the RF/IF strip inside the IC diminishes as the voltage on C_{AGC} decreases. By simply adding a capacitor to C_{AGC} pin, the attack/decay time constant ratio is fixed at 10:1. Modification of the attack/decay ratio is possible by adding resistance from the C_{AGC} pin to either VDD or VSS, as desired.

Both the push and pull current sources are disabled during shutdown, which maintains the voltage across C_{AGC}, and improves recovery time in duty-cycled applications. To further improve duty-cycle recovery, both push and pull currents are increased by 45 times for approximately 10ms after release of the SHUT pin. This allows rapid recovery of any voltage drop on C_{AGC} while in shutdown.

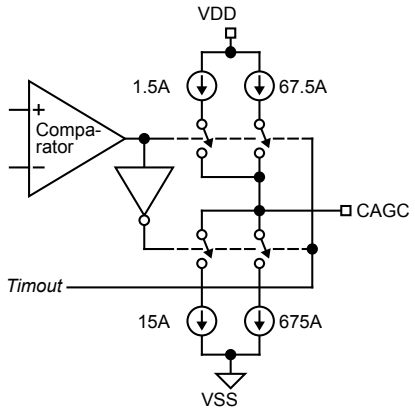


Figure 6. C_{AGC} Pin

DO Pin

The output stage for the digital output (DO) in Figure 7. The output is a 20µA push and 18µA pull switched-current stage. This output stage is capable of driving CMOS loads. An external buffer-driver is recommended for driving high capacitance loads.

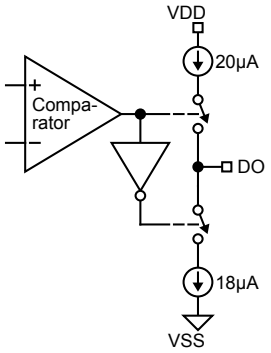


Figure 7. DO Pin

REFOSC Pin

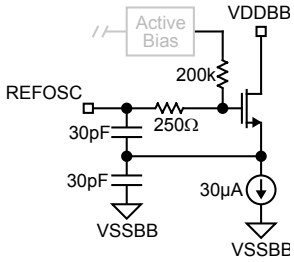


Figure 8. REFOSC Pin

The reference oscillator (REFOSC) input circuit is shown in Figure 8. Input impedance is high (290kΩ). This is a Colpitts oscillator with internal 30pF capacitors. This input is intended to work with standard crystal connected from this pin to the VSS pin. The nominal DC bias voltage on this pin is 1.4V.

SHUT Pin

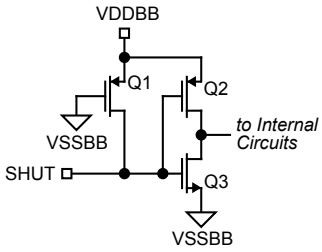


Figure 9. SHUT Pin

Control input circuitry is shown in Figure 9. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-Channel MOSFET Q1 is a large channel length device, which functions essentially as a “weak” pull-up to VDD. Typical pull-up current is 5µA.

Application Example

315MHz Receiver/Decoder Application

Figure 10 illustrates a typical application for the MICRF007 UHF Receiver IC. This receiver operates continuously (not duty cycled) in fixed-mode, and features 6-bit address decoding and two output code bits.

Operation in this example is at 315MHz, and may be customized by selection of the appropriate frequency reference (Y1), and adjustment of the antenna length. Changes from the 1Kbps data rate may require a change in the value of R1. A bill of materials accompanies the schematic.

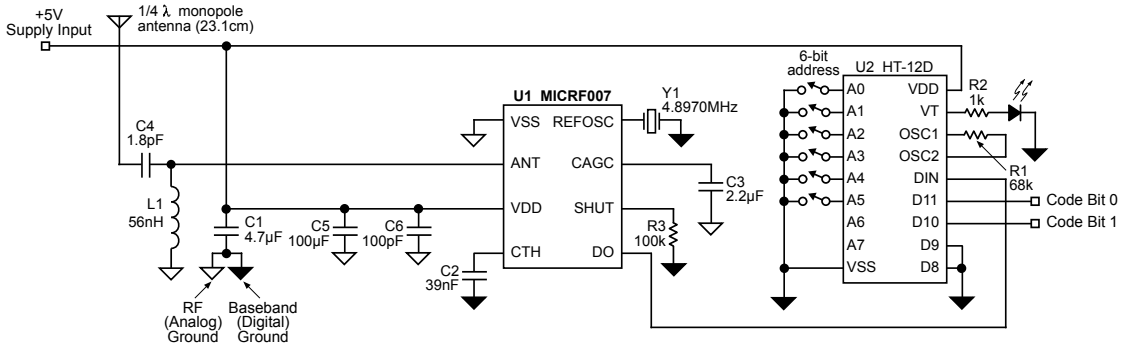


Figure 10. 315MHz, 1Kbps On-Off Keyed Receiver with Decoder

Bill of Materials

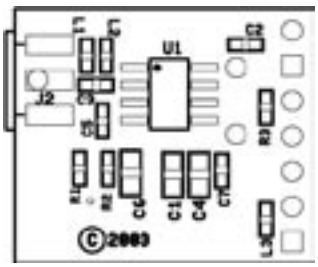
Item	Part Number	Manufacturer	Description	Qty.
C1	GRM21BF51A475ZA01L	Murata(7)	4.7µF Y5V	1
C2	VJ0603Y393KXXA	Vishay(1)	39nF	1
C3	GRM188R61A225XE348	Murata(7)	2.2µF X5R	1
C4	GRM1885C1H1R8CZ01B	Murata(7)	1.8pF COG ceramic capacitor	1
C5	GRM188R71E104KA01B	Murata(7)	100nF capacitor	1
C6	GRM1885C1H101JA01B	Murata(7)	100pF capacitor	1
D1	SSF-LX100LID	Lumex(2)	red LED	1
L1	0603CS-56NX-B	Coilcraft(6)	56mH wire wound, Q=38	1
R1	CRCW06036812F	Vishay(1)	68k; 1/4W; 5%	1
R2	CRCW06031001F	Vishay(1)	1k; 1/4W; 5%	1
R3	CRCW06031003F	Vishay(1)	100k	1
U1	MICRF007BM	Micrel(3)	UHF Reciever	1
U2	HT-12D	Holtek(4)	Logic decoder	1
Y1	AB-4.8970MHZ-20-D	Abracon(5)	4.8970MHz crystal	1

Notes:

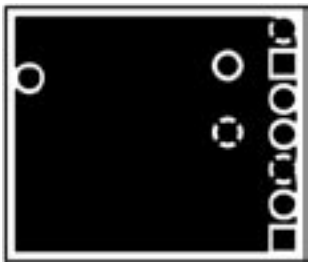
1. Vishay, tel. (203) 268-6261
2. Lumex, tel. (800) 278-5666
3. Micrel Inc., tel (408) 944-0800
4. Holteck, tel (408) 894-9046
5. Abracon, tel. (949) 448-7070
6. Coilcraft, tel. (510) 814-8954
7. Murata, tel (408) 397-1284

PCB Layout Information

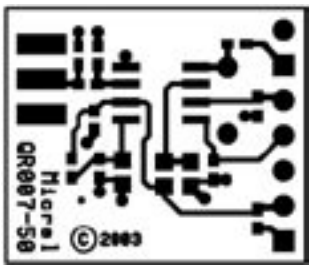
The MICRF007 evaluation board was designed and characterized using double sided 0.031 inch thick FR4 material with 1 ounce copper clad. If another type of printed circuit board material is substituted, impedance matching and characterization data may not be as stated in this document.



PCB Silk Screen



PCB Component Side Layout



PCB Solder Side Layout

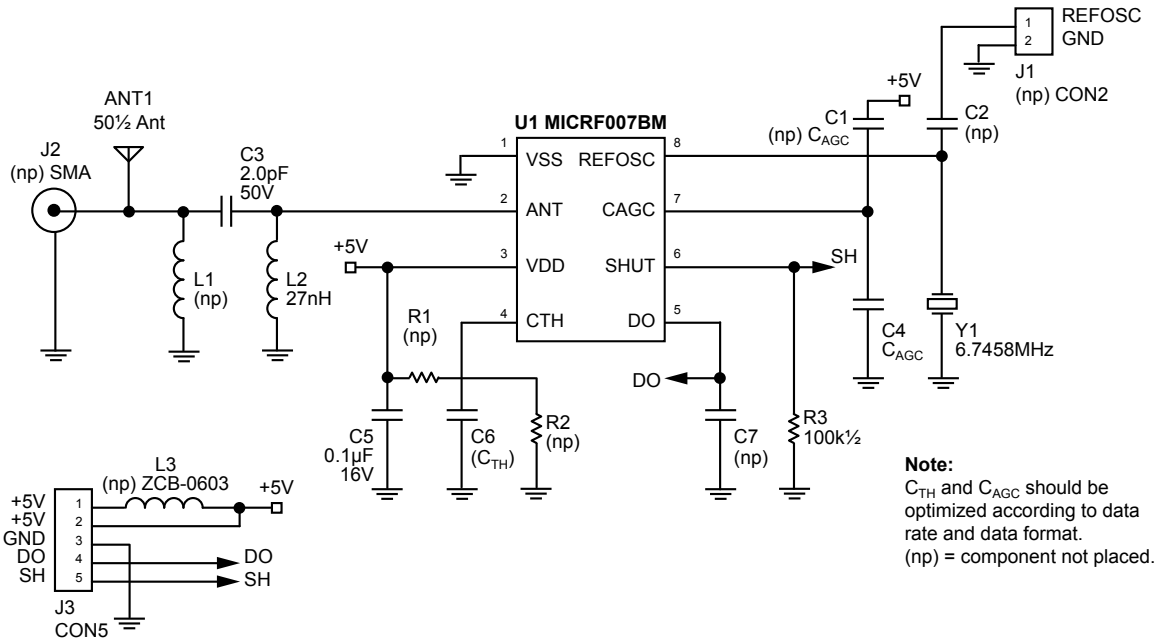
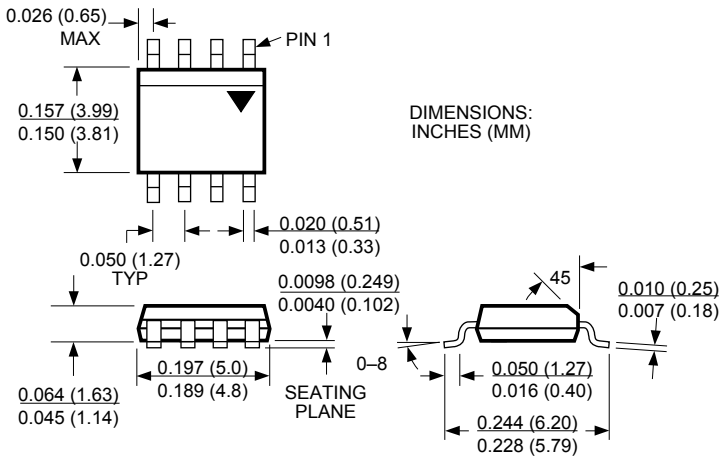


Figure 11. 433.92MHz Schematic QR007-50-433

Package Information



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