



PMH950UPE

20 V, P-channel Trench MOSFET

5 April 2019

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN0606-3 (SOT8001) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 1 kV HBM
- Leadless ultra small and ultra thin SMD plastic package: 0.62 × 0.62 × 0.37 mm

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

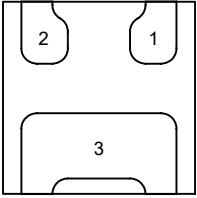
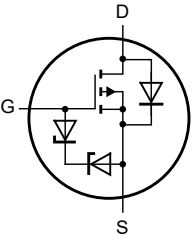
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V
V _{GS}	gate-source voltage			-8	-	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-	-530	mA
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -500 mA; T _j = 25 °C		-	1	1.4	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN0606-3 (SOT8001)	 017aaa259
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMH950UPE	DFN0606-3	plastic, leadless ultra small package; 3 terminals; body 0.62 x 0.62 x 0.37 mm	SOT8001

7. Marking

Table 4. Marking codes

Type number	Marking code
PMH950UPE	0001 0100

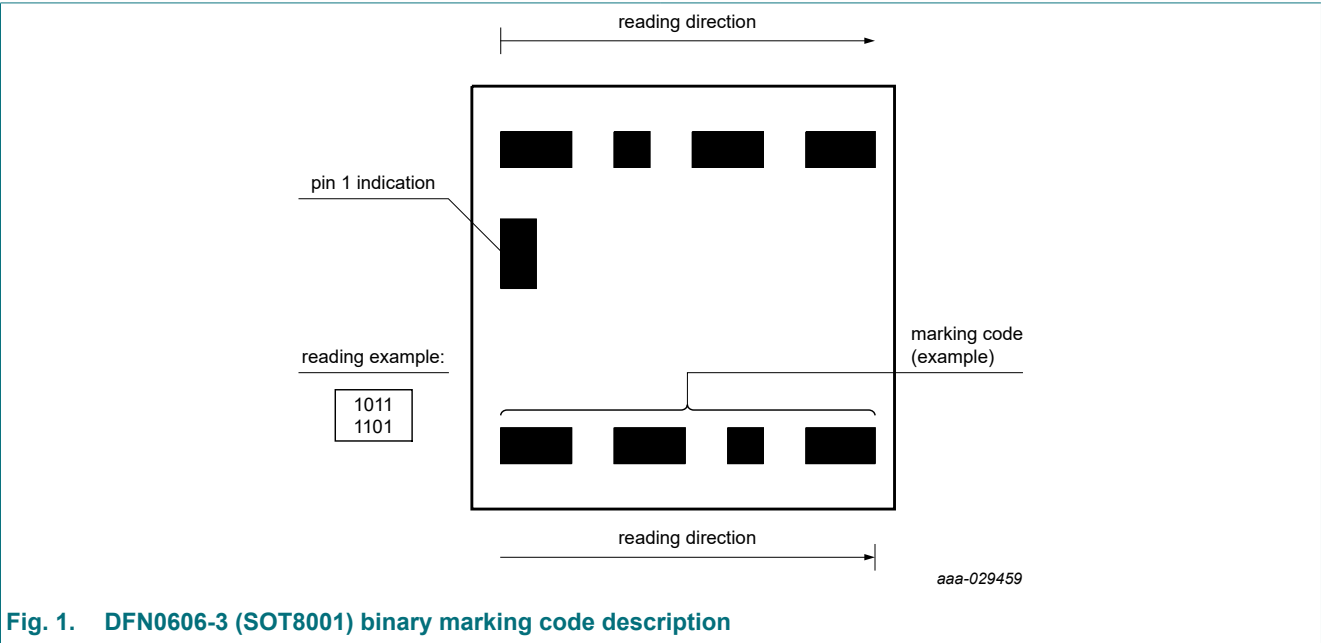


Fig. 1. DFN0606-3 (SOT8001) binary marking code description

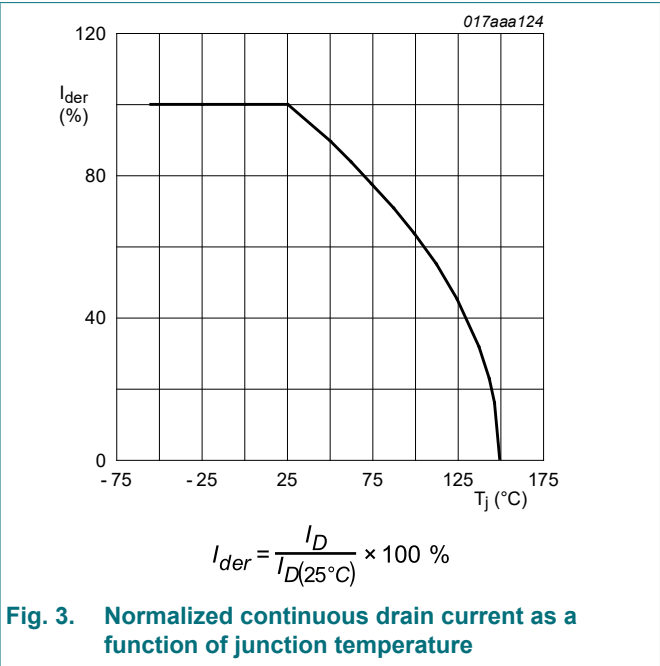
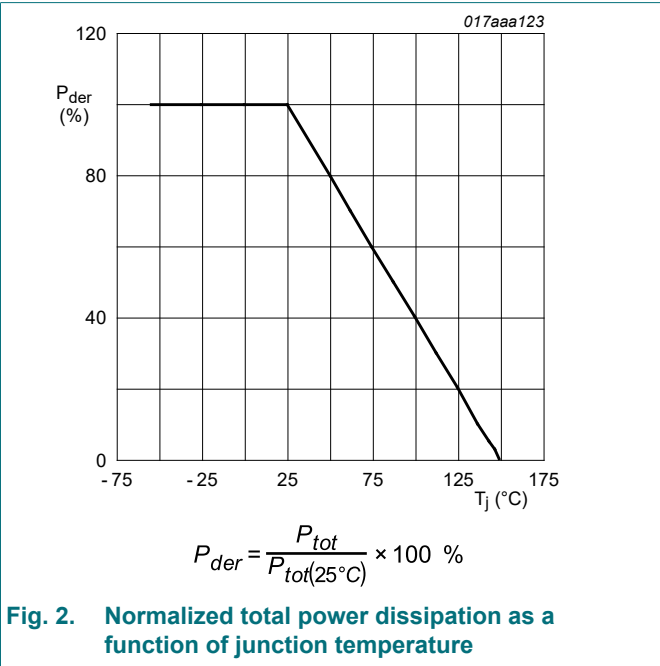
8. Limiting values

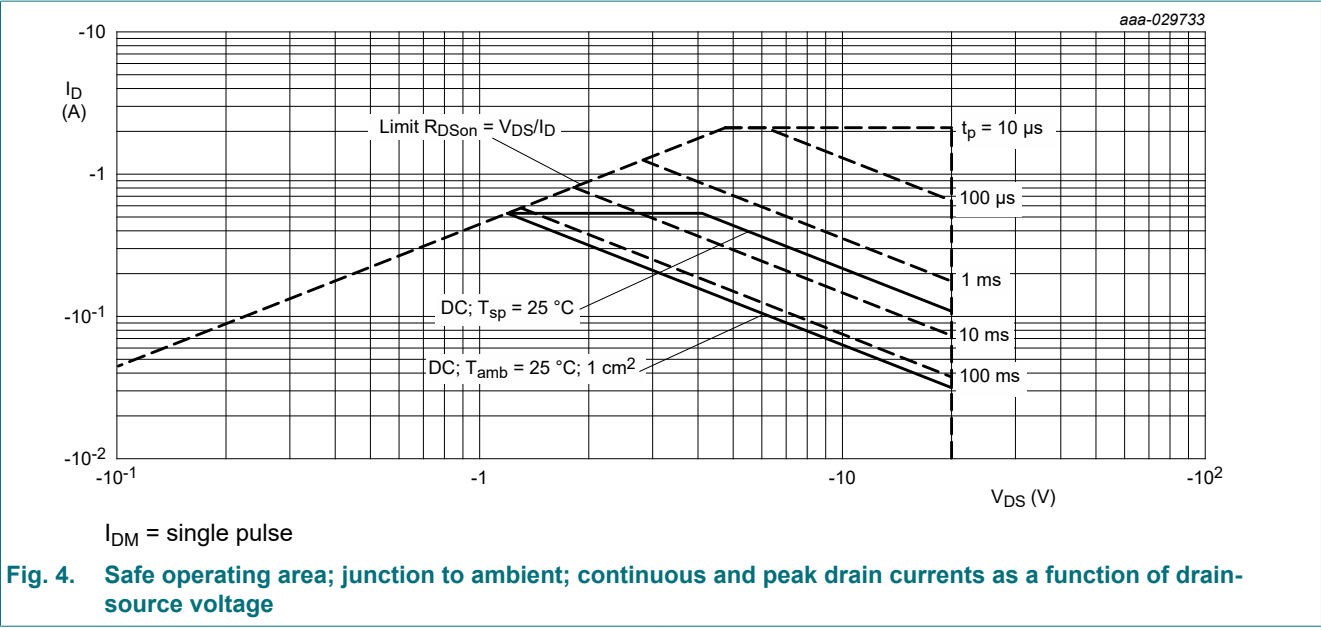
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-530	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-360	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	370	mW
			[1]	-	625	mW
		T _{sp} = 25 °C		-	2.2	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-530	mA

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	300	340	K/W
			[2]	-	175	200	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	50	58	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

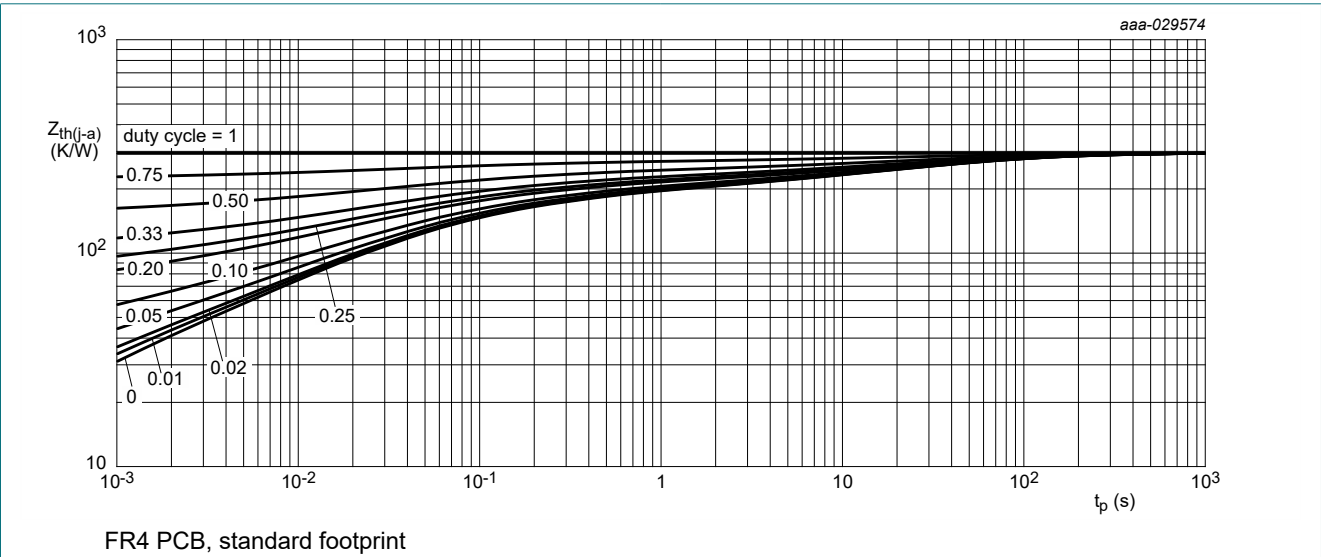


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

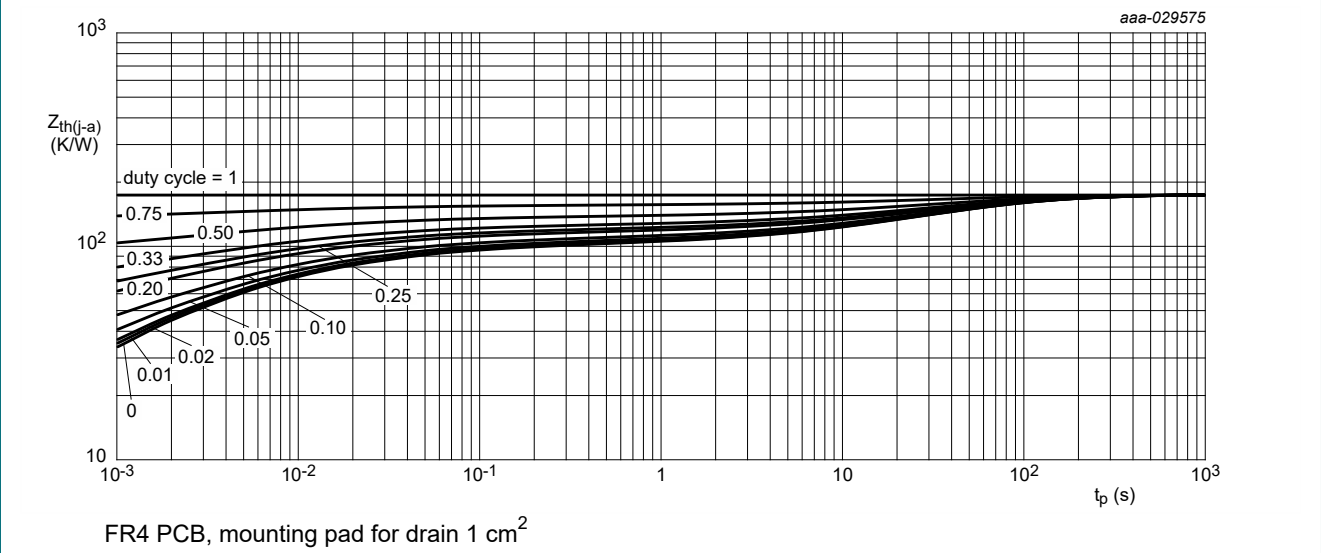


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-0.45	-0.7	-0.95	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{GS} = 2.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
		V _{GS} = -2.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -500 mA; T _j = 25 °C		-	1	1.4	Ω
		V _{GS} = -4.5 V; I _D = -500 mA; T _j = 150 °C		-	1.6	2.3	Ω
		V _{GS} = -2.5 V; I _D = -200 mA; T _j = 25 °C		-	1.4	2.2	Ω
		V _{GS} = -1.8 V; I _D = -40 mA; T _j = 25 °C		-	1.8	3.3	Ω
		V _{GS} = -1.5 V; I _D = -40 mA; T _j = 25 °C		-	2.1	5.5	Ω
		V _{GS} = -1.2 V; I _D = -10 mA; T _j = 25 °C		-	2.9	-	Ω
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -600 mA; T _j = 25 °C		-	700	-	mS
R _G	gate resistance	f = 1 MHz		-	3.7	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -600 mA; V _{GS} = -4 V; T _j = 25 °C		-	0.29	0.5	nC
Q _{GS}	gate-source charge			-	0.08	-	nC
Q _{GD}	gate-drain charge			-	0.08	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	36	-	pF
C _{oss}	output capacitance			-	6.3	-	pF
C _{rss}	reverse transfer capacitance			-	4.7	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -600 mA; V _{GS} = -4 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	1	-	ns
t _r	rise time			-	2	-	ns
t _{d(off)}	turn-off delay time			-	4	-	ns
t _f	fall time			-	6	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -600 mA; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V

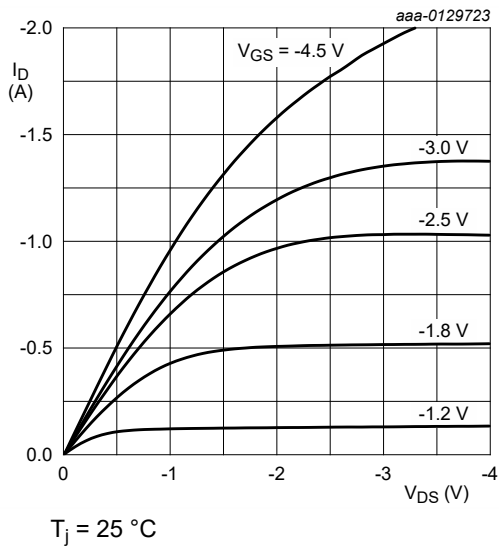


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

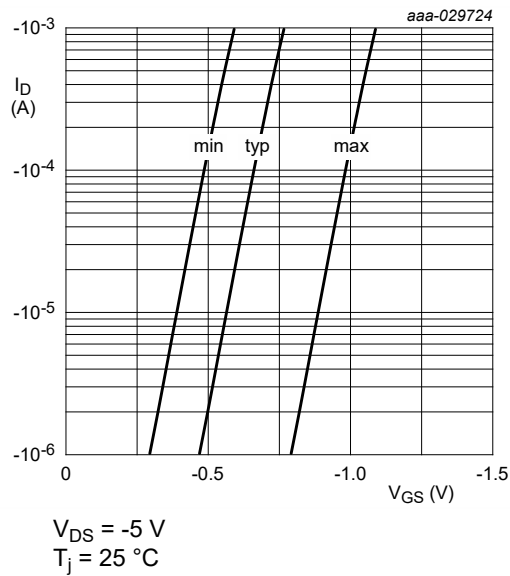


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

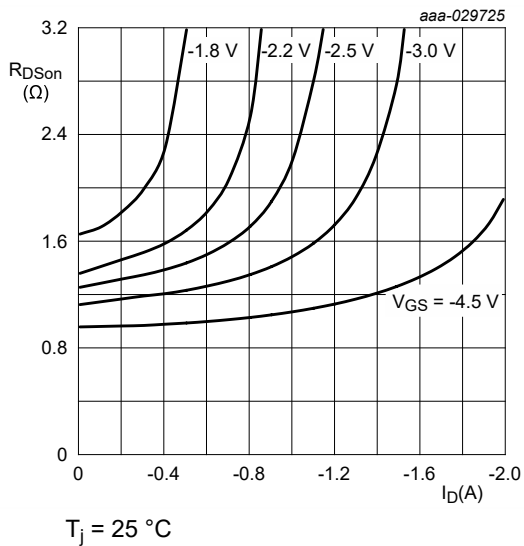


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

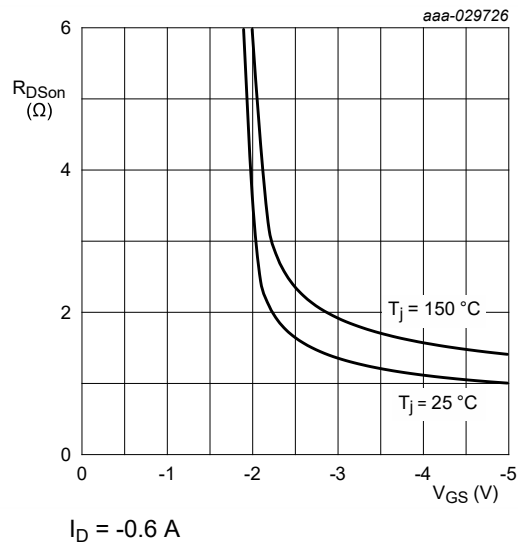


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

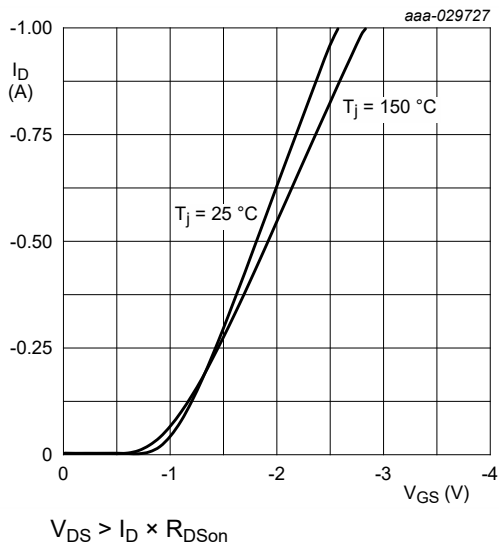


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

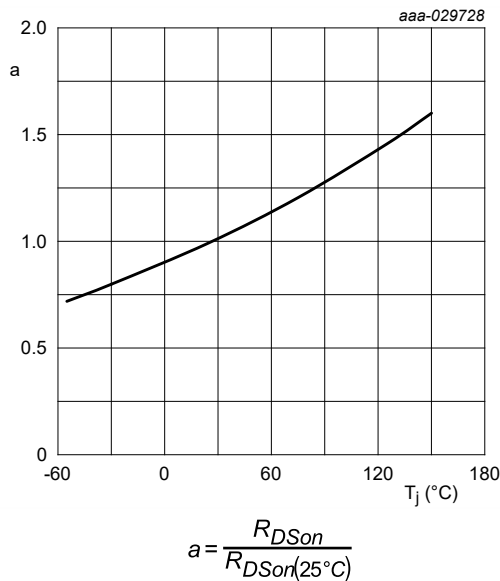


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

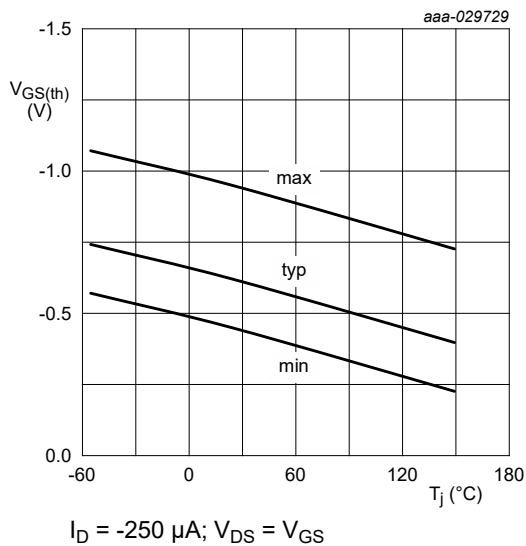


Fig. 13. Gate-source threshold voltage as a function of junction temperature

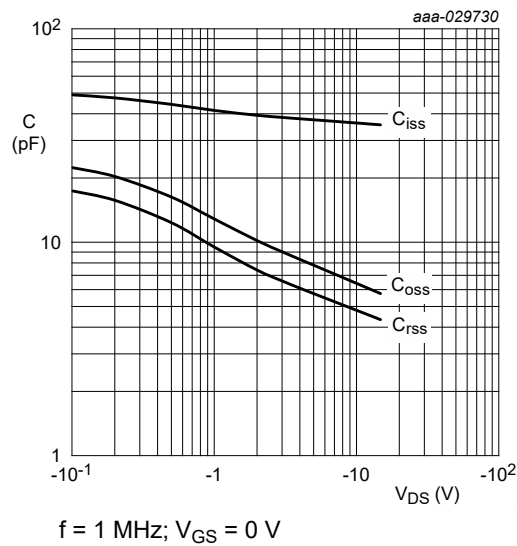


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

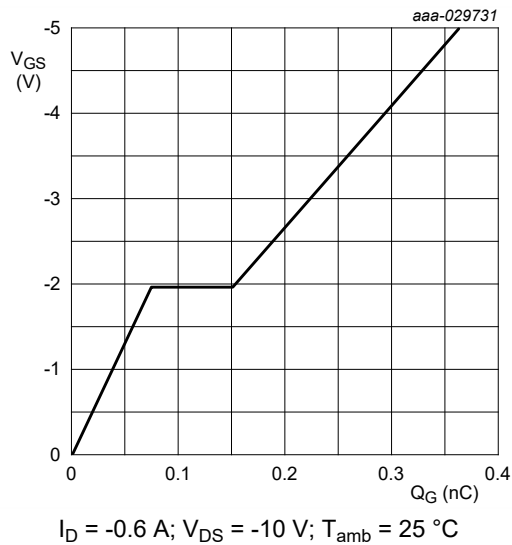


Fig. 15. Gate-source voltage as a function of gate charge; typical values

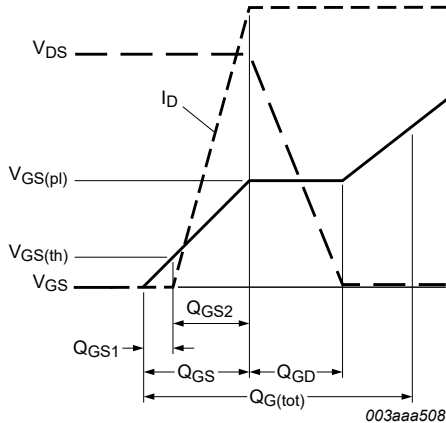
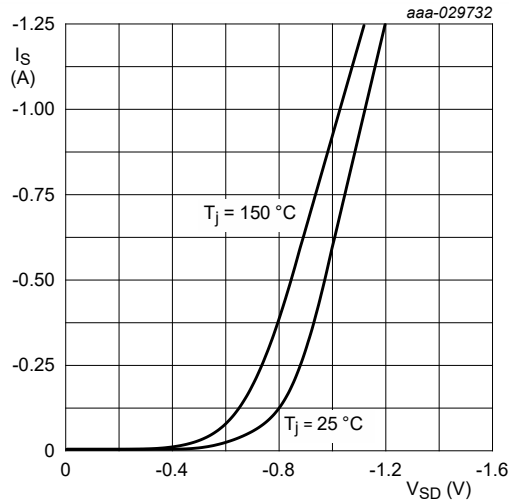


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

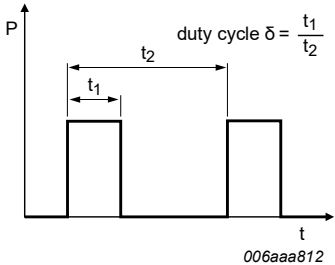
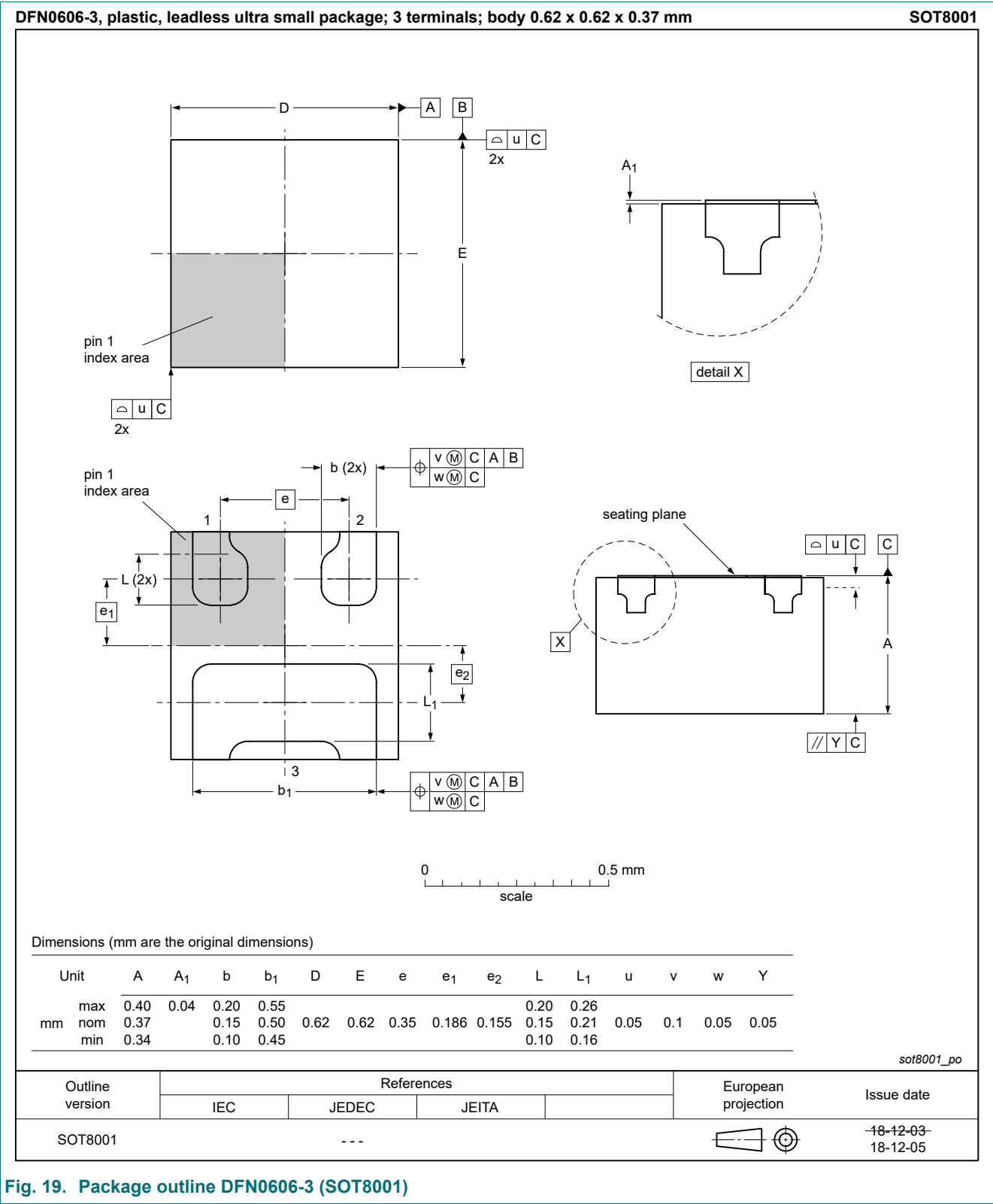


Fig. 18. Duty cycle definition

12. Package outline



13. Soldering

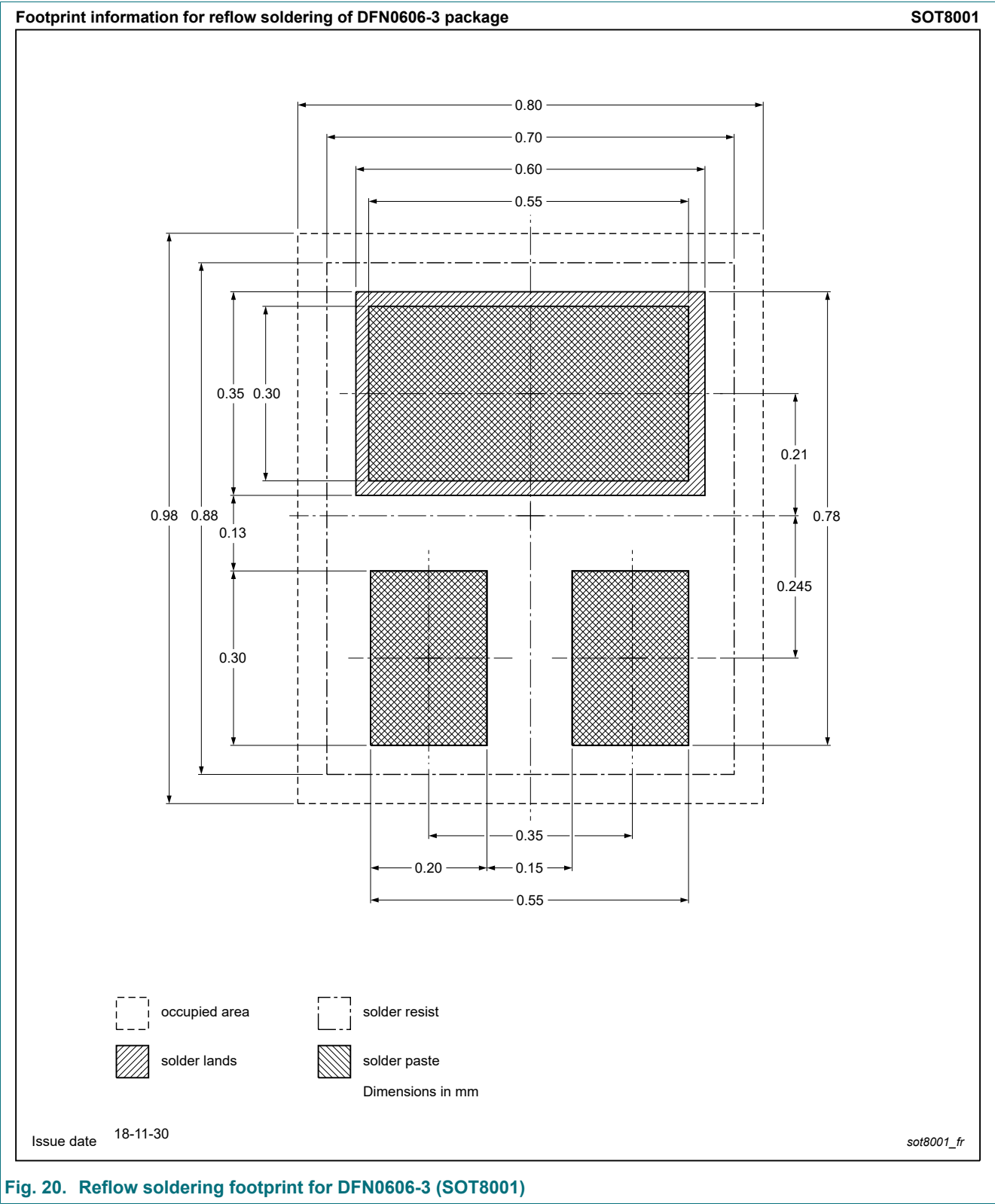


Fig. 20. Reflow soldering footprint for DFN0606-3 (SOT8001)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMH950UPE v.1	20190405	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Thermal characteristics..... 5

10. Characteristics.....6

11. Test information..... 9

12. Package outline..... 10

13. Soldering..... 11

14. Revision history.....12

15. Legal information.....13

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Date of release: 5 April 2019

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