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### FDG316P

### P-Channel Logic Level PowerTrench® MOSFET

#### **General Description**

This P-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

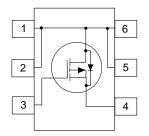
#### **Applications**

- DC/DC converter
- Load switch
- Power Management

#### **Features**

- -1.6 A, -30 V.  $R_{DS(ON)} = 0.19 \ \Omega \ @ \ V_{GS} = -10 \ V$   $R_{DS(ON)} = 0.30 \ \Omega \ @ \ V_{GS} = -4.5 \ V.$
- Low gate charge (3.5nC typical).
- High performance trench technology for extremely low  $R_{\rm ps/Ohb}$ .
- Compact industry standard SC70-6 surface mount package.





#### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		-30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-1.6	A
	- Pulsed		-6	
$P_D$	Power Dissipation for Single Operation	(Note 1a)	0.75	W
		(Note 1b)	0.48	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### **Thermal Characteristics**

R. IA	Thermal Resistance, Junction-to-Ambient	(Note 1b)	260	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape Width	Quantity
.36	FDG316P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics			•	•	•
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-30			V
ΔBV <sub>DSS</sub> ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, Referenced to 25°C		-34		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I <sub>GSS</sub>	Gate-Body Leakage Forward	V <sub>GS</sub> = 16 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSS</sub>	Gate-Body Leakage Reverse	V <sub>GS</sub> = -16 V, V <sub>DS</sub> = 0 V			-100	nA
On Chara	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.6	-3	V
$\Delta V_{GS(th)} \ \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, Referenced to 25°C		3.5		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -1.6 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -1.6 \text{ A}, T_J = 125^{\circ}\text{C}$ $V_{GS} = -4.5 \text{ V}, I_D = -1.3 \text{ A}$		0.16 0.22 0.23	0.19 0.31 0.30	Ω
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, I_D = -1.3 \text{ A}$ $V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$	-3			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -0.5 \text{ A}$		3		S
Dvnamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$		165		pF
Coss	Output Capacitance	f = 1.0 MHz		60		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1		25		pF
Switchin	g Characteristics (Note 2)				•	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15 \text{ V}, I_D = -1 \text{ A},$		8	20	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS}$ = -10 V, $R_{GEN}$ = 6 $\Omega$		9	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	1		14	30	ns
t <sub>f</sub>	Turn-Off Fall Time	1		2	10	ns
Qg	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -1.6 \text{ A},$		3.5	5	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -10 V		0.6		nC
Q <sub>gd</sub>	Gate-Drain Charge			0.8		nC
Drain-So	urce Diode Characteristics a	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				-0.42	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -0.42 \text{ A}$ (Note 2)		0.75	-1.2	V

<sup>1.</sup> R<sub>6JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

a) 170°C/W when mounted on a 1 in² pad of 2oz copper.

b) 260°C/W when mounted on a minimum pad.

<sup>2.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%

### **Typical Characteristics**

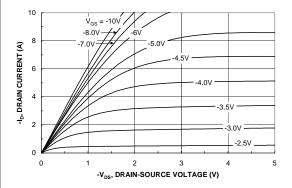


Figure 1. On-Region Characteristics.

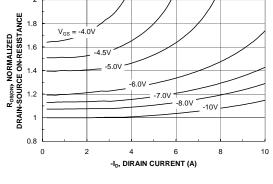


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

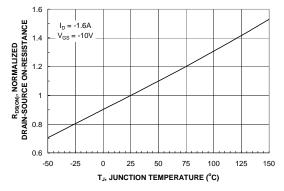


Figure 3. On-Resistance Variation with Temperature.

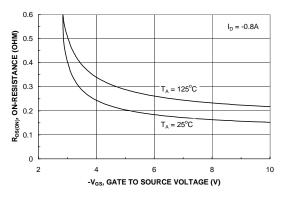


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

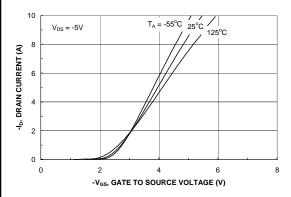


Figure 5. Transfer Characteristics.

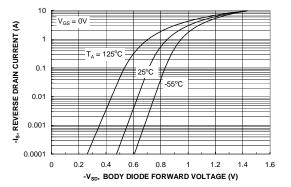
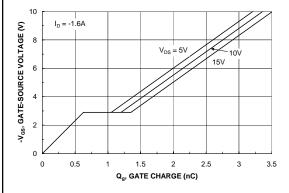


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics (continued)



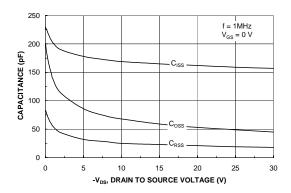
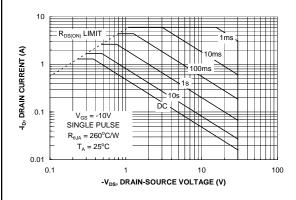


Figure 7. Gate-Charge Characteristics.

Figure 8. Capacitance Characteristics.



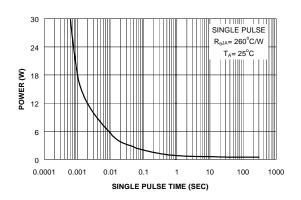


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

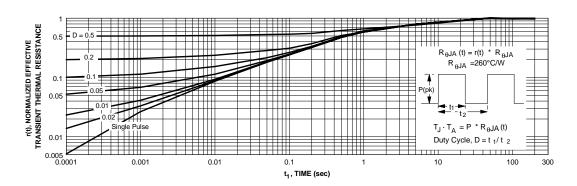


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient themal response will change depending on the circuit board design.

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105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

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moschip.ru moschip.ru\_6 moschip.ru 4 moschip.ru 9