Soft-Start Controlled Load Switch with Auto Discharge

The NCP331 is a low Ron N-channel MOSFET controlled by a soft-start sequence of 2 ms for mobile applications. The very low $R_{DS(on)}$ allows system supplying or battery charging up to DC 2A. The device is enable due to external, active high, enable pin.

Due to a current consumption optimization, leakage current is drastically decreased from the battery connected to the device, allowing long battery life.

Features

- 1.8 V 5.5 V Operating Range
- 33 mΩ N MOSFET
- DC Current Up to 2 A
- Peak Current Up to 5 A
- Built-in Soft-Start 2 ms
- Reverse Voltage Protection
- Output Discharge
- EN Logic Pin: Active High
- ESD Ratings:
 Machine Model = B
 Human Body Model = 2
- TSOP23-6 package
- This is a Pb-Free Device

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Computers

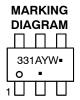


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TSOP-6 SN SUFFIX CASE 318G

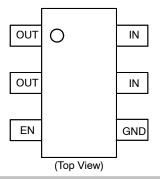


331 = Specific Device Code A = Assembly Location

Y = Year
W = Work Week
Pb-Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

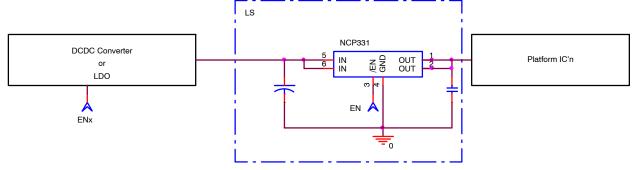
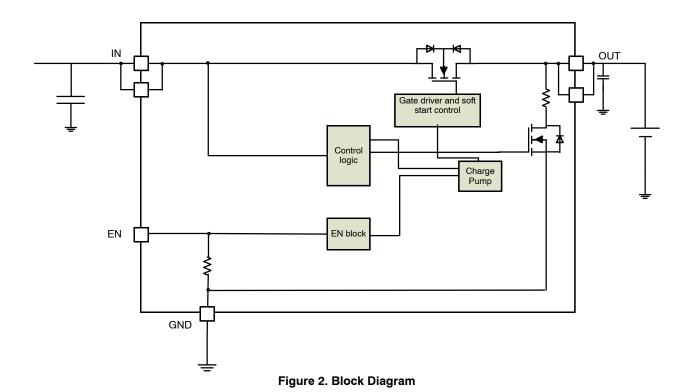


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description	
IN	5,6	POWER	Power–switch input voltage; connect a 0.1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.	
GND	4	POWER	Ground connection.	
EN	3	INPUT	Enable input, logic high turns on power switch.	
OUT	1,2	OUTPUT	Power–switch output; connect a 0.1 μF ceramic capacitor from OUT to GND as close possible to the IC is recommended.	

BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins:	V _{EN,} V _{IN,} V _{OUT}	-0.3 to +7.0	V
From IN to OUT Pins: Input/Output	$V_{IN,}V_{OUT}$	-7.0 to +7.0	V
Maximum Junction Temperature Range	TJ	-40 to +125	°C
Storage Temperature Range	T _{STG}	-40 to +150	°C
ESD Withstand Voltage Human Body model (HBM), model = 2, Machine Model (MM) model = B, (Note 1)	Vesd	2500 200	V
Moisture Sensitivity (Note 2)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22–A108.

2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J–STD–020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IN}	Operational Power Supply		1.8		5.5	V
V _{EN}	Enable Voltage		0		5.5	
T _A	Ambient Temperature Range		-40	25	+ 85	°C
T_J	Junction Temperature Range		-40	25	+ 125	°C
C _{IN}	Decoupling Input Capacitor		0.1			μF
C _{OUT}	Decoupling Output Capacitor		0.1			μF
$R_{\theta JA}$	Thermal Resistance – Junction-to-Air	(Notes 3 and 4)		305		°C/W
lout	Maximum DC Current				2	Α
P _D	Power Dissipation Rating (Note 7)	T _A ≤ 25°C		0.37		W
		T _A = 85°C		0.13		W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The R_{θJA} is dependent of the PCB heat dissipation.

- 4. The maximum power dissipation (P_{D}) is given by the following formula:

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to +85°C and T_J up to + 125°C for V_{IN} between 1.8 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
POWER S	WITCH							
R _{DS(on)}	Static drain-source on-state resistance	V _{IN} = 3 V, V _{IN} = 5 V, TSOP package	T _J = 25°C		33		mΩ	
			–40°C < T _J < 125°C			60		
T _{EN} Gate turn on	Gate turn on	V _{IN} = 3.3 V	From EN Vih to V _{OUT} rising. (Note 5), C _{LOAD} = 0.1 μ F, R _{LOAD} = 10 Ω		60	200	μs	
	Same tann en	V _{IN} = 3.0 V	From EN Vih to 10% V_{OUT} rising. C_{LOAD} = 1 μ F, R_{LOAD} = 25 Ω		278	500	μs	
	Output sing time	V _{IN} = 3.3 V	C_{LOAD} = 0.1 μ F, R_{LOAD} = 10 Ω (Note 5), from En to 95% V_{OUT}	1.2	2.05	3		
T _R	Output rise time	V _{IN} = 3.0 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 6), from 10% to 90% V_{OUT}	1.00	1.65	2.36		
Tdis	Disable time	V _{IN} = 3.0 V	From EN high to low to V _{OUT} falling		0.3		ms	
T _F	Output fall time	V _{IN} = 3 V	C_{LOAD} = 1 μ F, R_{LOAD} = 25 Ω (Note 6)	0.1	0.18	0.5		
T _{OFF}	Output off time	V _{IN} = 3 V	C_{LOAD} = 1 μ F, R_{LOAD} = 25 Ω (Notes 6 & 7), from EN to 10% V_{OUT}	0.3	0.5	0.8		
ENABLE I	NPUT EN					•	•	
V _{IH}	High-level input voltage			1.15			V	
V _{IL}	Low-level input voltage					0.85	V	
R _{pd}	En pull-down resistor			1.1	1.5	1.8	МΩ	
R _{dis}	Output discharge resistor			200	400	600	Ω	
REVERSE	-LEAKAGE PROTECTION							
I _{REV}	I_{REV} Reverse-current $V_{IN} = 0 \text{ V}, V_{OUT} = 4.2 \text{ V} \text{ (part disable)}, T_A = 25^{\circ}\text{C}$				0.3	1.2	μА	
QUIESCE	NT CURRENT							
Istb	Standby current	En low, Vin = 3 V			1.3	3	μΑ	
Iq	Current consumption	No load, En high, Vin = 3 V			11	15	μΑ	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Guaranteed by correlation with 3.0 V production test.
 Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.
 Guaranteed by T_{fall} and R_{discharge} tests.

TIMINGS

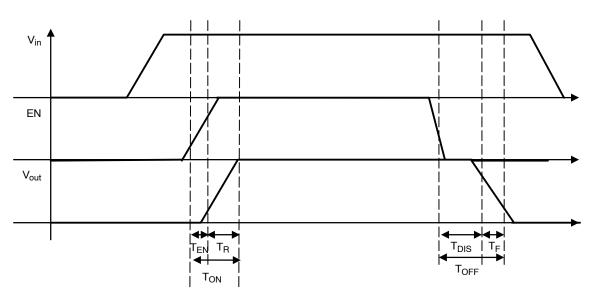
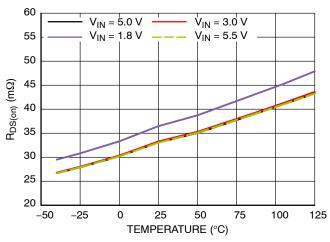


Figure 3. Timings

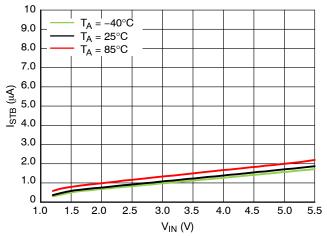
TYPICAL CHARACTERISTICS



50 45 40 $R_{DS(on)}$ (m Ω) 35 30 25 20 1.5 2 2.5 3 3.5 4 4.5 5.5 $V_{IN}(V)$

Figure 4. R_{DS(on)} versus Temperature

Figure 5. R_{DS(on)} versus Input Voltage, Ambient Temperature



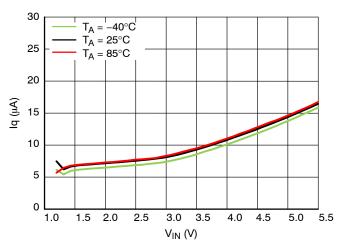


Figure 6. Standby Current versus Input Voltage

Figure 7. Quiescent Current versus Input Voltage

FUNCTIONAL DESCRIPTION

Overview

The NCP331 is a high side N channel MOSFET power distribution switch designed to connect external voltage directly to the system.

Enable Input

Enable pin is an active high.

The part is in disable mode when EN is tied to low. Power MOSFET is opened. Pull down resistor is placed to maintained the part off if En pin is not externally driven.

The parts becomes in enable mode if EN is tied high and Power MOSFET is turned of after ten and t_{rise} times.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level.

Blocking Control

The blocking control circuitry switches the bulk of the power NMOS. When the part is off (No V_{in} or EN tied to GND externally), the body diode limits the leakage current I_{REV} from OUT to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUT pin. In operating condition, anode of the body diode is connected to OUT pin and cathode is connected to IN pin preventing the discharge of the power supply.

APPLICATION INFORMATION

Power Dissipation

The device's junction temperature depends on different contributor factor such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times (I_{OUT})^2$$

P_D = Power dissipation (W)

 $R_{DS(on)}$ = Power MOSFET on resistance (Ω)

 I_{OUT} = Output current (A)

$T_{J} = P_{D} \times R_{\theta,JA} + T_{A}$

 T_J = Junction temperature (°C)

 $R_{\theta JA}$ = Package thermal resistance (°C/W)

 T_A = Ambient temperature (°C)

PCB Recommendations

The NCP331 integrates an up to 2A rated NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

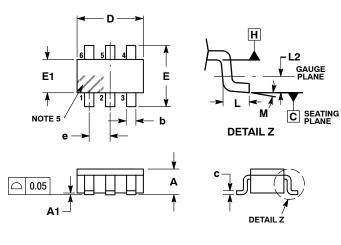
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NCP331SNT1G	331	TSOP-6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE V

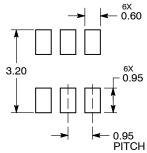


- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.

- CONTROLLING DIMENSION: MILLIMETERS.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
 PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS				
DIM	MIN	NOM	MAX		
Α	0.90	1.00	1.10		
A1	0.01	0.06	0.10		
b	0.25	0.38	0.50		
С	0.10	0.18	0.26		
D	2.90	3.00	3.10		
E	2.50	2.75	3.00		
E1	1.30	1.50	1.70		
е	0.85	0.95	1.05		
L	0.20	0.40	0.60		
L2	0.25 BSC				
M	0° – 10°				

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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