Triple and Octal Channel Protectors

ADG466/ADG467

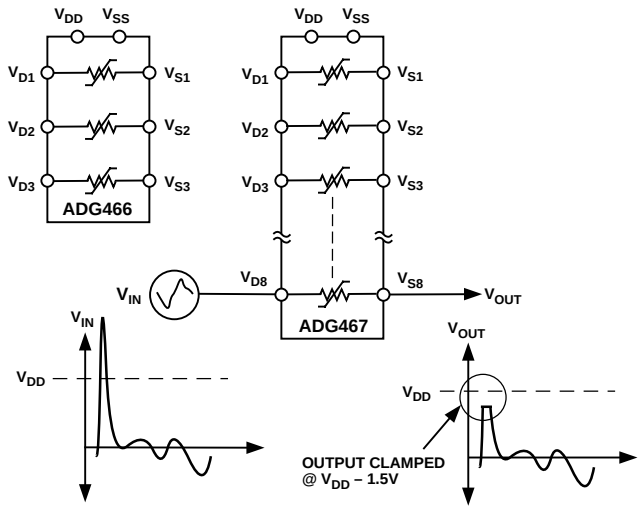
FEATURES

Fault and Overvoltage Protection up to ±40 V
Signal Paths Open Circuit with Power Off
Signal Path Resistance of R_{ON} with Power On
44 V Supply Maximum Ratings
Low On Resistance
ADG466/ADG467 60 Ω typ
1 nA Max Path Current Leakage @ +25°C
Low R_{ON} Match (5 Ω max)
Low Power Dissipation 0.8 μW typ
Latch-Up Proof Construction

APPLICATIONS

ATE Equipment
Sensitive Measurement Equipment
Hot-Insertion Rack Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG466 and ADG467 are triple and octal channel protectors, respectively. The channel protector is placed in series with the signal path. The channel protector will protect sensitive components from voltage transience in the signal path whether the power supplies are present or not. Because the channel protection works whether the supplies are present or not, the channel protectors are ideal for use in applications where correct power sequencing can't always be guaranteed (e.g., hot-insertion rack systems) to protect analog inputs. This is discussed further, and some example circuits are given in the Applications section of this data sheet.

Each channel protector has an independent operation and consists of an n-channel MOSFET, a p-channel MOSFET and an n-channel MOSFET, connected in series. The channel protector behaves just like a series resistor during normal operation, i.e., $(V_{SS} + 2\,V) < V_{IN} < (V_{DD} - 1.5\,V)$. When a channel's analog input exceeds the power supplies (including V_{DD} and V_{SS} = 0 V), one of the MOSFETs will switch off, clamping the output to either V_{SS} + 2 V or V_{DD} – 1.5 V. Circuitry and signal source protection is provided in the event of an overvoltage or power loss. The channel protectors can withstand overvoltage inputs from –40 V to +40 V. See the Circuit Information section of this data sheet.

The ADG466 and ADG467 can operate off both bipolar and unipolar supplies. The channels are normally on when power is connected and open circuit when power is disconnected. With power supplies of ±15 V, the on-resistance of the ADG466 and ADG467 is 60 Ω typ with a leakage current of ±1 nA max. When power is disconnected, the input leakage current is approximately ±5 nA typ.

The ADG466 is available in 8-lead DIP, SOIC and μSOIC packages. The ADG467 is available in an 18-lead SOIC package and a 20-lead SSOP package.

PRODUCT HIGHLIGHTS

1. Fault Protection.
   The ADG466 and ADG467 can withstand continuous voltage inputs from –40 V to +40 V. When a fault occurs due to the power supplies being turned off or due to an overvoltage being applied to the ADG466 and ADG467, the output is clamped. When power is turned off, current is limited to the microampere level.
2. Low Power Dissipation.
3. Low R_{ON}.
   ADG466/ADG467 60 Ω typ.
4. Trench Isolation Latch-Up Proof Construction.
   A dielectric trench separates the p- and n-channel MOSFETs thereby preventing latch-up.

REV. A

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ADG466/ADG467–SPECIFICATIONS

Dual Supply[1] (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	ADG466 +25°C	ADG466 B[1]	ADG467 +25°C	ADG467 B[1]	Units	Test Conditions/Comments
FAULT PROTECTED CHANNEL						
Fault-Free Analog Signal Range[2]		V_{SS} + 1.2		V_{SS} + 1.2	V min	Output Open Circuit
		V_{DD} – 0.8		V_{DD} – 0.8	V max	
R_{ON}	60	75	62	80	Ω typ	–10 V ≤ V_S ≤ +10 V, I_S = 1 mA
		80		95	Ω max	
ΔR_{ON}	3	4		6	Ω max	–5 V ≤ V_S ≤ +5 V
R_{ON} Match	4	6	5	6	Ω max	V_S = ±10 V, I_S = 1 mA
LEAKAGE CURRENTS						
Channel Output Leakage, $I_{S(ON)}$						V_S = V_D = ±10 V
(without Fault Condition)	±0.1	±1	±0.04	±0.2	nA typ	
	±1	±5	±1	±5	nA max	
Channel Input Leakage, $I_{D(ON)}$						V_S = ±25 V
(with Fault Condition)	±0.2	±0.4	±0.2	±0.4	nA typ	V_D = Open Circuit
	±2	±5	±2	±5	nA max	
Channel Input Leakage, $I_{D(OFF)}$						V_{DD} = 0 V, V_{SS} = 0 V
(with Power Off and Fault)	±0.5	±2	±0.5	±2	nA typ	V_S = ±35 V,
	±1	±5	±2	±10	nA max	V_D = Open Circuit
Channel Input Leakage, $I_{D(OFF)}$						V_{DD} = 0 V, V_{SS} = 0 V
(with Power Off and Output S/C)	±0.005	±0.1	±0.006	±0.16	µA typ	V_S = ±35 V, V_D = 0 V
	±0.015	±0.5	±0.015	±0.5	µA max	
POWER REQUIREMENTS						
I_{DD}	±0.05		±0.05		µA typ	
	±0.5	±8	±0.5	±8	µA max	
I_{SS}	±0.05		±0.05		µA typ	
	±0.5	±8	±0.5	±8	µA max	
V_{DD}/V_{SS}	0	0	0	0	V min	
	±20	±20	±20	±20	V max	

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . +44 V
V_S, V_D, Analog Input Overvoltage with Power ON[2]
. . . . . V_{SS} – 20 V to V_{DD} + 20 V
V_S, V_D, Analog Input Overvoltage with Power OFF[2]
. . . . . –35 V to +35 V
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D . . . . . 40 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +125°C
Junction Temperature . . . . . +150°C
Plastic DIP Package
θ_{JA}, Thermal Impedance . . . . . 125°C/W
Lead Temperature, Soldering (10 sec) . . . . . +260°C
SOIC Package
θ_{JA}, Thermal Impedance . . . . . 160°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
µSOIC Package
θ_{JA}, Thermal Impedance . . . . . 160°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
SSOP Package
θ_{JA}, Thermal Impedance . . . . . 130°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

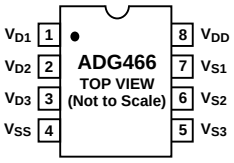
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

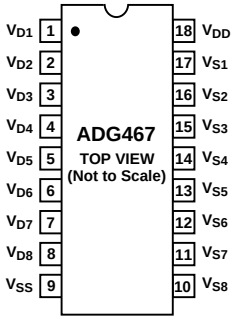
[2]Overvoltages at S or D will be clamped by the channel protector, see Circuit Information section of the data sheet.

PIN CONFIGURATIONS

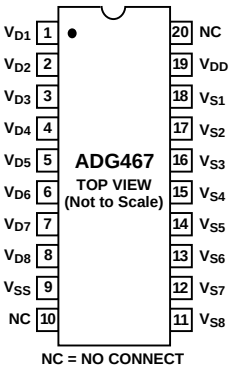
8-Lead DIP, SOIC and µSOIC



18-Lead SOIC



20-Lead SSOP



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
ADG466BN	–40°C to +85°C	8-Lead Plastic DIP	N-8
ADG466BR	–40°C to +85°C	8-Lead Small Outline Package	SO-8
ADG466BRM	–40°C to +85°C	8-Lead Micro Small Outline Package	RM-8
ADG467BR	–40°C to +85°C	18-Lead Small Outline Package	R-18
ADG467BRS	–40°C to +85°C	20-Lead Shrink Small Outline Package	RS-20

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG466/ADG467 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADG466/ADG467–Typical Performance Characteristics

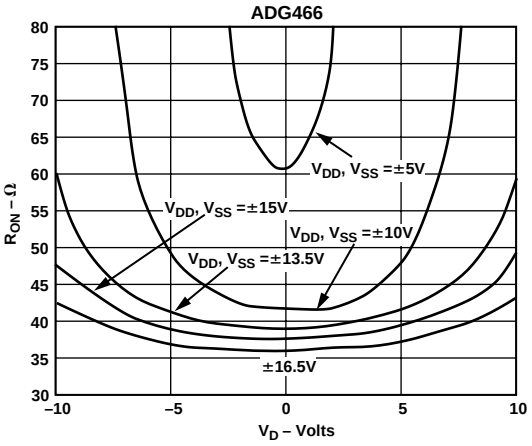


Figure 1. On Resistance as a Function of V_{DD} and V_D (Input Voltage)

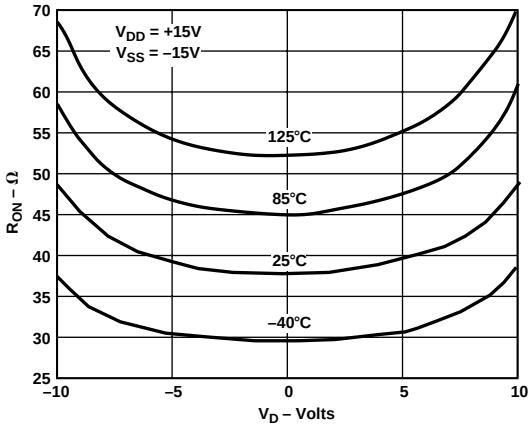


Figure 2. On Resistance as a Function of Temperature and V_D (Input Voltage)

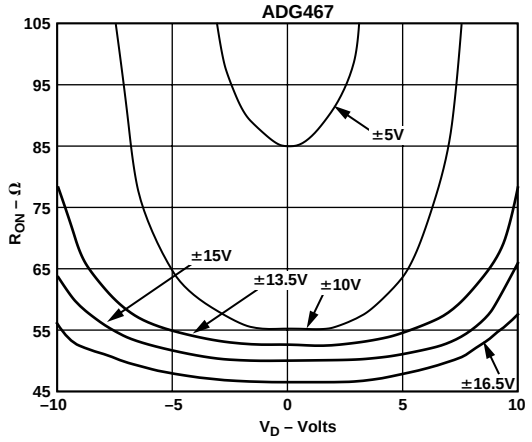


Figure 3. On Resistance as a Function of V_{DD} and V_D (Input Voltage)

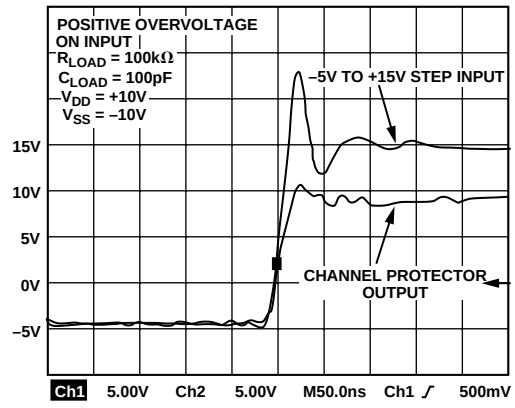


Figure 4. Positive Overvoltage Transience Response

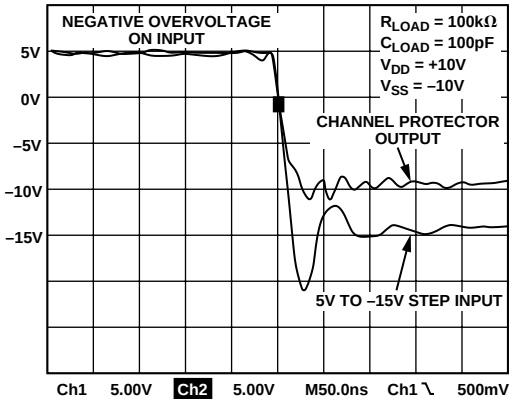


Figure 5. Negative Overvoltage Transience Response

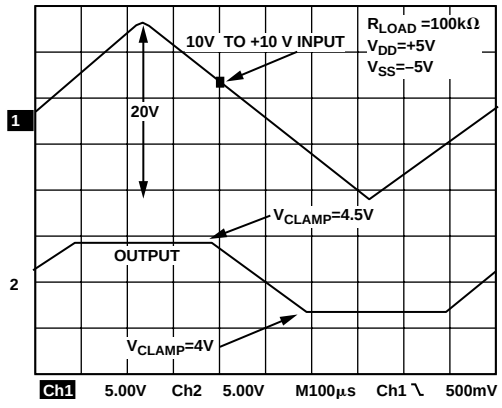


Figure 6. Overvoltage Ramp

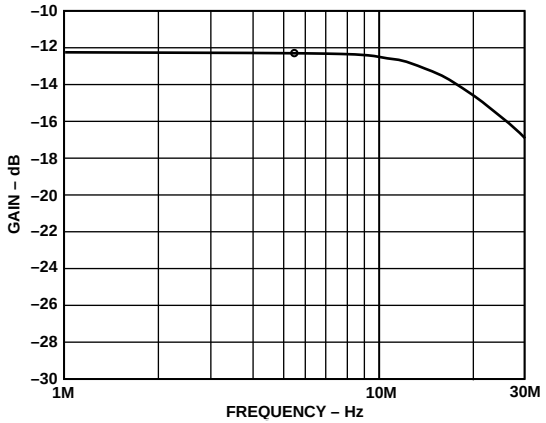


Figure 7. Frequency Response (Magnitude) of the ADG467, V_{DD}/V_{SS} = ±15 V and Input Signal Level of ±100 mV

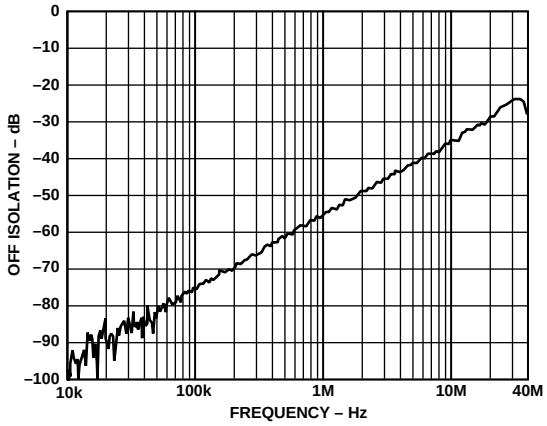


Figure 10. Off Isolation of the ADG467, V_{DD}/V_{SS} = 0 V and Input Signal Level of ±100 mV

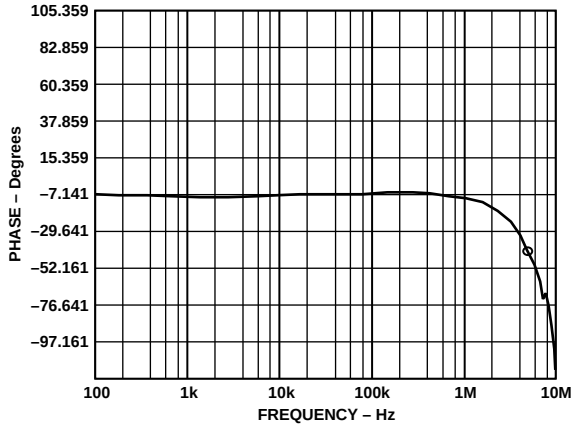


Figure 8. Frequency Response (Phase) of the ADG467, V_{DD}/V_{SS} = ±15 V and Input Signal Level of ±100 mV

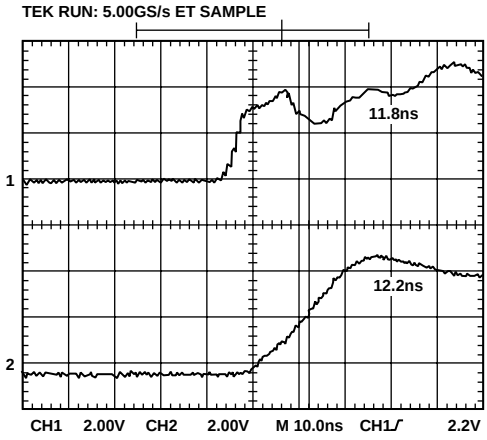


Figure 11. Propagation Delay Through ADG467, V_{DD}/V_{SS} = ±15 V, Channel 1 Input and Channel 2 Output

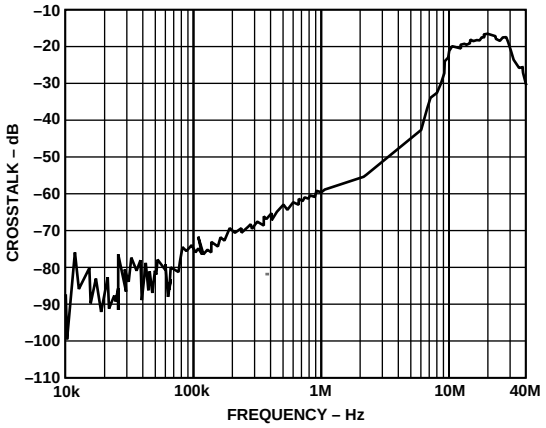


Figure 9. Crosstalk Between Adjacent Channels of the ADG467, V_{DD}/V_{SS} = ±15 V and Input Signal Level of ±100 mV

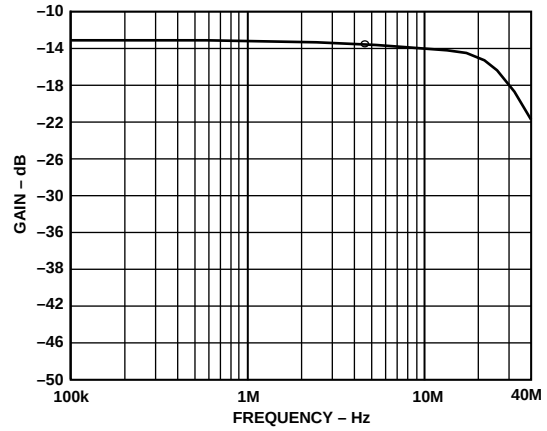


Figure 12. Frequency Response (Magnitude) of the ADG466, V_{DD}/V_{SS} = ±15 V and Input Signal Level of ±100 mV

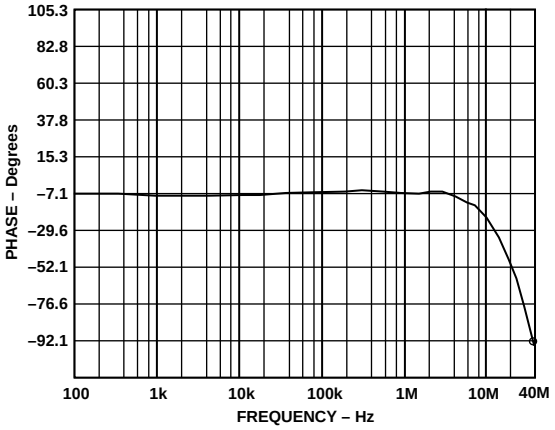


Figure 13. Frequency Response (Phase) of the ADG466, V_{DD}/V_{SS} = ±15 V and Input Signal Level of ±100 mV

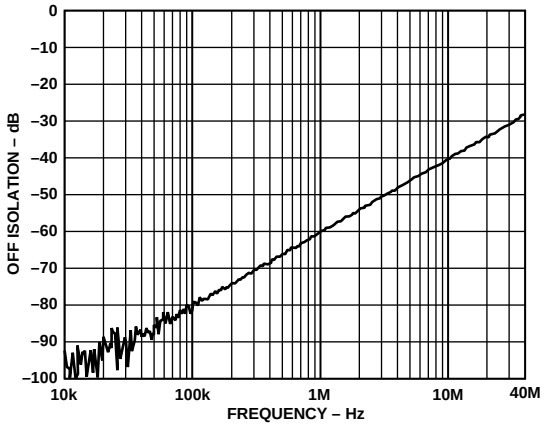


Figure 15. Off Isolation of the ADG466, V_{DD}/V_{SS} = 0 V and Input Signal Level of ±100 mV

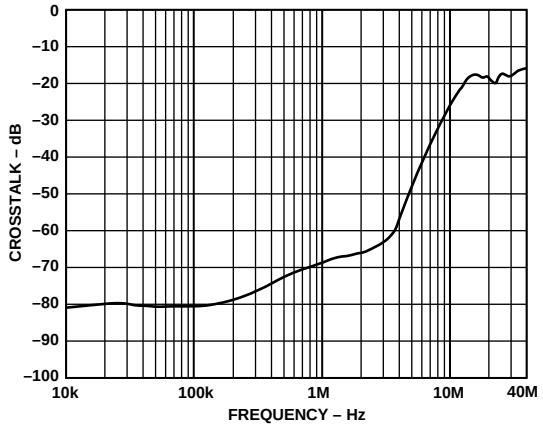


Figure 14. Crosstalk Between Adjacent Channels of the ADG466, V_{DD}/V_{SS} = ±15 V and Input Signal Level of ±100 mV

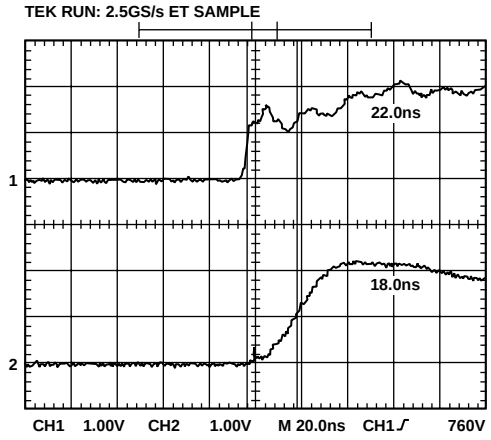


Figure 16. Propagation Delay Through ADG466, V_{DD}/V_{SS} = ±15 V, Channel 1 Input and Channel 2 Output

CIRCUIT INFORMATION

Figure 17 below shows a simplified schematic of a channel protector circuit. The circuit is made up of four MOS transistors—two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and so increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason. During normal operation the channel protectors have a resistance of 60 Ω typ. The channel protectors are very low power devices, and even under fault conditions the supply current is limited to sub microampere levels. All transistors are dielectrically isolated from each other using a trench isolation method. This makes it impossible to latch up the channel protectors. For an explanation, see Trench Isolation section.

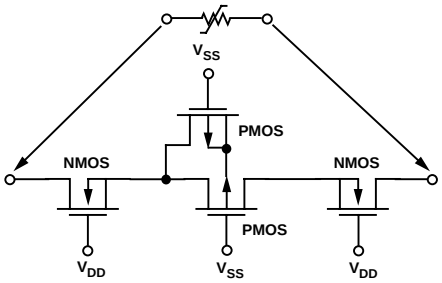


Figure 17. The Channel Protector Circuit

Overvoltage Protection

When a fault condition occurs on the input of a channel protector, the voltage on the input has exceeded some threshold voltage set by the supply rail voltages. The threshold voltages are related to the supply rails as follows. For a positive overvoltage, the threshold voltage is given by $V_{DD} - V_T$ where V_{TN} is the threshold voltage of the NMOS transistor (1.5 V typ). In the case of a negative overvoltage the threshold voltage is given by $V_{SS} - V_{TP}$ where V_{TP} is the threshold voltage of the PMOS device (2 V typ). If the input voltage exceeds these threshold voltages, the output of the channel protector (no load) is clamped at these threshold voltages. However, the channel protector output will clamp at a voltage that is inside these thresholds if the output is loaded. For example with an output load of 1 kΩ, V_{DD} = 15 V and a positive overvoltage. The output will clamp at $V_{DD} - V_{TN} - \Delta V$ = 15 V – 1.5 V – 0.6 V = 12.9 V where ΔV is due to I × R voltage drop across the channels of the MOS devices (see Figure 19). As can be seen from Figure 19, the current during fault condition is determined by the load on the output (i.e., V_{CLAMP}/R_L). However, if the supplies are off, the fault current is limited to the nano-ampere level.

Figures 18, 20 and 21 show the operating conditions of the signal path transistors during various fault conditions. Figure 18 shows how the channel protectors operate when a positive overvoltage is applied to the channel protector.

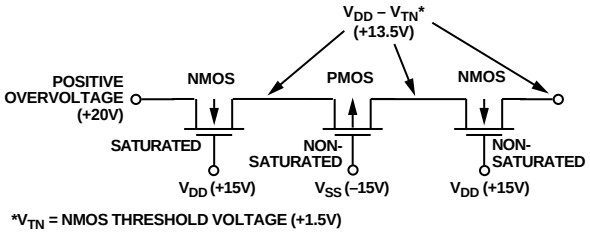


Figure 18. Positive Overvoltage on the Channel Protector

The first NMOS transistor goes into a saturated mode of operation as the voltage on its Drain exceeds the Gate voltage (V_{DD}) – the threshold voltage (V_{TN}). This situation is shown in Figure 19. The potential at the source of the NMOS device is equal to $V_{DD} - V_{TN}$. The other MOS devices are in a nonsaturated mode of operations.

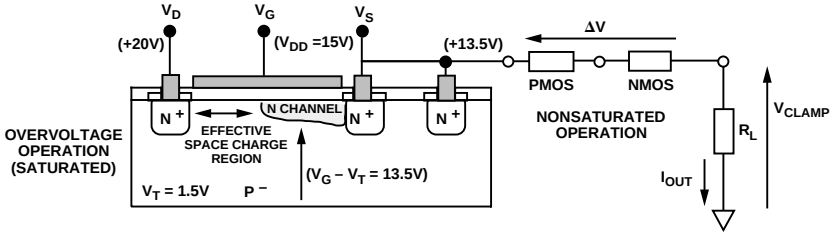


Figure 19. Positive Overvoltages Operation of the Channel Protector

When a negative overvoltage is applied to the channel protector circuit, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds $V_{SS} - V_{TP}$. See Figure 20 below. As in the case of the positive overvoltage, the other MOS devices are nonsaturated.

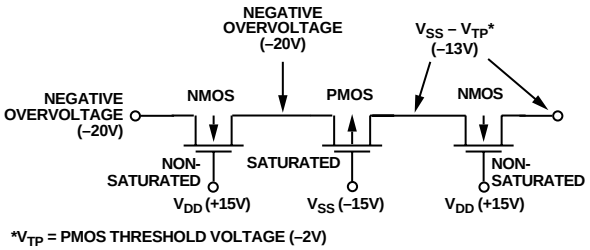


Figure 20. Negative Overvoltage on the Channel Protector

The channel protector is also functional when the supply rails are down (e.g., power failure) or momentarily unconnected (e.g., rack system). This is where the channel protector has an advantage over more conventional protection methods such as diode clamping (see Applications Information). When V_{DD} and V_{SS} equal 0 V, all transistors are off and the current is limited to subnano-ampere levels (see Figure 21).

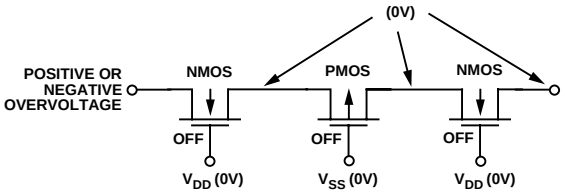


Figure 21. Channel Protector Supplies Equal to Zero Volts

TRENCH ISOLATION

The MOS devices that make up the channel protector are isolated from each other by an oxide layer (trench) (see Figure 22). When the NMOS and PMOS devices are not electrically isolated from each other, there exists the possibility of "latch-up" caused by parasitic junctions between CMOS transistors. Latch-up is caused when P-N junctions that are normally reverse biased become forward biased, causing large currents to flow, which can be destructive.

CMOS devices are normally isolated from each other by *Junction Isolation*. In Junction Isolation, the *N* and *P* wells of the CMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With Trench Isolation, this diode is removed; the result is a latch-up proof circuit.

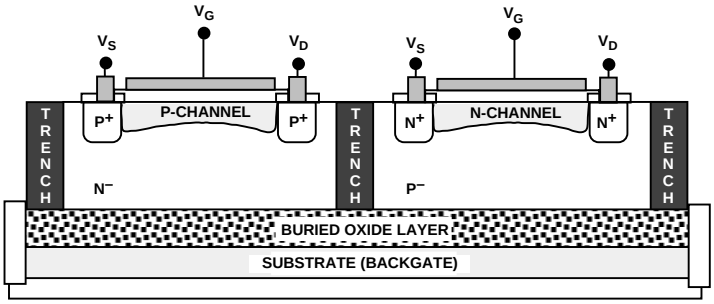


Figure 22. Trench Isolation

APPLICATIONS INFORMATION

Overvoltage and Power Supply Sequencing Protection

The ADG466 and ADG467 are ideal for use in applications where input overvoltage protection is required and correct power supply sequencing cannot always be guaranteed. The overvoltage protection ensures that the output voltage of the channel protector will not exceed the threshold voltages set by the supplies (see Circuit Information) when there is an overvoltage on the input. When the input voltage does not exceed these threshold voltages, the channel protector behaves like a series resistor (60 Ω typ). The resistance of the channel protector does vary slightly with operating conditions (see Typical Performance Graphs).

The power sequencing protection is afforded by the fact that when the supplies to the channel protector are not connected, the channel protector becomes a high resistance device. Under this condition all transistors in the channel protector are off and the only currents that flow are leakage currents, which are at the μA level.

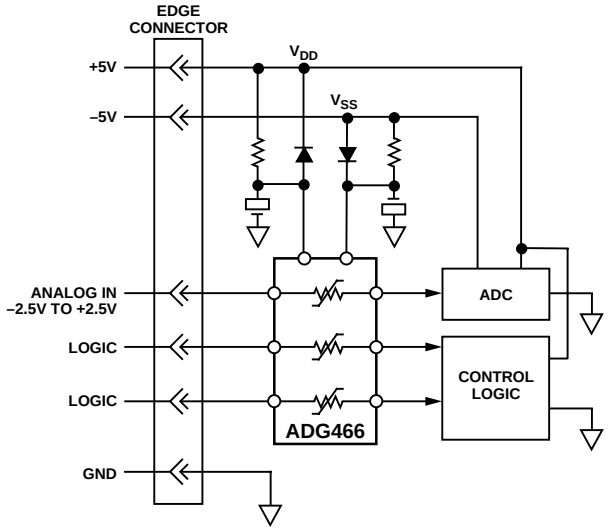


Figure 23. Overvoltage and Power Supply Sequencing Protection

Figure 23 shows a typical application that requires overvoltage and power supply sequencing protection. The application shows a Hot-Insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected before any external signals. Incorrect power sequencing can cause a CMOS device to "latch up." This is true of most CMOS devices regardless of the functionality. RC networks are used on the supplies of the channel protector (Figure 23) to ensure that the rest of the circuitry is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails of the board when it is being disconnected. Again this ensures that signals on the inputs of the CMOS devices never exceed the supplies.

High Voltage Surge Suppression

The ADG466 and ADG467 are not intended for use in high voltage applications like surge suppression. The ADG466 and ADG467 have breakdown voltages of V_{SS} – 20 V and V_{DD} + 20 V on the inputs when the power supplies are connected. When the power supplies are disconnected, the breakdown voltages on the input of the channel protector are ±35 V. In applications where inputs are likely to be subject to overvoltages exceeding the breakdown voltages quoted for the channel protectors, transient voltage suppressors (TVSs) should be used. These devices are commonly used to protect vulnerable circuits from electric overstress such as that caused by electrostatic discharge, inductive load switching and induced lightning. However, TVSs can have a substantial standby (leakage) current (300 μA typ) at the reverse standoff voltage. The reverse standoff voltage of a TVS is the normal peak operating voltage of the circuit. Also TVS offer no protection against latch-up of sensitive CMOS devices when the power supplies are off. The best solution is to use a channel protector in conjunction with a TVS to provide the best leakage current specification and circuit protection.

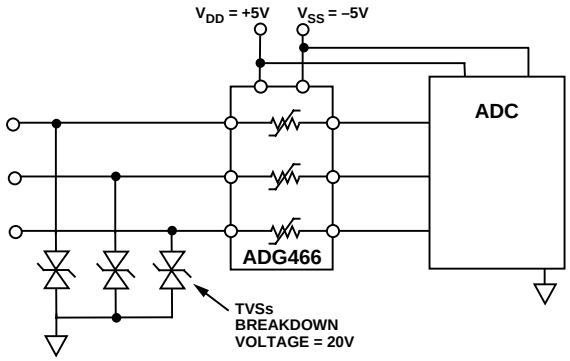


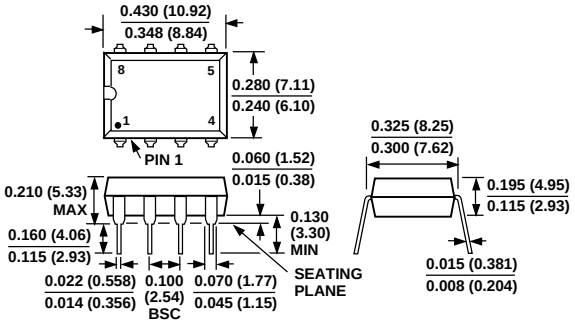
Figure 24. High Voltage Protection

Figure 24 shows an input protection scheme that uses both a TVS and channel protector. The TVS is selected with a reverse standoff voltage that is much greater than operating voltage of the circuit (TVSs with higher breakdown voltages tend to have better standby leakage current specifications) but is inside the breakdown voltage of the channel protector. This circuit protects the circuitry whether the power supplies are present or not.

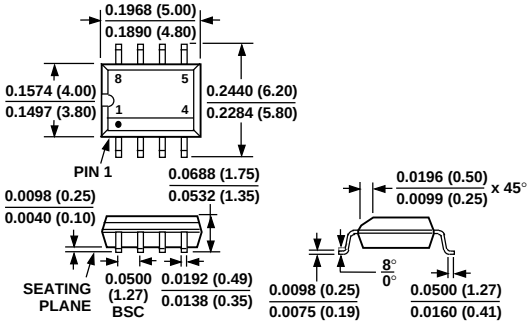
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

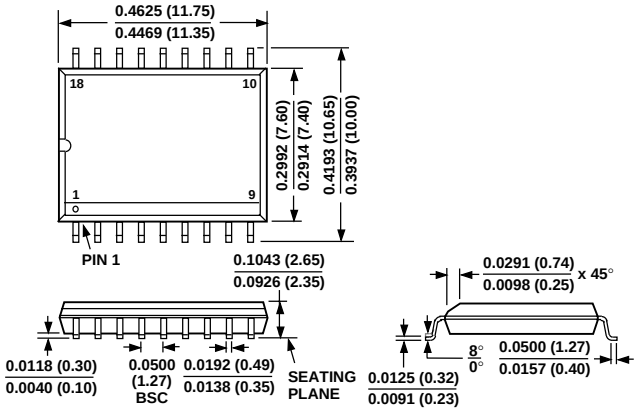
8-Lead Plastic DIP (N-8)



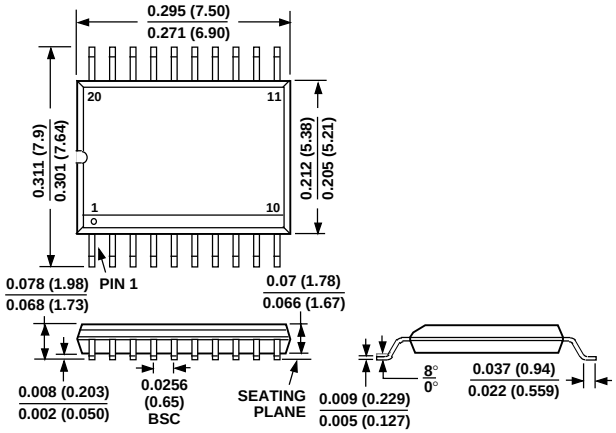
8-Lead Small Outline IC (SO-8)



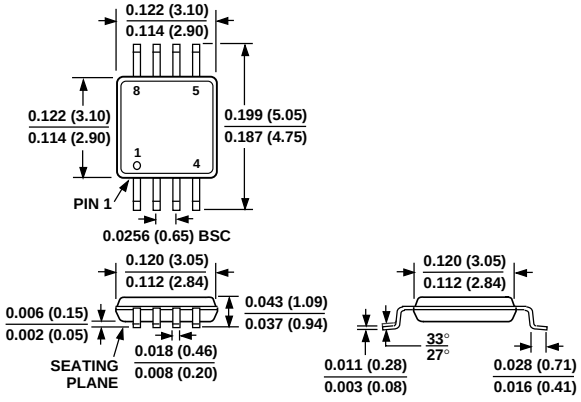
18-Lead Small Outline IC (R-18)



20-Lead Shrink Small Outline Package (RS-20)



8-Lead Micro Small Outline IC (RM-8)



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