

MC74HCT373A

Octal 3-State Noninverting Transparent Latch with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT373A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT373A is identical in pinout to the LS373.

The eight latches of the HCT373A are transparent D-type latches. While the Latch Enable is high the Q outputs follow the Data Inputs. When Latch Enable is taken low, data meeting the setup and hold times becomes latched.

The Output Enable does not affect the state of the latch, but when Output Enable is high, all outputs are forced to the high-impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT373A is identical in function to the HCT573A, which has the input pins on the opposite side of the package from the output pins. This device is similar in function to the HCT533A, which has inverting outputs.

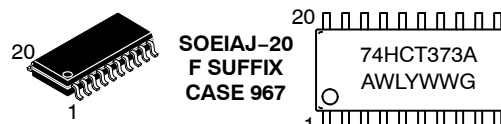
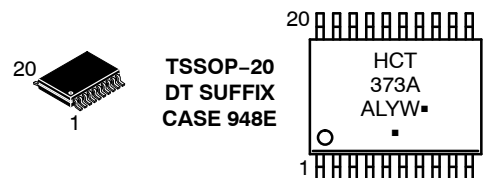
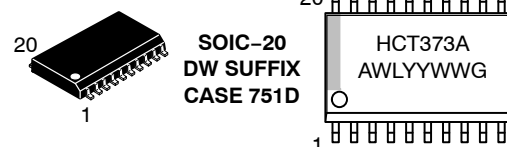
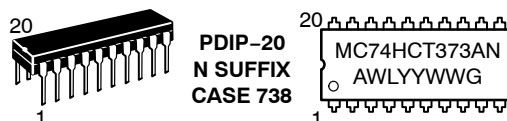
- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 196 FETs or 49 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

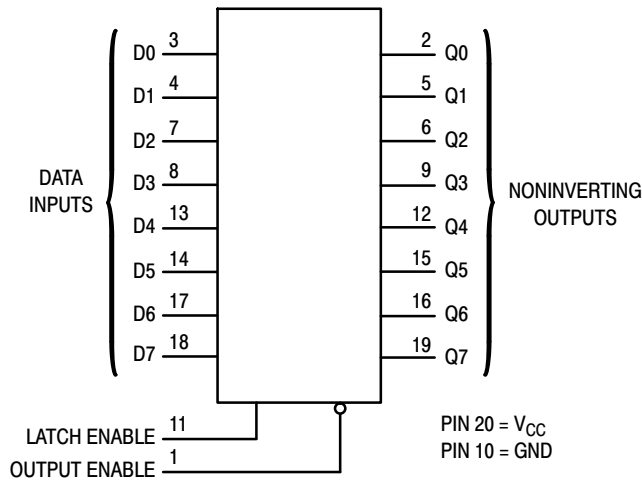
ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|-----------|-------------|
| MC74HCT373ANG | PDIP-20 | 18 / Box |
| MC74HCT373ADWG | SOIC-20 | 38 / Rail |
| MC74HCT373ADWR2G | SOIC-20 | 1000 / Reel |
| MC74HCT373AFELG | SOEIAJ-20 | 2000 / Reel |
| MC74HCT373ADTR2G | TSSOP-20 | 2500 / Reel |

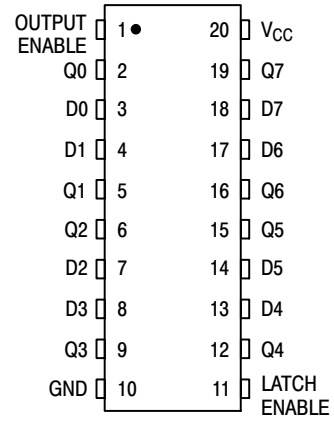
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | | Output |
|---------------|--------------|---|-----------|
| Output Enable | Latch Enable | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | No Change |
| H | X | X | Z |

X = don't care

Z = high impedance

| Design Criteria | Value | Units |
|---------------------------------|--------|-------|
| Internal Gate Count* | 49 | ea. |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μW |
| Speed Power Product | 0.0075 | pJ |

*Equivalent to a two-input NAND gate.

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 35 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package† | 750 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 †Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C
 TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|------|----------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | - 55 | + 125 | °C |
| t_p, t_f | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|----------|--|--|---------------|------------------|-----------|----------|---------------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | 5.4 | |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 6.0 \text{ mA}$ | 4.5 | 3.98 | 3.84 | 3.7 | V |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| I_{in} | Maximum Input Leakage Current | $V_{in} = V_{CC} \text{ or } GND$ | 4.5 | 0.1 | 0.1 | 0.1 | μA |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| I_{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND$ | 5.5 | ± 0.5 | ± 5.0 | ± 10 | μA |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$ | 5.5 | 4.0 | 40 | 160 | μA |

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| | | | | | | |
|-----------------|-------------------------------------|---|-----|----------------------------|---|----|
| ΔI_{CC} | Additional Quiescent Supply Current | $V_{in} = 2.4\text{ V}$, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0\ \mu\text{A}$ | 5.5 | $\geq -55^{\circ}\text{C}$ | $25^{\circ}\text{C to }125^{\circ}\text{C}$ | mA |
| | | | | 2.9 | 2.4 | |

NOTE: 1. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|--------------------------|--|--|---------------------------|----------------------------|------|
| | | $-55\text{ to }25^{\circ}\text{C}$ | $\leq 85^{\circ}\text{C}$ | $\leq 125^{\circ}\text{C}$ | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Input D to Q (Figures 1 and 5) | 28 | 35 | 42 | ns |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Latch Enable to Q (Figures 2 and 5) | 32 | 40 | 48 | ns |
| t_{PLZ} , t_{PHZ} | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 30 | 38 | 45 | ns |
| t_{PZL} , t_{PZH} | Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6) | 35 | 44 | 53 | ns |
| t_{TLH} , t_{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 5) | 12 | 15 | 18 | ns |
| C_{in} | Maximum Input Capacitance | 10 | 10 | 10 | pF |
| C_{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | 15 | 15 | 15 | pF |
| C_{PD} | Power Dissipation Capacitance (Per Latch)* | Typical @ 25°C , $V_{CC} = 5.0\text{ V}$ | | | pF |
| | | 65 | | | |

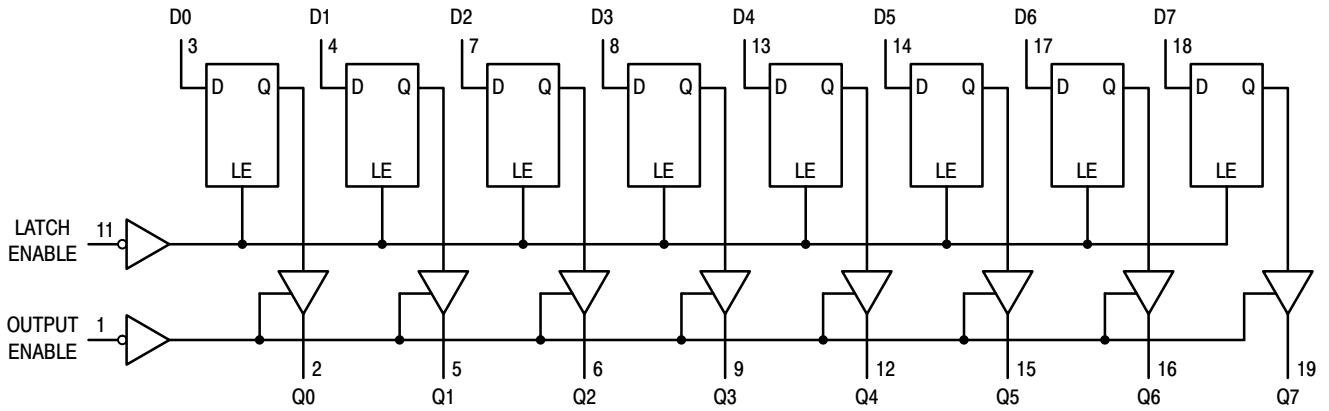
* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS ($V_{CC} = 5.0\text{ V} \pm 10\%$, Input $t_r = t_f = 6.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|---------------|---|------------------------------------|---------------------------|----------------------------|------|
| | | $-55\text{ to }25^{\circ}\text{C}$ | $\leq 85^{\circ}\text{C}$ | $\leq 125^{\circ}\text{C}$ | |
| t_{su} | Minimum Setup Time, Input D to Latch Enable (Figure 4) | 10 | 13 | 15 | ns |
| t_h | Minimum Hold Time, Latch Enable to Input D (Figure 4) | 10 | 13 | 15 | ns |
| t_w | Minimum Pulse Width, Latch Enable (Figure 2) | 12 | 15 | 18 | ns |
| t_r , t_f | Maximum Input Rise and Fall Times (Figure 1) | 500 | 500 | 500 | ns |

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EXPANDED LOGIC DIAGRAM



SWITCHING WAVEFORMS

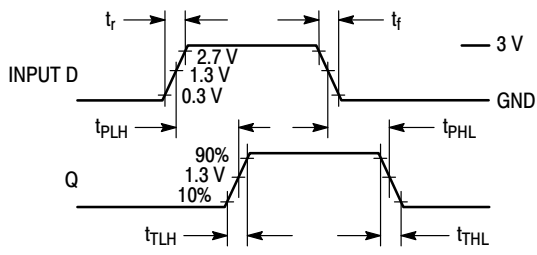


Figure 1.

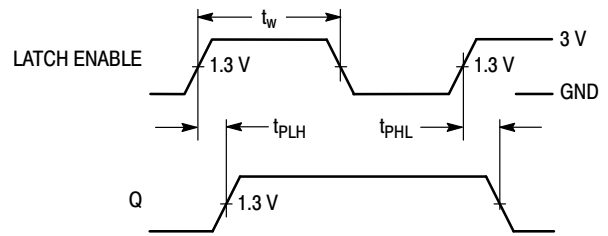


Figure 2.

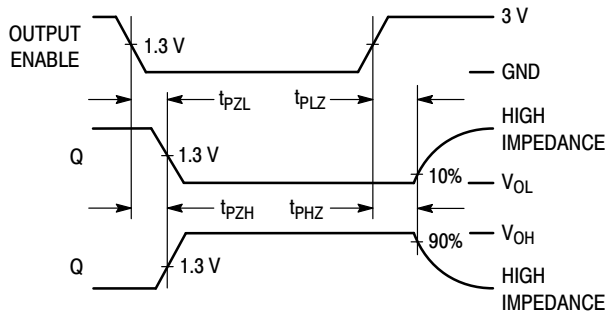


Figure 3.

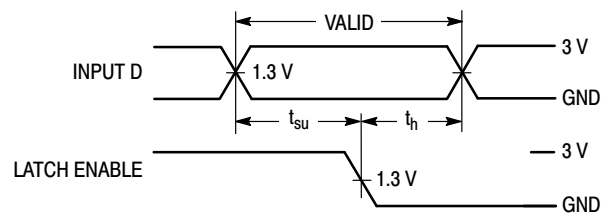
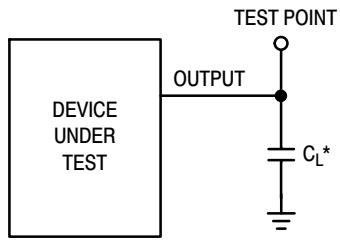


Figure 4.

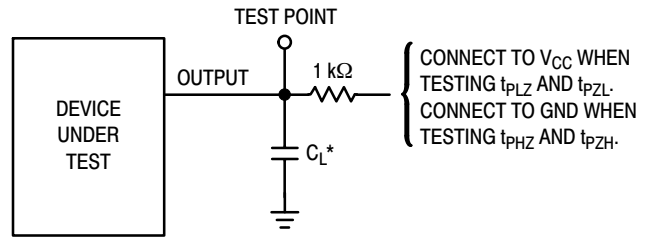
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TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5.



*Includes all probe and jig capacitance

Figure 6.

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PACKAGE DIMENSIONS

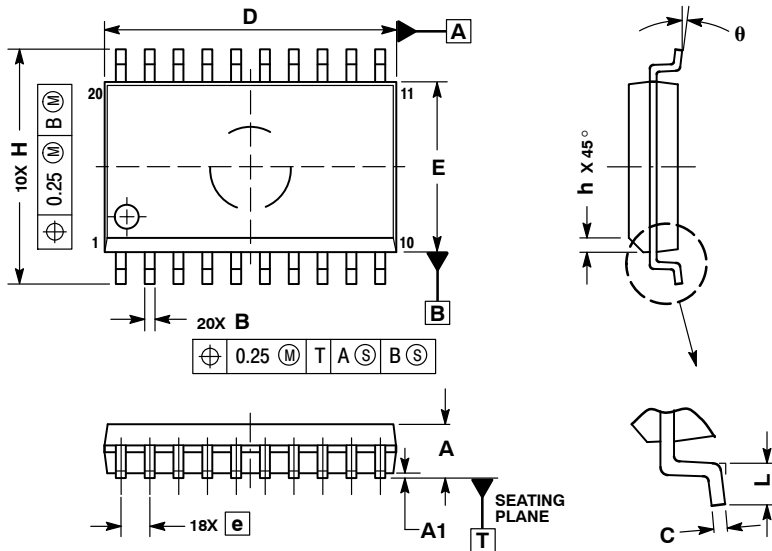
PDIP-20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-20
DW SUFFIX
CASE 751D-05
ISSUE G



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| theta | 0° | 7° |

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PACKAGE DIMENSIONS

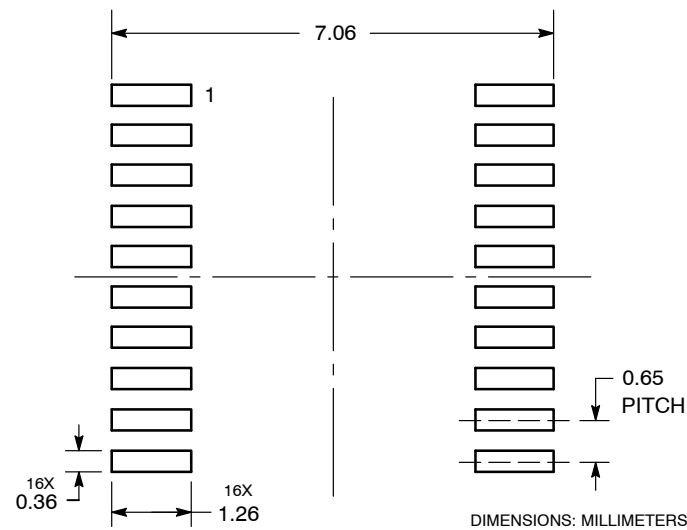
TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

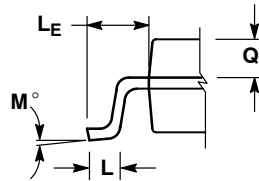
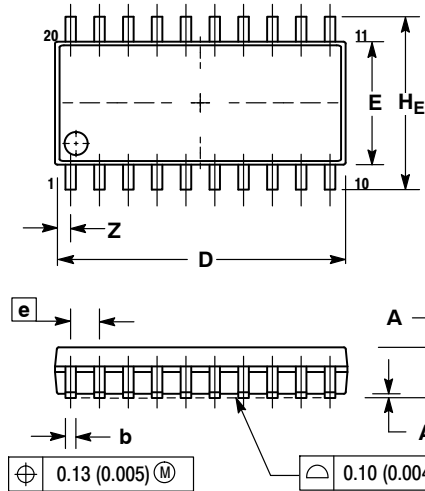
SOLDERING FOOTPRINT



MC74HCT373A

PACKAGE DIMENSIONS

SOEIAJ-20
F SUFFIX
CASE 967-01
ISSUE A



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.15 | 0.25 | 0.006 | 0.010 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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