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February 2015

FDMA6676PZ

Single P-Channel PowerTrench® MOSFET

-30 V, -11 A, 13.5 m Ω

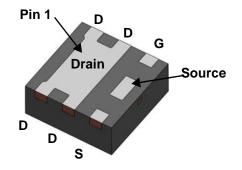
Features

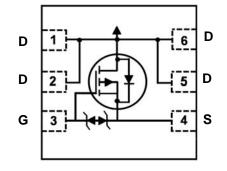
- Max $r_{DS(on)} = 13.5 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$
- 25V V_{GS} Extended Operating Rating
- 30V V_{DS} Blocking
- 2x2mm Form Factor
- Low Profile 0.8 mm maximum
- Integrated Protection Diode
- RoHS Compliant
- Halogen Free



General Description

This device is an ultra low resistance P-Channel FET. It is designed for power line load switching applications and reverse polarity protection. It is especially optimized for voltage rails that can climb as high as 25V. Typical end systems include laptop computers, tablets and mobile phone. Applications include battery protection, input power line protection and charge path protection, including USB and other charge paths. The FDMA6676PZ has an enhanced $V_{\rm GS}$ rating of 25V specifically designed to simplify installation. When used as reverse polarity protection, with gate tied to ground and drain tied to V input, it is designed to support operating input voltages that can raise as high as 25V without the need for external Zener protection on the gate. Its small 2x2x0.8 form factor make it an ideal part for mobile and space constrained applications.





MicroFET 2X2 (Bottom View)

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Paran	neter		Ratings	Units
V _{DS}	Drain to Source Voltage			-30	V
V _{GS}	Gate to Source Voltage			±25	V
1	Drain Current -Continuous	T _A = 25 °C	(Note 1a)	-11	۸
'D	-Pulsed		(Note 3)	-165	Α
D	Power Dissipation	T _A = 25 °C	(Note 1a)	2.4	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1b)	0.9	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
676	FDMA6676PZ	MicroFET 2X2	7 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Parameter

Off Characteristics							
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V	
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-19		mV/°C	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μΑ	
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μΑ	

Test Conditions

Min

Тур

Max

Units

On Characteristics

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1.2	-2	-2.6	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		5.9		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}, I_D = -11 \text{ A}$		11	13.5	mΩ
		$V_{GS} = -4.5 \text{ V}, I_D = -8 \text{ A}$		19	27	
		$V_{GS} = -10 \text{ V}, I_D = -11 \text{ A},$ $T_J = 125 \text{ °C}$		14.5	21	
9 _{FS}	Forward Transconductance	$V_{DD} = -5 \text{ V}, \ I_{D} = -11 \text{ A}$		38		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45 V V 0 V	1440	2160	pF
C _{oss}	Output Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	477	720	pF
C _{rss}	Reverse Transfer Capacitance	1 = 1 101112	458	690	pF
R_q	Gate Resistance		12		Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	.,	8.8	18	ns
t _r	Rise Time	$V_{DD} = -15 \text{ V, } I_{D} = -11 \text{ A,}$ $V_{GS} = -10 \text{ V, } R_{GEN} = 6 \Omega$	19	34	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = -10 V, K _{GEN} = 6 12	87	139	ns
t _f	Fall Time		72	115	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to -10 V	33	46	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } -4.5 \text{ V} V_{DD} = -15 \text{ V},$	20	28	nC
Q _{gs}	Gate to Source Charge	I _D = -11 A	4.5		nC
Q _{gd}	Gate to Drain "Miller" Charge		13		nC

Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2 \text{ A}$ (Note 2)	-0.7	-1.2	V
		$V_{GS} = 0 \text{ V}, I_S = -11 \text{ A}$ (Note 2)	-0.9	-1.4	V
t _{rr}	Reverse Recovery Time	- I _E = -11 A, di/dt = 100 A/μs	31	50	ns
Q _{rr}	Reverse Recovery Charge	T _F = -11 A, αι/αι = 100 A/μs	9	18	nC

NOTES:

^{1.} R_{8JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{9CA} is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.

^{3.} Pulse Id refers to Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25 °C unless otherwise noted

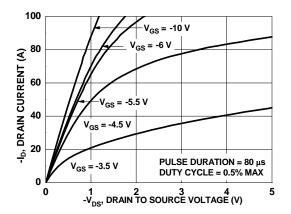


Figure 1. On-Region Characteristics

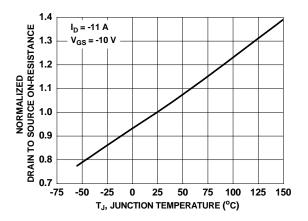


Figure 3. Normalized On-Resistance vs Junction Temperature

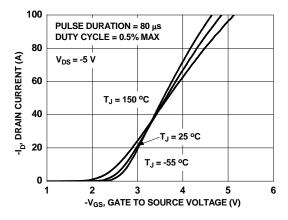


Figure 5. Transfer Characteristics

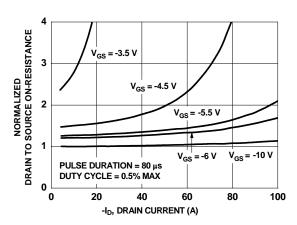


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

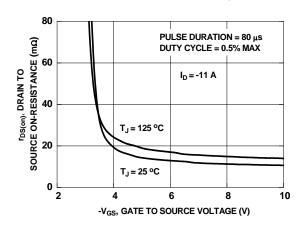


Figure 4. On-Resistance vs Gate to Source Voltage

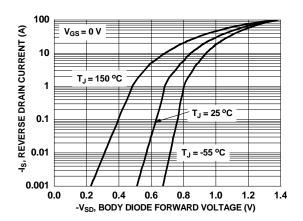


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

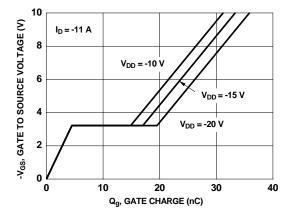


Figure 7. Gate Charge Characteristics

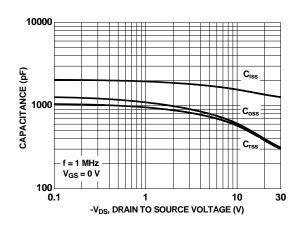


Figure 8. Capacitance vs Drain to Source Voltage

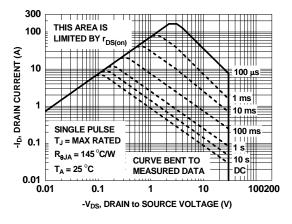


Figure 9. Forward Bias Safe Operating Area

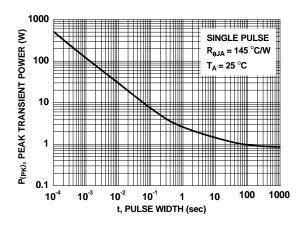


Figure 10. Single Pulse Maximum Power Dissipation

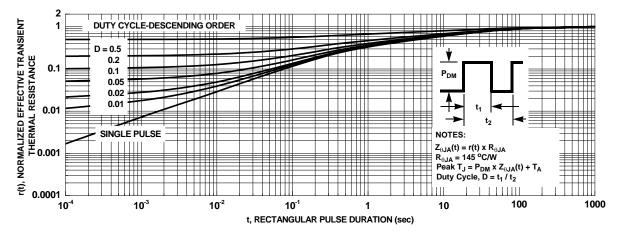
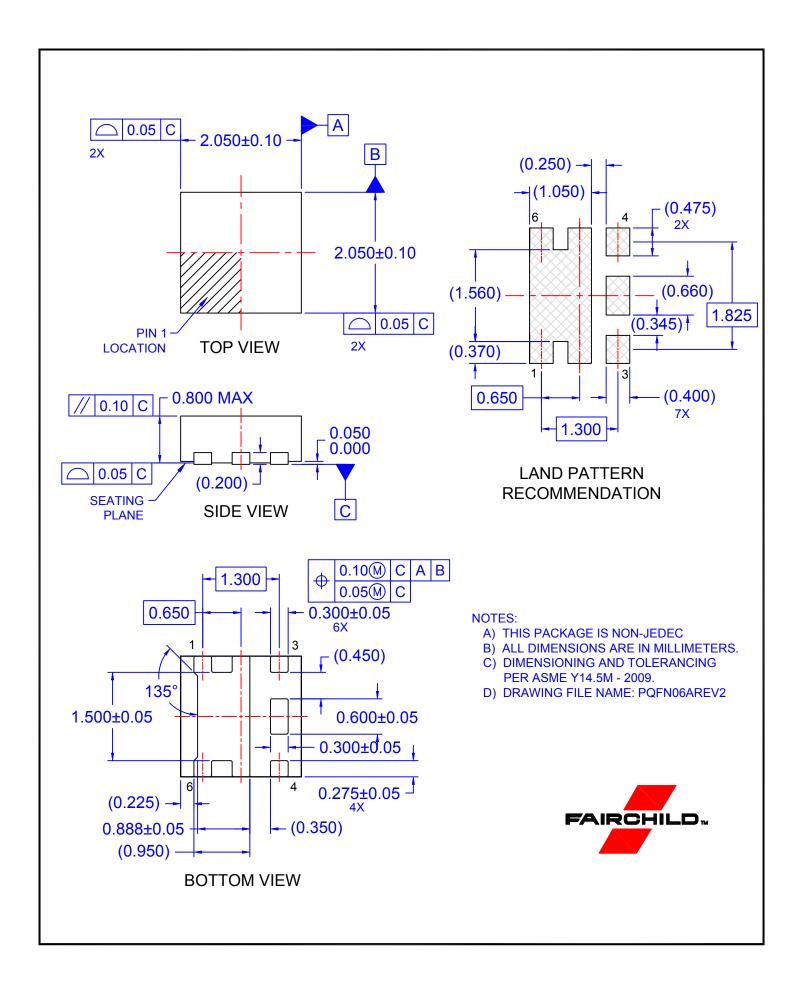


Figure 11. Junction-to-Ambient Transient Thermal Response Curve



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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru 4 moschip.ru 9