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July 2016

FDD86581_F085

N-Channel PowerTrench[®] MOSFET 60 V, 25 A, 15 m Ω

Features

- Typical $R_{DS(on)}$ = 12.3 m Ω at V_{GS} = 10V, I_D = 25 A
- Typical $Q_{g(tot)}$ = 12.6 nC at V_{GS} = 10V, I_D = 25 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

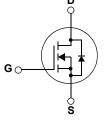
Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems





(TO-252)



For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/package-drawings/TO/TO252A03.pdf

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units	
V_{DSS}	Drain-to-Source Voltage		60	V	
V_{GS}	Gate-to-Source Voltage		±20	V	
	Drain Current - Continuous (V_{GS} =10) (Note 1) T_C = 25°C Pulsed Drain Current T_C = 25°C		25	A	
I _D			See Figure 4		
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	14.5	mJ	
D	Power Dissipation		48.4	W	
P_D	Derate Above 25°C		0.32	W/°C	
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.1	°C/W	
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	52	°C/W	

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^{\circ}C$, $L = 60 \mu H$, $I_{AS} = 22A$, $V_{DD} = 60 V$ during inductor charging and $V_{DD} = 0 V$ during time in avalanche.
- 3: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86581	FDD86581_F085	D-PAK(TO-252)	13"	16mm	2500units

Units

Max.

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

Parameter

Off Characteristics							
B _{VDSS}	Drain-to-Source Breakdown Voltage	I _D = 250μA,	V _{GS} = 0V	60	-	-	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} =60V,	$T_J = 25^{\circ}C$	-	-	1	μΑ
		$V_{GS} = 0V$	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	-	1	mA
less	Gate-to-Source Leakage Current	$V_{CS} = \pm 20V$,	-	-	±100	nA

Test Conditions

Min.

Тур.

On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.0	2.8	4.0	V
R _{DS(on)} Drain to Source On Resistance	Drain to Source On Begintance	I _D = 25A,	$T_{J} = 25^{\circ}C$	-	12.3	15	mΩ
	V _{GS} = 10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	24.4	30	mΩ	

Dynamic Characteristics

C _{iss}	Input Capacitance	.,		-	880	-	pF
C _{oss}	Output Capacitance		$V_{DS} = 30V, V_{GS} = 0V,$ f = 1MHz		280	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112			15	-	pF
R_g	Gate Resistance	V _{GS} = 0.5V, f = 1M	V _{GS} = 0.5V, f = 1MHz		3.1	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V _{GS} = 0 to 10V	V _{DD} = 30V	-	12.6	19	nC
$Q_{g(th)}$	Threshold Gate Charge	V _{GS} = 0 to 2V	I _D = 25A	-	1.7	-	nC
Q_{gs}	Gate-to-Source Gate Charge		-	-	4.3	-	nC
Q_{ad}	Gate-to-Drain "Miller" Charge			-	2.8	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	21	ns
t _{d(on)}	Turn-On Delay		-	7.5	-	ns
t _r	Rise Time	V _{DD} = 30V, I _D = 25A,	-	6.5	-	ns
t _{d(off)}	Turn-Off Delay	V_{GS} = 10V, R_{GEN} = 6Ω	-	14.6	-	ns
t _f	Fall Time		-	4.2	-	ns
t _{off}	Turn-Off Time		-	-	28	ns

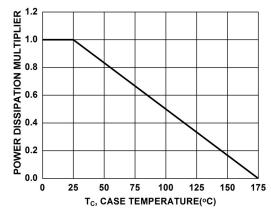
Drain-Source Diode Characteristics

I Source-to-Drain Dione Voltage	Source to Drain Diode Voltage	$I_{SD} = 25A, V_{GS} = 0V$	-	0.92	1.3	V
	$I_{SD} = 12.5A, V_{GS} = 0V$	-	0.85	1.2	V	
t _{rr}	Reverse-Recovery Time	V _{DD} = 48V, I _F = 25A,	-	35	52	ns
Q _{rr}	Reverse-Recovery Charge	$dI_{SD}/dt = 100A/\mu s$	-	21	32	nC

Note

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics



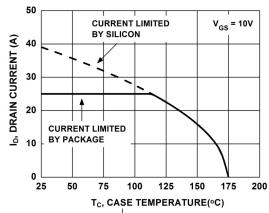


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

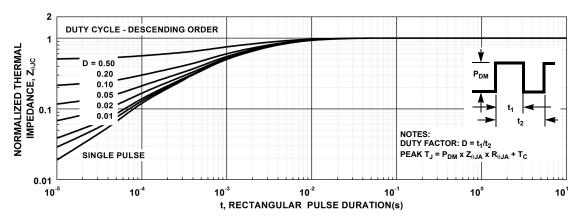


Figure 3. Normalized Maximum Transient Thermal Impedance

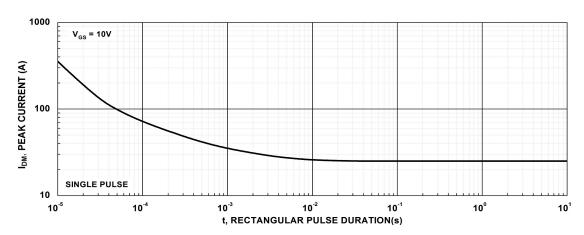
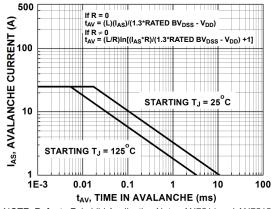


Figure 4. Peak Current Capability

Typical Characteristics 1000 ID, DRAIN CURRENT (A) 100 10 100us **OPERATION IN THIS** 1ms AREA MAY BE SINGLE PULSE LIMITED BY RDS(on) 10ms TJ = MAX RATED 100ms TC = 25°C 0.01 10 100 0.1

Figure 5. Forward Bias Safe Operating Area

V_{DS}, DRAIN TO SOURCE VOLTAGE (V)



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

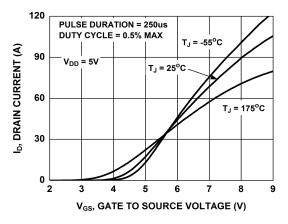


Figure 7. Transfer Characteristics

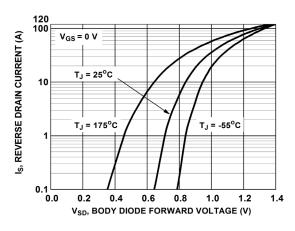


Figure 8. Forward Diode Characteristics

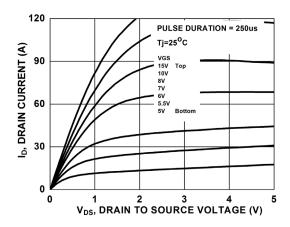


Figure 9. Saturation Characteristics

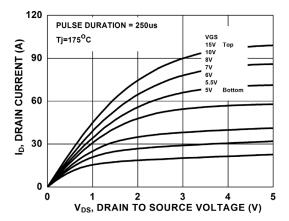


Figure 10. Saturation Characteristics

Typical Characteristics

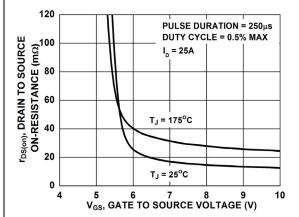


Figure 11. R_{DSON} vs. Gate Voltage

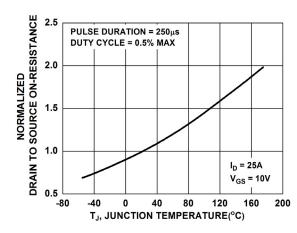


Figure 12. Normalized R_{DSON} vs. Junction Temperature

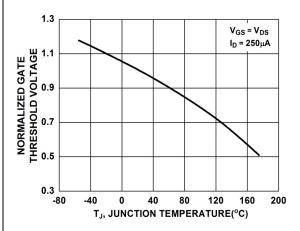


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

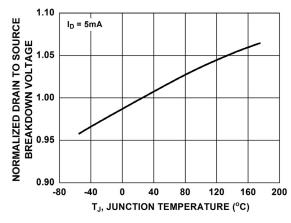


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

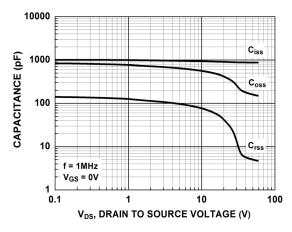


Figure 15. Capacitance vs. Drain to Source Voltage

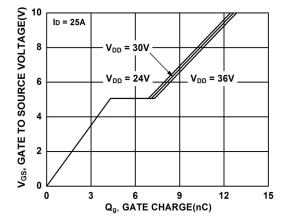


Figure 16. Gate Charge vs. Gate to Source Voltage





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