REFERENCE DESIGN

IRAUDAMP5

120W x 2 Channel Class D Audio Power Amplifier Using the IRS2092S and IRF6645

By

Jun Honda, Manuel Rodríguez and Jorge Cerezo

Fig 1

CAUTION: International Rectifier suggests the following guidelines for safe operation and handling of IRAUDAMP5 Demo Board;

- **Always wear safety glasses whenever operating Demo Board**
- **Avoid personal contact with exposed metal surfaces when operating Demo Board**
- **Turn off Demo Board when placing or removing measurement probes**

Table of Contents

Introduction

The IRAUDAMP5 reference design is a two-channel, 120W half-bridge Class D audio power amplifier. This reference design demonstrates how to use the IRS2092S Class D audio controller and gate driver IC, implement protection circuits, and design an optimum PCB layout using the IRF6645 DirectFET MOSFETs. The resulting design requires no heatsink for normal operation (one-eighth of continuous rated power). The reference design provides all the required housekeeping power supplies for ease of use. The two-channel design is scalable for power and the number of channels.

Applications

AV receivers
Home theater systems
Mini component stereos
Powered speakers
Sub-woofers
Musical Instrument amplifiers
Automotive after market amplifiers

Features

Output Power:	120W x 2 channels, Total Harmonic Distortion (THD+N) = 1%, 1 kHz
Residual Noise:	170µV, IHF-A weighted, AES-17 filter
Distortion:	0.005% THD+N @ 60W, 4Ω
Efficiency:	96% @ 120W, 4Ω, single-channel driven, Class D stage
Multiple Protection Features:	Over-current protection (OCP), high side and low side Over-voltage protection (OVP), Under-voltage protection (UVP), high side and low side DC-protection (DCP), Over-temperature protection (OTP)
PWM Modulator:	Self-oscillating half-bridge topology with optional clock synchronization

Specifications

General Test Conditions (unless otherwise noted)		Notes / Conditions
Supply Voltage	±35V	
Load Impedance	8-4Ω	
Self-Oscillating Frequency	400kHz	No input signal, Adjustable
Gain Setting	26dB	1Vrms input yields rated power

Electrical Data	Typical	Notes / Conditions
IR Devices Used	IRS2092S Audio Controller and Gate-Driver, IRF6645 DirectFET MOSFETs	
Modulator	Self-oscillating, second order sigma-delta modulation, analog input	
Power Supply Range	± 25V to ±35V	Bipolar power supply
Output Power CH1-2: (1% THD+N)	120W	1kHz
Output Power CH1-2: (10% THD+N)	170W	1kHz
Rated Load Impedance	8-4Ω	Resistive load
Standby Supply Current	±100mA	No input signal
Total Idle Power Consumption	7W	No input signal
Channel Efficiency	96%	Single-channel driven, 120W, Class D stage

.

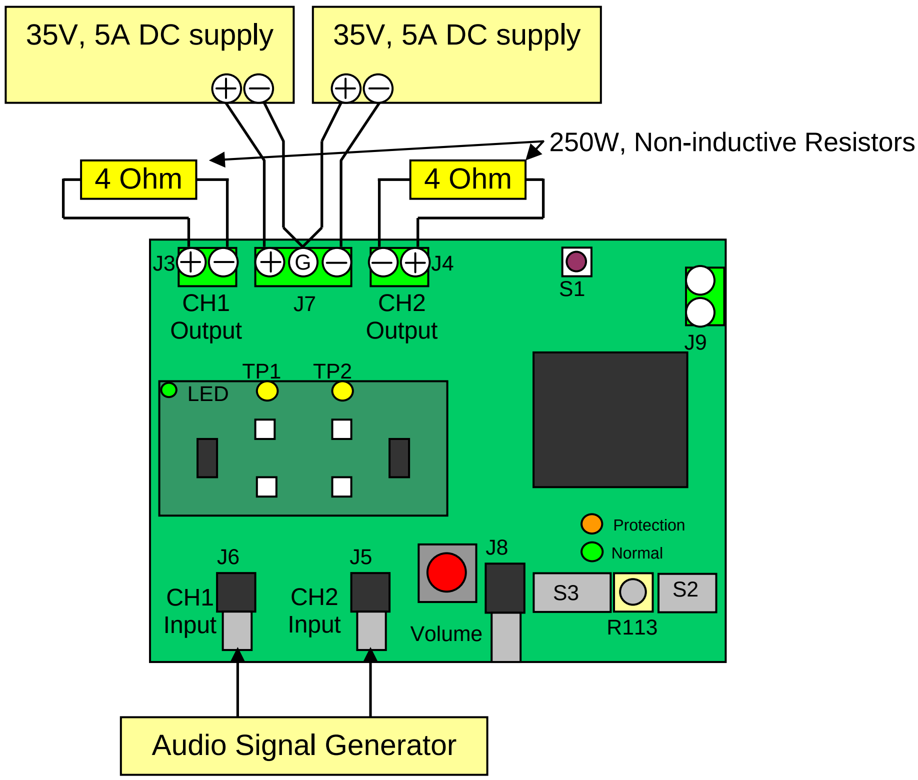
Audio Performance	*Before Demodulator	Class D Output	Notes / Conditions
THD+N, 1W	0.009%	0.01%	
THD+N, 10W	0.003%	0.004%	1kHz, Single-channel driven
THD+N, 60W	0.003%	0.005%	
THD+N, 100W	0.008%	0.010%	
Dynamic Range	101dB	101dB	A-weighted, AES-17 filter, Single-channel operation
Residual Noise, 22Hz - 20kHzAES17	170µV	170µV	Self-oscillating – 400kHz
Damping Factor	2000	170	1kHz, relative to 4Ω load
Channel Separation	95dB	90dB	100Hz
	85dB	80dB	1kHz
	75dB	65dB	10kHz
Frequency Response : 20Hz-20kHz	N/A	±1dB	1W, 4Ω - 8Ω Load
: 20Hz-35kHz		±3dB	

Thermal Performance	Typical	Notes / Conditions
Idling	T_C =30°C T_{PCB}=37°C	No signal input, T_A=25°C
2ch x 15W (1/8 rated power)	T_C =54°C T_{PCB}=67°C	Continuous, T_A=25°C
2ch x 120W (Rated power)	T_C =80°C T_{PCB}=106°C	At OTP shutdown @ 150 sec, T_A=25°C

Physical Specifications	
Dimensions	5.8”(L) x 5.2”(W)

Note: Class D Specifications are typical
*Before demodulator refers to audio performance measurements of the Class D output power stage only, with preamp and output filter bypassed this means performance measured before the low pass filter.

Connection Setup



Typical Test Setup

Fig 2

Connector Description

CH1 IN	J6	Analog input for CH1
CH2 IN	J5	Analog input for CH2
POWER	J7	Positive and negative supply (+B / -B)
CH1 OUT	J3	Output for CH1
CH2 OUT	J4	Output for CH2
EXT CLK	J8	External clock sync
DCP OUT	J9	DC protection relay output

Test Procedures

1. Connect 4Ω, 250W load to outputs connectors, J3 and J4 and Audio Precision analyzer (AP).
2. Connect Audio Signal Generator to J6 and J5 for CH1 and CH2 respectively (AP).
3. Connect a dual power supply to J7, pre-adjusted to ±35V, as shown in Figure 2 above.
4. Set switch S3 to middle position (self oscillating).
5. Set volume level knob R108 fully counter-clockwise (minimum volume).
6. Turn on the power supply. Note: always apply or remove the ±35V at the same time.
7. Orange LED (Protection) should turn on almost immediately and turn off after about 3s.
8. Green LED (Normal) then turns on after orange LED is extinguished and should stay on.
9. One second after the green LED turns on; the two blue LEDS on the Daughter Board should turn on and stay on for each channel, indicating that a PWM signal is present at LO
10. With an Oscilloscope, monitor switching waveform at test points TP1 and TP2 of CH1 and CH2 on Daughter Board.
11. If necessary, adjust the self-oscillating switching frequency of AUDAMP5 to 400KHz ±5kHz using potentiometer R29P. For IRAUDAMP5, the self-oscillating switching frequency is pre-calibrated to 400 KHz. To modify the AUDAMP5 frequency, change the values of potentiometers R21 and R22 for CH1 and CH2 respectively.
12. Quiescent current for the positive supply should be 70mA ±10mA at +35V.
13. Quiescent current for the negative supply should be 100mA ±10mA at –35V.
14. Push S1 switch, (Trip and Reset push-button) to restart the sequence of LEDs indicators, which should be the same as noted above in steps 6-9.

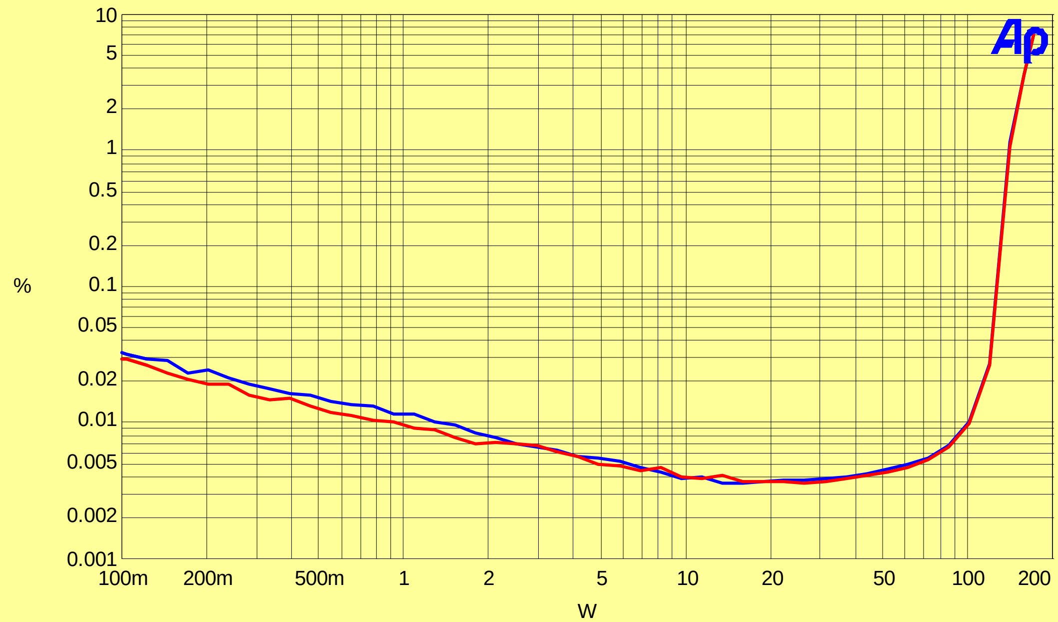
Audio Tests:

15. Apply 1 V RMS at 1KHz from the Audio Signal Generator
16. Turn control volume up (R108 clock-wise) to obtain an output reading of 100Watts for all subsequent tests as shown on the Audio Precision graphs below, where measurements are across J3 and J2 with an AES-17 Filter

Typical Performance

The tests below were performed under the following conditions:
±B supply = ±35V, load impedance = 4Ω resistive load, 1kHz audio signal,
Self oscillator @ 400kHz and internal volume-control set to give required output with 1Vrms input signal, with AES-17 Filter, unless otherwise noted.

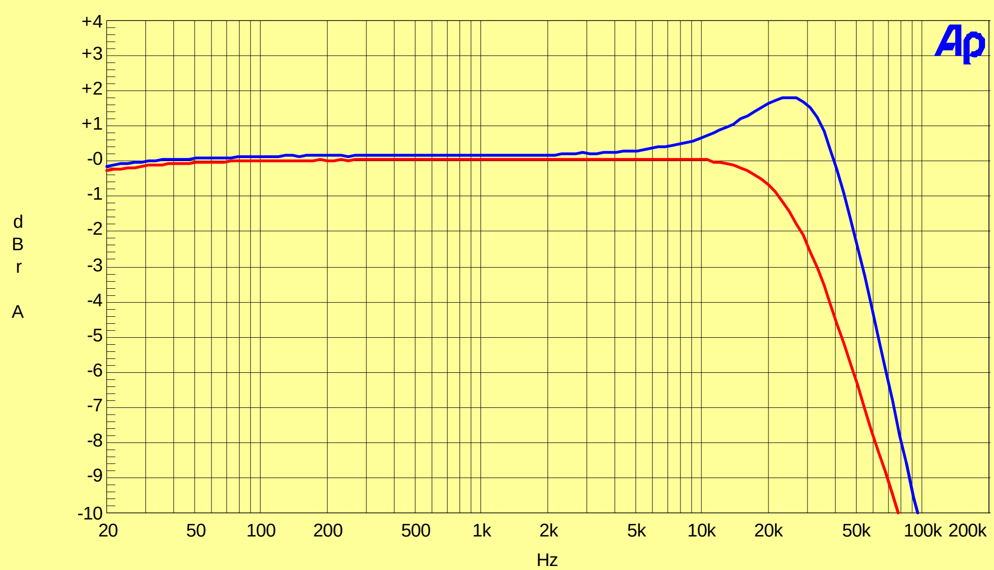
THD versus Power:



Blue, CH1 - 4 Ohm
Red, CH2 - 4 Ohm

Figure 18. Total Harmonics Distortion + Noise (THD+N) versus power output

Fig 3



Frequency Response:

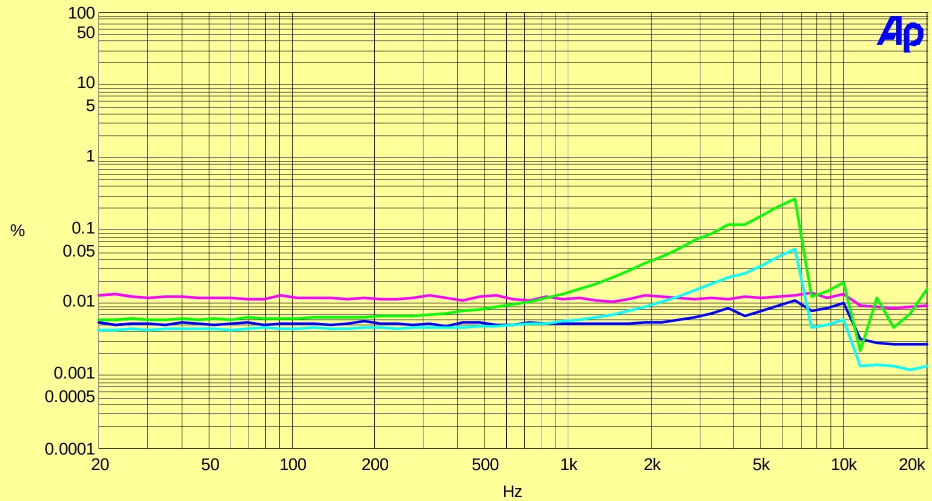
Red CH1 - 4 Ohm, 2V Output
Blue CH1 - 8 Ohm, 2V Output

Frequency Characteristics vs. Load Impedance

Fig 4

•

THD versus Frequency:

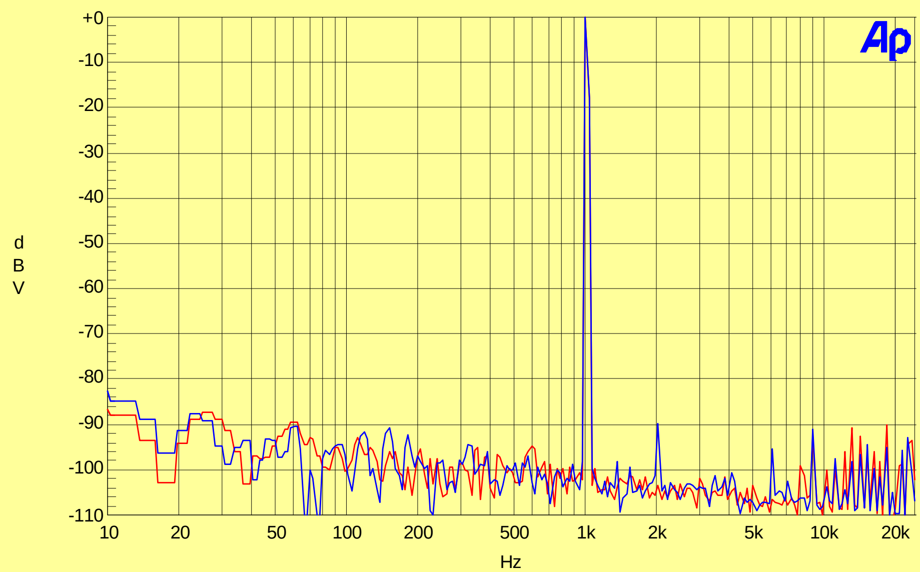


Pink	CH1, 1W Output
Blue	CH1, 10W Output
Cyan	CH1, 50W Output
Green	CH1, 100W Output

THD+N Ratio vs. Frequency

Fig 5

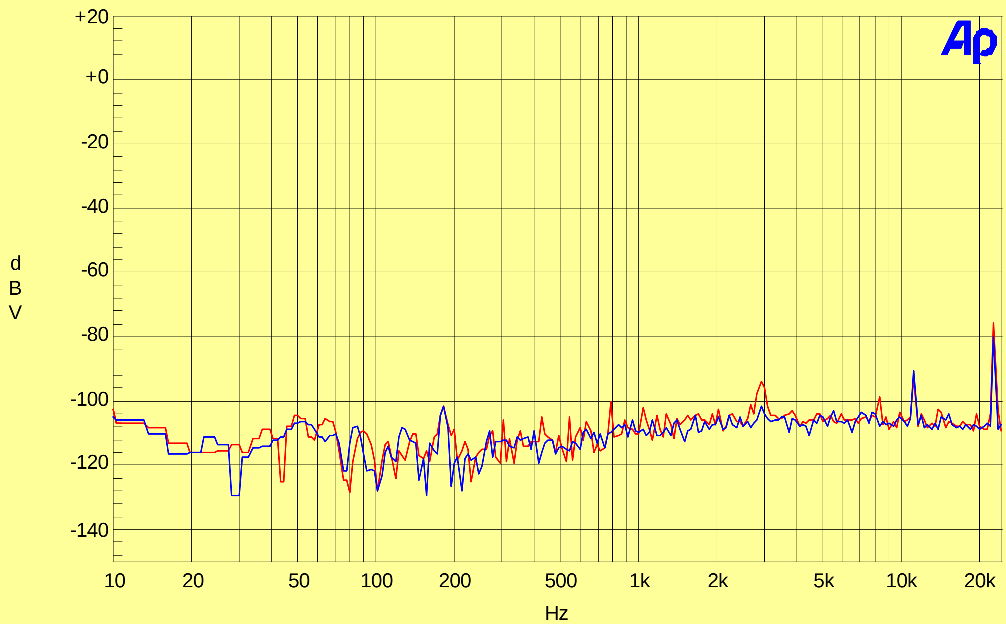
Frequency Spectrum :



Red	CH1, 1V, 1kHz, Self Oscillator @ 400kHz
Blue	CH2, 1V, 1kHz, Self Oscillator @ 400kHz

Fig 6 ***Frequency Spectrum***

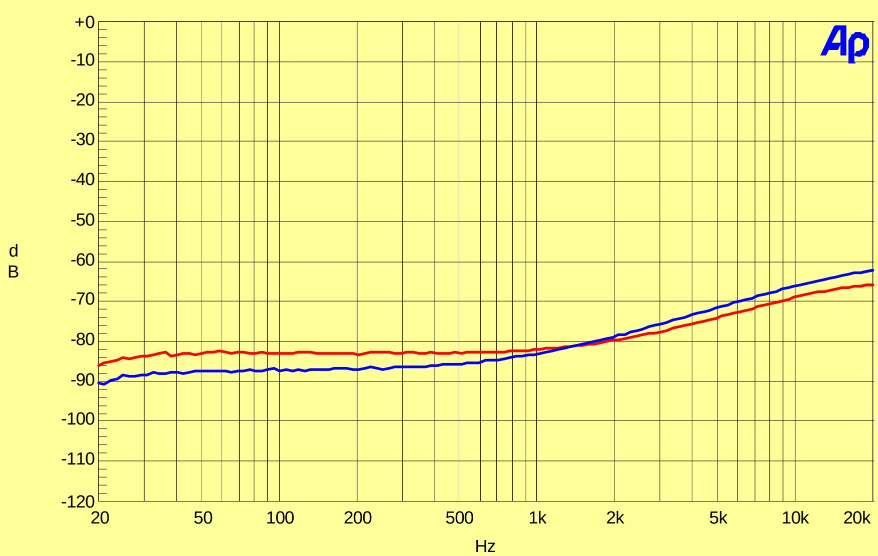
Floor Noise:



Red CH1 - ACD, No signal, Self Oscillator @ 400kHz
Blue CH2 - ACD, No signal, Self Oscillator @ 400kHz

***Fig 7** Residual Noise (ACD)*

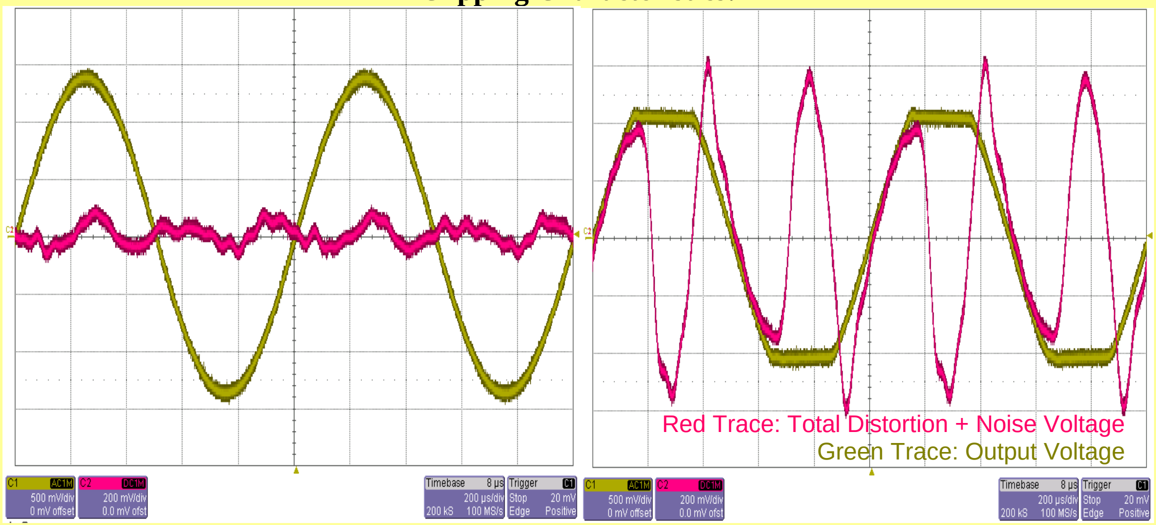
Channel Separation:



Red CH1 – CH2, 60W
Blue CH2 – CH1, 60W

***Fig 8** Channel Separation vs. Frequency*

Clipping Characteristics:



60W / 4Ω, 1kHz, THD+N=0.008%

174W / 4Ω, 1kHz, THD+N=10%

Measured Output and Distortion Waveforms

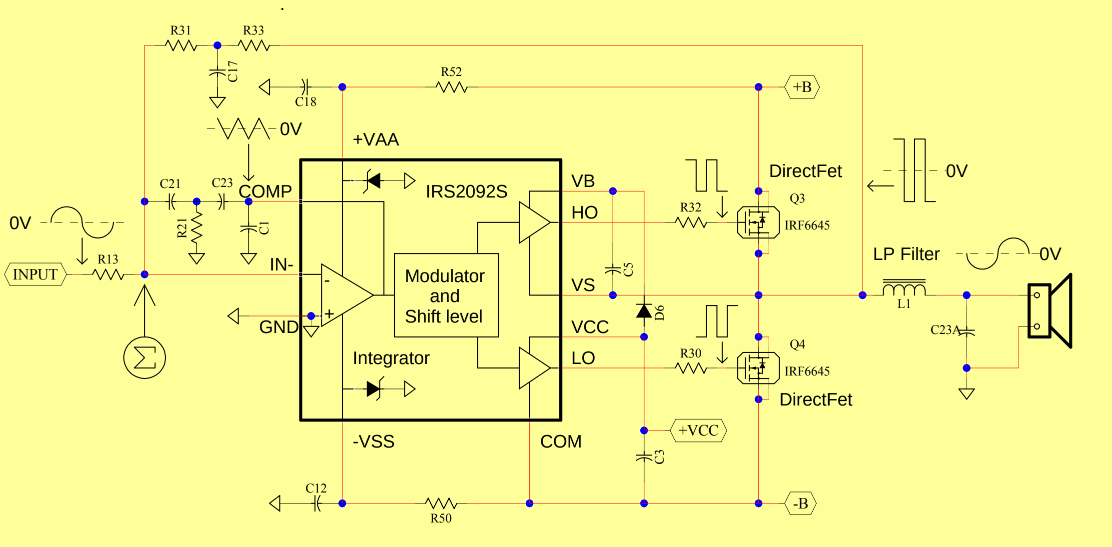
Fig 9

IRAUDAMP5 Theory of Operation

Referring to Fig 10 below, the input error amplifier of the IRS2092S forms a front-end second-order integrator with C1, C21, C23 and R21. This integrator also receives a rectangular feedback waveform from R31, R33 and C17 into the summing node at IN- from the Class D power stage switching node (connection of DirectFET Q3 and DirectFET Q4). The quadratic oscillatory waveform of the switch node serves as a powered carrier signal from which the audio is recovered at the speaker load through a single-stage LC filter. The modulated signal is created by the fluctuations of the analog input signal at R13 that shifts the average value of this quadratic waveform through the gain relationship between R13 and R31 + R33 so that the duty cycle varies according to the instantaneous signal level of the analog input signal at R13.

R33 and C17 act to immunize the rectangular waveform from possible narrow noise spikes that may be created by parasitic impedances on the power output stage. The IRS2092S input integrator then processes the signal from the summing node to create the required triangle wave amplitude at the COMP output. The triangle wave then is converted to Pulse Width Modulation, or PWM, signals that are internally level-shifted Down and Up to the negative and positive supply rails. The level shifted PWM signals are called LO for low output, and HO for high output, and have opposite polarity. A programmable amount of dead time is added between the gate signals to avoid cross conduction between the power MOSFETs. The IRS2092S drives two IRF6645 DirectFET MOSFETs in the power stage to provide the amplified PWM waveform. The amplified analog output is reconstructed by demodulating the powered PWM at the switch node, called VS. (Show as VS on the schematic)This is done by means of the LC low-pass filter (LPF) formed by L1 and C23A, which filters out the Class D switching carrier signal, leaving the audio powered output at the speaker load. A single stage output filter can be used with switching

frequencies of 400 kHz and greater; lower switching frequencies may require additional filter components.
+VCC is referenced to –B and provides the supply voltage to the LO gate driver. D6 and C5 form a bootstrap supply that provides a floating voltage to the HO gate driver. The VAA and VSS input supplies are derived from +B and -B via R52 and C18, and R50 and C12, respectively. Thus, a fully functional Class D PWM amplifier plus driver circuit is realized in an SO16 package with just a few small components.



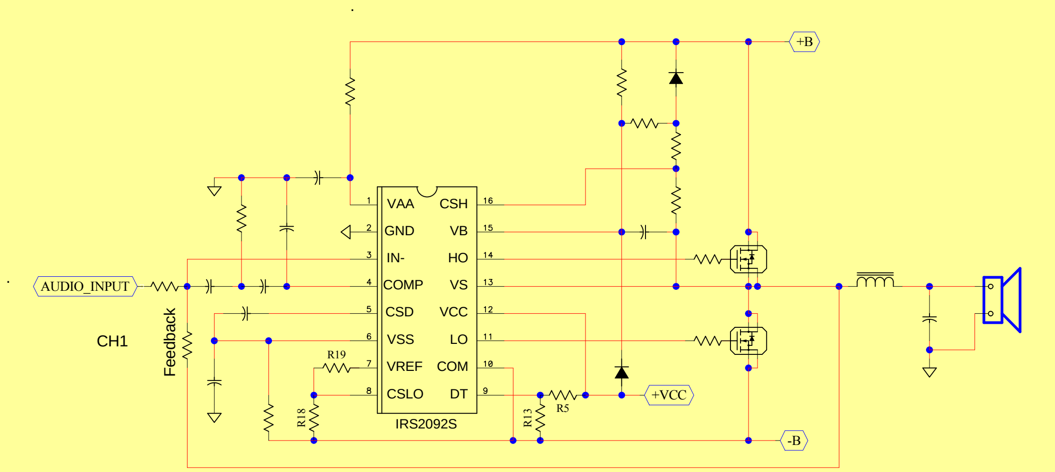
Simplified Block Diagram of IRAUDAMP5 Class D Amplifier

Fig 10

System overview

IRS2092S Gate Driver IC

The IRAUDAMP5 uses the IRS2092S, a high-voltage (up to 200V), high-speed power MOSFET PWM generator and gate driver with internal dead-time and protection functions specifically designed for Class D audio amplifier applications. These functions include OCP and UVP. Bi-directional current protection for both the high-side and low-side MOSFETs are internal to the IRS2092S, and the trip levels for both MOSFETs can be set independently. In this design, the dead time can be selected for optimized performance by minimizing dead time while preventing shoot-through. As a result, there is no gate-timing adjustment on the board. Selectable dead time through the DT pin voltage is an easy and reliable function which requires only two external resistors, R11 and R9 as shown on Fig11 below.



System-level View of Class D Controller and Gate Driver IRS2092S

Fig 11

Selectable Dead-Time

The dead time of the IRS2092S is based on the voltage applied to the DT pin. (Fig 12) An internal comparator determines the programmed dead time by comparing the voltage at the DT pin with internal reference voltages. An internal resistive voltage divider based on different ratios of VCC negates the need for a precise reference voltage and sets threshold voltages for each of the four programmable settings. Shown in the table below are component values for programmable dead times between 25 and 105 ns. To avoid drift from the input bias current of the DT pin, a bias current of greater than 0.5mA is suggested for the external resistor divider circuit. Resistors with up to 5% tolerance can be used.

Selectable Dead-Time

Dead-time mode	Dead time	R5	R13	DT voltage	
DT1	~25ns	3.3k	8.2k	0.71 x Vcc	Default
DT2	~40ns	5.6k	4.7k	0.46 x Vcc	
DT3	~65ns	8.2k	3.3k	0.29 x Vcc	
DT4	~105ns	open	<10k	0 x Vcc	

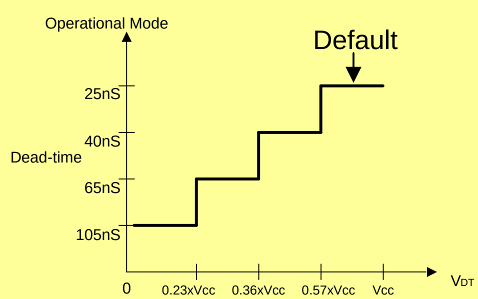


Fig 12 *Dead-time Settings vs. V_{DT} Voltage*

Over-Current Protection (OCP)

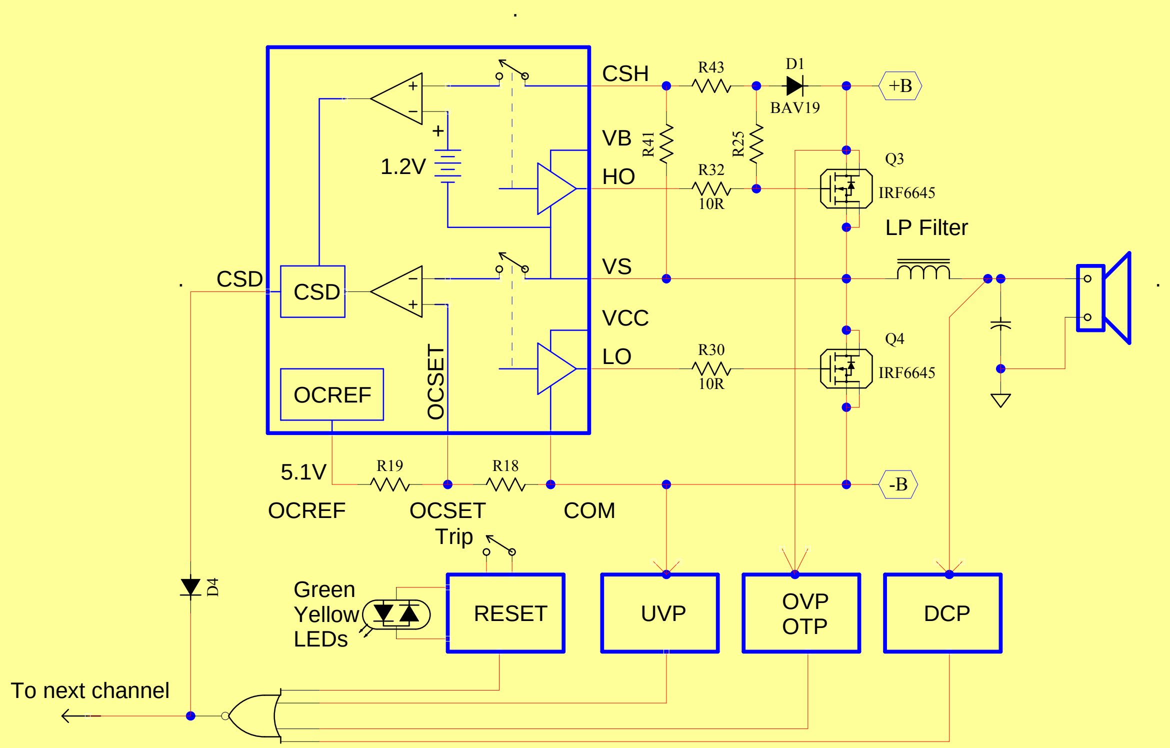
In the IRAUDAMP5, the IRS2092S gate driver accomplishes OCP internally, a feature discussed in greater detail in the "Protection" section.

Offset Null (DC Offset)

The IRAUDAMP5 is designed such that no output-offset nullification is required, thanks to closed loop operation. DC offsets are tested to be less than ±20mV.

Protection

The IRAUDAMP5 has a number of protection circuits to safeguard the system and speaker as shown in the figure 13 below, which fall into one of two categories – internal faults and external faults, distinguished by the manner in which a fault condition is treated. Internal faults are only relevant to the particular channel, while external faults affect the whole board. For internal faults, only the offending channel is stopped. The channel will hiccup until the fault is cleared. For external faults, the whole board is stopped using the shutdown sequencing described earlier. In this case, the system will also hiccup until the fault is cleared, at which time it will restart according to the startup sequencing described earlier.



Functional Block Diagram of Protection Circuit Implementation

Fig 13

Internal Faults

OCP and OTP are considered internal faults, which will only shutdown the particular channel by pulling low the relevant CSD pin. The channel will shutdown for about one-half a second and will hiccup until the fault is cleared.

Over-Temperature Protection (OTP, Fig 14)

A separate PTC resistor is placed in close proximity to the high-side IRF6645 DirectFET MOSFET for each of the amplifier channels. If the resistor temperature rises above 100°C, the OTP is activated. The OTP protection will only shutdown the relevant channel by pulling the CSD pin low and will recover once the temperature at the PTC has dropped sufficiently. This temperature protection limit yields a PCB temperature at the MOSFET of about 100°C, which is limited by the PCB material and not by the operating range of the MOSFET.

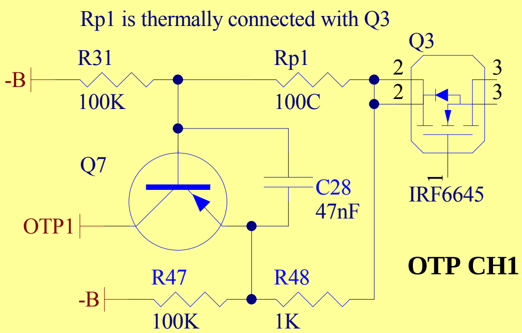


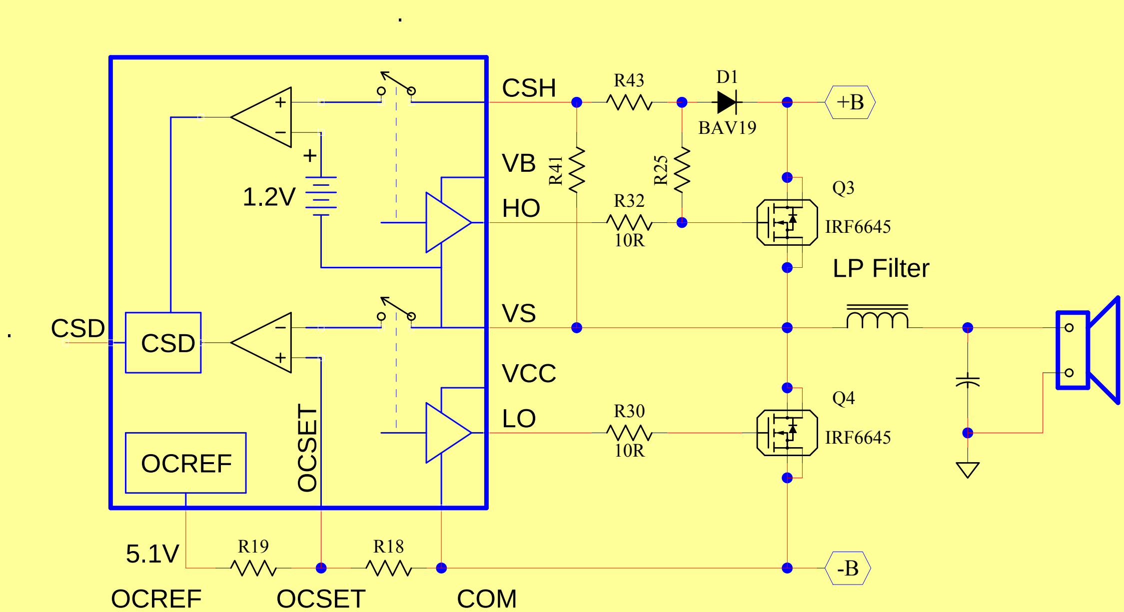
Fig 14

Over-Current Protection (OCP)

The OCP internal to the IRS2092S shuts down the IC if an OCP is sensed in either of the output MOSFETs. For a complete description of the OCP circuitry, please refer to the IRS2092S datasheet. Here is a brief description:

Low-Side Current Sensing

Fig 15 shows the low side MOSFET as is protected from an overload condition by measuring the low side MOSFET drain-to-source voltage during the low side MOSFET on state, and will shut down the switching operation if the load current exceeds a preset trip level. The voltage setting on the OCSET pin programs the threshold for low-side over-current sensing. Thus, if the VS voltage during low-side conduction is higher than the OCSET voltage, the IRS2092S will trip and CSD goes down. It is recommended to use VREF to supply a reference voltage to a resistive divider (R19 and R18 for CH1) to generate a voltage to OCSET; this gives better variability against VCC fluctuations. For IRAUDAMP5, the low-side over-current trip level is set to 0.65V. For IRF6645 DirectFET MOSFETs with a nominal $R_{DS\text{-}ON}$ of 28mOhms at 25°C, this results in a ~23A maximum trip level. Since the $R_{DS\text{-}ON}$ is a function of temperature, the trip level is reduced to ~15A at 100°C.



Simplified Functional Block Diagram of High-Side and Low-Side Current Sensing (CH1)

Fig 15

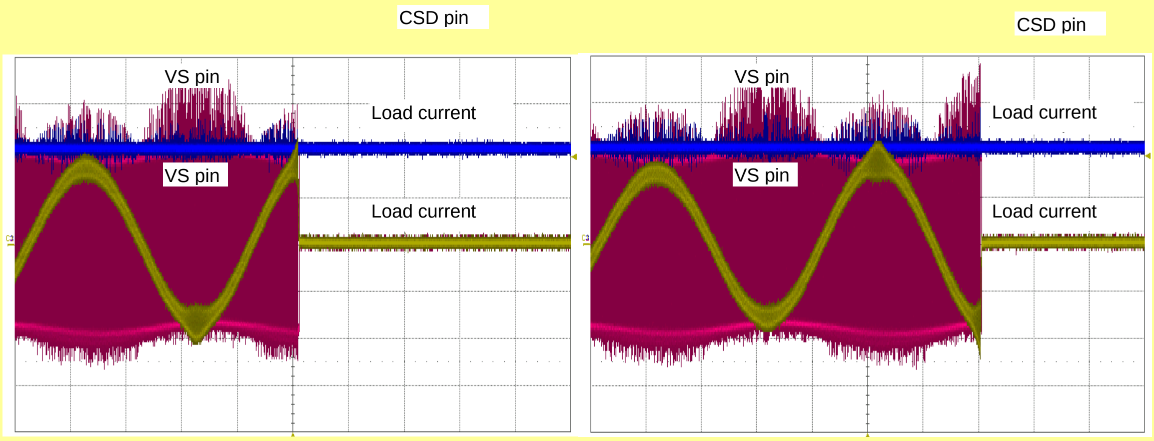
High-Side Current Sensing (Fig15)

The high-side MOSFET is protected from an overload condition and will shutdown the switching operation if the load current exceeds a preset trip level. High-side over-current sensing monitors detect an overload condition by measuring the high side MOSFET's drain-to-source voltage (V_{DS}) through the CSH and VS pins. The CSH pin detects the drain voltage with reference to the VS pin, which is the source of the high-side MOSFET. In contrast to the low-side current sensing, the threshold of CSH pin to engage OC protection is internally fixed at 1.2V. An external resistive divider R43+R25 and R41 (for Ch1) can be used to program a higher threshold. An additional external reverse blocking diode (D1 for CH1) is required to block high voltage feeding into the CSH pin during low-side conduction. By subtracting a forward voltage drop of 0.6V at D1, the minimum threshold which can be set for the high-side is 0.6V across the drain-to-source. For IRAUDAMP5, the high-side over-current trip level is set to 0.6V across the high-side MOSFET. For the IRF6645 MOSFETs with a nominal $R_{DS\text{-}ON}$ of 28 mOhms at 25°C, this results in a ~21A maximum trip level. Since the $R_{DS\text{-}ON}$ is a function of temperature, the trip level is reduced to ~14A at 100°C.
For a complete description of calculating and designing the over-current trip limits, please refer to the IRS2092S datasheet.

Positive and Negative Side of Short Circuit, versus switching output shut down:

The plots below show the speed that the IRS2092S responds to a short circuit condition. Notice that the envelope behind the sine wave output is actually the switching frequency ripple. Bus pumping naturally affects this topology.

Positive and Negative side of Short Circuit, versus switching output shut down:

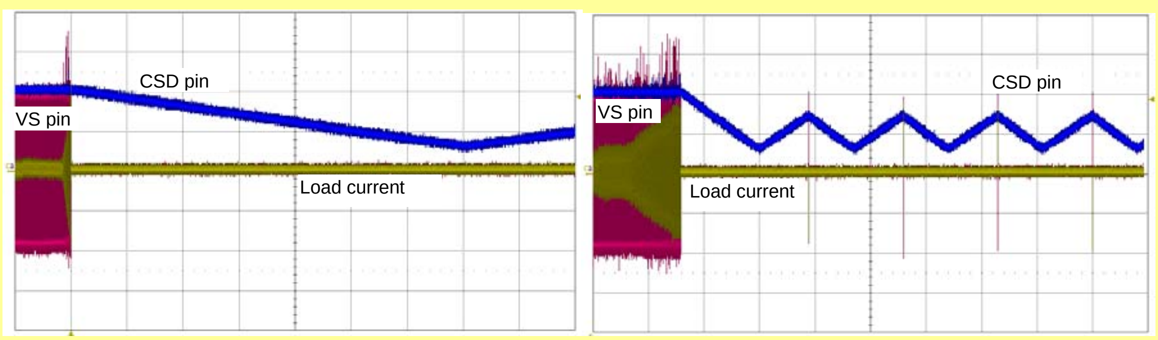


OCP Waveforms Showing Load Current and Switch Node Voltage (VS)

Fig 16

.

Short Circuit Response:



OCP Waveforms Showing CSD Trip and Hiccup

Fig 17

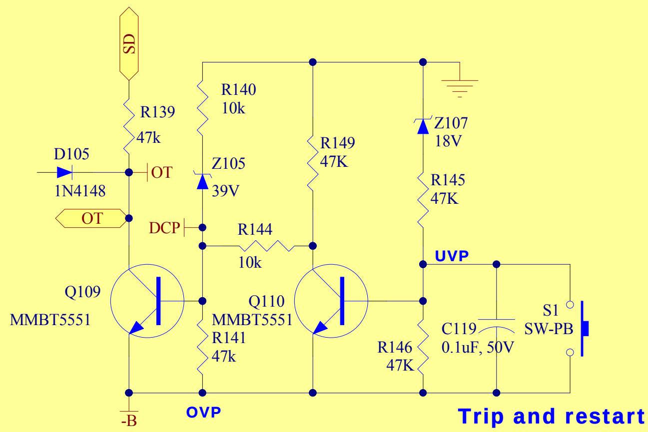
External Faults

OVP, UVP and DCP are considered external faults. In the event that any external fault condition is detected, the shutdown circuit will disable the output for about three seconds, during which time the orange AUDAMP5 "Protection" LED will turn on. If the fault condition has not cleared, the protection circuit will hiccup until the fault is removed. Once the fault is cleared, the green "Normal" LED will turn on. There is no manual reset option.

Over-Voltage Protection (OVP Fig 18)

OVP will shut down the amplifier if the bus voltage between GND and -B exceeds 40V. The threshold is determined by the voltage sum of the Zener diode Z105, R140, and V_{BE} of Q109. As a result, it protects the board from hazardous bus pumping at very low audio signal frequencies by shutting down the amplifier. OVP will automatically reset after three seconds. Since the +B and –B supplies are assumed to be symmetrical (bus pumping, although asymmetrical in time, will pump the bus symmetrically in voltage level over a complete audio frequency cycle), it is sufficient to sense only one of the two supply voltages for OVP. *It is therefore up to the user to ensure that the power supplies are symmetrical.*

Q109 Over-Voltage Protection (OVP)



Q110 Under-Voltage Protection (UVP)

Fig 18

Under-Voltage Protection (UVP, Fig18)

UVP will shutdown the amplifier if the bus voltage between GND and -B falls below 20V. The threshold is determined by the voltage sum of the Zener diode Z107, R145 and V_{BE} of Q110. As with OVP, UVP will automatically reset after three seconds, and only one of the two supply voltages needs to be monitored.

Speaker DC-Voltage Protection (DCP, Fig 19)

DCP is provided to protect against DC current flowing into the speakers. This abnormal condition is rare and is likely caused when the power amplifier fails and one of the high-side or low-side IRF6645 DirectFET MOSFETs remain in the ON state. DCP is activated if either of the outputs has more than ±4V DC offset (typical). Under this fault condition, it is normally required to shutdown the feeding power supplies. Since these are external to the reference design board, an isolated relay P1 is provided for further systematic evaluation of DC-voltage protection. This condition is transmitted to the power supply controller through connector J9, whose pins are shorted during a fault condition.

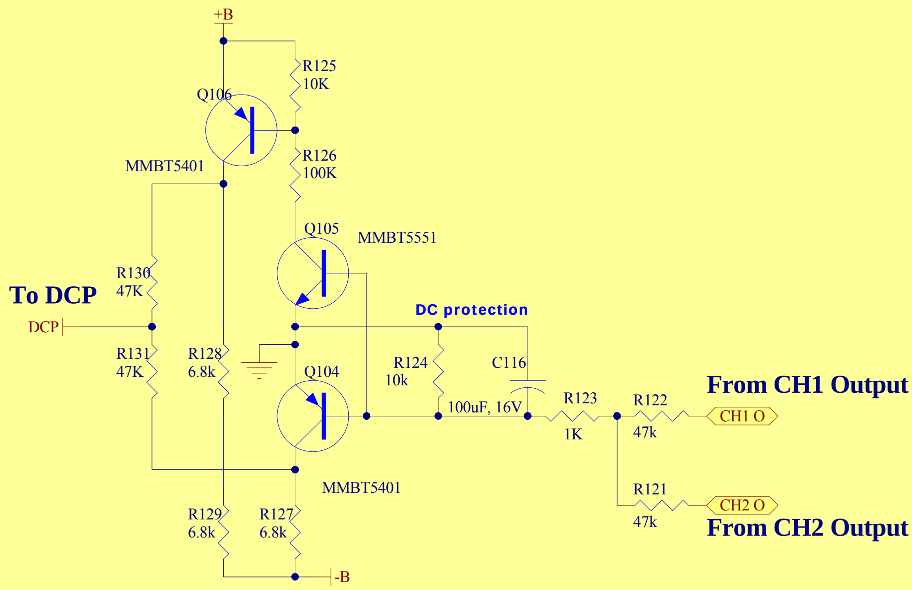
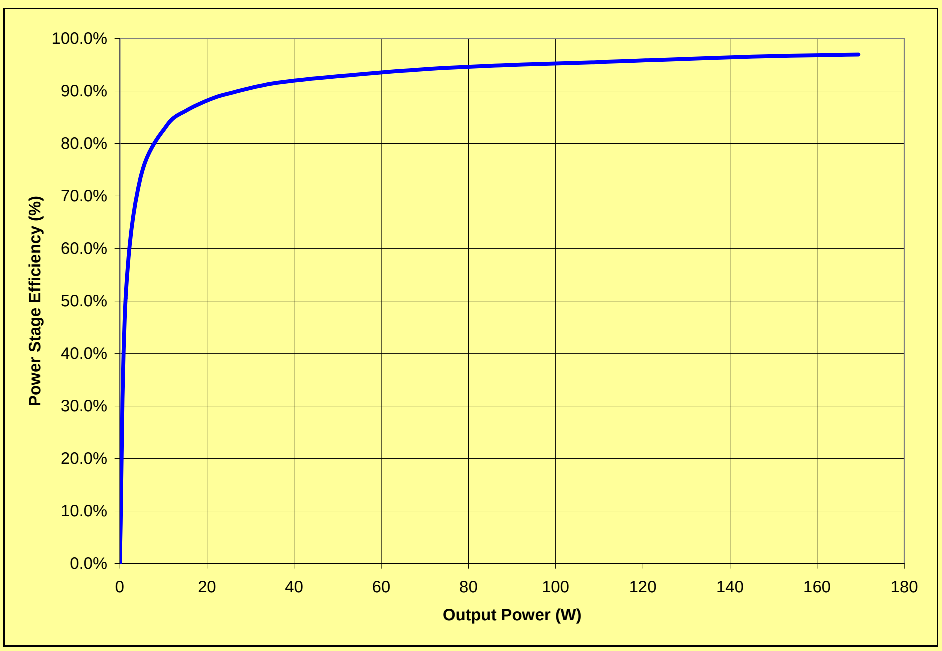


Fig 19

Efficiency

Figs 20 demonstrate that IRAUDAM5 is highly efficient, due to two main factors:

a.) DirectFETs offer low $R_{DS(ON)}$ and very low input capacitance, and b). The PWM operates as Pulse Density Modulation.



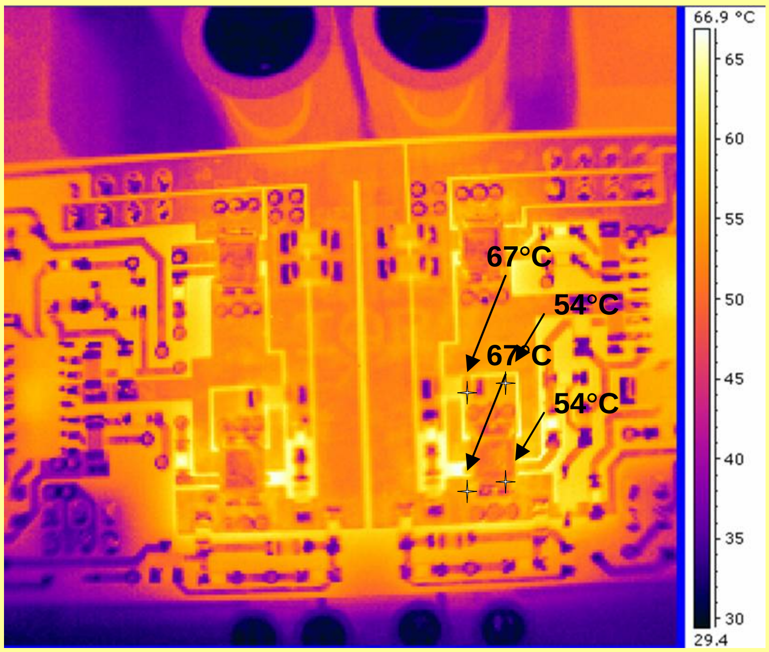
Efficiency vs. Output Power, 4Ω Single Channel Driven, ±B supply = ±35V, 1kHz Audio Signal

Fig20

Thermal Considerations

The daughter-board design can handle one-eighth of the continuous rated power, which is generally considered to be a normal operating condition for safety standards. Without the addition of a heatsink or forced air-cooling, the daughter board cannot handle fully rated continuous power. A thermal image of the daughter board is as shown in Fig 21 below.

Thermal Distribution



Thermal image of Daughter-Voard
Two-Channel x 1/8th Rated Power (15W) in Operation, TC = 54°C at Steady State
±B supply = ±35V, 4Ω Load, 1kHz audio signal, Temp ambient = 25°C

Fig 21

Click and POP noise:

One of the most important aspects of any audio amplifier is the startup and shutdown procedures. Typically, transients occurring during these intervals can result in audible pop- or click-noise from the output speaker. Traditionally, these transients have been kept away from the speaker through the use of a series relay that connects the speaker to the audio amplifier only after the startup transients have passed and disconnects the speaker prior to shutting down the amplifier.

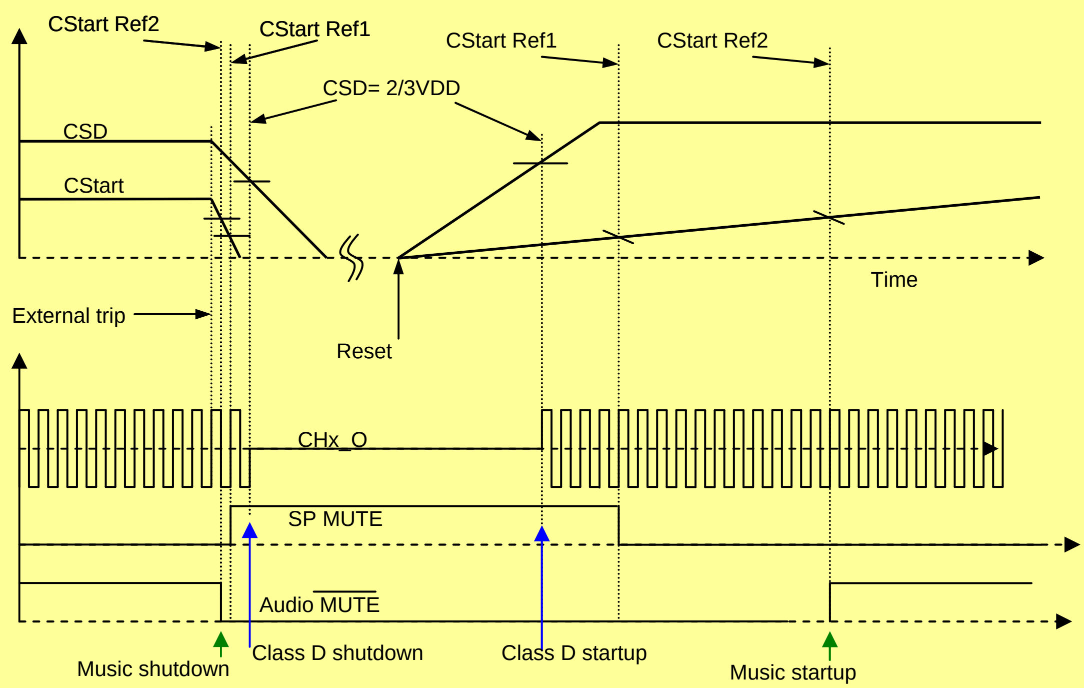
Thanks to the click and pop elimination function in the IRS2092S, IRAUDAMP5 does not use any series relay to disconnect the speaker from the audible transient noise.

Click-Noise Reduction Circuit (Solid-State Shunt)

IRS2092S controller is relatively quiet with respect to class AB, but for additional click or POP noise reduction you may add a shunt circuit that further attenuates click or pop transients during turn on sequencing. The circuit is not populated on the present demo board; for implementation details, please refer to the IRAUDAMP4 user's manual at http://www.irf.com/technical-info/refdesigns/audiokits.html

Startup and Shutdown Sequencing (Fig 22)

The IRAUDAMP5 sequencing is achieved through the charging and discharging of the CStart capacitor C117. Along with the charging and discharging of the CSD voltage (C10 on daughter board for CH1) of the IRS2092S, this is all that is required for complete sequencing. The startup and shutdown timing diagrams are show in Figure 22A below:

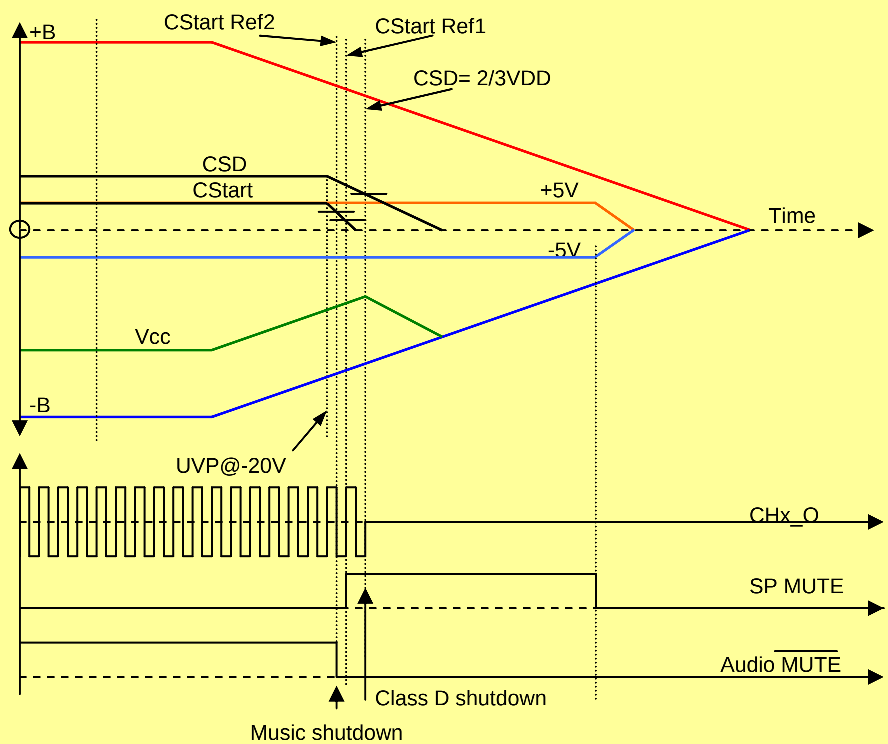


Click Noise Reduction Sequencing at Trip and Reset

Fig 22A

For startup sequencing, the control power supplies start up at different intervals depending on the ±B supplies. As the +/-B supplies reach +5 volts and -5 volts respectively, the +/-5V control supplies for the analog input start charging. Once +B reaches ~16V, VCC charges. Once –B reaches -20V, the UVP is released and CSD and CStart (C117) start charging. The Class D amplifier is now operational, but the preamp output remains muted until CStart reaches Ref2. At this point, normal operation begins. The entire process takes less than three seconds.

For Shutdown (Fig22B) sequencing is initiated once UVP is activated. As long as the supplies do not discharge too quickly, the shutdown sequence can be completed before the IRS2092S trips UVP. Once UVP is activated, CSD and CStart are discharged at different rates. In this case, threshold Ref2 is reached first and the preamp audio output is muted. It is then possible to shutdown the Class D stage (CSD reaches two-thirds VDD). This process takes less than 200ms.



Conceptual Shutdown Sequencing of Power Supplies and Audio Section Timing

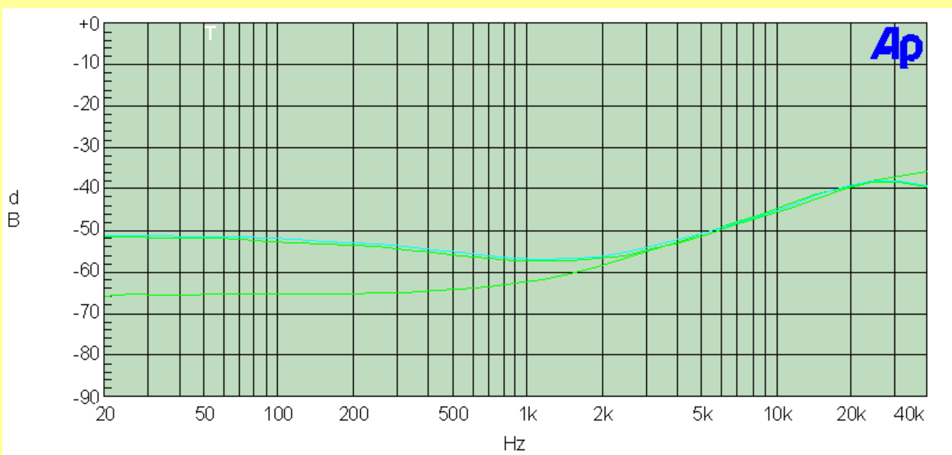
Fig22B

For any external fault condition (OTP, OVP, UVP or DCP – see "Protection") that does not lead to power supply shutdown, the system will trip in a similar manner as described above. Once the fault is cleared, the system will reset (similar sequence as startup).

Power Supplies

The IRAUDAMP5 has all the necessary housekeeping power supplies onboard and only requires a pair of symmetric power supplies ranging from ±25V to ±35V (+B, GND, -B) for operation. The internally-generated housekeeping power supplies include a ±5V supply for analog signal processing (preamp etc.), while a +12V supply (VCC), referenced to –B, is included to supply the low and high side Class D gate-driver stages.

For the externally-applied power, a regulated power supply is preferable for performance measurements, but is not always necessary. The bus capacitors, C31 and C32 on the motherboard, along with high-frequency bypass-caps C14, C15; C32 and C33 on the daughter board, address the high-frequency ripple current that results from switching action. In designs involving unregulated power supplies, the designer should place a set of external bus capacitors having enough capacitance to handle the audio-ripple current. Overall regulation and output voltage ripple for the power supply design are not critical when using the IRAUDAMP5 Class D amplifier as the power supply rejection ratio (PSRR) of the IRAUDAMP5 is excellent, as shown on Figure 23 below.



Power Supply Rejection Ratio
Green: IRAUDAMP5, Cyan: VAA/VSS are fed by Vbus

Fig 23

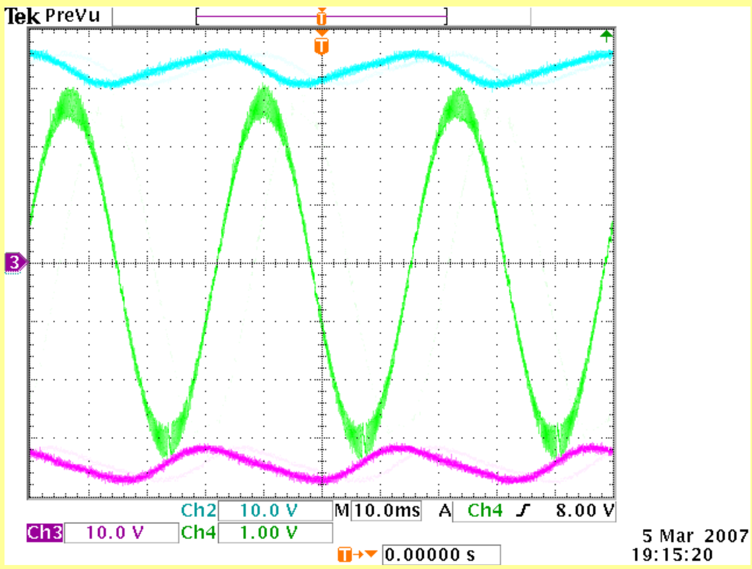
Bus Pumping (Fig24)

Since the IRAUDAMP5 is a half-bridge configuration, bus pumping does occur. Under normal operation during the first half of the cycle, energy flows from one supply through the load and into the other supply, thus causing a voltage imbalance by pumping up the bus voltage of the receiving power supply. In the second half of the cycle, this condition is reversed, resulting in bus pumping of the other supply.
These conditions worsen bus pumping:

1. Lower frequencies (bus-pumping duration is longer per half cycle)
2. Higher power output voltage and/or lower load impedance (more energy transfers between supplies)

3. Smaller bus capacitors (the same energy will cause a larger voltage increase)

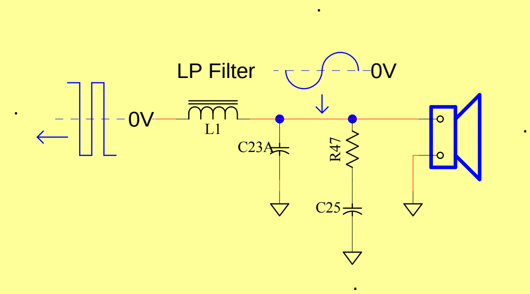
The IRAUDAMP5 has protection features that will shut down the switching operation if the bus voltage becomes too high (>40V) or too low (<20V). One of the easiest countermeasures is to drive both of the channels in a stereo configuration out of phase so that one channel consumes the energy flow from the other and does not return it to the power supply. Bus voltage detection is only done on the –B supply, as the effect of the bus pumping on the supplies is assumed to be symmetrical in amplitude (although opposite in phase) with the +B supply.



Bus Pumping Figure:
Cyan = Positive Rail voltage (+B)
Green = Speaker Output
Pink = Negative Rail voltage (-B)
Fig 24

Input Signal

A proper input signal is an analog signal below 20 kHz, up to ±3.5V peak, having a source impedance of less than 600 ohms. A 30-60 kHz input signal can cause LC resonance in the output LPF, resulting in an abnormally large amount of reactive current flowing through the switching stage (especially at 8 ohms or higher impedance towards open load), and causing OCP activation. The IRAUDAMP5 has an RC network (Fig25), or Zobel network (R47 and C25 [CH1]), to dampen the resonance and protect the board in such an event, but is not thermally rated to handle continuous supersonic frequencies. *These supersonic input frequencies therefore should be avoided.* Separate mono RCA connectors provide input to each of the two channels. Although both channels share a common ground, it is necessary to connect each channel separately to limit noise and crosstalk between channels.



Zobel Filter and Output filter demodulator
Fig 25

Output

Both outputs for the IRAUDAMP5 are single-ended and therefore have terminals labeled (+) and (-), with the (-) terminal connected to power ground. Each channel is optimized for a 4-Ohm speaker load for a maximum output power (120W), but is capable of operating with higher load impedances (at reduced power), at which point the frequency response will have a small peak at the corner frequency of the output LC low pass filter. The IRAUDAMP5 is stable with capacitive-loading; however, it should be noted that the frequency response degrades with heavy capacitive loading of more than 0.1μF.

Gain Setting / Volume Control

The IRAUDAMP5 has an internal volume control (potentiometer R108 labeled, "VOLUME", Fig 26) for gain adjustment. Gain settings for both channels are tracked and controlled by the volume control IC (U_2), setting the gain from the microcontroller IC (U_1). The maximum volume setting (clockwise rotation) corresponds to a total gain of +37.9dB (78.8V/V). The total gain is a product of the power-stage gain, which is constant (+23.2dB), and the input-stage gain that is directly-controlled by the volume adjustment. The volume range is about 100dB, with minimum volume setting to mute the system with an overall gain of less than -60dB. <u>For best performance in testing, the internal volume control should be set to a gain of 21.9V/V,</u> such that 1Vrms input will result in rated output power (120W into 4Ω), allowing for a >11dB overdrive.

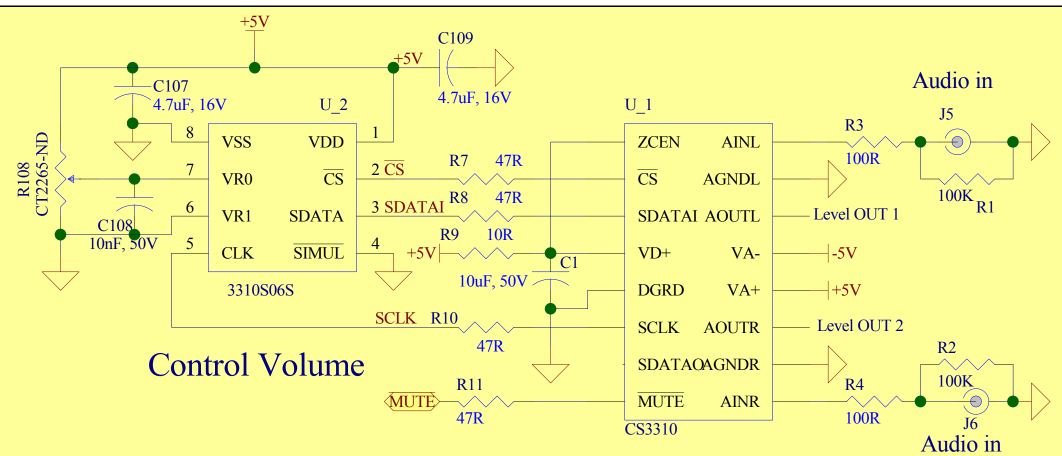
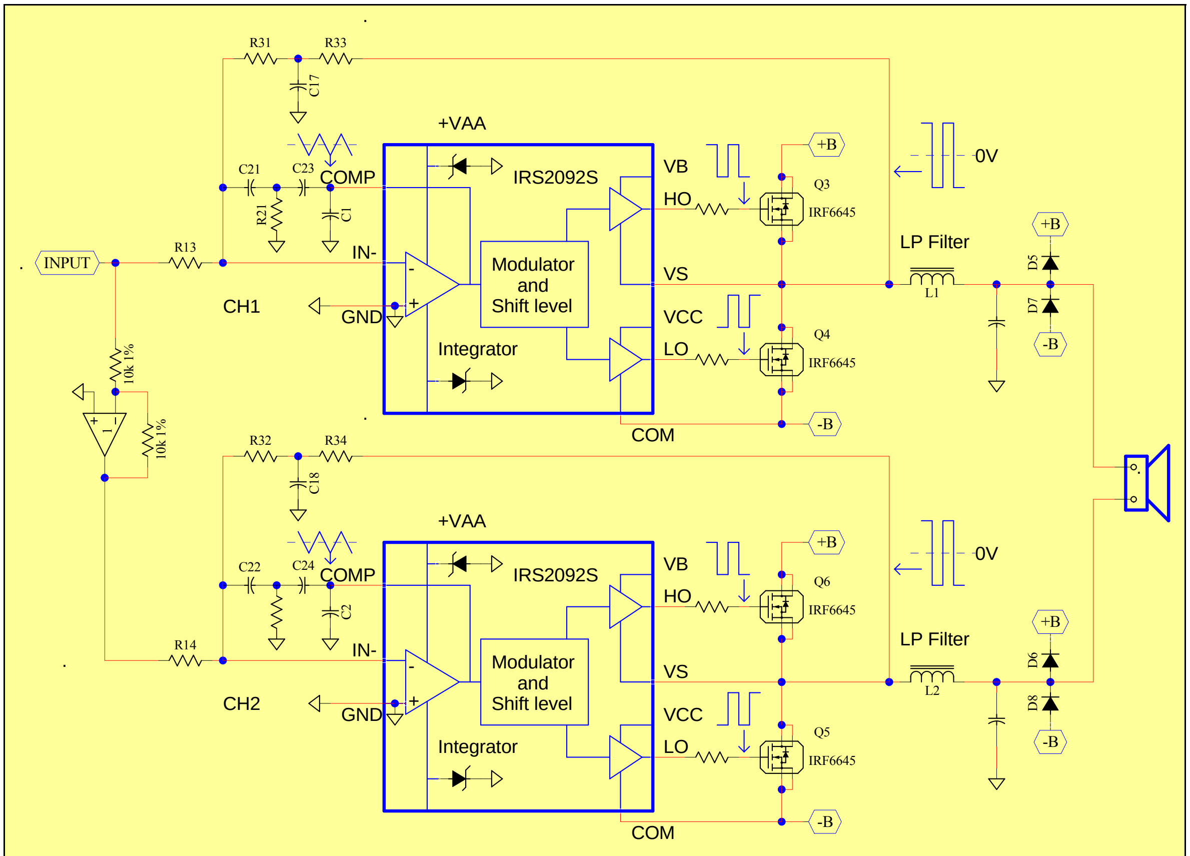


Fig 26 Digital volume Control

Bridged Output

The IRAUDAMP5 is not intended for a bridge-tied-load, or BTL configuration. However, BTL operation can be achieved by feeding out-of-phase audio input signals to the two input channels as shown in the figure 27 below. In BTL operation, minimum load impedance is 8 Ohms and rated power is 240W non-clipping. The installed clamping diodes D5 – D8 are required for BTL operation, since reactive energy flowing from one output to the other during clipping can force the output voltage beyond the voltage supply rails if not clamped.



Bridged configuration

Fig 27

Output Filter Design, Preamplifier and Performance

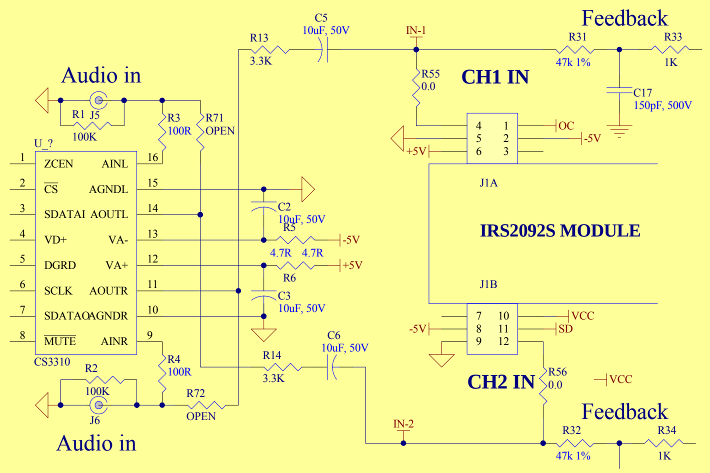
The audio performance of IRAUDAMP5 depends on a number of different factors. The section entitled, “Typical Performance” presents performance measurements based on the overall system, including the preamp and output filter. While the preamp and output filter are not part of the Class D power stage, they have a significant effect on the overall performance.

Output filter

Since the output filter is not included in the control loop of the IRAUDAMP5, the reference design cannot compensate for performance deterioration due to the output filter. Therefore, it is important to understand what characteristics are preferable when designing the output filter:

1) The DC resistance of the inductor should be minimized to 20 mOhms or less.
2) The linearity of the output inductor and capacitor should be high with respect to load current and voltage.

Preamplifier *(Fig 28)*
The preamp allows partial gain of the input signal, and controls the volume in the IRAUDAMP5. The preamp itself will add distortion and noise to the input signal, resulting in a gain through the Class D output stage and appearing at the output. Even a few micro-volts of noise can add significantly to the output noise of the overall amplifier.

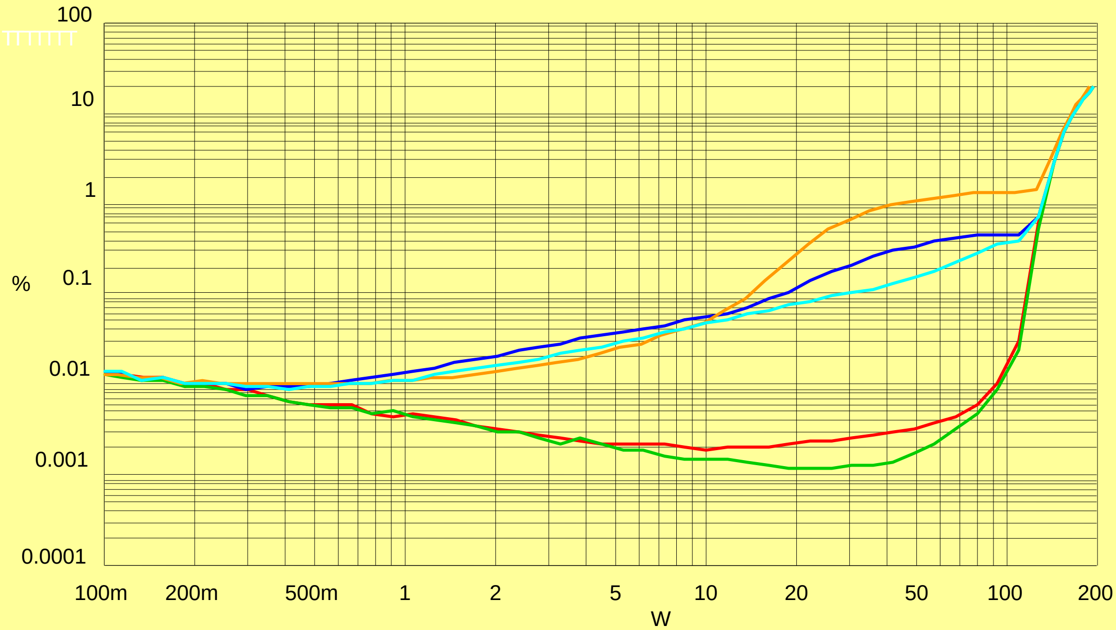


Preamplifier
Fig28

It is possible to evaluate the performance without the preamp and volume control, by moving resistors R13 and R14 to R71 and R72, respectively. This effectively bypasses the preamp and connects the RCA inputs directly to the Class D power stage input. Improving the selection of preamp and/or output filter components will improve the overall system performance, approaching that of the stand-alone Class D power stage. In the "Typical Performance" section, only limited data for the stand-alone Class D power stage is given. For example, Fig 20 below shows the results for THD+N vs. Output Power are provided, utilizing a range of different inductors. By changing the inductor and repeating this test, a designer can quickly evaluate a particular inductor.

I

IRAUDAMP5 can be used as output inductors evaluation tool



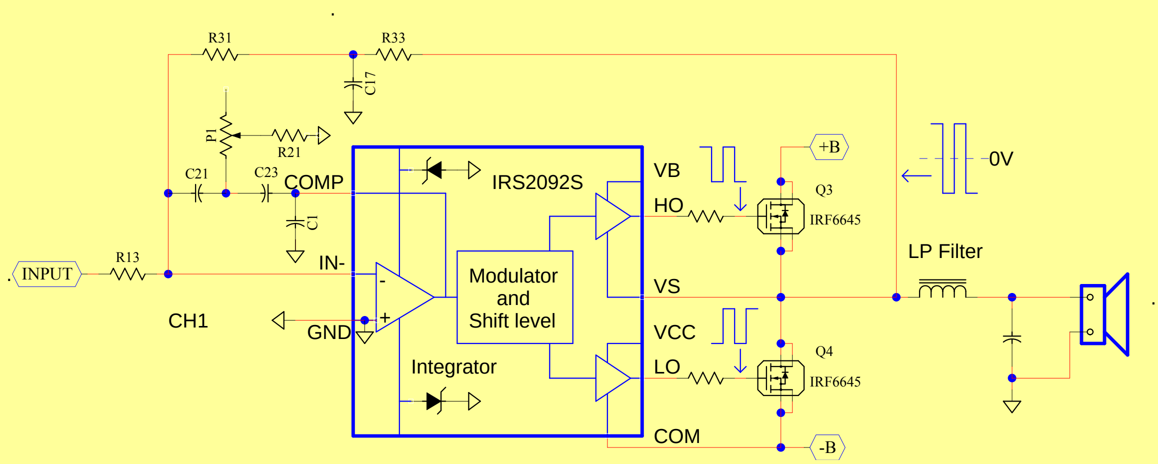
Results of THD+N vs. Output Power with Different Output Inductors

Fig 29

Self-Oscillating PWM Modulator

The IRAUDAMP5 Class D audio power amplifier features a self-oscillating type PWM modulator for the lowest component count, highest performance and robust design. This topology represents an analog version of a second-order sigma-delta modulation having a Class D switching stage inside the loop. The benefit of the sigma-delta modulation, in comparison to the carrier-signal based modulation, is that all the error in the audible frequency range is shifted to the inaudible upper-frequency range by nature of its operation. Also, sigma-delta modulation allows a designer to apply a sufficient amount of correction.

The self-oscillating frequency (Fig 30) is determined by the total delay time inside the control loop of the system. The delay of the logic circuits, the IRS2092S gate-driver propagation delay, the IRF6645 switching speed, the time-constant of front-end integrator (e.g.R13, R33, R31, R21, P1, C17, C21, C23 and C1 for CH1) and variations in the supply voltages are critical factors of the self-oscillating frequency. Under nominal conditions, the switching-frequency is around 400kHz with no audio input signal and a +/-35V supply.



Self Oscillating determined components

Fig 30

Adjustments of Self-Oscillating Frequency

The PWM switching frequency in this type of self-oscillating switching scheme greatly impacts the audio performance, both in absolute frequency and frequency relative to the other channels. In absolute terms, at higher frequencies distortion due to switching-time becomes significant, while at lower frequencies, the bandwidth of the amplifier suffers. In relative terms, interference between channels is most significant if the relative frequency difference is within the audible range. Normally, when adjusting the self-oscillating frequency of the different channels, it is best to either match the frequencies accurately, or have them separated by at least 25kHz. With the installed components, it is possible to change the self-oscillating frequency from about 300kHz up to 450kHz, as shown on Fig 30

Switches and Indicators

There are four different indicators on the reference design as shown in the figure 31 below:

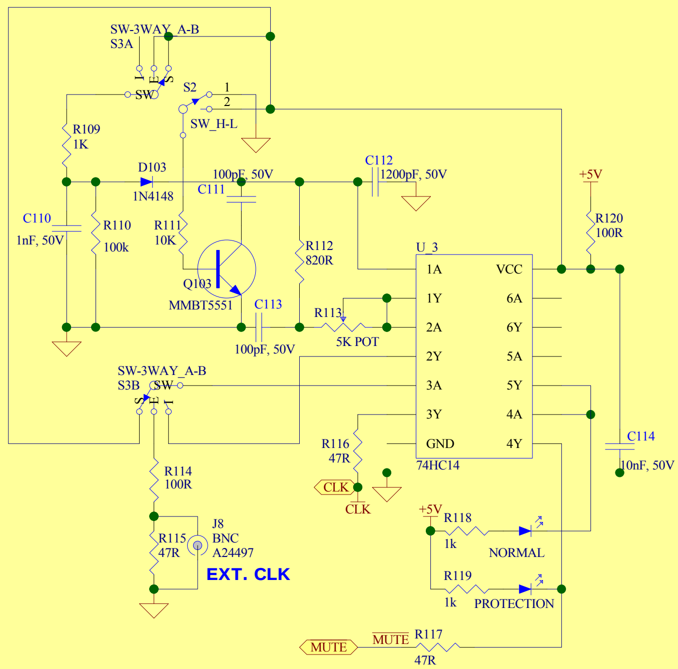
1. An orange LED, signifying a fault / shutdown condition when lit.
2. A green LED on the motherboard, signifying conditions are normal and no fault condition is present.
3. A blue LED on the daughter board module, signifying there are HO pulses for CH1
4. A blue LED on the daughter board module signifying there are HO pulses for CH2

There are three switches on the reference design:

1. Switch S1 is a trip and reset push-button. Pushing this button has the same effect as a fault condition. The circuit will restart about three seconds after the shutdown button is released.
2. Switch S2 is an internal clock-sync frequency selector. This feature allows the designer to modify the switching frequency in order to avoid AM radio interference. With S3 set to INT, the two settings “H” and “L” will modify the internal clock frequency by about

20 kHz to 40 kHz, either higher "H" or lower "L." The actual internal frequency is set by potentiometer R113 - "INT FREQ."

3. Switch S3 is an oscillator selector. This three-position switch is selectable for internal self oscillator (middle position – "SELF"), or either internal ("INT") or external ("EXT") clock synchronization.

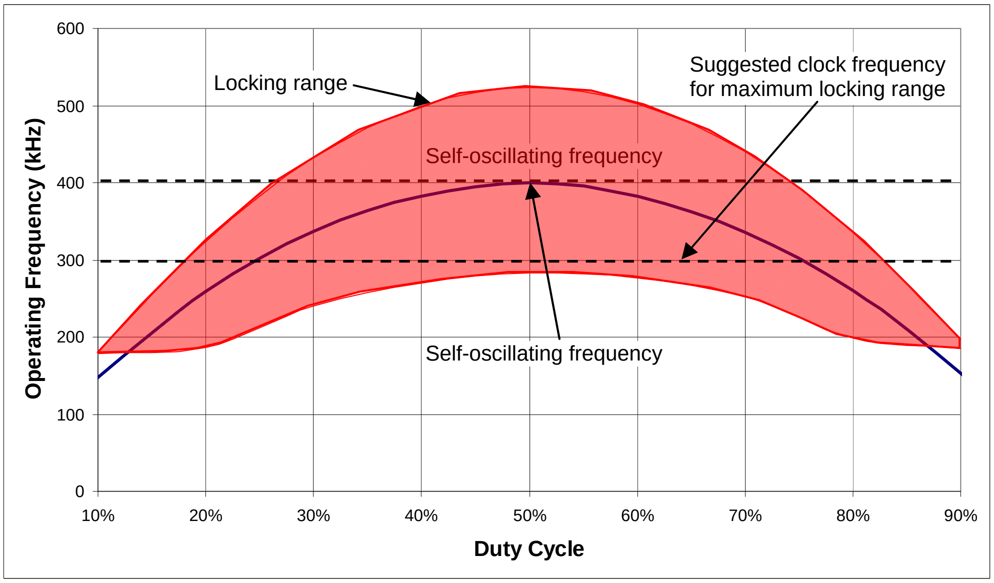


LED, Switches and Sync frequencies
Fig 31

Switching Frequency Lock / Synchronization Feature

For single-channel operation, the use of the self-oscillating switching scheme will yield the best audio performance. The self-oscillating frequency, however, changes with the duty ratio. This varying frequency can interfere with AM radio broadcasts, where a constant-switching frequency with its harmonics shifted away from the AM carrier frequency is preferred. In addition to AM broadcasts, multiple channels can also reduce audio performance at low power, and can lead to increased residual noise. Clock frequency locking/synchronization can address these unwanted characteristics.

Please note that the switching frequency lock / synchronization feature is not possible for all frequencies and duty ratios, and operates within a limited frequency and duty-ratio range around the self-oscillating frequency (Figure 32 below).

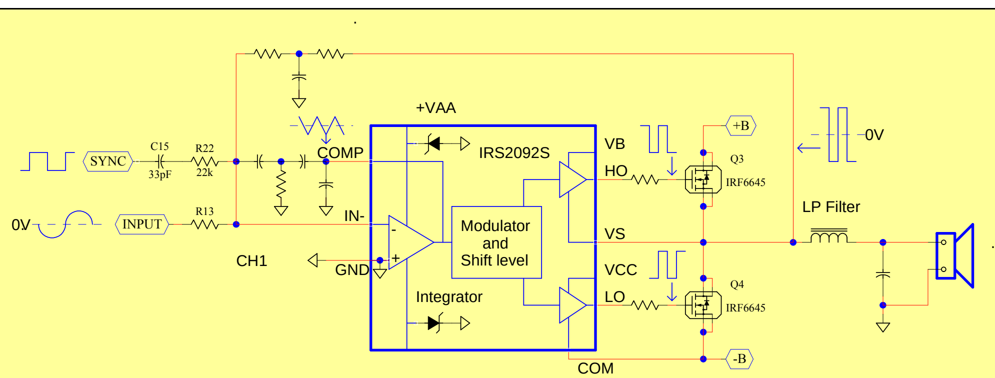


Typical Lock Frequency Range vs. PWM Duty Ratio
(Self-oscillating frequency set to 400 kHz with no input)

Fig 32

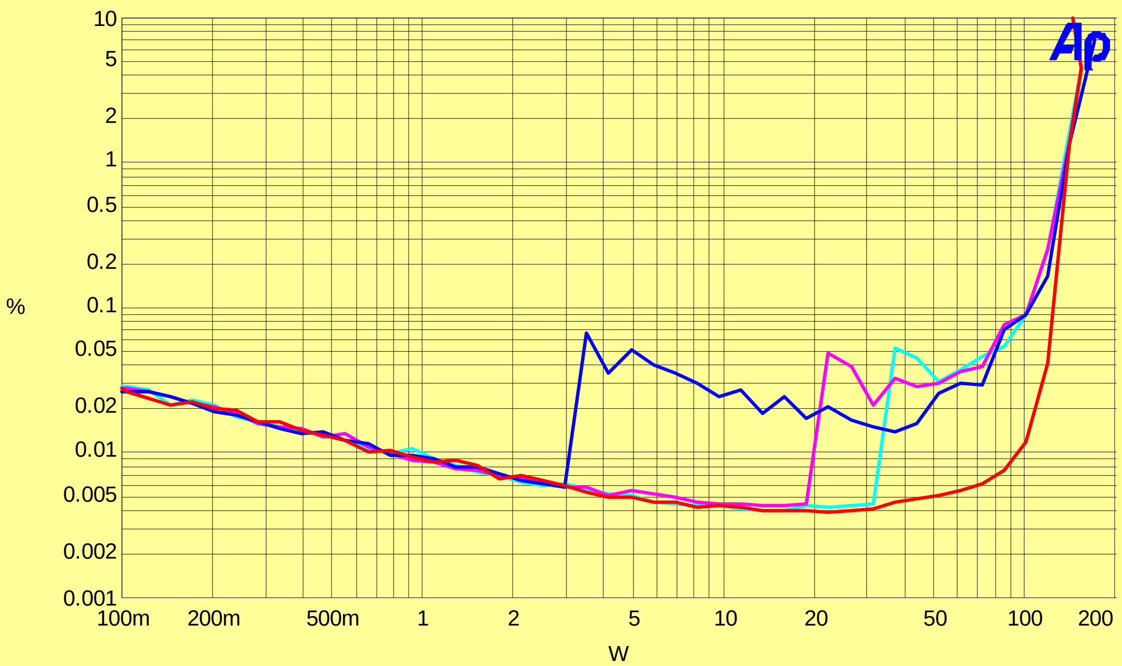
The output power range, for which frequency-locking is successful, depends on what the locking frequency is with respect to the self-oscillating frequency. As illustrated in Figure 33, the locking frequency is lowered (from 450kHz to 400kHz to 350kHz and then 300kHz) as the output power range (where locking is achieved) is extended. Once locking is lost, however, the audio performance degrades, but the increase in THD seems independent from the clock frequency. Therefore, a 300 kHz clock frequency is recommended, as shown on Fig 34

It is possible to improve the THD performance by increasing the corner frequency of the high pass filter (HPF) (R17 and C15 for Ch1 Fig 33) that is used to inject the clock signal, as shown in Figure 33 below.
This drop in THD, however, comes at the cost of reducing the locking range. Resistor values of up to 100 kOhms and capacitor values down to 10pF may be used.



Switching Frequency Lock / Synchronization Feature
Fig 33

In IRAUDAMP5, this switching frequency lock/synchronization feature (Fig 31 and Fig 33) is achieved with either an internal or external clock input (selectable through S3). If an internal (INT) clock is selected, an internally-generated clock signal is used, adjusted by setting potentiometer R113 "INT FREQ." If external (EXT) clock signal is selected, a 0-5V square-wave (~50% duty ratio) logic signal must be applied to BNC connector J17.



Red	CH1, = Self Oscillator @ 400kHz
Pink	CH1, = Sync Oscillator @ 400kHz
Blue	CH1, = Sync Oscillator @ 450kHz
Cyan	CH1, = Sync Oscillator @ 350kHz

THD+N Ratio vs. Output Power for Different Switching Frequency Lock/Synchronization Conditions

Fig 34

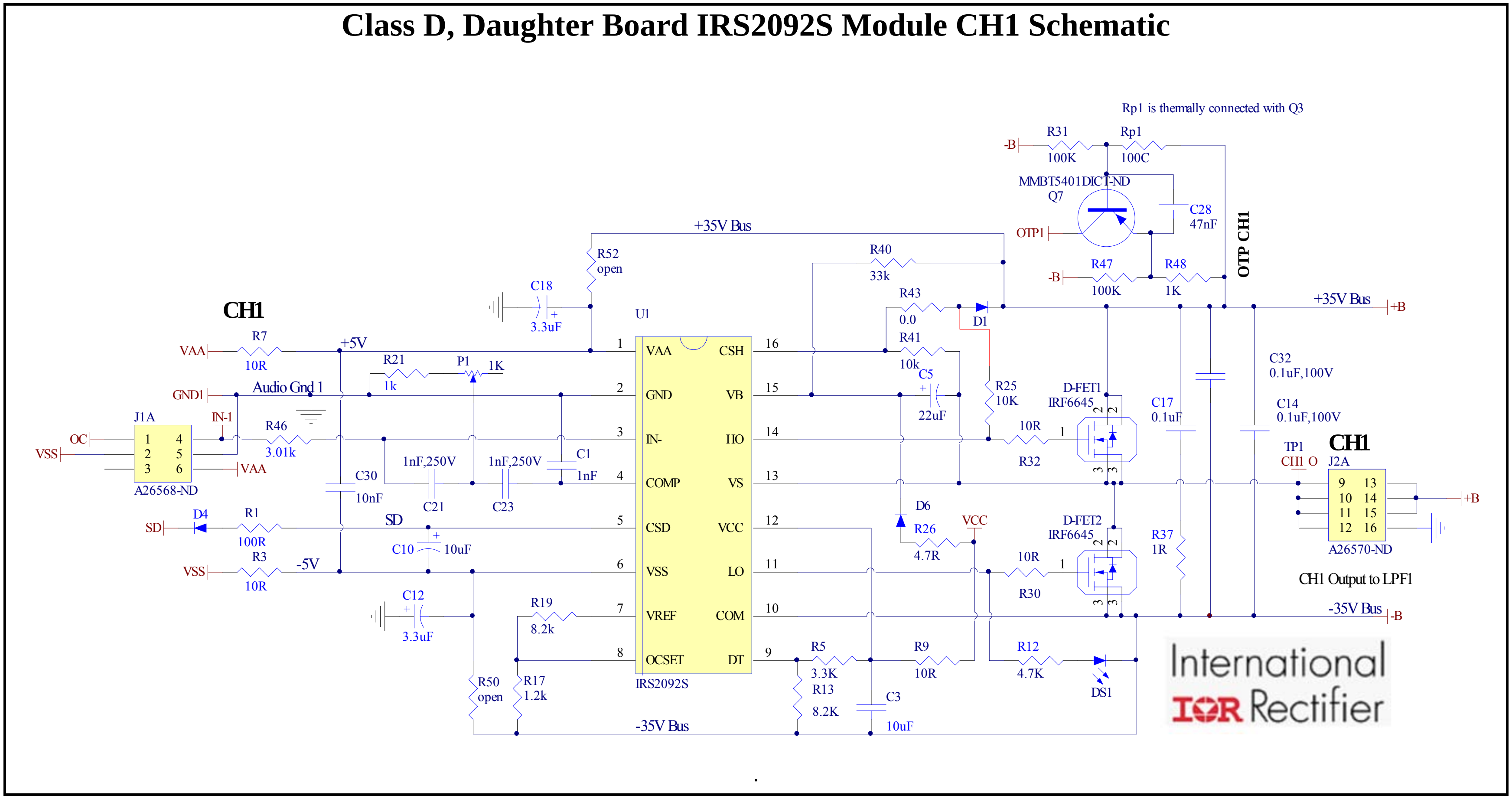

Class D, Daughter Board IRS2092S Module CH1 Schematic
Rp1 is thermally connected with Q3
R31 100K
Rp1 100C
MMBT5401DICT-ND Q7
C28 47nF
OTP1
OTP CH1
+35V Bus
R40 33k
R47 100K
R48 1K
R52 open
C18 3.3uF
R43 0.0
D1
R41 10k
CH1
U1
VAA CSH
GND VB
IN- HO
COMP VS
CSD VCC
VSS LO
VREF COM
OCSET DT
IRS2092S
R7 10R
+5V
R21 1k
P1 1K
Audio Gnd 1
J1A
A26568-ND
R46 3.01k
C30 10nF
1nF,250V
C21
C23
C1 1nF
R1 100R
D4
SD
C10 10uF
R3 10R
-5V
C12 3.3uF
R19 8.2k
R50 open
R17 1.2k
-35V Bus
C5 22uF
R25 10K
D-FET1 IRF6645
R32 10R
C17 0.1uF
C32 0.1uF,100V
C14 0.1uF,100V
D6
R26 4.7R
VCC
D-FET2 IRF6645
R30 10R
R37 1R
TP1
CH1 O
J2A
A26570-ND
CH1 Output to LPF1
R5 3.3K
R13 8.2K
C3 10uF
R9 10R
R12 4.7K
DS1
International
IOR Rectifier

Fig 35

Class D, Daughter Board IRS2092S Module CH2 Schematic

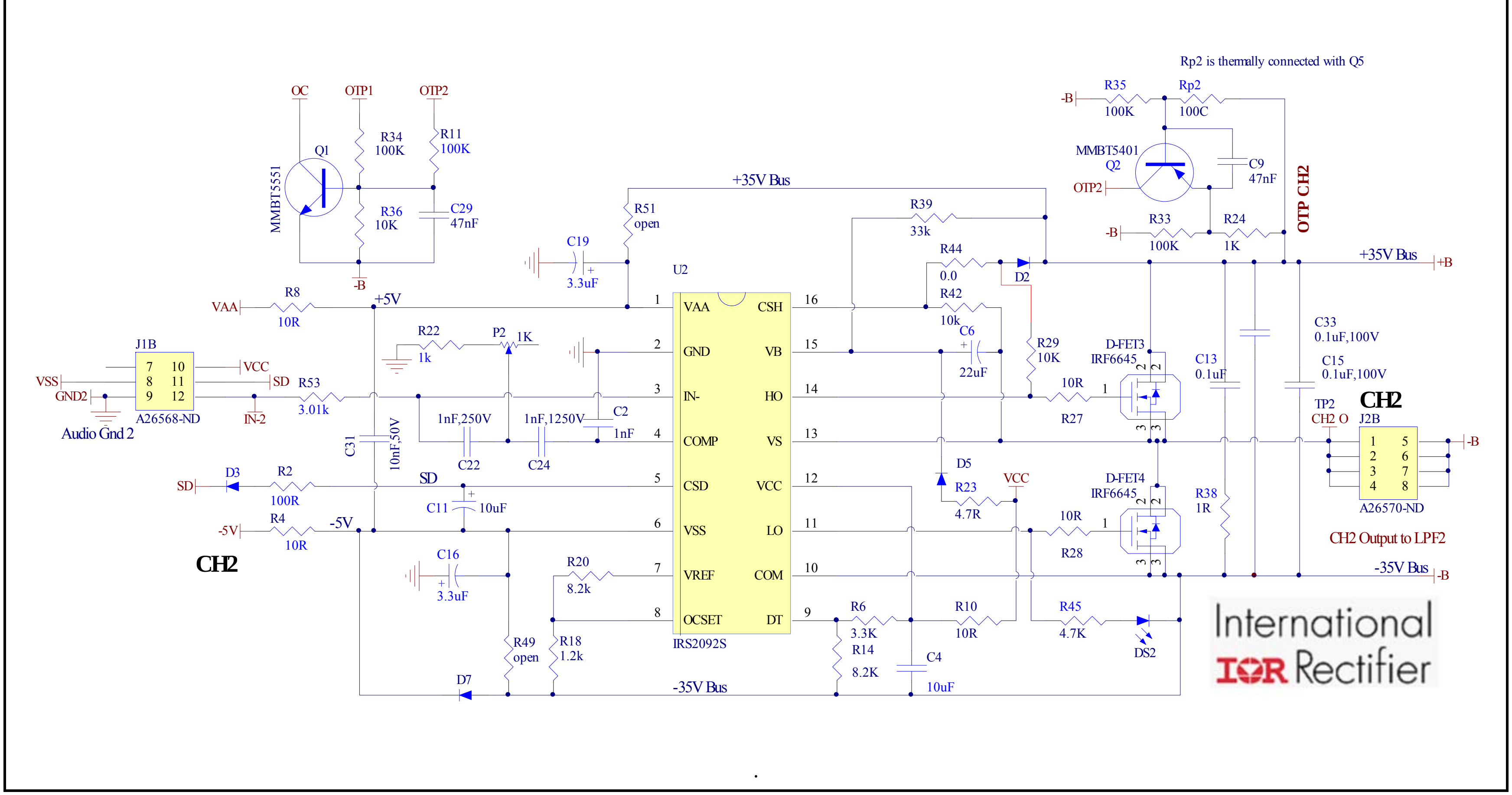


Fig 36

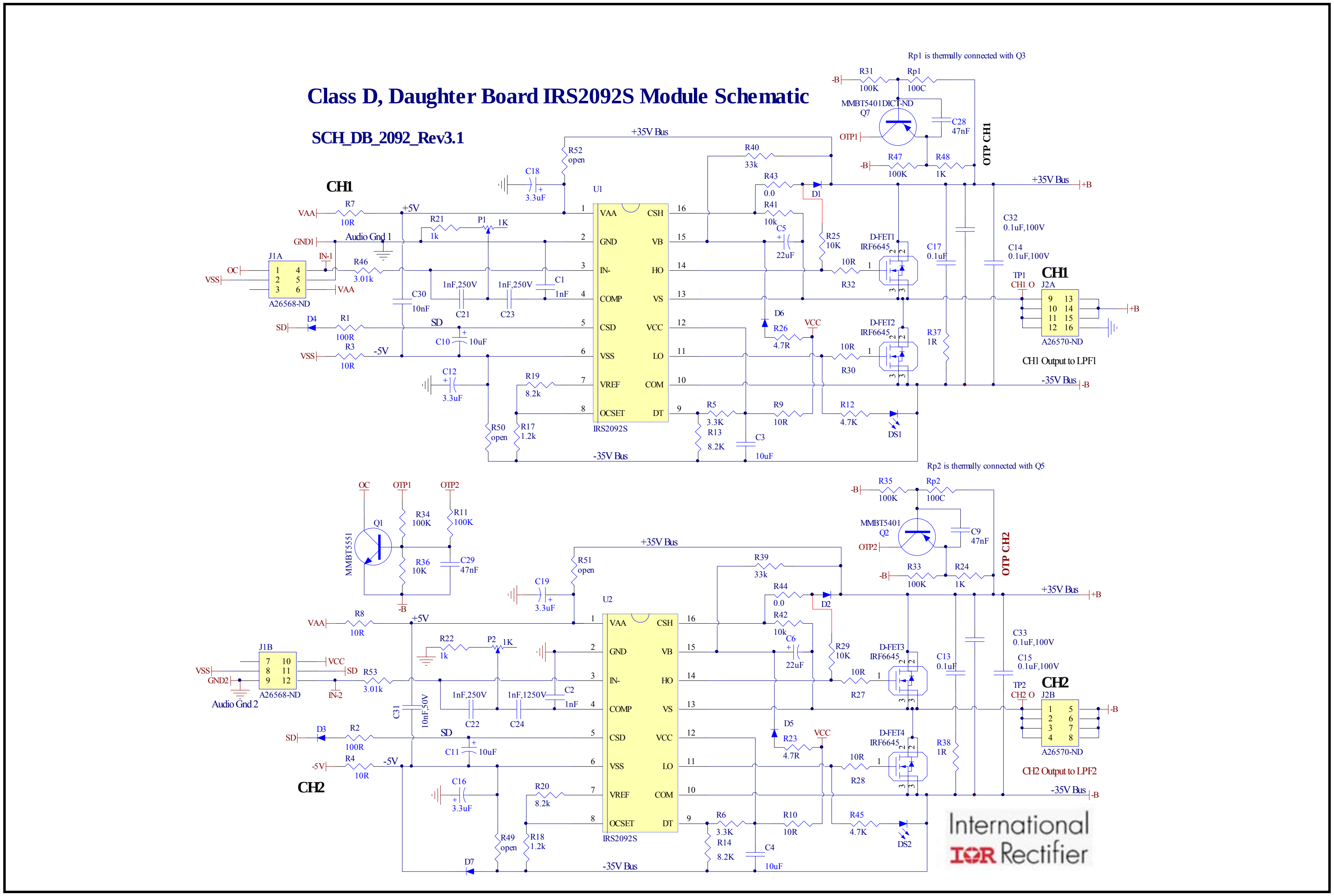

Class D, Daughter Board IRS2092S Module Schematic
SCH_DB_2092_Rev3.1
CH1
CH2
Rp1 is thermally connected with Q3
Rp2 is thermally connected with Q5
OTP CH1
OTP CH2
CH1 Output to LPF1
CH2 Output to LPF2
+35V Bus
-35V Bus
IRS2092S
International
IOR Rectifier

Fig 37

Class D, Mother Board Control Volume and Power Supplies Schematic

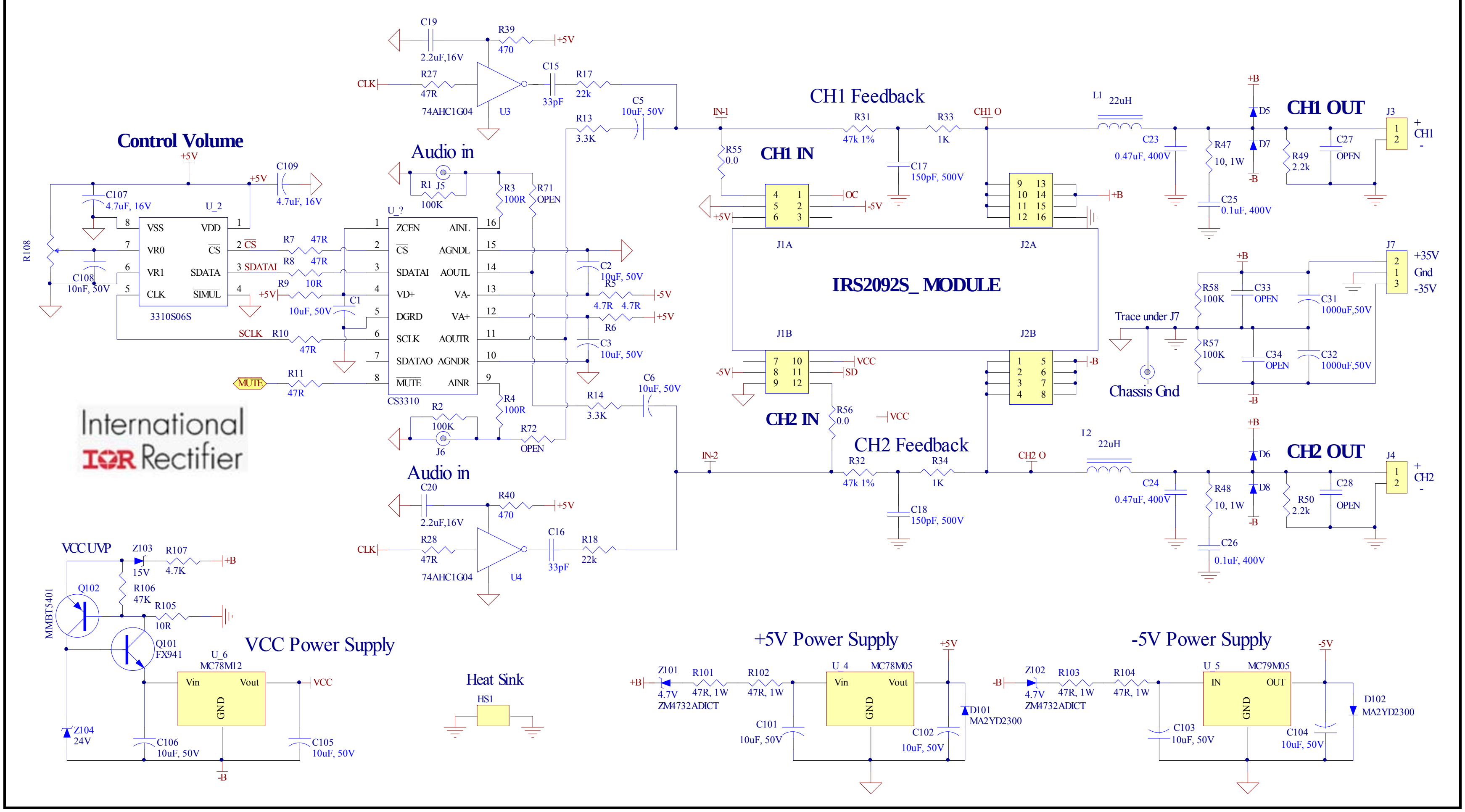


Fig 38

Class D, Mother Board Clock and House Keeping Schematic

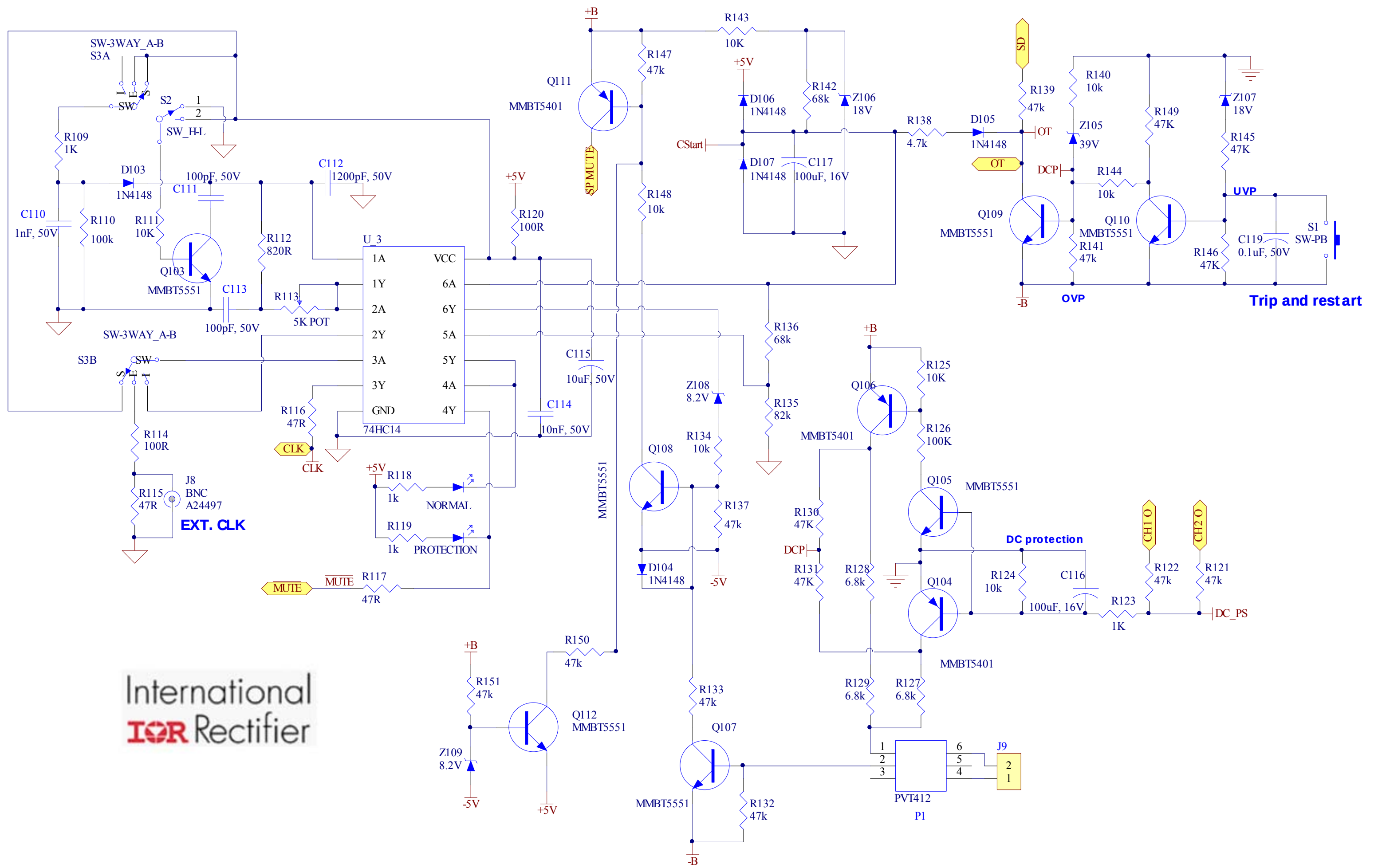


Fig 39

IRAUDAMP5 Bill of Materials

Class D, Daughter Board:

Amp5_DB_2092_Rev 3.1_BOM					
Designator	Footprint	PartType	Quantity	PART NO	VENDER
C1, C2, C21,C22,C23,C24	805	1nF,250V,COG	6	445-2325-1-ND	DIGI KEY
C3, C4	TAN-A	10uF, 16V, Tan	2	495-2236-1-ND	DIGI KEY
C5, C6	TAN-B	10uF, 16V, Tan	2	399-3706-1-ND	DIGI KEY
C9, C28, C29	0805	47nF,50V, X7R	3	PCC1836CT-ND	DIGI KEY
C10, C11	TAN-B	10uF, 16V, Tan	2	399-3706-1-ND	DIGI KEY
C12, C16, C18, C19	TAN-B	3.3uF, 16V, X7R	4	445-1432-1-ND	DIGI KEY
C13, C17	0805	0.1uF,100V, X7R	2	399-3486-1-ND	DIGI KEY
C14, C15, C32, C33	1206	0.1uF,100V, X7R	3	PCC2239CT-ND	DIGI KEY
C20	0805	open	1	open	
C30, C31	0805	10nF,50V, X7R	2	PCC103BNCT-ND	DIGI KEY
D1, D2	SOD-323	BAV19WS-7-F	2	BAV19WS-FDICT-ND	DIGI KEY
D3, D4	SOD-323	1N4148WS-7-F	2	1N4148WS-FDICT-ND	DIGI KEY
D5, D6	SMA	MURA120T3G	2	MURA120T3GOSCT-ND	DIGI KEY
D7	SMA	ES1D	1	ES1DFSCT-ND	DIGI KEY
DS1, DS2	805	LTST-C171TBKT	2	160-1645-1-ND	DIGI KEY
J1A	CON EISA31	CON EISA31	1	A26568-ND	DIGI KEY
J1B	CON EISA31	CON EISA31	1	A26568-ND	DIGI KEY
J2A	CON_POWER	CON_POWER	1	A26570-ND	DIGI KEY
J2B	CON_POWER	CON_POWER	1	A26570-ND	DIGI KEY
Q1	SOT23-BCE	MMBT5551	1	MMBT5551FSCT-ND	DIGI KEY
Q2, Q7	SOT23-BCE	MMBT5401-7	2	MMBT5401-FDICT-ND	DIGI KEY

D-FET1, D-FET2, D-FET3, D-FET4	Direct Fet SJ	IRF6645	4	IRF6645	IR
R1, R2	0805	100R	2	P100ACT-ND	DIGI KEY
R3,R4,R9,R10,R15,R16,R27,R28,R30,R32,R8	0805	10R	11	P10ACT-ND	DIGI KEY
R5, R6	0805	3.3K	2	P3.3KACT-ND	DIGI KEY
R7	1206	10R	1	P10ECT-ND	DIGI KEY
R11, R31, R33, R34, R35, R47	0805	100K	2	P100KACT-ND	DIGI KEY
R12, R45	0805	4.7K	2	P4.7KACT-ND	DIGI KEY
R13, R14,R19,R20	0805	8.2K	2	P8.2KACT-ND	DIGI KEY
R24, R48	0805	1K	2	P1.0KACT-ND	DIGI KEY
R7,R18	805	1.2k		RHM1.2KARCT-ND	DIGI KEY
R21, R22	0805	1k	2	P1.0KACT-ND	DIGI KEY
R23, R26	0805	4.7R	2	P4.7ACT-ND	DIGI KEY
R25, R29,R36,R41, R42	0805	10K	5	P10KACT-ND	DIGI KEY
R37, R38	0805	1R	3	P1.0ACT-ND	DIGI KEY
R39, R40	0805	33K	3	RHM33KARCT-ND	DIGI KEY
R43, R44	0805	0	3	RHM0.0ARCT-ND	DIGI KEY
R49, R50, R51, R52,	1206	open	3	open	
Rp1, Rp2	805	100C	3	594-2381-675-21007	MOUSER
P1,P2	ST-32 3mm SQ	1k		ST32ETB102TR-ND	DIGI KEY
R46,R53	805	3.01k		RHM3.01KCCT-ND	DIGI KEY
U1, U2	SOIC16	IR Driver	3	IRS2092S	IR

Class D Motherboard:

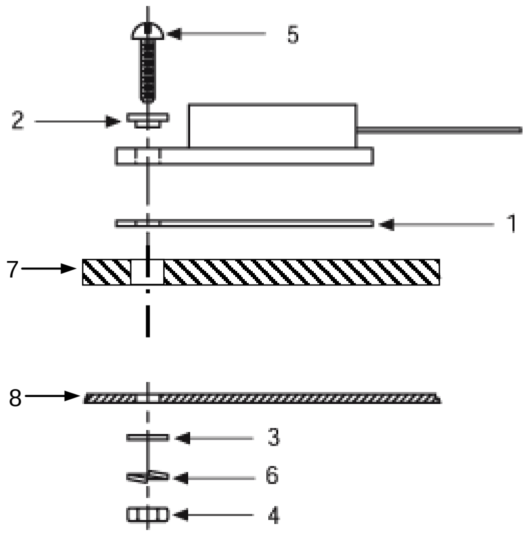
IRAUDAMP5 MOTHERBOARD BILL OF MATERIAL						
NO	Designator	#	Footprint	Part Type	Part No	Vender
1	C1, C5, C6, C101, C102, C103, C104, C105, C106, C115	10	RB2/5	10uF, 50V	565-1106-ND	Digikey
2	C2, C3	2	RB2/5	2.2uF, 50V	565-1103-ND	Digikey
3	C7, C8, C9, C10	4	open			
4	C11, C12, C13, C14	4	open			
5	C15, C16	2	805	33pF	478-1281-1-ND	Digikey
6	C17, C18	2	AXIAL0.19R	150pF, 500V	338-2598-ND	Digikey
7	C19, C20	2	1206	2.2uF, 16V	PCC1931CT-ND	Digikey
8	C119	1	1206	0.1uF, 50V	PCC104BCT-ND	Digikey
9	C23, C24	2	CAP MKP	0.47uF, 400V	495-1315-ND	Digikey
10						
11	C25, C26	2	CAP MKPs	0.1uF, 400V	495-1311-ND	Digikey
12	C27, C28, C29, C30, C40, C41, C42, C43, C44, C45, C46, C47	12	805	OPEN		
13	R29, R30, R55, R56, R60, R61, R62, R63, R64, R65, R66, R67, R71, R72	14	805	OPEN		
14	C31, C32	2	RB5/12_5	1000uF,50V	565-1114-ND	Digikey
15	C33, C34, C48, C49	4	AXIAL0.1R	OPEN	-	Digikey
16	C107, C109	2	805	4.7uF, 16V	PCC2323CT-ND	Digikey
17	C108, C114	2	805	10nF, 50V	PCC103BNCT-ND	Digikey
18	C110	1	805	1nF, 50V	PCC102CGCT-ND	Digikey
19	C111, C113	2	805	100pF, 50V	PCC101CGCT-ND	Digikey
20	C112	1	805	1200pF, 50V	478-1372-1-ND	Digikey
21	C116, C117	2	rb2/5	100uF, 16V	565-1037-ND	Digikey
22	D103, D104, D105, D106, D107	5	SOD-123	1N4148W-7-F	1N4148W-FDICT-ND	Digikey
23	D5, D6, D7, D8	4	SMA	MURA120T3G	MURA120T3GOSCT-ND	Digikey
24	D101, D102	2	SOD-123	MA2YD2300	MA2YD2300LCT-ND	Digikey
25	HS1	1	Heat_S6in1	HEAT SINK	294-1086-ND	Digikey
26	J1A, J1B	2	CON EISA-31	CON EISA31	A32934-ND	Digikey
27	J2A, J2B	2	CON_POWER	CON_POWER	A32935-ND	Digikey
28	J3, J4	2	MKDS5/2-9.5	277-1022	277-1271-ND or 651-1714971	Digikey or Mouser
29	J5, J6	2	Blue RCA	RCJ-055	CP-1422-ND	Digikey
30	J7	1	J HEADER3	277-1272	277-1272-ND or 651-1714984	Digikey or Mouser
31	J8	1	BNC_RA CON	BNC	A32248-ND	Digikey
32	J9	1	ED1567	ED1567	ED1567	Digikey
33	L1, L2	2	Inductor	Sagami 7G17A- Or 1D17A-220M	Sagami 7G17A- Or 1D17A-220M	Inductors, Inc Or ICE Components, Inc.
34	NORMAL	1	Led rb2/5	404-1106-ND	160-1143-ND	Digikey
35	P1	1	DIP-6	PVT412	PVT412PBF-ND	Digikey
36	PROTECTION	1	Led rb2/5	404-1109-ND	160-1140-ND	Digikey
37	Q101	1	SOT89	FX941	FCX491CT-ND	Digikey
38	Q102, Q104, Q106, Q111	4	SOT23-BCE	MMBT5401-7-F	MMBT5401-FDICT-ND	Digikey
39	Q103, Q105, Q107, Q108, Q109, Q110, Q112	7	SOT23-BCE	MMBT5551	MMBT5551-FDICT-ND	Digikey
40	R1, R2, R57, R58, R110, R126	6	805	100K	P100KACT-ND	Digikey
41	R3, R4, R114	3	805	100R	P100ACT-ND	Digikey
42	R5, R6	2	1206	4.7R	P4.7ECT-ND	Digikey
43	R7, R8, R10, R11, R27, R28, R115, R116, R117	9	805	47R	P47ACT-ND	Digikey
44	R9, R105	2	805	10R	P10ACT-ND	Digikey
45	R13, R14	2	805	3.3K, 1%	P3.3KZCT-ND	Digikey
46	R17, R18	2	805	22k	P22KACT-ND	Digikey
47	R106, R121, R122, R130, R131, R132, R133, R137, R139, R141, R145, R146, R147, R149, R150, R151	16	805	47k	P47KACT-ND	Digikey
48	R152	1	805	OPEN	-	Digikey
49	R55, R56	2	805	0.0 Ohms	P0.0ACT-ND	Digikey
50	R39, R40	2	805	470R	P470ACT-ND	Digikey
51	R21, R22, R23, R24	4	open			
52	R120	1	1206	100R	P100ECT-ND	Digikey
53	R29P, R30P	2	open			
54	R31, R32	2	2512	47K, 1%	PT47KAFCT-ND	Digikey
55	R33, R34	2	1206	1K	P1.0KECT-ND	Digikey

56	R109, R118, R119, R123	4	805	1K	P1.0KACT-ND	Digikey
57	R47, R48	2	2512	10, 1W	PT10XCT	Digikey
58	R49, R50	2	1206	2.2k	P2.2KECT-ND	Digikey
59	R68, R69	2	AXIAL-0.3	OPEN	-	Digikey
60	R101, R102, R103, R104	4	2512	47R, 1W	PT47XCT-ND	Digikey
61	R107, R138	2	805	4.7K	P4.7KACT-ND	Digikey
62	R108	1	V_Control	CT2265	CT2265-ND	Digikey
63	R111, R124, R125, R134, R140, R143, R144, R148	8	805	10K	P10KACT-ND	Digikey
64	R112	1	805	820R	P820ACT-ND	Digikey
65	R113	1	POTs	5K POT	3362H-502LF-ND	Digikey
66	R127, R128, R129	3	1206	6.8k	P6.8KECT-ND	Digikey
67	R135	1	805	82k	P82KACT-ND	Digikey
68	R136, R142	2	805	68k	P68KACT-ND	Digikey
69	S1	1	Switch	SW-PB	P8010S-ND	Digikey
70	S2	1	SW-EG1908-ND	SW_H-L	EG1908-ND	Digikey
71	S3	1	SW-EG1944-ND	SW-3WAY	EG1944-ND	Digikey
72	U1, U2	2	open			
73	U3, U4	2	SOT25	74AHC1G04	296-1089-1-ND	Digikey
74	U7, U8	2	MINI5	open	open	
75	U9, U10	2	SO-8	open	open	
76	U_1	1	SOIC16	CS3310	73C8016 or 72J5420	Newark
77	U_2	1	N8A	3310S06S	3310-IR01	*Tachyonix
78	U_3	1	M14A	74HC14	296-1194-1-ND	Digikey
79	U_4	1	TO-220	MC78M05CTG	MC78M05CTGOS-ND	Digikey
80	U_5	1	TO-220	LM79M05CT	LM79M05CT-ND	Digikey
81	U_6	1	TO-220	LM78M12CT	LM78M12CT-ND	Digikey
82	Z1, Z2, Z103	3	SOD-123	15V	BZT52C15-FDICT-ND	Digikey
83	Z101, Z102	2	SMA	4.7V	1SMA5917BT3GOSCT-ND	Digikey
84	Z104	1	SOD-123	24V	BZT52C24-FDICT-ND	Digikey
85	Z105	1	SOD-123	39V	BZT52C39-13-FDICT-ND	Digikey
86	Z106, Z107	2	SOD-123	18V	BZT52C18-FDICT-ND	Digikey
87	Z108, Z109	2	SOD-123	8.2V	BZT52C8V2-FDICT-ND	Digikey
88	Volume Knob	1	Blue Knob	MC21060	10M7578	Newark
89	Thermalloy TO-220 mounting kit with screw	3	Kit screw, ROHS	AAVID 4880G	82K6096	Newark
90	1/2" Standoffs 4-40	5	Standoff		8401K-ND	Digikey
91	4-40 Nut	5	100 per bag		H724-ND	Digikey
92	No. 4 Lock Washer	5	100 per bag		H729-ND	Digikey

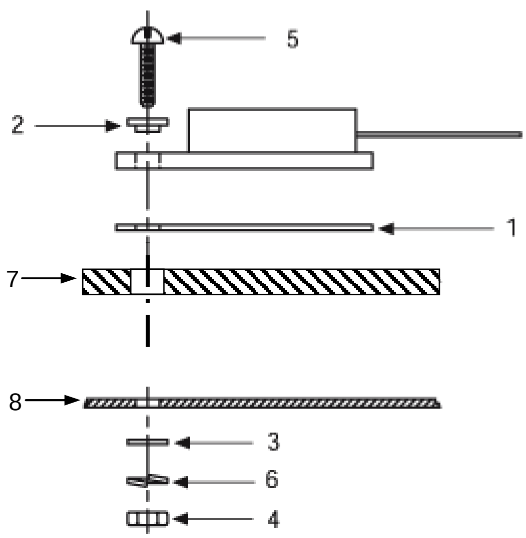
*Tachyonix Corporation, 14 Gonaka Jimokuji Jimokuji-cho, Ama-gun Aichi, JAPAN 490-1111 http://www.tachyonix.co.jp info@tachyonix.co.jp

IRAUDAMP5 Hardware

Voltage regulator mounting:



Item	Description
1	Insulator Thermalfilm
2	Shoulder Washer
3	Flat Washer #4
4	No. 4-40 UNC-2B Hex Nut
5	No. 4-40 UNC-2A X 1/2 Long Phillips Pan Head Screw
6	Lockwasher, No.4
7	Heatsink
8	PCB



Item	Description
1	Insulator Thermalfilm
2	Shoulder Washer
3	Flat Washer #4
4	No. 4-40 UNC-2B Hex Nut
5	No. 4-40 UNC-2A X 1/2 Long Phillips Pan Head Screw
6	Lockwasher, No.4
7	Heatsink
8	PCB

Fig 40

IRAUDAMP5 PCB Specifications

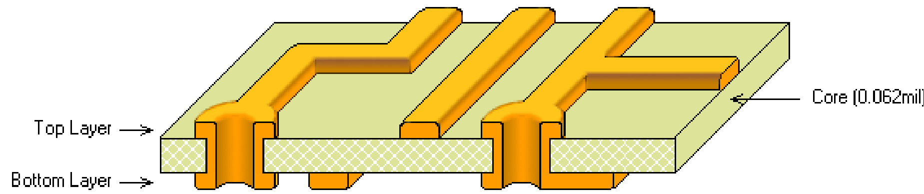


Figure 41

Motherboard and Daughter-board Layer Stack

Daughter board:

Material:	FR4, UL 125°C
Layer Stack:	2 Layers, 1 oz. Cu each, Through-hole plated
Dimensions:	3.125” x 1.52” x 0.062”
Solder Mask:	LPI Solder mask, SMOBC on Top and Bottom Layers
Plating:	Open copper solder finish
Silkscreen:	On Top and Bottom Layers

Motherboard:

Material:	FR4, UL 125°C
Layer Stack:	2 Layers, 1 oz. Cu
Dimensions:	5.2” x 5.8” x 0.062”
Solder Mask:	LPI Solder mask, SMOBC on Top and Bottom Layers
Plating:	Open copper solder finish
Silkscreen:	On Top and Bottom Layers

IRAUDAMP5 PCB layers

Class D, Daughter-board:

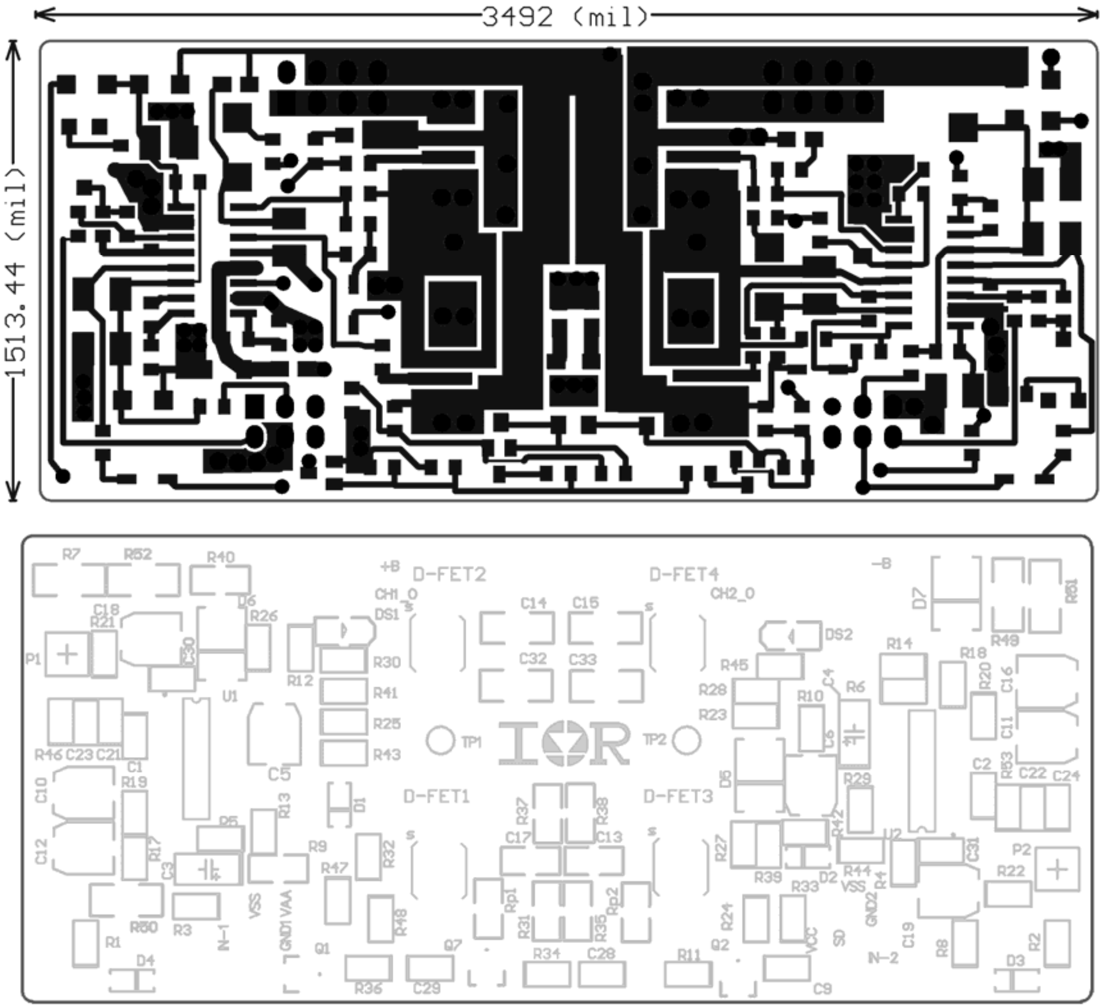


Figure 42 PCB Layout – Top-Side Solder-Mask and Silkscreen

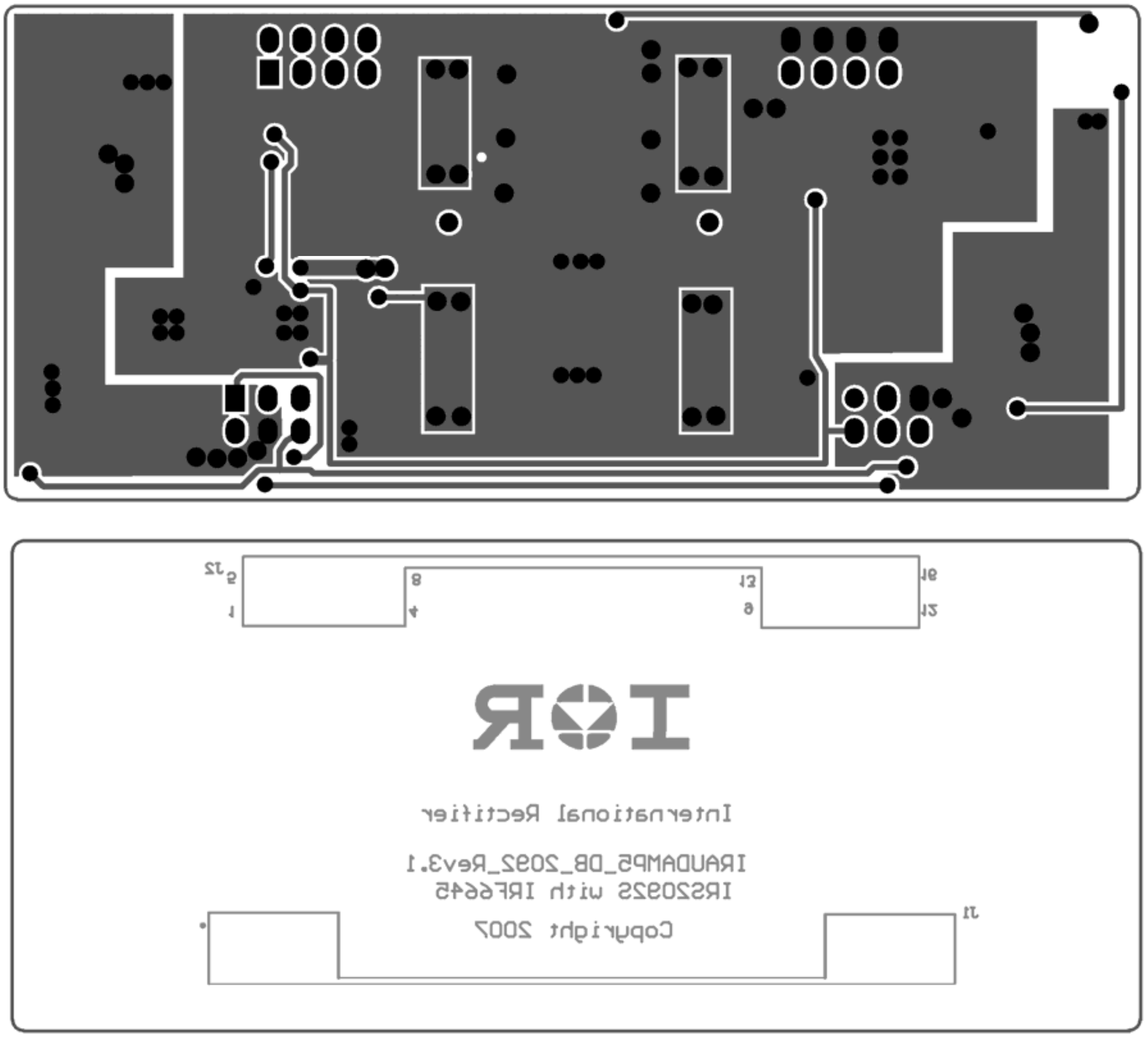


Figure 43. PCB Layout – Bottom Layer and Pads and bottom silk screen

PCB Layout Motherboard:

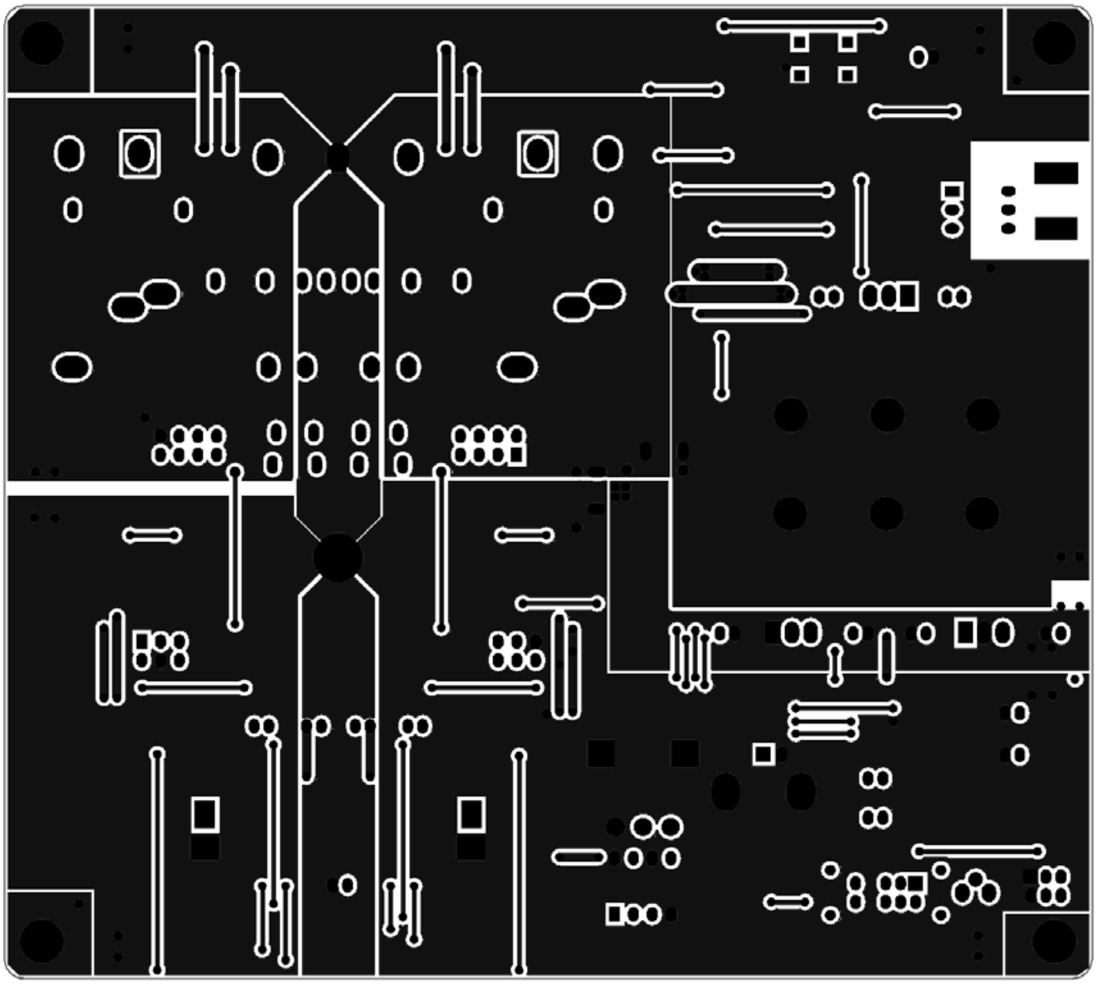


Fig 44 Top Layer

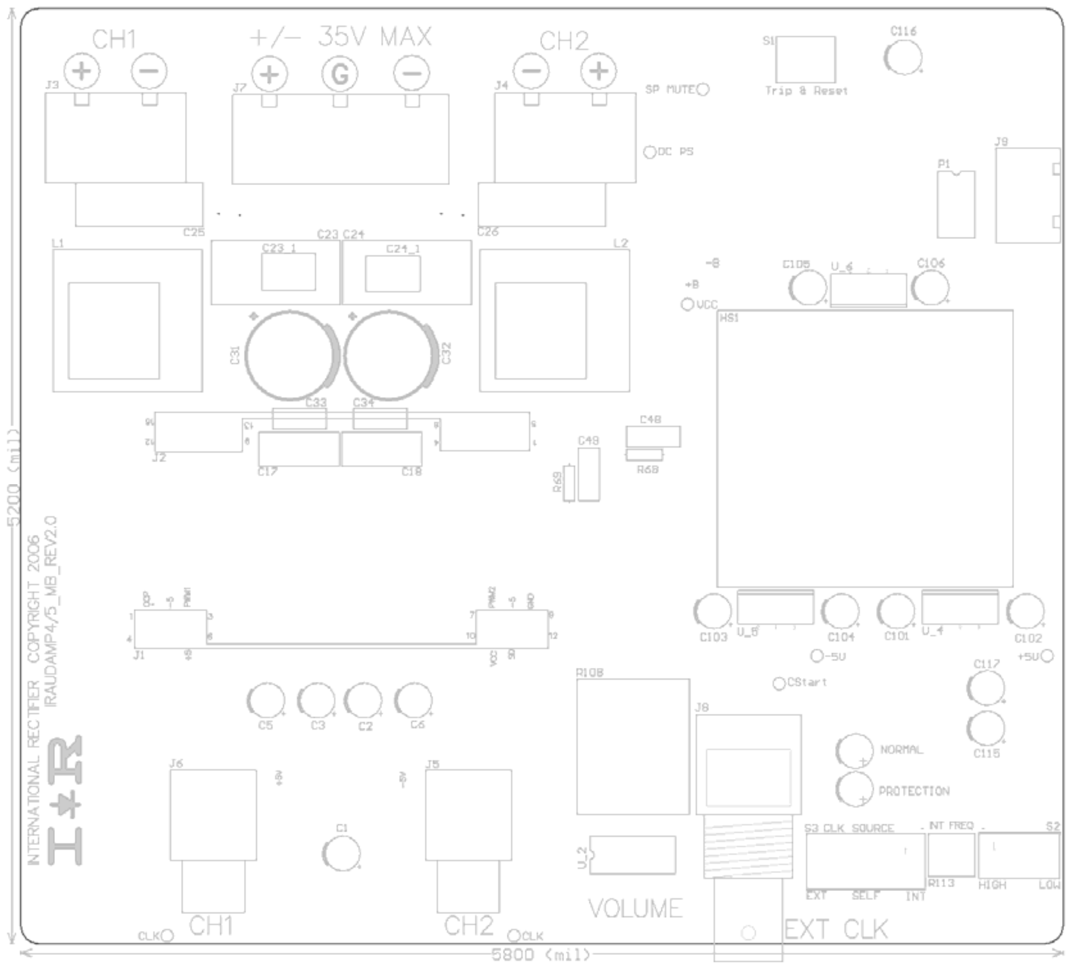


Fig 45 Top silk screen

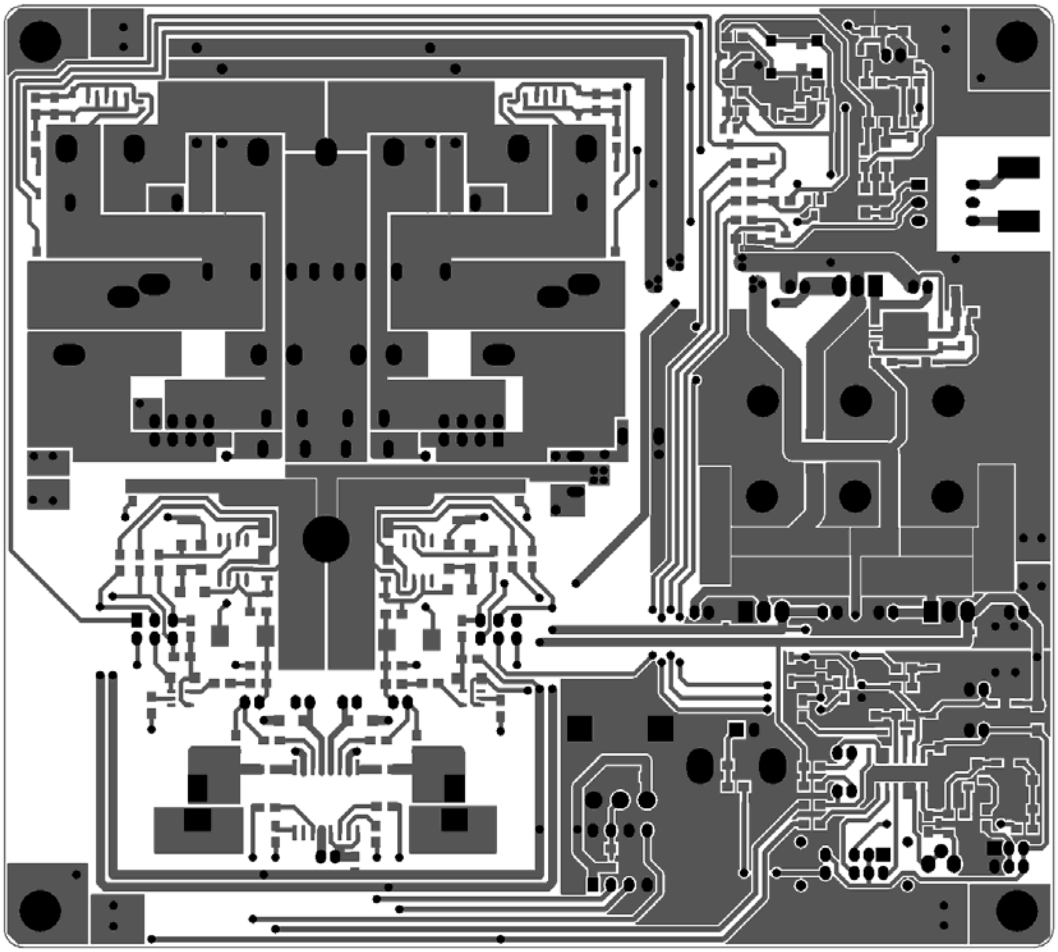


Fig 46 Bottom

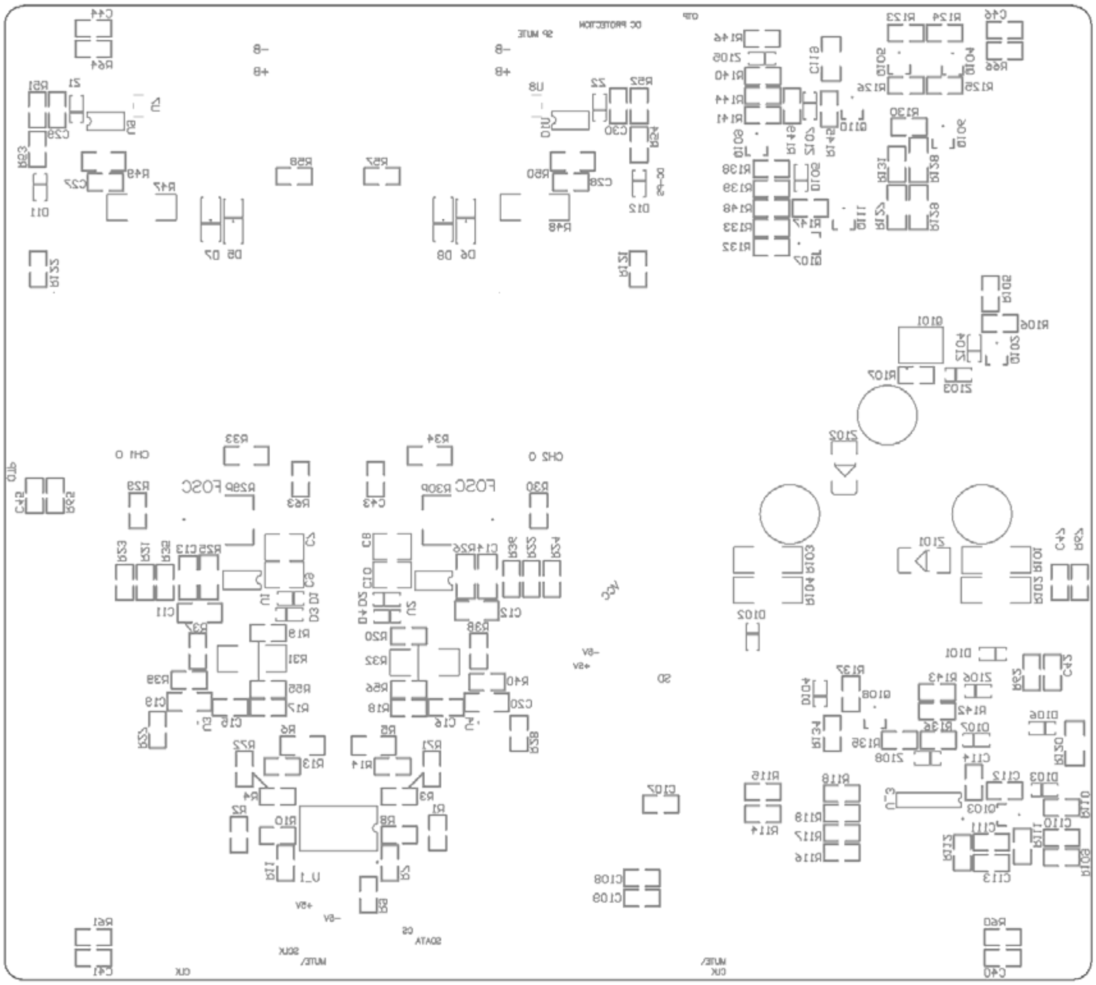


Fig 47

4.0

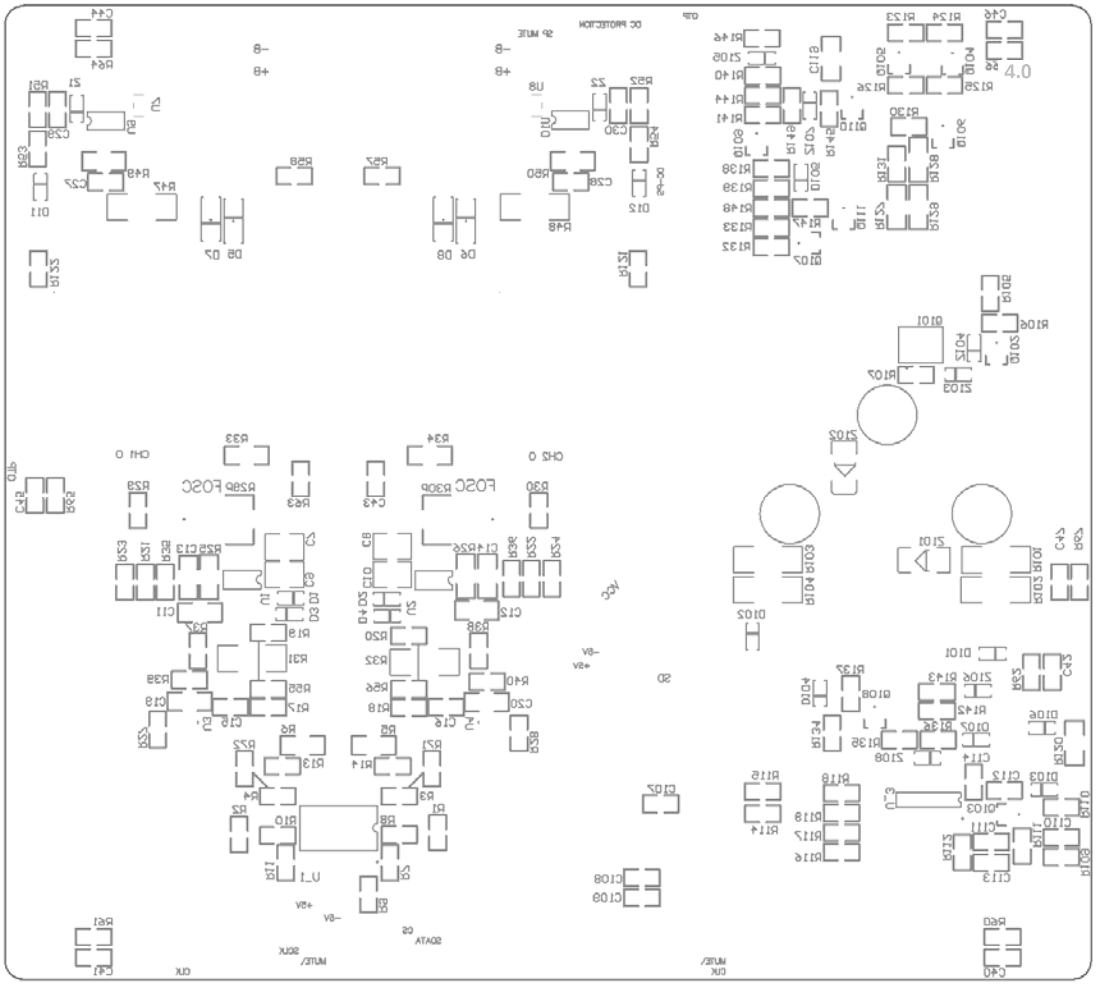


Fig 48 Bottom Silkscreen

Revision changes descriptions

Revision	Changes description	Date
3.0	Released	7/27/07
3.1	Schematic error marked on red pages 31-33 R25 and R29 was connected to CSH Fig 40 and Fig 41 updated	1/28/08
3.2	ROHS Compliant (BOM updated)	5/29/09
3.3	Deleted drawings author and e-mail	10/21/09
3.4	BOM updated :Ice Components as a second vender of the inductor	10/28/09
3.5	Correct Deadtime setting graph Fig 12	05/03/11

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9