MCP37210-200
MCP37D10-200

200 Msps, 12-Bit Low-Power Single-Channel ADC

Features

- Sample Rates: 200 Msps
- Signal-to-Noise Ratio (SNR) with f_{IN} = 15 MHz and -1 dBFS:
  - 67 dBFS (typical) at 200 Msps
- Spurious-Free Dynamic Range (SFDR) with f_{IN} = 15 MHz and -1 dBFS:
  - 96 dBc (typical) at 200 Msps
- Power Dissipation with LVDS Digital I/O:
  - 338 mW at 200 Msps
- Power Dissipation with CMOS Digital I/O:
  - 306 mW at 200 Msps, output clock = 100 MHz
- Power Dissipation Excluding Digital I/O:
  - 257 mW at 200 Msps
- Power-Saving Modes:
  - 80 mW during Standby
  - 33 mW during Shutdown
- Supply Voltage:
  - Digital Section: 1.2V, 1.8V
  - Analog Section: 1.2V, 1.8V
- Selectable Full-Scale Input Range: up to 1.8 V_{P-P}
- Analog Input Bandwidth: 650 MHz
- Output Interface:
  - Parallel CMOS, DDR LVDS
- Output Data Format:
  - Two's complement or offset binary
- Optional Output Data Randomizer
- Digital Signal Post-Processing (DSPP) Options:
  - Decimation filters for improved SNR
  - Offset and Gain adjustment
  - Noise-Shaping Requantizer (NSR)
  - Digital Down-Conversion (DDC) with I/Q or $f_S/8$ output (MCP37D10-200)
- Built-In ADC Linearity Calibration Algorithms:
  - Harmonic Distortion Correction (HDC)
  - DAC Noise Cancellation (DNC)
  - Dynamic Element Matching (DEM)
  - Flash Error Calibration
- Serial Peripheral Interface (SPI)
- Package Options:
  - VTLA-124 (9 mm x 9 mm x 0.9 mm)
  - TFBGA-121 (8 mm x 8 mm x 1.08 mm)
- No external reference decoupling capacitor required for TFBGA Package
- Industrial Temperature Range: –40°C to +85°C

Typical Applications

- Communication Instruments
- Microwave Digital Radio
- Cellular Base Stations
- Radar
- Scanners and Low-Power Portable Instruments
- Industrial and Consumer Data Acquisition System

Device Offering[(1)]

Part Number	Sample Rate	Resolution	Digital Decimation (FIR Filters)	Digital Down-Conversion	Noise-Shaping Requantizer
MCP37210-200	200 Msps	12	Yes	No	Yes
MCP37D10-200	200 Msps	12	Yes	Yes	Yes
MCP37220-200	200 Msps	14	Yes	No	No
MCP37D20-200	200 Msps	14	Yes	Yes	No

Note 1: For TFBGA package, contact Microchip Technology Inc. for availability. Devices in the same package type are pin-compatible.

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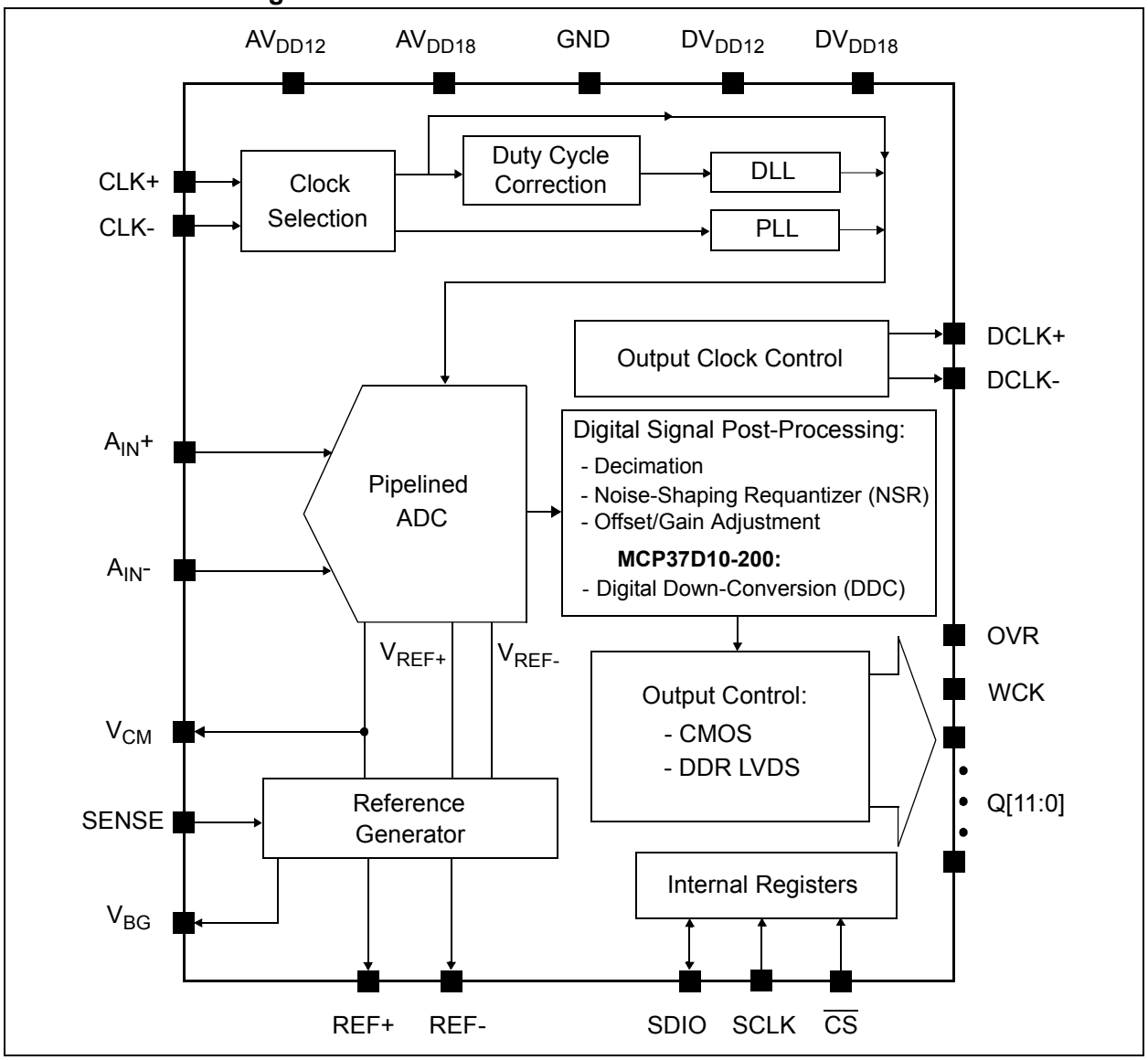
Functional Block Diagram



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Description

The MCP37210-200 is a single-channel 200 Msps 12-bit pipelined ADC, with built-in high-order digital decimation filters, Noise-Shaping Requantizer (NSR), gain and offset adjustment.

The MCP37D10-200 is also a single-channel 200 Msps 12-bit pipelined ADC, with built-in digital down-conversion in addition to the features offered by the MCP37210-200.

Both devices feature harmonic distortion correction and DAC noise cancellation that enables high-performance specifications with SNR of 67 dBFS (typical) and SFDR of 96 dBc (typical).

The output decimation filter option improves SNR performance up to 73.5 dBFS with the 64x decimation setting.

The NSR feature reshapes the quantization noise level so that most of the noise power is pushed outside the frequency band of interest. As a result, SNR is improved within a selected frequency band of interest, while SFDR is not affected.

The digital down-conversion option in the MCP37D10-200 can be utilized with the decimation and quadrature output (I and Q data) options, and offers great flexibility in various digital communication system designs, including cellular base-stations and narrow-band communication systems.

These A/D converters exhibit industry-leading low-power performance with only 338 mW operation, while using the LVDS output interface at 200 Msps. This superior low-power operation, coupled with high dynamic performance, makes these devices ideal for portable high-frequency instrumentation, sonar, radar, and high-speed data acquisition systems.

These devices also include various features designed to maximize flexibility in the user's applications and minimize system cost, such as a programmable PLL clock, output data rate control and phase alignment, and programmable digital pattern generation. The device's operational modes and feature sets are configured by setting up the user-programmable internal registers.

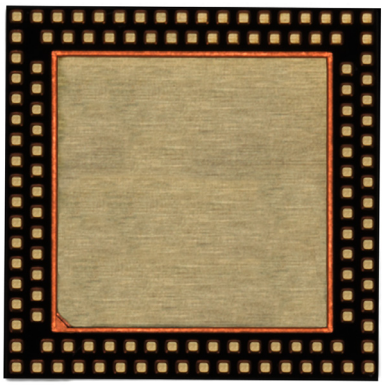
The device samples the analog input on the rising edge of the clock. The digital output code is available after 23 clock cycles of data latency. Latency will increase if any of the digital signal post-processing (DSPP) options are enabled.

The differential full-scale analog input range is programmable up to 1.8 V_{P-P}. The ADC output data can be coded in two's complement or offset binary representation, with or without the data randomizer option. The output data is available with a full-rate CMOS or Double-Data-Rate (DDR) LVDS interface.

The device is available in Pb-free VTLA-124 and TFBGA-121 packages. The device operates over the commercial temperature range of –40°C to +85°C.

Package Types

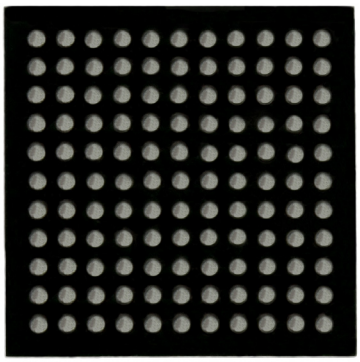
Bottom View



Dimension: 9 mm x 9 mm x 0.9 mm

(a) VTLA-124 Package.

Bottom View



Dimension: 8 mm x 8 mm x 1.08 mm
Ball Pitch: 0.65 mm
Ball Diameter: 0.4 mm

(b) TFBGA-121 Package.
(Contact Microchip Technology Inc. for availability)

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NOTES:

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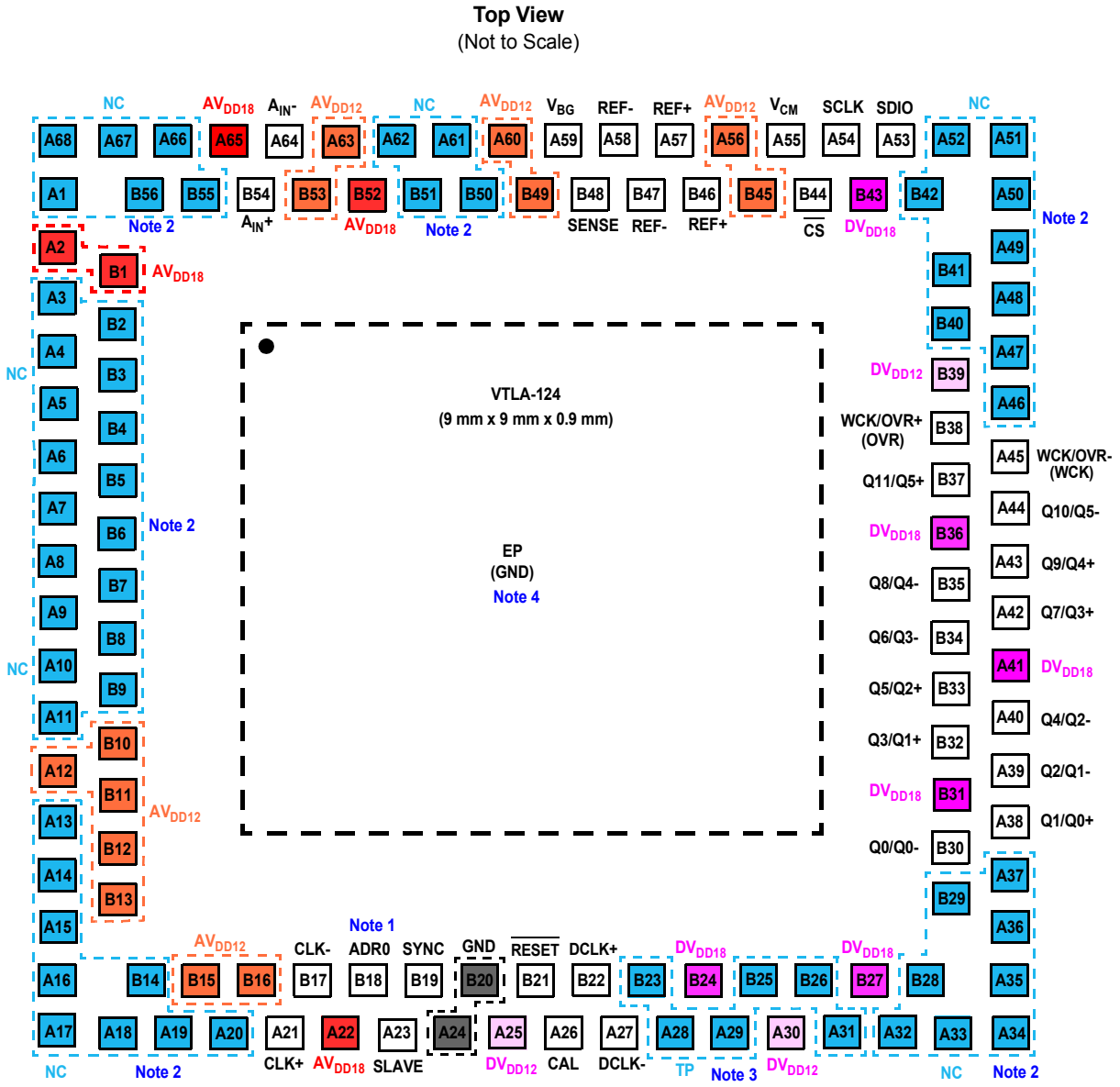
1.0 PACKAGE PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Note 1: Tie to GND or DV_{DD18}. ADR1 is internally bonded to GND.

2: NC – Not connected pin. This pin can float or be tied to ground.

3: TP – Test pin. Leave this pin floating and do not tie to ground or supply.

4: Exposed pad (EP – back pad of the package) is the common ground (GND) for analog and digital supplies. Connect this pad to a clean ground reference on the PCB.

FIGURE 1-1: *VTLA-124 Package.*

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124

Pin No.	Name	I/O Type	Description
Power Supply Pins			
A2, A22, A65, B1, B52	AV_{DD18}	Supply	Supply voltage input (1.8V) for analog section
A12, A56, A60, A63, B10, B11, B12, B13, B15, B16, B45, B49, B53	AV_{DD12}		Supply voltage input (1.2V) for analog section
A25, A30, B39	DV_{DD12}		Supply voltage input (1.2V) for digital section
A41, B24, B27, B31, B36, B43	DV_{DD18}		Supply voltage input (1.8V) for digital section and all digital I/O
EP	GND		Exposed pad: Common ground pin for digital and analog sections
ADC Analog Input Pins			
B54	A_{IN}+	Analog Input	Differential analog input (+)
A64	A_{IN}-		Differential analog input (-)
A21	CLK+		Differential clock input (+)
B17	CLK-		Differential clock input (-)
Reference Pins(1)			
A57, B46	REF+	Analog Output	Differential reference voltage (+)
A58, B47	REF-		Differential reference voltage (–)
SENSE, Bandgap and Common-Mode Voltage Pins			
B48	SENSE	Analog Input	Analog input full-scale range selection. See Table 4-2 for SENSE voltage settings.
A59	V_{BG}	Analog Output	Internal bandgap output voltage. Connect a decoupling capacitor (2.2 µF)
A55	V_{CM}		Common-mode output voltage for analog input signal. Connect a decoupling capacitor (0.1 µF)(2)
Digital I/O Pins			
B18	ADR0	Digital Input	SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}(3)
A23	SLAVE		Not used. Tie to GND(9)
B19	SYNC	Digital Input/Output	Not used. Leave this pin floating(9)
B21	$\overline{\text{RESET}}$	Digital Input	Reset control input: **High:** Normal operating mode **Low:** Reset mode(4)
A26	CAL	Digital Output	Calibration status flag digital output: **High:** Calibration is complete **Low:** Calibration is not complete(5)
B22	DCLK+		**LVDS**: Differential digital clock output (+) **CMOS:** Digital clock output(6)
A27	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)

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TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
ADC Output Pins[7]			
B30	Q0/Q0-	Digital Output	Digital data output: CMOS = Q0 DDR LVDS = Q0-
A38	Q1/Q0+		Digital data output: CMOS = Q1 DDR LVDS = Q0+
A39	Q2/Q1-		Digital data output: CMOS = Q2 DDR LVDS = Q1-
B32	Q3/Q1+		Digital data output: CMOS = Q3 DDR LVDS = Q1+
A40	Q4/Q2-		Digital data output: CMOS = Q4 DDR LVDS = Q2-
B33	Q5/Q2+		Digital data output: CMOS = Q5 DDR LVDS = Q2+
B34	Q6/Q3-		Digital data output: CMOS = Q6 DDR LVDS = Q3-
A42	Q7/Q3+		Digital data output: CMOS = Q7 DDR LVDS = Q3+
B35	Q8/Q4-		Digital data output: CMOS = Q8 DDR LVDS = Q4-
A43	Q9/Q4+		Digital data output: CMOS = Q9 DDR LVDS = Q4+
A44	Q10/Q5-		Digital data output: CMOS = Q10 DDR LVDS = Q5-
B37	Q11/Q5+		Digital data output: CMOS = Q11 DDR LVDS = Q5+
B38	WCK/OVR+ (OVR)		**OVR:** Input over-range indication digital output[8] **WCK:**
A45	WCK/OVR- (WCK)		- **MCP37210:** No output - **MCP37D10:** Word clock synchronizes with digital output in I/Q data mode
SPI Interface Pins			
A53	SDIO	Digital Input/Output	SPI data input/output
A54	SCLK	Digital Input	SPI serial clock input
B44	CS		SPI Chip Select input
Not Connected Pins			
A1, A3 - A7, A8 - A11, A13 - A20, A32 - A37, A46 - A52, A61 - A62, A66 - A68, B2 - B9, B14, B28, B29, B40, B41, B42, B50 - B51, B55, B56	NC		These pins can be tied to ground or left floating.

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
Pins that need to be grounded			
A24, A64, B20, B54	GND		These pins are not supply pins, but need to be tied to ground.
Output Test Pins			
A28 - A29, A31, B23, B25, B26	TP	Digital Output	Output test pins. Do not use. Always leave these pins floating. Do not tie to ground or supply.

Notes:

1. These pins are for the internal reference voltage output. They should not be driven. External decoupling circuit is required. See **Section 4.3.3 "Decoupling Circuits for Internal Voltage Reference and Bandgap Output"** for details.
2. When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), V_{CM} pin should be decoupled with a 0.1 µF capacitor.
3. ADR1 (for A1 bit) is internally bonded to GND ('0'). If ADR0 is dynamically controlled, ADR0 must be held constant while $\overline{CS}$ is "Low".
4. The device is in Reset mode while this pin stays "Low". On the rising edge of $\overline{RESET}$, the device exits the Reset mode, initializes all internal user registers to default values and begins power-up calibration.
5. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or a Soft Reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes, this pin will maintain the prior condition.
6. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital signal post-processing (DSPP) and PLL (or DLL). See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
7. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first", which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 (Register 5-20). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11) appear when DCLK+ is "Low". See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figure 2-2 for LVDS output timing diagrams.
8. **OVR:** OVR will be held "High"' when analog input overrange is detected. Digital signal post-processing (DSPP) will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
   WCK: Available for the I/Q output mode only in the MCP37D10. WCK is normally "Low" in I/Q output mode, and "High" when it outputs in-phase (I) data.
   (a) MCP37210 and MCP37D10 operating outside I/Q output mode: WCK/OVR+ is OVR, and WCK/OVR- is logic '0' (not used). In DDR LVDS output mode, the rising edge of DCLK+ is OVR.
   (b) I/Q output mode in MCP37D10: In CMOS output mode, WCK/OVR+ is OVR and WCK/OVR- is WCK. WCK is synchronized to in-phase (I) data. In DDR LVDS output mode, WCK/OVR+ and WCK/OVR- are multiplexed. The rising edge of DCLK+ is OVR and the falling edge is WCK.
9. This pin function is not released yet.

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Top View
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11
A	SDIO	V_{CM}	REF+	REF-	V_{BG}	TP1	TP1	A_{IN-}	A_{IN+}	GND	GND
B	SCLK	$\overline{CS}$	GND	GND	SENSE	AV_{DD12}	AV_{DD12}	AV_{DD18}	AV_{DD18}	GND	GND
C	WCK/ OVR- (WCK)	WCK/ OVR+ (OVR)	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
D	Q10/Q5-	Q11/Q5+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
E	Q8/Q4-	Q9/Q4+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
F	Q6/Q3-	Q7/Q3+	DV_{DD18}	DV_{DD18}	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
G	Q4/Q2-	Q5/Q2+	DV_{DD18}	DV_{DD18}	GND	GND	AV_{DD12}	AV_{DD12}	GND	GND	GND
H	Q2/Q1-	Q3/Q1+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	GND	GND
J	Q0/Q0-	Q1/Q0+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	GND	GND
K	TP2	TP2	TP2	DCLK-	CAL	GND	SLAVE	ADR0	ADR1	GND	GND
L	TP2	TP2	TP2	DCLK+	$\overline{RESET}$	SYNC	GND	CLK+	CLK-	GND	AV_{DD18}

Analog
Digital
All others: Supply Voltage

Notes:

- Die dimension: 8 mm x 8 mm x 1.08 mm.
- Ball dimension: (a) Ball Pitch = 0.65 mm, (b) Ball Diameter = 0.4 mm.
- Flip-chip solder ball composition: Sn with Ag 1.8%.
- Solder sphere composition: SAC-405 (Sn/Au 4%/Cu 0.5%).

FIGURE 1-2: *TFBGA-121 Package. Decoupling capacitors for reference pins and V_{BG} are embedded in the package.*

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121

Ball No.	Name	I/O Type	Description
A1	SDIO	Digital Input/Output	SPI data input/output
A2	V_{CM}	Analog Output	Common-mode output voltage for analog input signal Connect a decoupling capacitor (0.1 µF)[1]
A3	REF+		Differential reference voltage (+/-). Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating.
A4	REF-		
A5	V_{BG}		Internal bandgap output voltage A decoupling capacitor (2.2 µF) is embedded in the TFBGA package. Leave this pin floating.
A6	TP1	Analog Output	Analog test pins. Leave these pins floating.
A7			
A8	A_{IN-}	Analog Input	Differential analog input (-)
A9	A_{IN+}		Differential analog input (+)
A10	GND	Supply	Common ground for analog and digital sections
A11			
B1	SCLK	Digital Input	SPI serial clock input
B2	CS		SPI chip select input
B3	GND	Supply	Common ground for analog and digital sections
B4			
B5	SENSE	Analog Input	Analog input range selection. See Table 4-2 for SENSE voltage settings.
B6	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
B7			
B8	AV_{DD18}		Supply voltage input (1.8V) for analog section
B9			
B10	GND	Supply	Common ground for analog and digital sections
B11			
C1	WCK/OVR- (WCK)	Digital Output	**OVR:** Input overrange indication digital output[2] **WCK:** - **MCP37210**: No output - **MCP37D10:** Word clock synchronizes with digital output in I/Q data mode
C2	WCK/OVR+ (OVR)		
C3	GND	Supply	Common ground for analog and digital sections
C4			
C5	AV_{DD12}		Supply voltage input (1.2V) for analog section
C6			
C7			
C8	GND		Common ground pin for analog and digital sections
C9			
C10			
C11			
D1	Q10/Q5-	Digital Output	Digital data output[3] CMOS = Q10 DDR LVDS = Q5-
D2	Q11/Q5+		Digital data output[3] CMOS = Q11 DDR LVDS = Q5+

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TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
D3	GND	Supply	Common ground for analog and digital sections
D4			
D5	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
D6			
D7			
D8	GND	Supply	Common ground for analog and digital sections
D9			
D10			
D11			
E1	Q8/Q4-	Digital Output	Digital data output(3) CMOS = Q8 DDR LVDS = Q4-
E2	Q9/Q4+		Digital data output(3) CMOS = Q9 DDR LVDS = Q4+
E3	GND	Supply	Common ground for analog and digital sections
E4			
E5	AV_{DD12}		Supply voltage input (1.2V) for analog section
E6			
E7			
E8	GND		Common ground for analog and digital sections
E9			
E10			
E11			
F1	Q6/Q3-	Digital Output	Digital data output(3) CMOS = Q6 DDR LVDS = Q3-
F2	Q7/Q3+		Digital data output(3) CMOS = Q7 DDR LVDS = Q3+
F3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential.
F4			
F5	AV_{DD12}		Supply voltage input (1.2V) for analog section
F6			
F7			
F8	GND		Common ground for analog and digital sections
F9			
F10			
F11			
G1	Q4/Q2-	Digital Output	Digital data output(3) CMOS = Q4 DDR LVDS = Q2-
G2	Q5/Q2+		Digital data output(3) CMOS = Q5 DDR LVDS = Q2+

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
G3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential
G4			
G5	GND		Common ground for analog and digital sections
G6			
G7	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
G8			
G9	GND		Common ground for analog and digital sections
G10			
G11			
H1	Q2/Q1-	Digital Output	Digital data output(3) CMOS = Q2 DDR LVDS = Q1-
H2	Q3/Q1+		Digital data output(3) CMOS = Q3 DDR LVDS = Q1+
H3	DV_{DD12}	Supply	Supply voltage input (1.2V) for digital section
H4			
H5	GND		Common ground for analog and digital sections
H6			
H7			
H8			
H9			
H10			
H11			
J1	Q0/Q0-	Digital Output	Digital data output(3) CMOS = Q0 DDR LVDS = Q0-
J2	Q1/Q0+		Digital data output(3) CMOS = Q1 DDR LVDS = Q0+
J3	DV_{DD12}	Supply	DC supply voltage input pin for digital section (1.2V)
J4			
J5	GND		Common ground for analog and digital sections
J6			
J7			
J8			
J9			
J10			
J11			
K1	TP2	Digital Output	Output test pins. Do not use. Do not tie to ground or supply. Always leave this pin floating.
K2			
K3			
K4	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)
K5	CAL		Calibration status flag digital output(4): **High:** Calibration is complete **Low:** Calibration is not complete

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TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
K6	GND	Supply	Common ground pin for analog and digital sections
K7	SLAVE	Digital Input	Not used. Tie this pin to GND(8)
K8	ADR0		SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}(5)
K9	ADR1		SPI address selection pin (A1 bit). Tie to GND or DV_{DD18}(5)
K10	GND	Supply	Common ground for analog and digital sections
K11			
L1	TP2	Digital Output	Output test pins. Do not use. Do not tie to ground or supply. Always leave these pins floating.
L2			
L3			
L4	DCLK+		**LVDS:** Differential digital clock output (+) **CMOS:** Digital clock output(6)
L5	$\overline{\text{RESET}}$	Digital Input	Reset control input: **High**: Normal operating mode **Low:** Reset mode(7)
L6	SYNC	Digital Input/Output	Not used. Leave this pin floating(8)
L7	GND	Supply	Common ground for analog and digital sections
L8	CLK+	Analog Input	Differential clock input (+)
L9	CLK-		Differential clock input (-)
L10	GND	Supply	Common ground for analog and digital sections
L11	AV_{DD18}	Analog Input	Supply voltage input (1.8V) for analog section

Notes:

1. When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center tap of a balun), the V_{CM} pin should be decoupled with a 0.1 µF capacitor.
2. **OVR:** OVR will be held “High”’ when analog input overrange is detected. Digital signal post-processing (DSPP) will cause OVR to assert early relative to the output data. See Figure 2-2 for timing of these bits.
   WCK: Available for the I/Q output mode only in the MCP37D10. In the I/Q output mode, WCK is normally “Low”, but “High” when it outputs in-phase (I) data.
   (a) **MCP37210 and MCP37D10 operating outside I/Q output mode**: WCK/OVR+ is OVR and WCK/OVR- is logic ‘0’ (not used). In DDR LVDS output mode, the rising edge of DCLK+ is OVR.
   (b) **I/Q output mode in MCP37D10:** In CMOS output mode, WCK/OVR+ is OVR and WCK/OVR- is WCK. WCK is synchronized to in-phase (I) data. In DDR LVDS output mode, WCK/OVR+ and WCK/OVR- are multiplexed. The rising edge of DCLK+ is OVR and the falling edge is WCK.
3. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The even data bits (Q0, Q2, Q4, Q6, Q8, Q10) appear when DCLK+ is “High”. The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11) appear when DCLK+ is “Low”. See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figure 2-2 for LVDS output timing diagram.
4. CAL pin stays “Low” at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has “High” output. It stays “High” until the internal calibration is restarted by hardware or a Soft Reset command. In Reset mode, this pin is “Low”. In Standby and Shutdown modes this pin will maintain the prior condition.
5. If the SPI address is dynamically controlled, the Address pin must be held constant while $\overline{\text{CS}}$ is “Low”.
6. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital signal post-processing (DSPP) and PLL (or DLL). See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
7. The device is in Reset mode while this pin stays “Low”. On the rising edge of $\overline{\text{RESET}}$, the device exits the Reset mode, initializes all internal user registers to default values, and begins power-up calibration.
8. This pin function is not released yet.

NOTES:

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2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings †

Analog and Digital Supply Voltage (AV_{DD12}, DV_{DD12}) ..... –0.3V to 1.32V
Analog and Digital Supply Voltage (AV_{DD18}, DV_{DD18}) ..... –0.3V to 1.98V
All Inputs and Outputs with respect to GND ..... –0.3V to AV_{DD18} + 0.3V
Differential Input Voltage ..... $|AV_{DD18}$ - GND|
Current at Input Pins ..... ±2 mA
Current at Output and Supply Pins ..... ±250 mA
Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied (T_A) ..... –55°C to +125°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD Protection on all Pins ..... 2 kV HBM
Solder Reflow Profile ..... See Microchip Application Note AN233 (DS00233)

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Electrical Specifications

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Requirements						
Analog Supply Voltage	AV_{DD18}	1.71	1.8	1.89	V	
	AV_{DD12}	1.14	1.2	1.26	V	
Digital Supply Voltage	DV_{DD18}	1.71	1.8	1.89	V	**Note 1**
	DV_{DD12}	1.14	1.2	1.26	V	
Analog Supply Current						
Analog Supply Current during Conversion	I_{DD_A18}	—	1	1	mA	at AV_{DD18} Pin
	I_{DD_A12}	—	141	159	mA	at AV_{DD12} Pin
Digital Supply Current						
Digital Supply Current during Conversion	I_{DD_D12}	—	72	109	mA	at DV_{DD12} Pin
Digital I/O Current in CMOS Output Mode	I_{DD_D18}	—	27	—	mA	at DV_{DD18} Pin DCLK = 100 MHz
Digital I/O Current in LVDS Mode	I_{DD_D18}	Measured at DV_{DD18} Pin				
		—	45	66	mA	3.5 mA mode
			33	—	mA	1.8 mA mode
			57			5.4 mA mode
Supply Current during Power-Saving Modes						
During Standby Mode	$I_{STANDBY_AN}$	—	21	—	mA	Address 0x00<4:3> = 1,1 (2)
	$I_{STANDBY_DIG}$	—	41	—		
During Shutdown Mode	I_{DD_SHDN}	—	25	—	mA	Address 0x00<7,0> = 1,1 (3)

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PLL Circuit						
PLL Circuit Current	I_{DD_PLL}	—	21	—	mA	PLL enabled. Included in analog supply current specification.
Total Power Dissipation(4)						
Power Dissipation during Conversion, excluding Digital I/O	P_{DISS_ADC}	—	257	—	mW	
Total Power Dissipation during Conversion with CMOS Output Mode	P_{DISS_CMOS}	—	306	—	mW	f_S = 200 Msps, DCLK = 100 MHz
Total Power Dissipation during Conversion with LVDS Output Mode	P_{DISS_LVDS}	—	338	—	mW	3.5 mA mode
			317			1.8 mA mode
			360			5.4 mA mode
During Standby Mode	$P_{DISS_STANDBY}$	—	80	—	mW	Address 0x00<4:3> = 1,1(2)
During Shutdown Mode	P_{DISS_SHDN}	—	33	—	mW	Address 0x00<7,0> = 1,1(3)
Power-on Reset (POR) Voltage						
Threshold Voltage	V_{POR}	—	800	—	mV	Applicable to AV_{DD12} only (POR tracks AV_{DD12})
Hysteresis	V_{POR_HYST}	—	40	—	mV	
SENSE Input(5,7,13)						
SENSE Input Voltage	V_{SENSE}	GND	—	AV_{DD12}	V	V_{SENSE} selects reference
SENSE Pin Input Resistance	R_{IN_SENSE}	—	694	—	Ω	V_{SENSE} = 0.8V
		—	154.8	—	kΩ	V_{SENSE} = 1.2V
Current Sink into SENSE Pin	I_{SENSE}	—	360	—	µA	V_{SENSE} = 0.8V
		—	4.2	—	µA	V_{SENSE} = 1.2V
Reference and Common-Mode Voltages						
Internal Reference Voltage(7,8)	V_{REF}	—	0.4	—	V	V_{SENSE} = GND
		—	0.8	—		V_{SENSE} = AV_{DD12}
		—	V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Common-Mode Voltage Output	V_{CM}	—	0.55	—	V	Available at V_{CM} pin
Bandgap Voltage Output	V_{BG}	—	0.55	—	V	Available at V_{BG} pin

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TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Analog Inputs						
Full-Scale Differential Analog Input Range(5,7)	A_{FS}	—	0.9	—	V_{P-P}	V_{SENSE} = GND
		—	1.8	—		V_{SENSE} = AV_{DD12}
		—	2.25 x V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Analog Input Bandwidth	f_{IN_3dB}	—	650	—	MHz	A_{IN} = –3 dBFS
Differential Input Capacitance	C_{IN}		1.6		pF	**Note 5**, **Note 9**
Analog Input Leakage Current (A_{IN}+, A_{IN}- Pins)	I_{LI_AH}	—	—	50	µA	V_{IH} = AV_{DD12}
	I_{LI_AL}	-50	—	—	µA	V_{IL} = GND
ADC Conversion Rate						
Conversion Rate	f_S		—	200	Msps	Tested at 200 Msps
Clock Inputs (CLK+, CLK-)(10)						
Clock Input Frequency	f_{CLK}	—	—	250	MHz	**Note 5**
Differential Input Voltage	V_{CLK_IN}	300	—	800	mV_{P-P}	**Note 5**
Clock Jitter	CLK_{JITTER}	—	175	—	fS_{RMS}	**Note 5**
Clock Input Duty Cycle(5)		49	50	51	%	Duty cycle correction disabled
		30	50	70	%	Duty cycle correction enabled
Input Leakage Current at CLK Input Pin	I_{LI_CLKH}	—	—	+110	µA	V_{IH} = AV_{DD12}
	I_{LI_CLKL}	-15	—	—	µA	V_{IL} = GND
Converter Accuracy(6)						
ADC Resolution (with no missing code)		—	—	12	bits	
Offset Error		—	±3.75	±11.25	LSb	
Gain Error	G_{ER}	—	±0.5	—	% of FS	
Integral Nonlinearity	INL	—	±0.375	—	LSb	
Differential Nonlinearity	DNL	—	±0.1	—	LSb	
Analog Input Common-Mode Rejection Ratio	$CMRR_{DC}$	—	70	—	dB	DC measurement

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dynamic Accuracy(6,14)						
Spurious Free Dynamic Range	SFDR	82	96		dBc	f_{IN} = 15 MHz
			81		dBc	f_{IN} = 70 MHz
Signal-to-Noise Ratio (for all resolutions)	SNR	65.5	67		dBFS	f_{IN} = 15 MHz
			66.5			f_{IN} = 70 MHz
Effective Number of Bits (ENOB)(11)	ENOB		10.8		bits	f_{IN} = 15 MHz
			10.8			f_{IN} = 70 MHz
Total Harmonic Distortion (first 13 harmonics)	THD	83	89		dBc	f_{IN} = 15 MHz
			81		dBc	f_{IN} = 70 MHz
Worst Second or Third Harmonic Distortion	HD2 or HD3		95.8		dBc	f_{IN} = 15 MHz
			82		dBc	f_{IN} = 70 MHz
Two-Tone Intermodulation Distortion f_{IN1} = 15 MHz, f_{IN2} = 17 MHz	IMD	—	92.7	—	dBc	A_{IN} = –7 dBFS, with two input frequencies
Digital Logic Input and Output (Except LVDS Output)						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7 DV_{DD18}	—	DV_{DD18}	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	GND	—	0.3 DV_{DD18}	V	
Hysteresis of Schmitt Trigger Inputs (All digital inputs)	V_{HYST}	—	0.05 DV_{DD18}	—	V	
Low-Level Output Voltage	V_{OL}	—	—	0.3	V	I_{OL} = -3 mA, all digital I/O pins
High-Level Output Voltage	V_{OH}	DV_{DD18} – 0.5	1.8	—	V	I_{OL} = + 3mA, all digital I/O pins
Digital Data Output (CMOS Mode)						
Maximum External Load Capacitance	C_{LOAD}	—	10	—	pF	From output pin to GND
Internal I/O Capacitance	C_{INT}	—	4	—	pF	**Note 5**

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TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Digital Data Output (LVDS Mode)(5)						
LVDS High-Level Differential Output Voltage	V_{H_LVDS}	200	300	400	mV	100Ω differential termination, LVDS bias = 3.5 mA
LVDS Low-Level Differential Output Voltage	V_{L_LVDS}	-400	-300	-200	mV	100Ω differential termination, LVDS bias = 3.5 mA
LVDS Common-Mode Voltage	V_{CM_LVDS}	1	1.15	1.4	V	
Output Capacitance	C_{INT_LVDS}	—	4	—	pF	Internal capacitance from output pin to GND
Differential Load Resistance (LVDS)	R_{LVDS}	—	100	—	Ω	Across LVDS output pairs
Input Leakage Current on Digital I/O Pins						
Data Output Pins	I_{LI_DH}	—	—	+1	µA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-1	—	—	µA	V_{IL} = GND
I/O Pins except Data Output Pins	I_{LI_DH}	—	—	+6	µA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-35	—	—	µA	V_{IL} = GND(12)

Notes:

1. This 1.8V digital supply voltage is used for the digital I/O circuit, including SPI, CMOS and LVDS data output drivers.
2. Standby mode: Most of the internal circuits are turned-off, except internal reference, clock, bias circuits and SPI interface.
3. Shutdown mode: All circuits, including reference and clock, are turned-off, except the SPI interface.
4. The total power dissipation is calculated by using the following equation:
   $P_{DISS} = V_{DD18} \times (I_{DD_A18} + I_{DD_D18}) + V_{DD12} \times (I_{DD_A12} + I_{DD_D12})$, where I_{DD_D18} is the digital I/O current for LVDS or CMOS output. V_{DD18} = 1.8V and V_{DD12} = 1.2V are used for typical value calculation.
5. This parameter is ensured by design, but not 100% tested in production.
6. This parameter is ensured by characterization, but not 100% tested in production.
7. See Table 4-1 for details.
8. Differential reference voltage output at REF+/- pins. $V_{REF} = V_{REF}+ – V_{REF}-$.
   These references should not be driven.
9. Input capacitance refers to the effective capacitance between differential input pin pair.
10. See Figure 4-8 for details of clock input circuit.
11. ENOB = (SINAD - 1.76)/6.02.
12. This leakage current is due to internal pull-up resistor.
13. R_{IN_SENSE} is calculated from SENSE pin to virtual ground at 0.55V for 400 mV < V_{SENSE} <800 mV.
    $R_{SENSE} = (V_{SENSE} - 0.55V)/I_{SENSE}$.
14. Dynamic performance is characterized with DIG_GAIN<7:0> = 0011-1000.

TABLE 2-2: TIMING REQUIREMENTS – LVDS AND CMOS OUTPUTS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Aperture Delay	t_A	—	1	—	ns	**Note 1**
Out-of-Range Recovery Time	t_{OVR}	—	1	—	Clocks	**Note 1**
Output Clock Duty Cycle		—	50	—	%	**Note 1**
Pipeline Latency	$T_{LATENCY}$	—	23	—	Clocks	**Note 2**, **Note 4**
System Calibration(1)						
Power-Up Calibration Time	T_{PCAL}	—	3×2^{26}	—	Clocks	First 3×2^{26} sample clocks after power-up
Background Calibration Update Rate	T_{BCAL}	—	2^{30}	—	Clocks	Per 2^{30} sample clocks after T_{PCAL}
$\overline{\text{RESET}}$ Low Time	T_{RESET}	5	—	—	ns	See Figure 2-6 for details(1)
LVDS Data Output Mode						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	—	3.2	ns	
Output Clock to Data Propagation Delay	t_{DC}	-0.25	—	+0.25	ns	**Note 1**
Input Clock to Output Data Propagation Delay	t_{PD}	—	—	3.25	ns	
Rise Time (20% to 80% of Output Amplitude)(2,3)	t_{RISE_DATA}	—	0.25	0.5	ns	
	t_{RISE_CLK}	—	0.25	0.5	ns	
Fall Time (80% to 20% of Output Amplitude)(2,3)	t_{FALL_DATA}	—	0.25	0.5	ns	
	t_{FALL_CLK}	—	0.25	0.5	ns	
CMOS Data Output Mode						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	6	—	ns	DCLK = 100 MHz
Output Clock to Data Propagation Delay	t_{DC}	—	0.25	—	ns	DCLK = 100 MHz
Input Clock to Output Data Propagation Delay	t_{PD}	—	6.25	—	ns	DCLK = 100 MHz
Rise Time (20% to 80% of Output Amplitude)	t_{RISE_DATA}	TBD			ns	DCLK = 100 MHz
	t_{RISE_CLK}	TBD			ns	DCLK = 100 MHz
Fall Time (80% to 20% of Output Amplitude)	t_{FALL_DATA}	TBD			ns	DCLK = 100 MHz
	t_{FALL_CLK}	TBD			ns	DCLK = 100 MHz

Note 1: This parameter is ensured by design, but not 100% tested in production.

2: This parameter is ensured by characterization, but not 100% tested in production.

3: t_{RISE} = approximately less than 10% of duty cycle.

4: Output latency is measured without using decimation filter and digital down-converter options.

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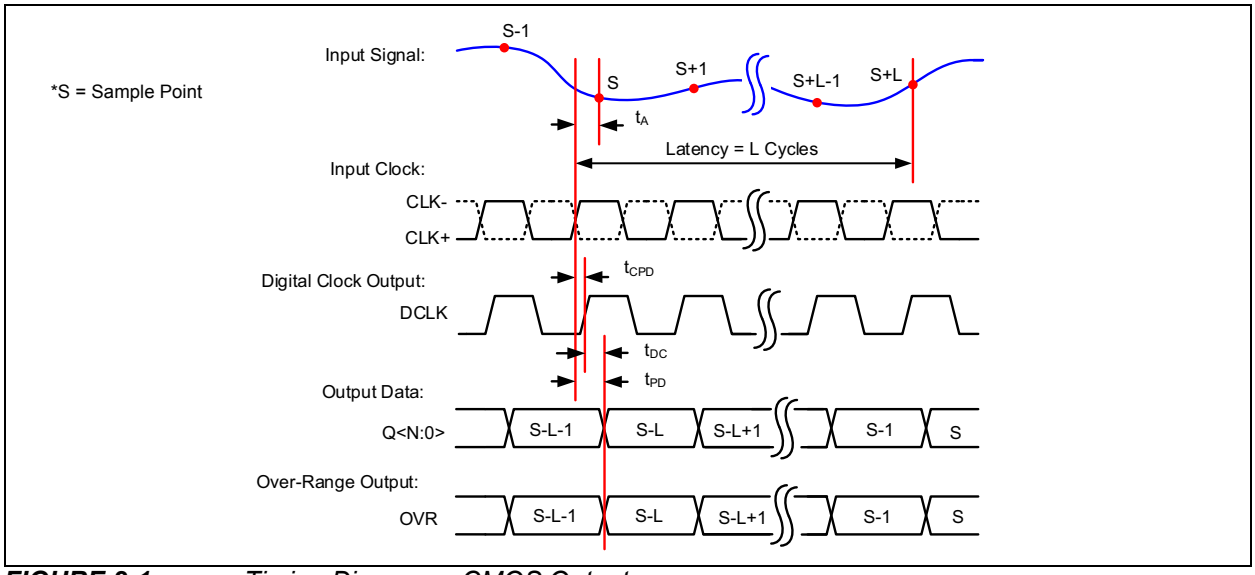
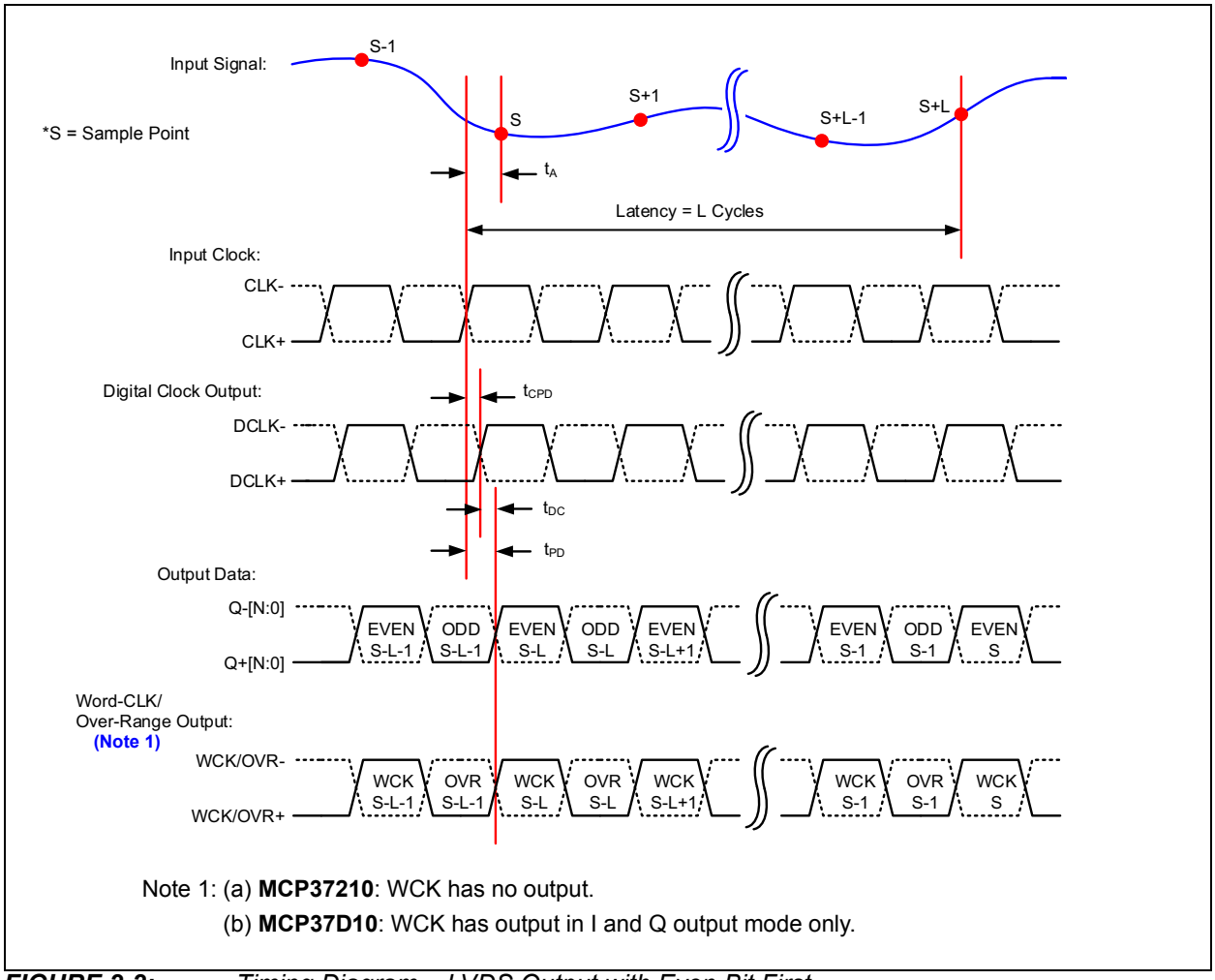


FIGURE 2-1: *Timing Diagram – CMOS Output.*



Note 1: (a) **MCP37210**: WCK has no output.
(b) **MCP37D10**: WCK has output in I and Q output mode only.

FIGURE 2-2: *Timing Diagram – LVDS Output with Even Bit First.*

TABLE 2-3: SPI SERIAL INTERFACE TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value. All timings are measured at 50%.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Serial Clock Frequency, f_{SCK} = 50 MHz						
$\overline{CS}$ Setup Time	t_{CSS}	10	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	20	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	20	—	—	ns	
Data Setup Time	t_{SU}	2	—	—	ns	
Data Hold Time	t_{HD}	4	—	—	ns	
Serial Clock High Time	t_{HI}	8	—	—	ns	
Serial Clock Low Time	t_{LO}	8	—	—	ns	**Note 1**
Serial Clock Delay Time	t_{CLD}	20	—	—	ns	
Serial Clock Enable Time	t_{CLE}	20	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	20	ns	
Output Disable Time	t_{DIS}	—	—	10	ns	**Note 1**

Note 1: This parameter is ensured by design, but not 100% tested in production.

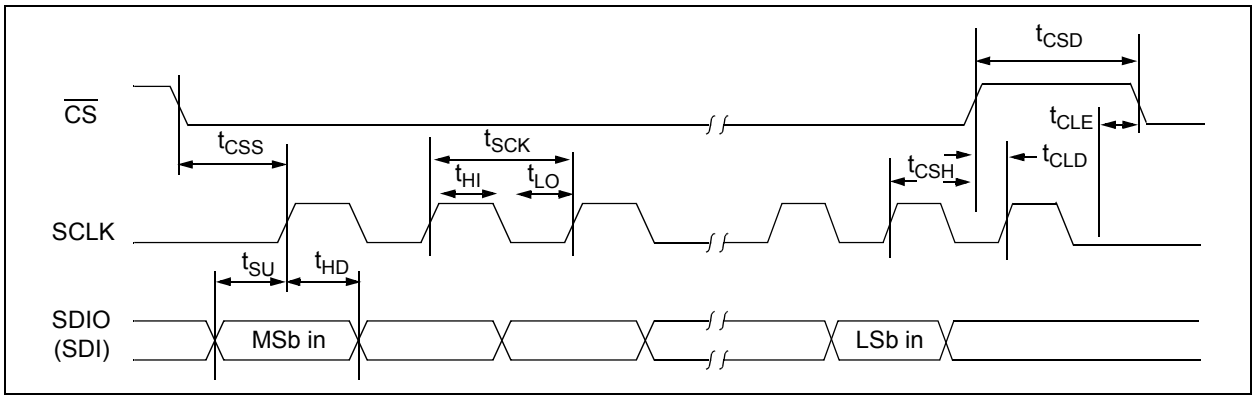


FIGURE 2-3: *SPI Serial Input Timing Diagram.*

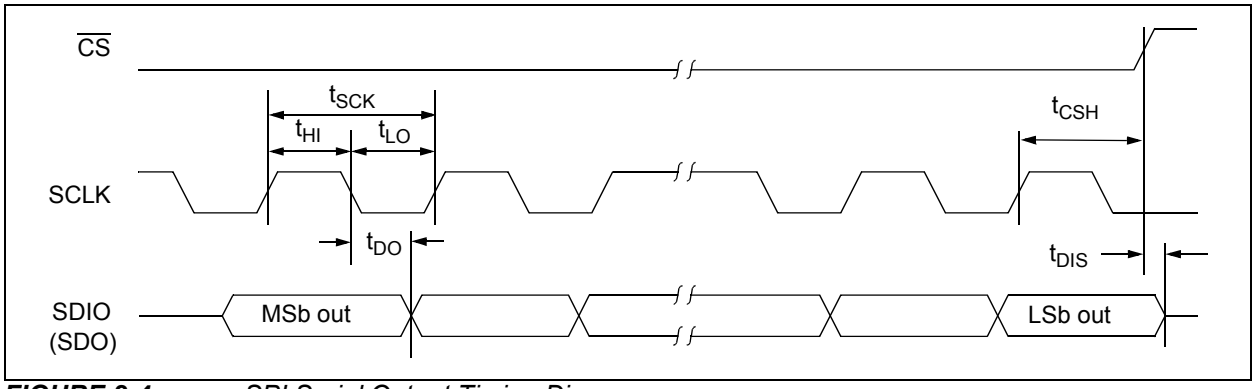


FIGURE 2-4: *SPI Serial Output Timing Diagram.*

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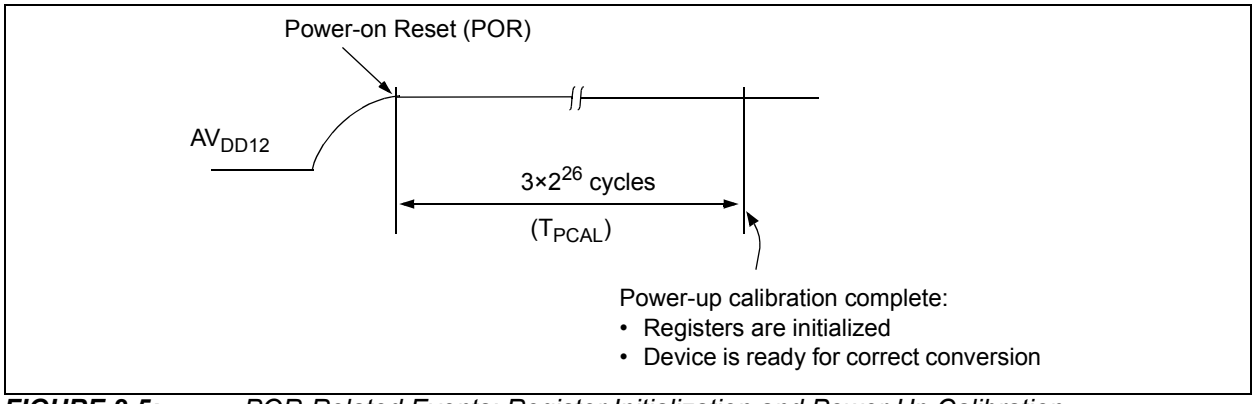

FIGURE 2-5: *POR-Related Events: Register Initialization and Power-Up Calibration.*

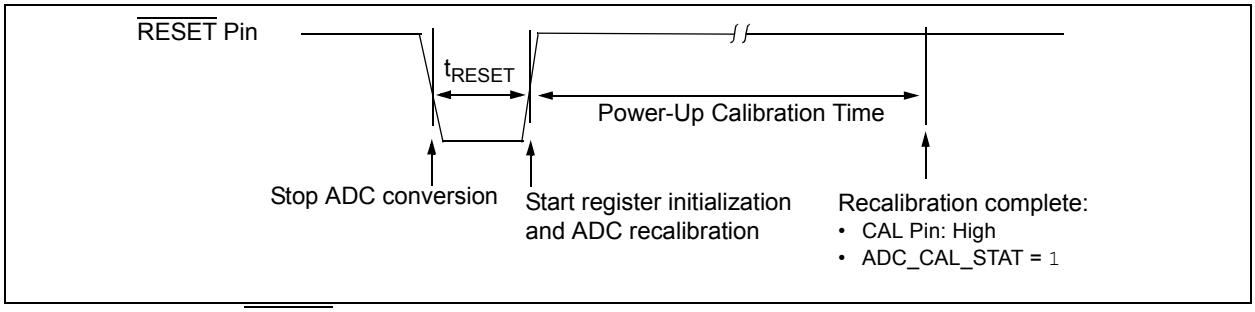

FIGURE 2-6: *$\overline{RESET}$ Pin Timing Diagram.*

TABLE 2-4: TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters		Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges(1)							
Operating Temperature Range		T_A	-40	—	+85	°C	
Thermal Package Resistances(2)							
121L Ball-TFBGA (8 mm x 8 mm)	Junction-to-Ambient Thermal Resistance	θ_{JA}	—	40.2	—	°C/W	
	Junction-to-Case Thermal Resistance	θ_{JC}	—	8.4	—	°C/W	
124L VTLA (9 mm x 9 mm)	Junction-to-Ambient Thermal Resistance	θ_{JA}	—	21	—	°C/W	
	Junction-to-Case (top) Thermal Resistance	θ_{JC}	—	8.7	—	°C/W	

Note 1: Maximum allowed power dissipation (P_{DMAX}) = (T_{JMAX} – T_A)/θ_{JA}.

2: This parameter value is achieved by package simulations.

NOTES:

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3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = 0011-1000. When NSR is enabled, 12-bit mode is used and the noise is calculated within the NSR bandwidth (25% of sampling frequency).

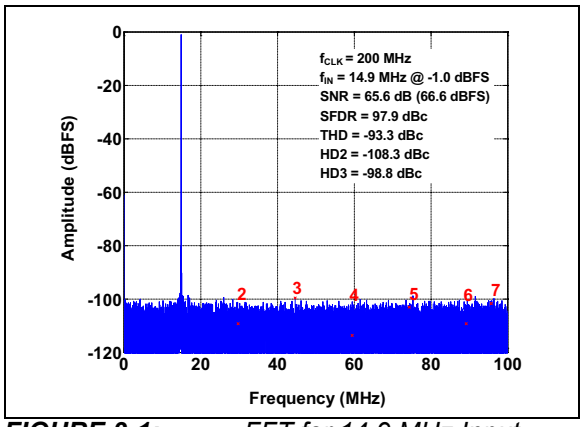

FIGURE 3-1: *FFT for 14.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -1 dBFS.*

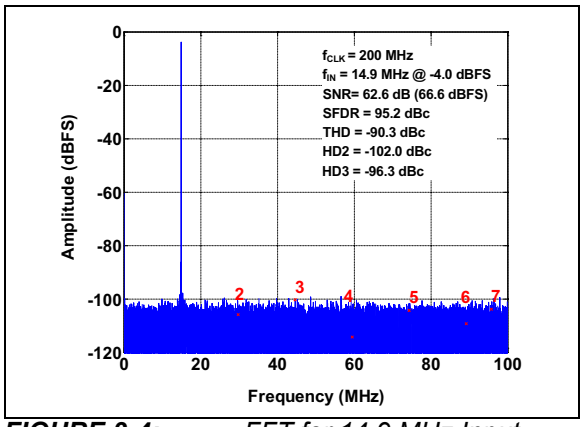

FIGURE 3-4: *FFT for 14.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -4 dBFS.*

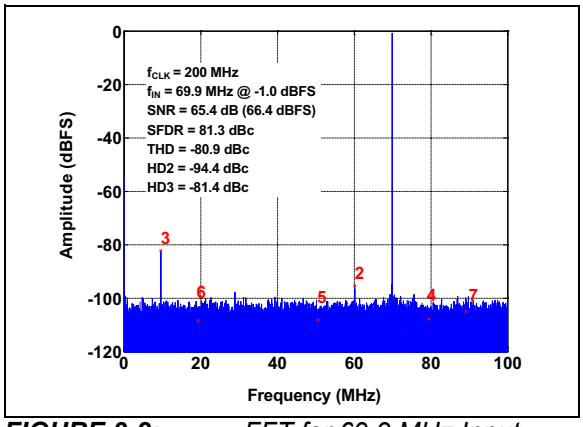

FIGURE 3-2: *FFT for 69.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -1 dBFS.*

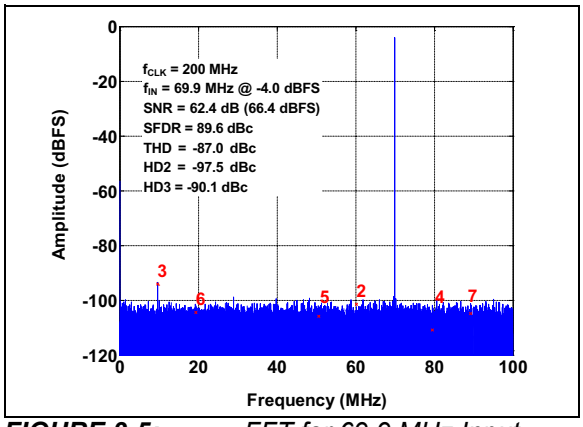

FIGURE 3-5: *FFT for 69.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -4 dBFS.*

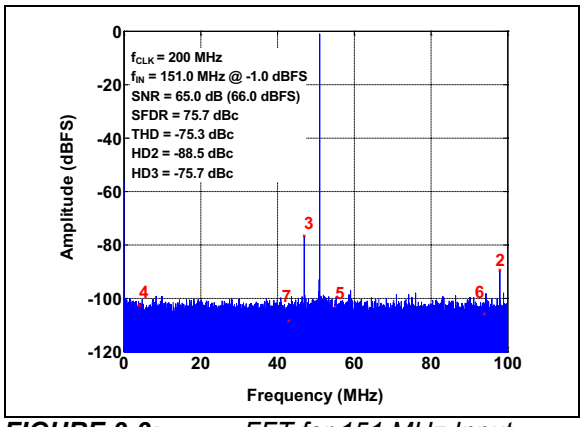

FIGURE 3-3: *FFT for 151 MHz Input Signal: f_S = 200 Msps, A_{IN} = -1 dBFS.*

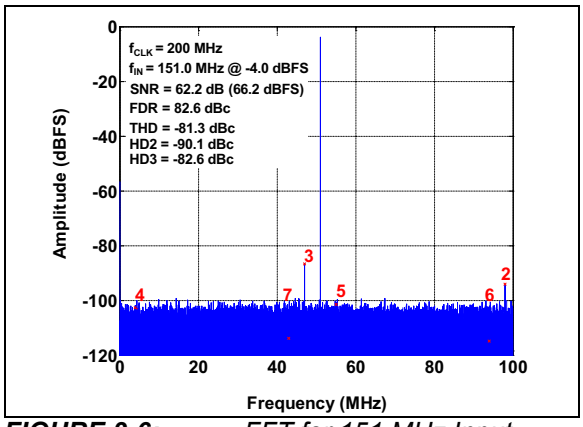

FIGURE 3-6: *FFT for 151 MHz Input Signal: f_S = 200 Msps, A_{IN} = -4 dBFS.*

Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = 0011-1000. When NSR is enabled, 12-bit mode is used and the noise is calculated within the NSR bandwidth (25% of sampling frequency).

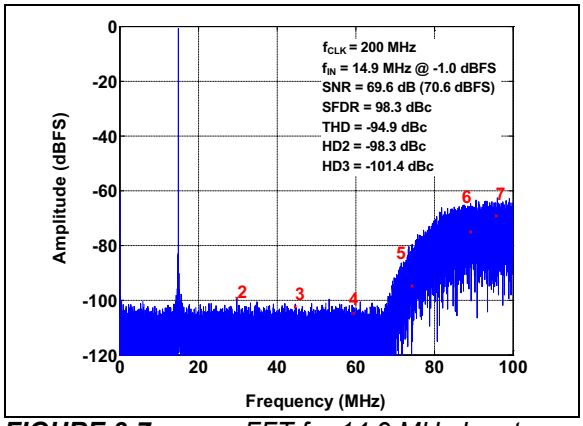

FIGURE 3-7: *FFT for 14.9 MHz Input Signal with NSR enabled: NSR = 63, f_S = 200 Msps, A_{IN} = -1 dBFS.*

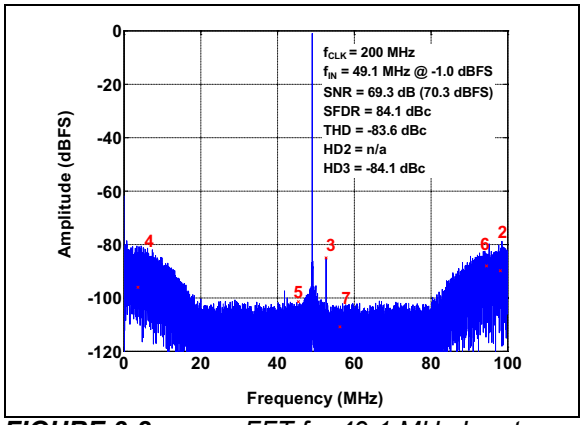

FIGURE 3-8: *FFT for 49.1 MHz Input Signal with NSR enabled: NSR = 69, f_S = 200 Msps, A_{IN} = -1 dBFS.*

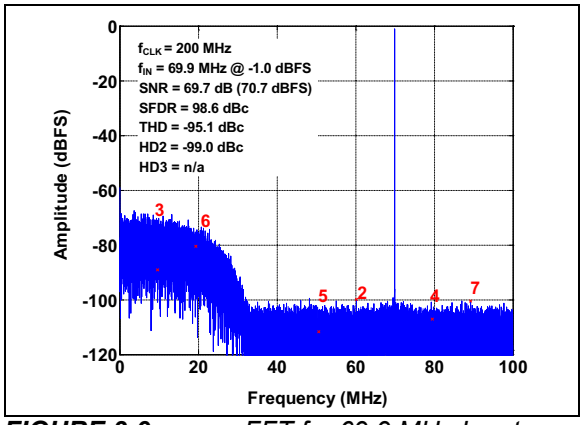

FIGURE 3-9: *FFT for 69.9 MHz Input Signal with NSR enabled: NSR = 75, f_S = 200 Msps, A_{IN} = -1 dBFS.*

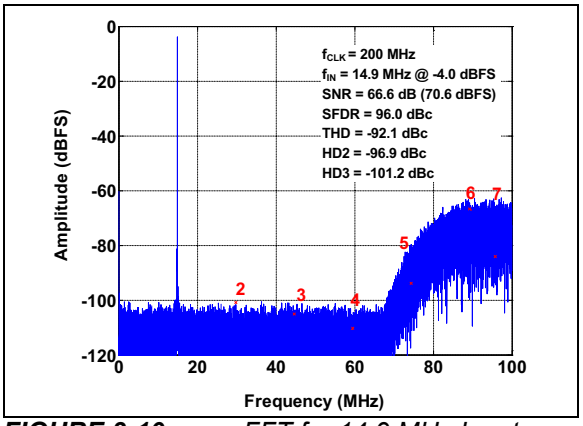

FIGURE 3-10: *FFT for 14.9 MHz Input Signal with NSR enabled: NSR = 63, f_S = 200 Msps, A_{IN} = -4 dBFS.*

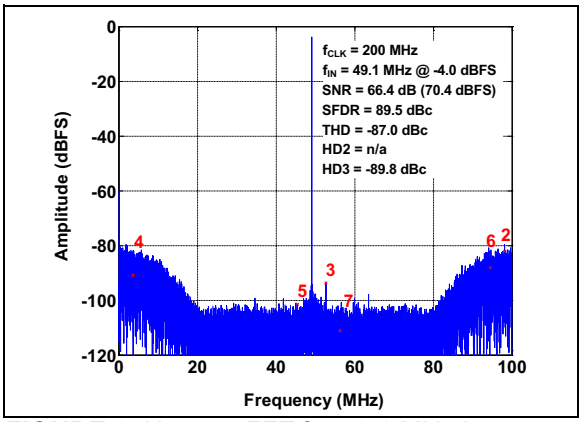

FIGURE 3-11: *FFT for 49.1 MHz Input Signal with NSR enabled: NSR = 69, f_S = 200 Msps, A_{IN} = -4 dBFS.*

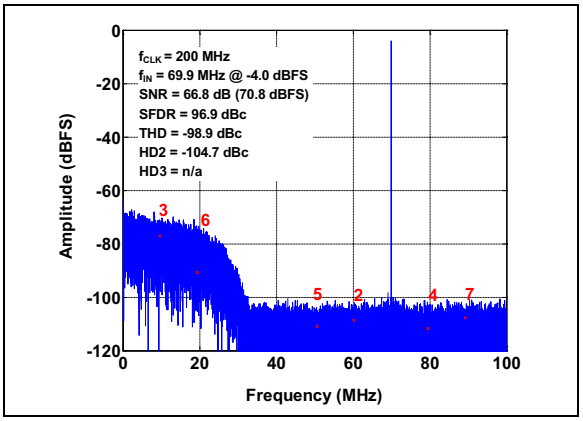

FIGURE 3-12: *FFT for 69.9 MHz Input Signal with NSR enabled: NSR = 75, f_S = 200 Msps, A_{IN} = -4 dBFS.*

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Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = 0011-1000. When NSR is enabled, 12-bit mode is used and the noise is calculated within the NSR bandwidth (25% of sampling frequency).

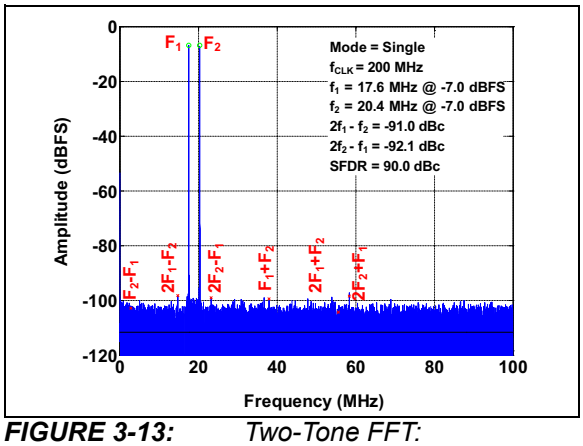

FIGURE 3-13: *Two-Tone FFT: f_{IN1} = 17.6 MHz and f_{IN2} = 20.4 MHz, A_{IN} = -7 dBFS per Tone, f_S = 200 Msps.*

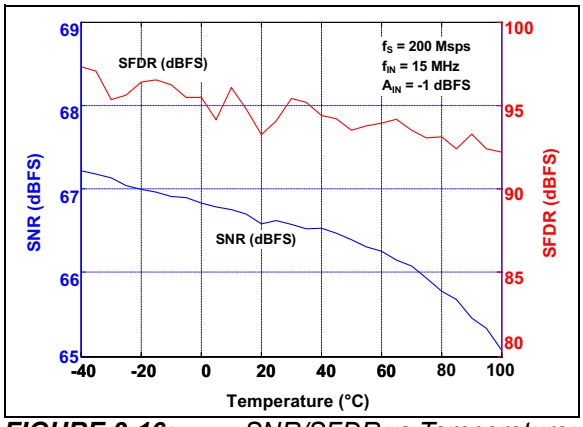

FIGURE 3-16: *SNR/SFDR vs. Temperature: f_S = 200 Msps, f_{IN} = 15 MHz.*

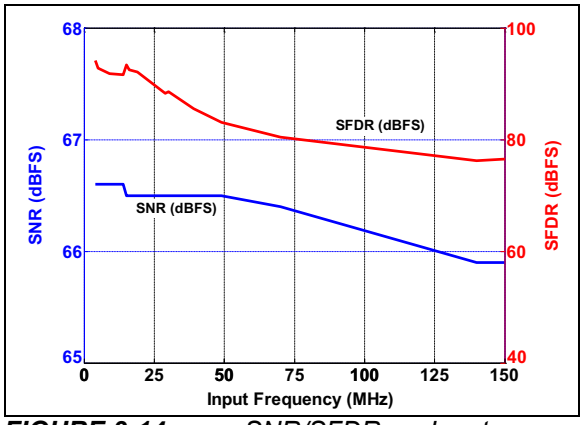

FIGURE 3-14: *SNR/SFDR vs. Input Frequency.*

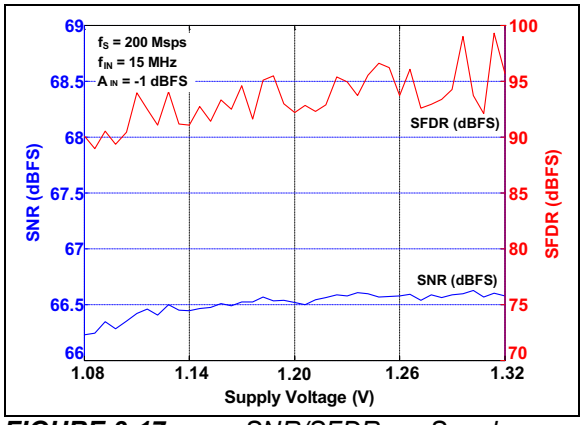

FIGURE 3-17: *SNR/SFDR vs. Supply Voltage: f_S = 200 Msps, f_{IN} = 15 MHz.*

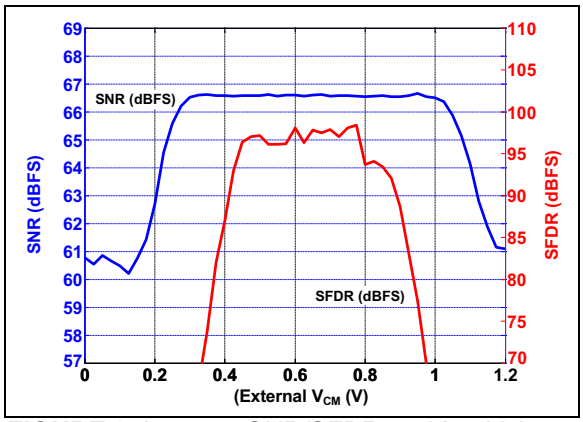

FIGURE 3-15: *SNR/SFDR vs. V_{CM} Voltage (Externally Applied): f_S = 200 Msps, f_{IN} = 15 MHz.*

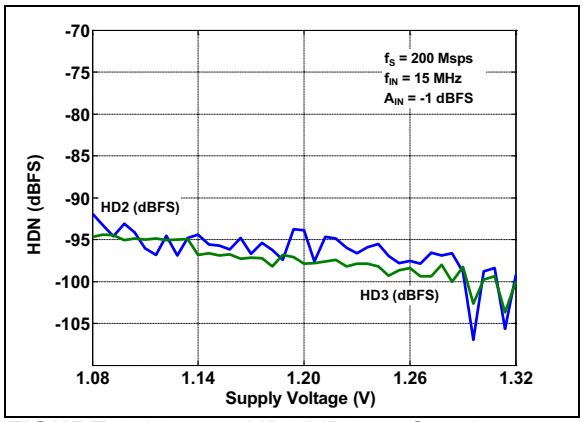

FIGURE 3-18: *HD2/HD3 vs. Supply Voltage: f_S = 200 Msps, f_{IN} = 15 MHz.*

Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = 0011-1000. When NSR is enabled, 12-bit mode is used and the noise is calculated within the NSR bandwidth (25% of sampling frequency).

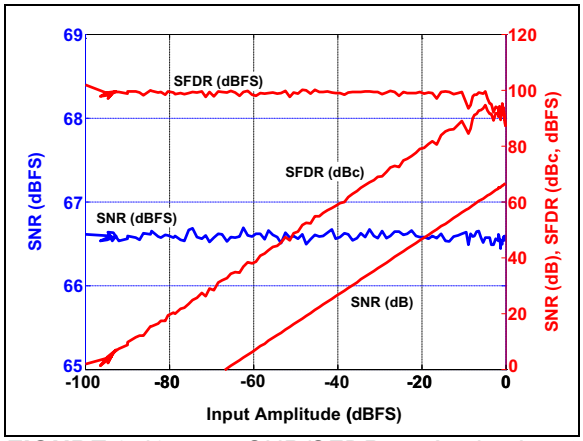

FIGURE 3-19: *SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 15 MHz.*

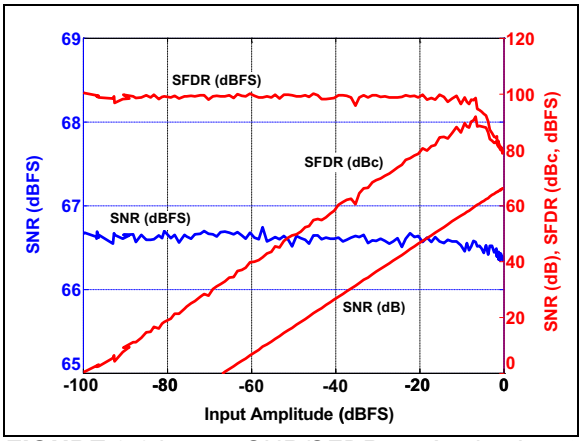

FIGURE 3-21: *SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 70 MHz.*

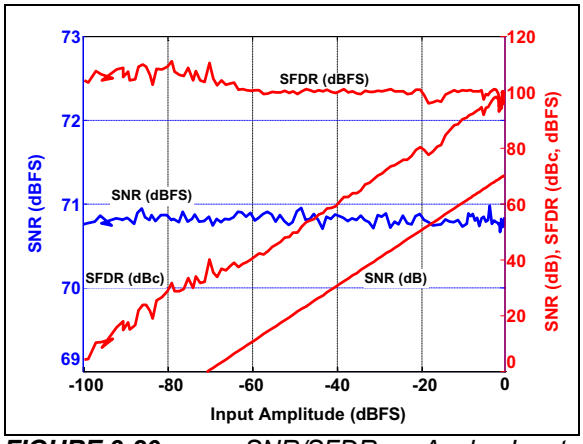

FIGURE 3-20: *SNR/SFDR vs. Analog Input Amplitude with NSR enabled: f_S = 200 Msps, f_{IN} = 15 MHz, A_{IN} ≤ -0.8 dBFS for NSR. NSR Filter Number = 63.*

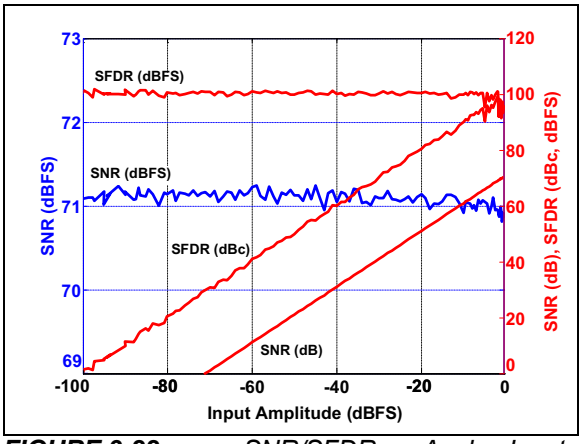

FIGURE 3-22: *SNR/SFDR vs. Analog Input Amplitude with NSR enabled: f_S = 200 Msps, f_{IN} = 70 MHz, A_{IN} ≤ -0.8 dBFS for NSR. NSR Filter Number = 75.*

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Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = 0011-1000. When NSR is enabled, 12-bit mode is used and the noise is calculated within the NSR bandwidth (25% of sampling frequency).

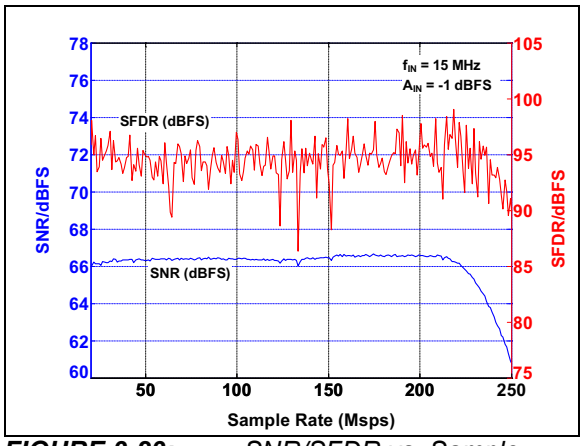

FIGURE 3-23: *SNR/SFDR vs. Sample Rate (Msps): f_{IN} = 15 MHz.*

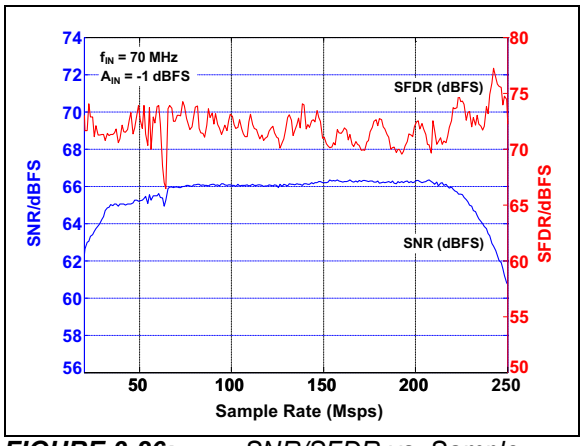

FIGURE 3-26: *SNR/SFDR vs. Sample Rate (Msps): f_{IN} = 70 MHz.*

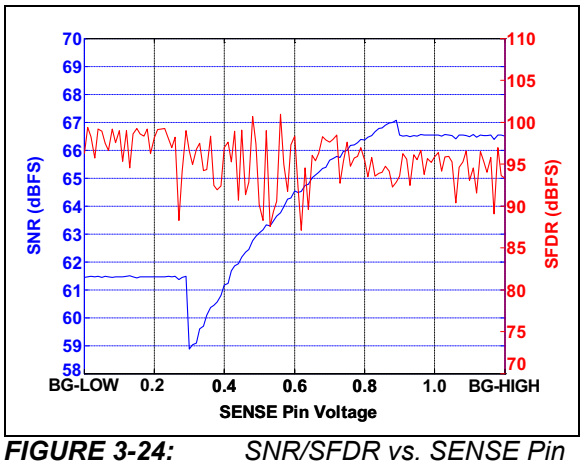

FIGURE 3-24: *SNR/SFDR vs. SENSE Pin Voltage: f_S = 200 Msps, f_{IN} = 15 MHz.*

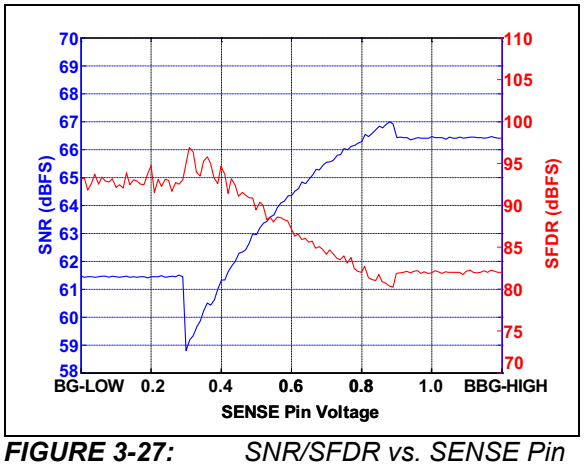

FIGURE 3-27: *SNR/SFDR vs. SENSE Pin Voltage: f_S = 200 Msps, f_{IN} = 70 MHz.*

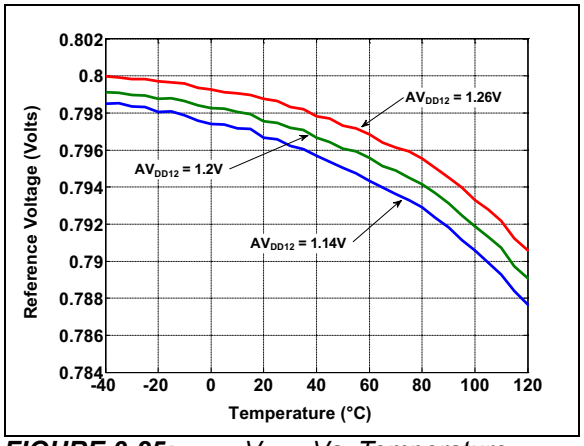

FIGURE 3-25: *V_{REF} Vs. Temperature.*

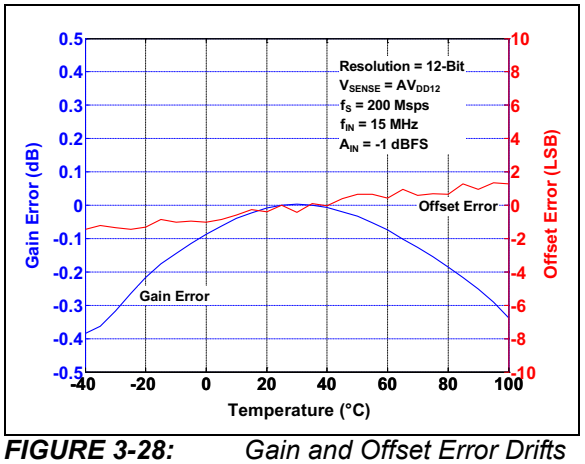

FIGURE 3-28: *Gain and Offset Error Drifts Vs. Temperature using Internal Reference, with Respect to 25 °C: f_S = 200 Msps.*

Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = 0011-1000. When NSR is enabled, 12-bit mode is used and the noise is calculated within the NSR bandwidth (25% of sampling frequency).

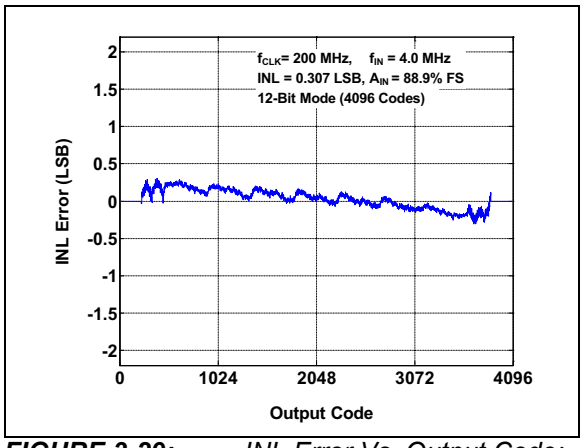

FIGURE 3-29: *INL Error Vs. Output Code: f_S = 200 Msps, f_{IN} = 4 MHz.*

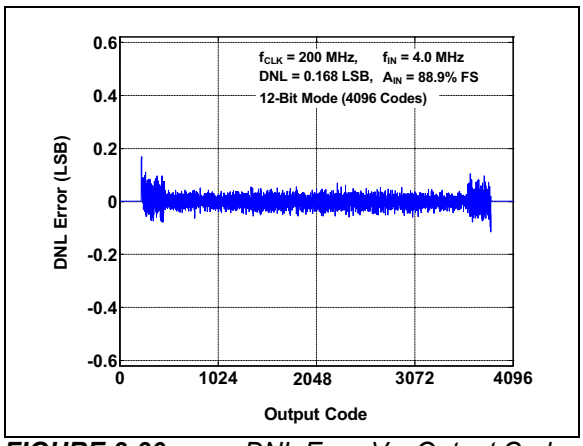

FIGURE 3-30: *DNL Error Vs. Output Code: f_S = 200 Msps, f_{IN} = 4 MHz.*

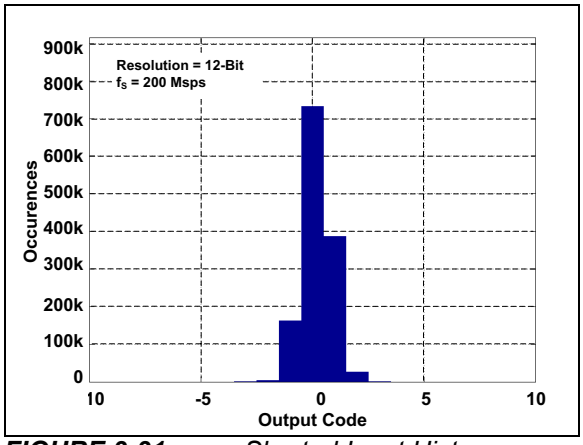

FIGURE 3-31: *Shorted Input Histogram: f_S = 200 Msps.*

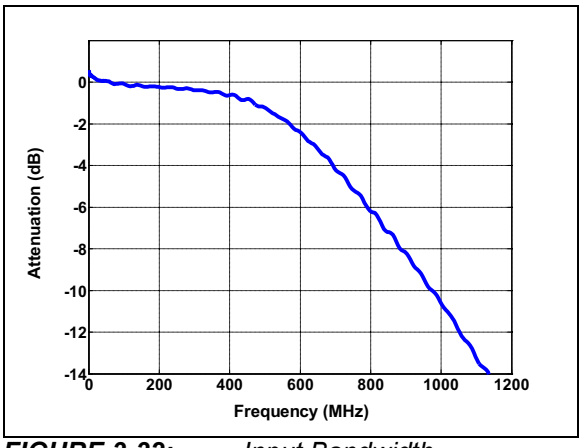

FIGURE 3-32: *Input Bandwidth.*

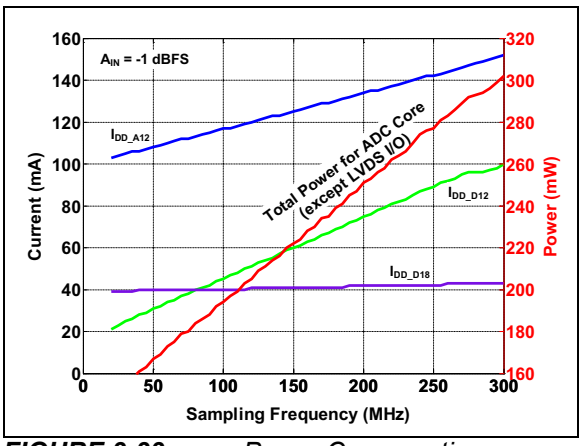

FIGURE 3-33: *Power Consumption vs. Sampling Frequency (LVDS Mode).*

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4.0 THEORY OF OPERATION

The MCP37210-200 and MCP37D10-200 devices are single-channel, low-power, 12-bit, 200 Msps Analog-to-Digital Converters (ADC) with built-in patented features that maximize performance. The features include Harmonic Distortion Correction (HDC), DAC Noise Cancellation (DNC), Dynamic Element Matching (DEM) and flash error calibration.

These devices include various built-in digital signal post-processing features. The MCP37210-200 includes FIR decimation filters and a noise-shaping requantizer. The MCP37D10-200 includes Digital Down-Conversion (DDC) in addition to the features offered by the MCP37210-200. Digital gain and offset correction features are also offered in both devices. These built-in advanced digital signal post-processing sub-blocks, which are individually enabled and controlled, can be used for various special applications such as I/Q demodulation, digital down-conversion, and imaging.

When the device is first powered-up, it performs internal calibrations by itself and is running with default settings. From this point, the user can configure the device registers using the SPI command.

The device samples the analog input on the rising edge of the clock. The digital output code is available after 23 clock cycles of data latency. Latency will increase if any of the digital signal post-processing (DSPP) options are enabled.

The output data can be coded in two's complement or offset binary format and can be randomized using the user option. The output data is available through the CMOS or LVDS (Low-Voltage Differential Signaling) interface.

4.1 ADC Core Architecture

Figure 4-1 shows the simplified block diagram of the ADC core. The ADC core consists of six stages. All stages consist of a multi-level flash ADC and DAC. Except the last stage, all have a residue amplifier with a gain of 4. Dither is added in each of the first two stages. The digital outputs from all six stages are combined in a digital error correction logic block and digitally processed for the final 12-bit output.

The first two stages include patented digital calibration features:

- Harmonic Distortion Correction (HDC) algorithm that digitally measures and cancels ADC errors arising from distortions introduced by the residue amplifiers
- DAC Noise Cancellation (DNC) algorithm that corrects DAC's nonlinearity errors
- Dynamic Element Matching (DEM) which randomizes DAC errors, thereby converting harmonic distortion to white noise

These digital correction algorithms are first applied during the Power-on Reset sequence and then operate in the background during normal operation of the pipelined ADC. These algorithms automatically track and correct any environmental changes in the ADC. More details of the system correction algorithms are shown in **Section 4.10 "System Calibration"**.

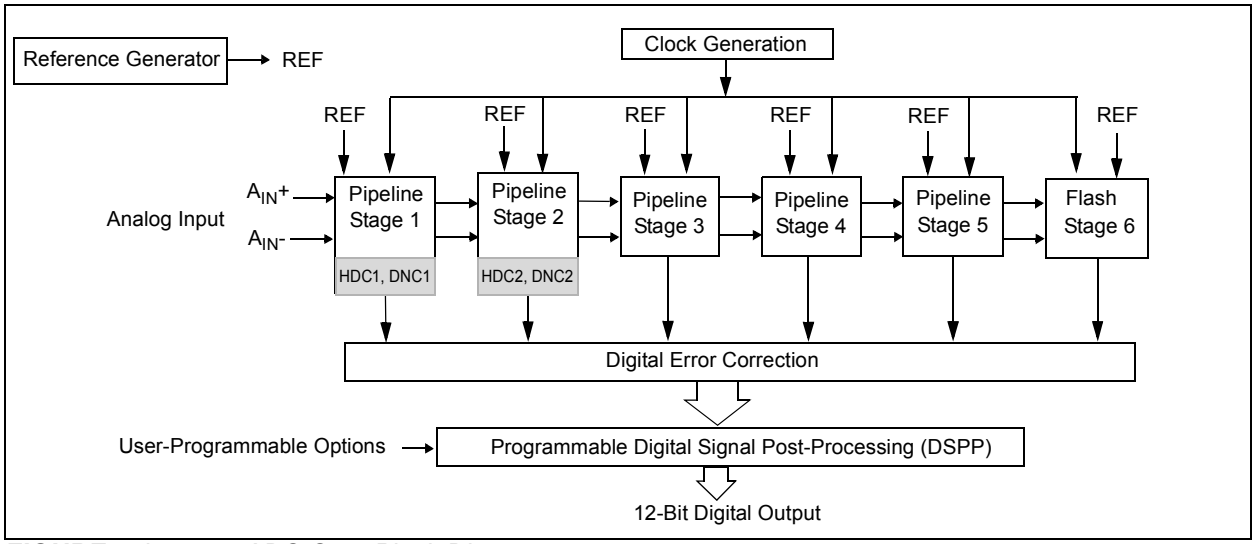

FIGURE 4-1: *ADC Core Block Diagram.*

4.2 Supply Voltage (DV_{DD}, AV_{DD}, GND)

The device operates from two sets of supplies and a common ground:

- Digital Supplies (DV_{DD}) for the digital section: 1.8V and 1.2V
- Analog Supplies (AV_{DD}) for the analog section: 1.8V and 1.2V
- Ground (GND): Common ground for both digital and analog sections.

The supply pins require an appropriate bypass capacitor (ceramic) to attenuate high-frequency noise present in most application environments. The ground pins provide the current return path. These ground pins must connect to the ground plane of the PCB through a low-impedance connection. A ferrite bead can be used to separate analog and digital supply lines if a common power supply is used for both analog and digital sections.

The voltage regulators for each supply need to have sufficient output current capabilities to support a stable ADC operation.

4.3 Analog Input Circuit

The analog inputs (A_{IN}) of all MCP37XXX devices are a differential CMOS switched capacitor sample-and-hold circuit. Figure 4-2 shows the equivalent input structure of the device.

The input impedance of the device is mostly governed by the input sampling capacitor (C_S = 1.6 pF) and input sampling frequency (f_S). The performance of the device can be affected by the input signal conditioning network (see Figure 4-3). The analog input signal source must have sufficiently low output impedance to charge the sampling capacitors (C_S = 1.6 pF) within one clock cycle. A small external resistor (e.g. 5Ω) in series with each input is recommended as it helps reduce transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low-pass filter with the capacitor and their values must be determined by application requirements and input frequency.

The V_{CM} pin provides a common-mode voltage reference (0.55V), which can be used for a center-tap voltage of an RF transformer or balun. If the V_{CM} pin voltage is not used, the user may provide a common-mode voltage (0.55V) from another supply.

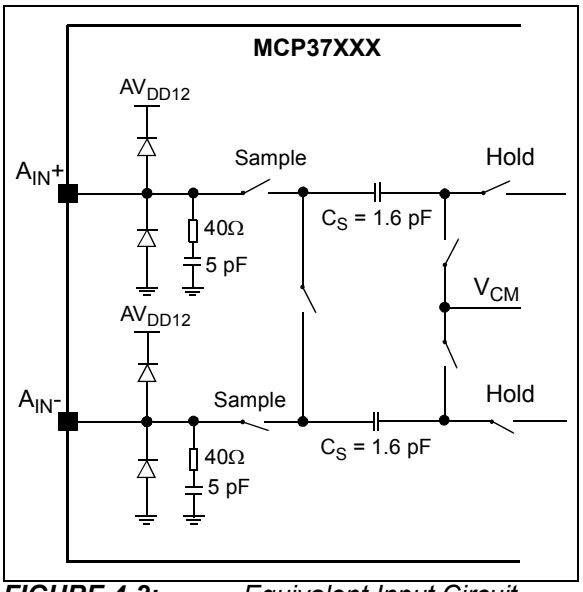

FIGURE 4-2: *Equivalent Input Circuit.*

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4.3.1 ANALOG INPUT DRIVING CIRCUIT

4.3.1.1 Differential Input Configuration

The device achieves optimum performance when the input is driven differentially, where common-mode noise immunity and even-order harmonic rejection are significantly improved. If the input is single-ended, it must be converted to a differential signal in order to properly drive the ADC input. The differential conversion and common-mode application can be accomplished by using an RF transformer or balun with a center-tap. Additionally, one or more anti-aliasing filters may be added for optimal noise performance and should be tuned such that the corner frequency is appropriate for the system.

Figure 4-3 shows an example of the differential input circuit with transformer. Note that the input driving circuits are terminated by 50Ω near the ADC side through a pair of 25Ω resistors from each input to the common-mode (V_{CM}) from the device. The RF transformer must be carefully selected to avoid artificially high harmonic distortion. The transformer can be damaged if a strong RF input is applied or an RF input is applied while the MCP37XXX is powered off. The transformer has to be selected to handle sufficient RF input power. Figure 4-4 shows an input configuration example when a differential output amplifier is used.

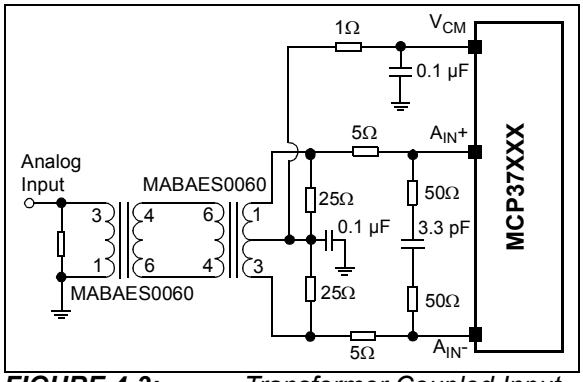


FIGURE 4-3: *Transformer Coupled Input Configuration.*

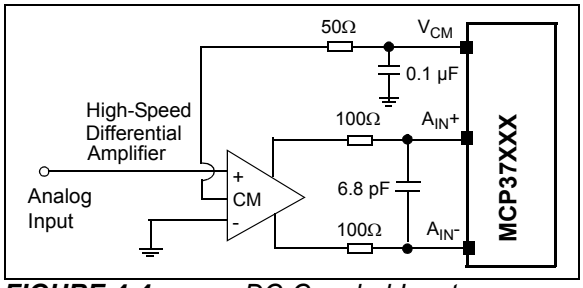


FIGURE 4-4: *DC-Coupled Input Configuration with Preamplifier: the external signal conditioning circuit and associated component values are for reference only. Typically, the amplifier manufacturer provides reference circuits and component values.*

4.3.1.2 Single-Ended Input Configuration

Figure 4-5 shows an example of a single-ended input configuration. SNR and SFDR performance degrades significantly when the device is operated in a single-ended configuration. The unused negative side of the input should be AC-coupled to ground using a capacitor.

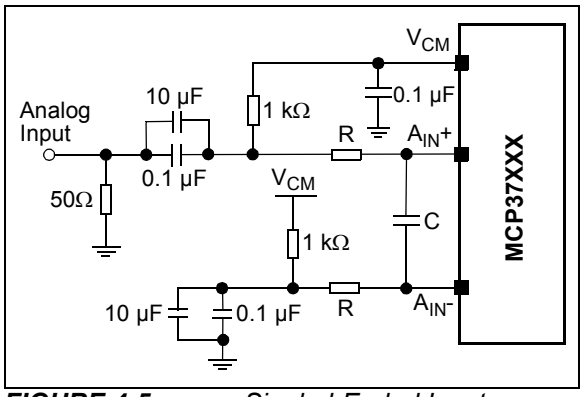
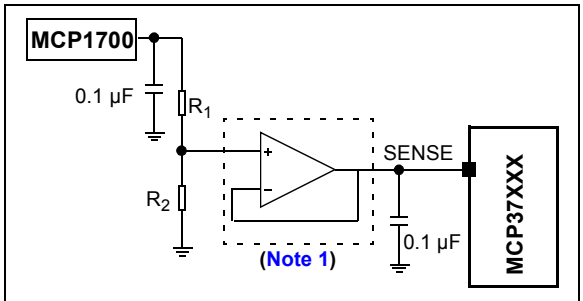


FIGURE 4-5: *Singled-Ended Input Configuration.*

4.3.2 SENSE VOLTAGE AND INPUT FULL-SCALE RANGE

The device has a bandgap-based differential internal reference voltage. The SENSE pin voltage is used to select the reference voltage source and configures the input full-scale range. A comparator detects the SENSE pin voltage and configures the full-scale input range into one of the three possible modes which are summarized in Table 4-1. Figure 4-6 shows an example of how the SENSE pin should be driven.

The SENSE pin can sink or source currents as high as 360 µA across all operational conditions. Therefore, it may require a driver circuit, unless the SENSE reference source provides sufficient output current.



Note 1: This voltage buffer can be removed if SENSE reference is coming from a stable source (such as MCP1700) which can provide a sufficient output current to the SENSE pin.

FIGURE 4-6: *SENSE Pin Voltage Setup.*

TABLE 4-1: SENSE PIN VOLTAGE AND INPUT FULL-SCALE RANGE

SENSE Pin Voltage (V_{SENSE})	Selected Reference Voltage (V_{REF})	Full-Scale Input Voltage Range (A_{FS})	LSb Size ($A_{FS}/2^{12}$)	Condition
Tied to GND	0.4V	0.9 V_{P-P}	219.72 µV	Low-Reference Mode(2)
0.4V – 0.8 V	0.4V – 0.8V	0.9 V_{P-P} to 1.8 V_{P-P}(1)	Adjustable	Sense Mode(3)
Tied to AV_{DD12}	0.8V	1.8 V_{P-P}	439.45 µV	High-Reference Mode(2)

Note 1: A_{FS} = 2.25 V_{P-P} x (V_{SENSE}) = 0.9 V_{P-P} to 1.8 V_{P-P}
2: Based on internal bandgap voltage
3: Based on V_{SENSE}

4.3.2.1 SENSE Selection Vs. SNR/SFDR Performance

The SENSE pin is used to configure the full-scale input range of the ADC. Depending on the application conditions, the SNR, SFDR and dynamic range performance are affected by the SENSE pin configuration. Table 4-2 summarizes these settings.

- **High-Reference Mode**

This mode is enabled by setting the SENSE pin to AV_{DD12} (1.2V). This mode provides the highest input full-scale range (1.8 V_{P-P}) and the highest SNR performance. Figures 3-19 and 3-21 show SNR/SFDR versus input amplitude in High-Reference mode.

- **Low-Reference Mode**

This mode is enabled by setting the SENSE pin to ground. This mode is suitable for applications which have a smaller input full-scale range. This mode provides improved SFDR characteristics, but SNR is reduced by -6 dB compared to the High-Reference mode.

- **SENSE Mode**

This mode is enabled by driving the SENSE pin with an external voltage source between 0.4V and 0.8V. This mode allows the user to adjust the input full-scale range such that SNR and dynamic range are optimized in a given application system environment.

- **NSR Mode**

The use of Noise-Shaping Requantizer (NSR), further described in **Section 4.6.1 "Noise-Shaping Requantizer (NSR)"**, is best suited for applications which require an improved SNR and a wide dynamic range within a relatively narrow bandwidth.

When the NSR is enabled, the noise level in a selected portion of the frequency band is reduced, while the noise level outside of this band is higher. This is an optimum selection for applications where the full Nyquist bandwidth of the ADC is not needed and where the digital signal post-processing of the ADC data is capable of removing the out-of-band noise added by the NSR.

Figures 3-20 and 3-22 show the SNR/SFDR versus input amplitude when NSR is enabled.

TABLE 4-2: SENSE VS. SNR/SFDR PERFORMANCE

SENSE	Descriptions
High-Reference Mode (SENSE pin = AV_{DD12})	High-input full-scale range (1.8 V_{P-P}) and optimized SNR
Low-Reference Mode (SENSE pin = ground)	Low-input full-scale range (0.9 V_{P-P}) and reduced SNR, but optimized SFDR
Sense Mode (SENSE pin = 0.4V to 0.8V)	Adjustable-input full-scale range (0.9 V_{P-P} - 1.8 V_{P-P}). Dynamic trade-off between High-Reference and Low-Reference modes can be used.
Noise-Shaping Requantizer (NSR)	Optimized SNR, but reduced usable bandwidth

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4.3.3 DECOUPLING CIRCUITS FOR INTERNAL VOLTAGE REFERENCE AND BANDGAP OUTPUT

4.3.3.1 Decoupling Circuits for REF Pins

The internal reference is available at REF pins. This internal reference requires external capacitors for stable operation.

VTLA-124 Package Device: Figure 4-7 shows the recommended circuit for the REF pins. A 2.2 µF ceramic capacitor with two additional optional capacitors (22 nF and 220 nF) is recommended between the positive and negative reference pins. The negative reference pin (REF-) is then grounded through a 220 nF capacitor. The capacitors should be placed as close to the ADC as possible with short and thick traces. Vias on the PCB are not recommended for this reference pin circuit.

TFBGA-121 Package Device: The decoupling capacitor is embedded in the package. Therefore, no external circuit is required on the PCB.

4.3.3.2 Decoupling Circuit for V_{BG} Pin

The bandgap circuit is a part of the reference circuit and the output is available at the V_{BG} pin.

VTLA-124 Package Device: V_{BG} pin needs an external decoupling capacitor (2.2 µF) as shown in Figure 4-7.

TFBGA-121 Package Device: The decoupling capacitor is embedded in the package. Therefore, no external circuit is required on the PCB.

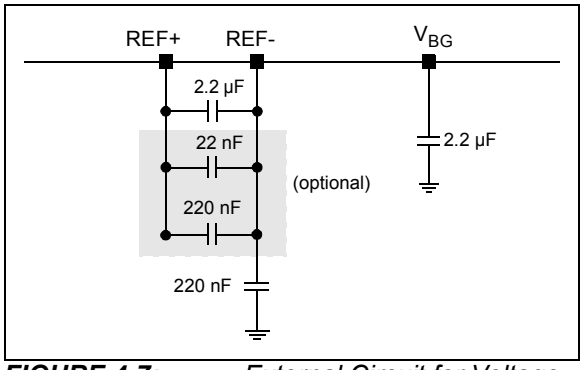

FIGURE 4-7: *External Circuit for Voltage Reference and V_{BG} pins for the VTLA-124 Package. Note that this external circuit is not required for the TFBGA-121 package.*

Note:	The internal reference output (REF+/REF-) and bandgap voltage output (V_{BG}) should not be driven.

4.4 External Clock Input

For optimum performance, the MCP37XXX requires a low-jitter differential clock input at the CLK+ and CLK− pins. Figure 4-8 shows the equivalent clock input circuit.

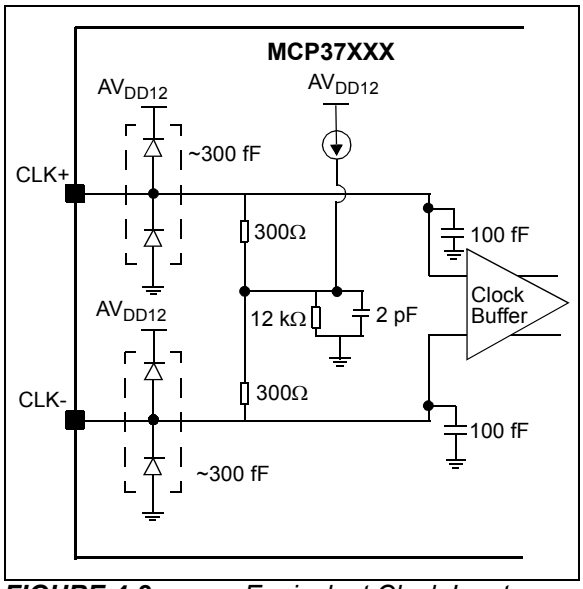

FIGURE 4-8: *Equivalent Clock Input Circuit.*

The clock input amplitude range is between 300 mV_{P-P} and 800 mV_{P-P}. When a single-ended clock source is used, an RF transformer or balun can be used to convert the clock into a differential signal for the best ADC performance. Figure 4-9 shows an example clock input circuit. The common-mode voltage is internally generated and a center-tap is not required. The back-to-back Schottky diodes across the transformer's secondary current limit the clock amplitude to approximately 0.8 V_{P-P} differential. This limiter helps prevent large voltage swings of the input clock while preserving the high slew rate that is critical for low jitter.

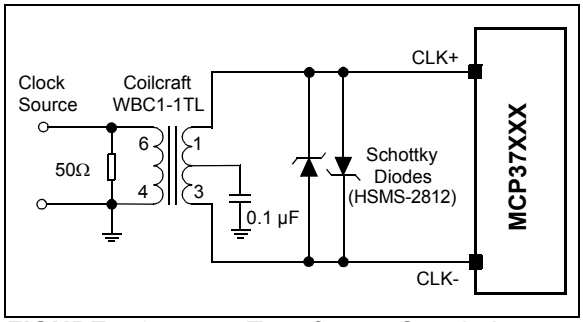

FIGURE 4-9: *Transformer-Coupled Differential Clock Input Configuration.*

4.4.1 CLOCK JITTER AND SNR PERFORMANCE

In a high-speed pipelined ADC, the SNR performance is directly limited by thermal noise and clock jitter. Thermal noise is independent of input clock and dominant term at low input frequency. On the other hand, the clock jitter becomes a dominant term as input frequency increases. Equation 4-1 shows the SNR jitter component, which is expressed in terms of the input frequency (f_{IN}) and the total amount of clock jitter (T_{Jitter}), where T_{Jitter} is a sum of the following two components:

- Input clock jitter (phase noise)
- Internal aperture jitter (due to noise of the clock input buffer).

EQUATION 4-1: SNR VS.CLOCK JITTER

$$SNR_{Jitter}(dBc) = -20 \times log_{10}(2\pi \times f_{IN} \times T_{Jitter})$$

where the total jitter term (T_{jitter}) is given by:

$$T_{Jitter} = \sqrt{(t_{Jitter,\ Clock\ Input})^2 + (t_{Aperture,\ ADC})^2}$$

The clock jitter can be minimized by using a high-quality clock source and jitter cleaners, as well as a band-pass filter at the external clock input, while a faster clock slew rate improves the ADC aperture jitter.

With a fixed amount of clock jitter, the SNR degrades as the input frequency increases. This is illustrated in Figure 4-10. If the input frequency increases from 10 MHz to 20 MHz, the maximum achievable SNR degrades about 6 dB. For every decade (e.g. 10 MHz to 100 MHz), the maximum achievable SNR due to clock jitter is reduced by 20 dB.

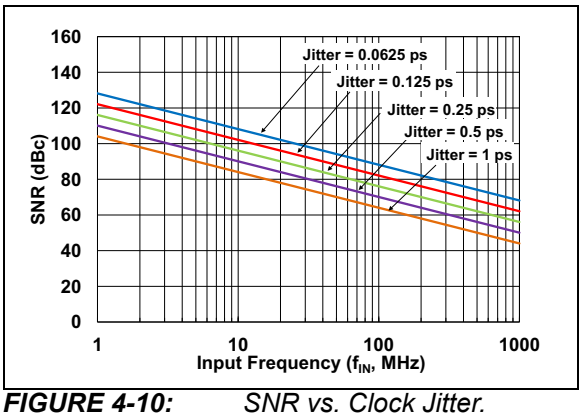

FIGURE 4-10: *SNR vs. Clock Jitter.*

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4.5 ADC Clock Selection

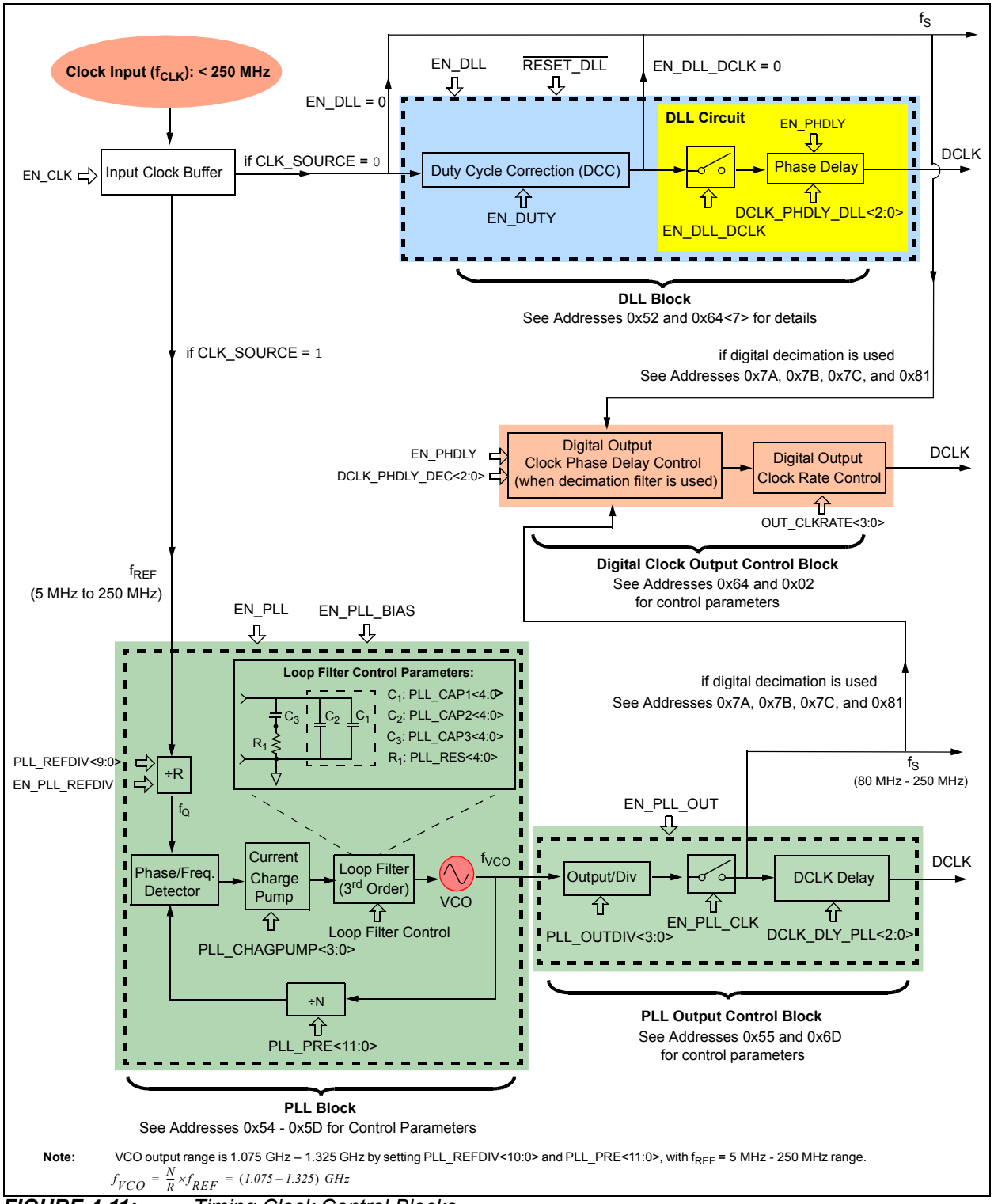
This section describes the ADC clock selection and how to use the built-in Delay-Locked Loop (DLL) and Phase-Locked Loop (PLL) blocks.

When the device is first powered-up, the external clock input (CLK+/-) is directly used for the ADC timing as default. After this point, the user can enable the DLL or PLL circuit by setting the register bits. Figure 4-11 shows the clock control blocks. Table 4-3 shows an example of how to select the ADC clock depending on the operating conditions.

TABLE 4-3: ADC CLOCK SELECTION (EXAMPLE)

Operating Conditions	Control Bit Settings[1]	Features	
		Input Clock Duty Cycle Correction	DCLK Output Phase Delay Control
CLK_SOURE = 0 (Default)[2]			
• DLL output is not used • Decimation is not used **(Default)**[3]	EN_DLL = 0 EN_DLL_DCLK = 0 EN_PHDLY = 0	Not Available	Not Available
	EN_DLL = 1 EN_DLL_DCLK = 0 EN_PHDLY = 0	Available	
• DLL output is used • Decimation is not used	EN_DLL = 1 EN_DLL_DCLK = 1 EN_PHDLY = 1	Available	Available
• DLL output is not used • Decimation is used[4]	EN_DLL = 0 EN_DLL_DCLK = X EN_PHDLY = 1	Not Available	
	EN_DLL = 1 EN_DLL_DCLK = 0 EN_PHDLY = 1	Available	
CLK_SOURCE = 1[5]			
• Decimation is not used	EN_DLL = X EN_DLL_DCLK = X EN_PHDLY = 0	Not Available	Available
• Decimation is used[4]	EN_DLL = X EN_DLL_DCLK = X EN_PHDLY = 1		

Note 1: See Addresses 0x52, 0x53, and 0x64 for bit settings.
2: The sampling frequency (f_S) of the ADC core comes directly from the input clock buffer
3: Output data is synchronized with the output data clock (DCLK), which comes directly from the input clock buffer.
4: While using decimation, output clock rate and phase delay are controlled by the digital clock output control block
5: The sampling frequency (f_S) is generated by the PLL circuit. The external clock input is used as the reference input clock for the PLL block.



Note: VCO output range is 1.075 GHz – 1.325 GHz by setting PLL_REFDIV<10:0> and PLL_PRE<11:0>, with f_{REF} = 5 MHz - 250 MHz range.

$$f_{VCO} = \frac{N}{R} \times f_{REF} = (1.075 - 1.325)\ GHz$$

FIGURE 4-11: *Timing Clock Control Blocks.*

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4.5.1 USING DLL MODE

Using the DLL block is the best option when output clock phase control is needed while the clock multiplication and the digital decimation are not required. When the DLL block is enabled, the user can control the input clock Duty Cycle Correction (DCC) and the output clock phase delay.

See the DLL block in Figure 4-11 for details. Table 4-4 summarizes the DLL control register bits. See also Table 4-18 for the output clock phase control.

TABLE 4-4: DLL CONTROL REGISTER BITS

Control Parameter	Register	Descriptions
CLK_SOURCE	0x53	CLK_SOURCE = 0: External clock input becomes input of the DLL block
EN_DLL	0x52	EN_DLL = 1: Enable DLL block
EN_DUTY	0x52	Input clock duty cycle correction control bit(1)
EN_DLL_DCLK	0x52	DLL output clock enable bit
EN_PHDLY	0x64	Enable digital output clock phase delay control
DCLK_PHDLY_DLL<2:0>	0x52	Phase delay control bits of digital output clock (DCLK) when DLL is used(2)
$\overline{\text{RESET_DLL}}$	0x52	Reset control bit for the DLL block

Note 1: Duty cycle correction is not recommended when a high-quality external clock is used.

2: If decimation is used, the output clock phase delay is controlled using DCLK_PHDLY_DEC<2:0> in Address 0x64.

4.5.1.1 Input Clock Duty Cycle Correction

The ADC performance is sensitive to the clock duty cycle. The ADC achieves optimum performance with 50% duty cycle, and all performance characteristics are ensured when the duty cycle is 50% with ±1% tolerance.

When CLK_SOURCE = 0, the external clock is used as the sampling frequency (f_S) of the ADC core. When the external input clock is not high quality (for example, duty cycle is not 50%), the user can enable the internal clock duty cycle correction circuit by setting the EN_DUTY bit in Address 0x52 (Register 5-7). When duty cycle correction is enabled (EN_DUTY = 1), only the falling edge of the clock signal is modified (rising edge is unaffected).

The duty cycle correction process adds additional jitter noise to the clock signal. Therefore, using this option is only recommended when an asymmetrical input clock source causes significant performance degradation or when the input clock source is not stable.

Note:	The clock duty cycle correction is only applicable when DLL black is enabled (EN_DLL=1). It is not applicable for the PLL output.

4.5.1.2 DLL Block Reset Event

The DLL must be reset if the clock is removed or the clock frequency is changed. The DLL reset is controlled by using the $\overline{\text{RESET_DLL}}$ bit in Address 0x52 (Register 5-7). The DLL has an automatic reset with the following events:

- During power-up: Stay in reset until the $\overline{\text{RESET_DLL}}$ bit is cleared.
- When the $\overline{\text{SOFT_RESET}}$ command is issued while the DLL is enabled: the $\overline{\text{RESET_DLL}}$ bit is automatically cleared after reset.

4.5.2 USING PLL MODE

The PLL block is mainly used when clock multiplication is needed. When CLK_SOURCE = 1, the sampling frequency (f_S) of the ADC core is coming from the internal PLL block.

The recommended PLL output clock range is from 80 MHz to 250 MHz. The external clock input is used as the PLL reference frequency. The range of the clock input frequency is from 5 MHz to 250 MHz.

Note:	The PLL mode is only supported for sampling frequencies between 80 MHz and 250 MHz.

4.5.2.1 PLL Output Frequency and Output Control Parameters

The internal PLL can provide a stable timing output ranging from 80 MHz to 250 MHz. Figure 4-11 shows the PLL block using a charge-pump-based integer N PLL and the PLL output control block. The PLL block includes various user control parameters for the desired output frequency. Table 4-5 summarizes the PLL control register bits and Table 4-6 shows an example of register bit settings for the PLL charge pump and loop filter.

The PLL block consists of:

- Reference Frequency Divider (R)
- Prescaler - which is a feedback divider (N)
- Phase/Frequency Detector (PFD)
- Current Charge Pump
- Loop Filter – a 3rd order RC low-pass filter
- Voltage-Controlled Oscillator (VCO)

The external clock at the CLK+ and CLK- pins is the input frequency to the PLL. The range of input frequency (f_{REF}) is from 5 MHz to 250 MHz. This input frequency is divided by the reference frequency divider (R) which is controlled by the 10-bit-wide PLL_REFDIV<9:0> setting. In the feedback loop, the VCO frequency is divided by the prescaler (N) using PLL_PRE<11:0>.

The ADC core sampling frequency (f_S), ranging from 80 MHz to 250 MHz, is obtained after the output frequency divider (PLL_OUTDIV<3:0>). For stable operation, the user needs to configure the PLL with the following limits:

- Input clock frequency (f_{REF}) = 5 MHz to 250 MHz
- Charge pump input frequency (after PLL reference divider) = 4 MHz to 50 MHz
- VCO output frequency = 1.075 to 1.325 GHz
- PLL output frequency after output divider = 80 MHz to 250 MHz

The charge pump is controlled by the PFD, and forces sink (DOWN) or source (UP) current pulses onto the loop filter. The charge pump bias current is controlled by the PLL_CHAGPUMP<3:0> bits: approximately 25 µA per step. The loop filter consists of a 3rd order passive RC filter. Table 4-6 shows the recommended settings of the charge pump and loop filter parameters, depending on the charge pump input frequency range (output of the reference frequency divider).

When the PLL is locked, it tracks the input frequency (f_{REF}) with the ratio of dividers (N/R). The PLL operating status is monitored by the PLL status indication bits: <PLL_VCOL_STAT> and <PLL_VCOH_STAT> in Address 0xD1 (Register 5-69).

Equation 4-2 shows the VCO output frequency (f_{VCO}) as a function of the two dividers and reference frequency:

EQUATION 4-2: VCO OUTPUT FREQUENCY

$$f_{VCO} = \left(\frac{N}{R}\right) f_{REF} = 1.075\ (GHz)\ to\ 1.325\ (GHz)$$

Where:

N = 1 to 4095 controlled by PLL_PRE<11:0>

R = 1 to 1023 controlled by PLL_REFDIV<9:0>

See Addresses 0x54 to 0x57 (Register 5-9 to 5-12) for these bit settings.

The tuning range of the VCO is 1.075 GHz to 1.325 GHz. N and R values must be chosen such that the VCO is within this range. In general, lower values of the VCO frequency (f_{VCO}) and higher values of the charge pump frequency (f_Q) should be chosen to optimize the clock jitter. Once the VCO output frequency is determined to be within this range, the user needs to set the final ADC sampling frequency (f_S) with the PLL output divider using PLL_OUTDIV<3:0>. Equation 4-3 shows how to obtain the ADC core sampling frequency:

EQUATION 4-3: SAMPLING FREQUENCY

$$f_S = \left(\frac{f_{VCO}}{PLL_OUTDIV}\right) = 80\ MHz\ to\ 250\ MHz$$

Table 4-7 shows an example of generating f_S = 200 MHz output using the PLL control parameters.

4.5.2.2 PLL Calibration

The PLL should be recalibrated following a change in clock input frequency or in the PLL Configuration register bit settings (Addresses 0x54 - 0x57; Registers 5-9 – 5-12).

The PLL can be calibrated by toggling the PLL_CAL_TRIG bit in Address 0x6B (Register 5-27) or by sending a SOFT_RESET command (See Address 0x00, Register 5-1). The PLL calibration status is observed by the PLL_CAL_STAT bit in Address 0xD1 (Register 5-69).

4.5.2.3 Monitoring of PLL Drifts

The PLL drifts can be monitored using the status monitoring bits in Address 0xD1 (Register 5-69). Under normal operation, the PLL maintains lock across all temperature ranges.

It is not necessary to actively monitor the PLL unless extreme variations in the supply voltage are expected or if the input reference clock frequency has been changed.

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TABLE 4-5: PLL CONTROL REGISTER BITS

Control Parameter	Register	Descriptions
PLL Calibration and Status Indication Bits		
PLL Global Control Bits		
EN_PLL	0x59	Master enable bit for the PLL circuit
EN_PLL_OUT	0x5F	Master enable bit for the PLL output
EN_PLL_BIAS	0x5F	Master enable bit for the PLL bias
EN_PLL_REFDIV	0x59	Master enable bit for the PLL reference divider
PLL Block Setting Bits		
PLL_REFDIV<9:0>	0x54-0x55	PLL reference divider (R) (See Table 4-7)
PLL_PRE<11:0>	0x56-0x57	PLL prescaler (N) (See Table 4-7)
PLL_CHAGPUMP<3:0>	0x58	PLL charge pump bias current control: from 25 µA to 375 µA, 25 µA per step
PLL_RES<4:0>	0x5A	PLL loop filter resistor value selection (See Table 4-6)
PLL_CAP3<4:0>	0x5B	PLL loop filter capacitor 3 value selection (See Table 4-6)
PLL_CAP2<4:0>	0x5D	PLL loop filter capacitor 2 value selection (See Table 4-6)
PLL_CAP1<4:0>	0x5C	PLL loop filter capacitor 1 value selection (See Table 4-6)
PLL Output Control Bits		
PLL_OUTDIV<3:0>	0x55	PLL output divider (See Table 4-7)
DCLK_DLY_PLL<2:0>	0x6D	Delay DCLK output up to 15 cycles of VCO clocks
EN_PLL_CLK	0x6D	EN_PLL_CLK = 1 enable PLL output clock to the ADC circuits
PLL Drift Monitoring Bits		
PLL_VCOL_STAT	0xD1	PLL drift status monitoring bit
PLL_VCOH_STAT	0xD1	PLL drift status monitoring bit
PLL Block Calibration Bits		
PLL_CAL_TRIG	0x6B	Forcing recalibration of the PLL
$\overline{\text{SOFT_RESET}}$	0x00	PLL is calibrated when exiting soft reset mode
PLL_CAL_STAT	0xD1	PLL auto-calibration status indication

TABLE 4-6: RECOMMENDED PLL CHARGE PUMP AND LOOP FILTER BIT SETTINGS

PLL Charge Pump and Loop Filter Parameter	$f_Q = f_{REF}/PLL_REFDIV$		
	$f_Q < 5$ MHz	5 MHz $\leq f_Q < 25$ MHz	$f_Q \geq 25$ MHz
PLL_CHAGPUMP<3:0>	0x04	0x04	0x04
PLL_RES<4:0>	0x1F	0x1F	0x07
PLL_CAP3<4:0>	0x07	0x02	0x07
PLL_CAP2<4:0>	0x07	0x01	0x08
PLL_CAP1<4:0>	0x07	0x01	0x08

TABLE 4-7: EXAMPLE OF PLL CONTROL BIT SETTINGS FOR f_S = 200 MHz WITH f_{REF} = 100 MHz

PLL Control Parameter	Value	Descriptions
f_{REF}	100 MHz	f_{REF} is coming from the external clock input
Target f_S(1)	200 MHz	ADC sampling frequency
Target f_{VCO}(2)	1.2 GHz	Range of f_{VCO} = 1.0375 GHz – 1.325 GHz
Target f_Q(3)	10 MHz	$f_Q = f_{REF}/PLL_REFDIV$ (See Table 4-6)
PLL Reference Divider (R)	10	PLL_REFDIV<9:0> = 0x0A
PLL Prescaler (N)	120	PLL_PRE<11:0> = 0x78
PLL Output Divider	6	PLL_OUTDIV<3:0> = 0x06

Note 1: $f_S = f_{VCO}/PLL_OUTDIV = 1.2\ GHz/6 = 200\ MHz$

2: $f_{VCO} = (N/R) \times f_{REF} = (12) \times 100\ MHz = 1.2\ GHz$

3: f_Q should be maximized for the best noise performance

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4.6 Digital Signal Post-Processing (DSPP) Options

While the device converts the analog input signals to digital output codes, the user can enable various Digital Signal Post-Processing (DSPP) options for special applications. These options are individually enabled or disabled by setting the Configuration bits. Table 4-8 summarizes the DSPP options that are available for each device.

TABLE 4-8: DIGITAL SIGNAL POST PROCESSING (DSPP) OPTIONS

Digital Signal Post Processing Option	Offering Device
FIR Decimation Filters	MCP37210-200 MCP37D10-200
Digital Gain and Offset Correction	
Noise-Shaping Requantizer (NSR)	
Digital Down-Conversion (DDC)	MCP37D10-200

4.6.1 NOISE-SHAPING REQUANTIZER (NSR)

The device includes 11-bit and 12-bit digital Noise-Shaping Requantizer (NSR) options. When this function is enabled (see Register 5-35), the output data bits are requantized to 11-bit or 12-bit, respectively. The NSR reshapes the requantization noise function, which pushes most of the noise outside the frequency band of interest. As a result, the noise floor within the selected bandwidth becomes lower.

To ensure the stability of the NSR, the input signal to the NSR should be limited to less than -0.8 dBFS (≈90% of full-scale). This can be achieved either by limiting the analog input level or by adjusting the digital gain control. See **Section 4.7 "Digital Offset and Digital Gain Settings"** and Registers 5-60 to 5-60 for details on the digital gain control. Input levels higher than -0.8 dBFS may corrupt the NSR output and should be avoided.

The NSR block consists of a series of filters, which are selectable using the NSR<6:0> register bit setting. Each filter is defined by a specific percentage bandwidth and center frequency. The available percentage bandwidths are:

- 11-bit mode: 22% and 25% of the sampling frequency
- 12-bit mode: 25% and 29% of the sampling frequency

The center frequency of the band is tunable such that the frequency band of interest can be placed anywhere within the Nyquist band. Table 4-9 lists all NSR-related registers. Equations 4-4 and 4-5 describe the NSR bandwidth of the 11-bit and 12-bit option, respectively.

EQUATION 4-4: NSR BANDWIDTH FOR 11-BIT OPTION

(a) 22% BW:

$$\frac{f_{Center}}{f_S} = 0.12 + \frac{0.26}{20} \times NSR$$

where $0 \le NSR \le 20$

(b) 25% BW:

$$\frac{f_{Center}}{f_S} = 0.125 + \frac{0.25}{20} \times (NSR - 21)$$

where $21 \le NSR \le 41$

EQUATION 4-5: NSR BANDWIDTH FOR 12-BIT OPTION

(a) 25% BW:

$$\frac{f_{Center}}{f_S} = 0.125 + \frac{0.25}{20} \times (NSR - 42)$$

where $42 \le NSR \le 62$

(b) 29% BW:

$$\frac{f_{Center}}{f_S} = 0.15 + \frac{0.2}{12} \times (NSR - 63)$$

where $63 \le NSR \le 76$

In these two equations, NSR is the NSR filter number.

Figure 4-12 shows a graphical demonstration of the NSR bandwidth, which is a percentage of the ADC sampling frequency.

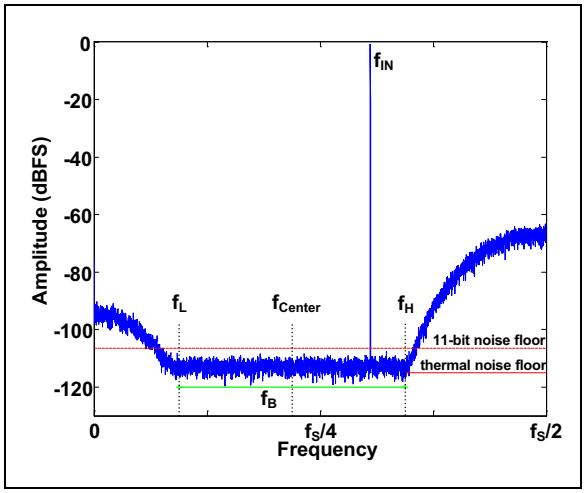

FIGURE 4-12: *Graphical Demonstration of the NSR Filter's Transfer Function. Note that f_B is controlled as a percentage of the sampling frequency (f_S).*

Tables 4-10 and 4-11 show the NSR filter selections. The selectable filters (tuning word) for each mode are:

- 11-bit mode: 0 to 41
- 12-bit mode: 42 to 76

NSR does not affect harmonic distortion. Various FFT spectrum plots when NSR is applied are shown in Figures 3-7 to 3-12. SNR and SFDR performance versus input amplitude when NSR is enabled are shown in Figures 3-20 and 3-22.

In the plots, SNR and SFDR are measured within the 12-bit-mode NSR bandwidth (25% of the sampling frequency). When the NSR block is disabled, the ADC data is provided directly to the output.

TABLE 4-9: REGISTER CONTROL PARAMETERS FOR NSR

Control Parameter	Register	Descriptions
NSR Enable Bits		
<EN_NSR_11>	0x7A	Enable 11-bit NSR
<EN_NSR_12>	0x7A	Enable 12-bit NSR
NSR Filter Setting		
NSR<6:0>	0x78	NSR filter settings
NSR Block Reset Control		
<EN_NSR_RESET>	0x78	Resets NSR in the event of overload

TABLE 4-10: 11-BIT NSR FILTER SELECTION(1)

NSR Filter No. (Tuning Word)	f_{Center}/f_S(1)	f_B (% of f_S)	NSR<6:0>
0	0.12	22	000-0000
1	0.133	22	000-0001
2	0.146	22	000-0010
—			
—			
19	0.367	22	001-0011
20	0.38	22	001-0100
21	0.125	25	001-0101
22	0.1375	25	001-0110
23	0.15	25	001-0111
—			
—			
40	0.3625	25	010-1000
41	0.375	25	010-1001

Note 1: Filters 0 - 41 are used for 11-bit mode only. If these are used for 12-bit mode, the output becomes unknown state.

TABLE 4-11: 12-BIT NSR FILTER SELECTION(1)

NSR Filter No. (Tuning Word)	f_{Center}/f_S(1)	f_B (% of f_S)	NSR<6:0>
42	0.125	25	010-1010
43	0.1375	25	010-1011
44	0.15	25	010-1100
—			
61	0.3625	25	011-1101
62	0.375	25	011-1110
63	0.15	29	011-1111
64	0.1667	29	100-0000
65	0.1833	29	100-0001
—			
—			
75	0.35	29	100-1011
76	0.3667	29	100-1100

Note 1: Filters 42 - 76 are used for 12-bit mode only. If these are used for 11-bit mode, the output becomes unknown state.

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4.6.2 DECIMATION FILTERS

Figure 4-13 shows a simplified decimation filter block diagram, and Table 4-13 summarizes the related control parameters for using decimation filters.

- **MCP37210-200:** Decimation rate is controlled by FIR_A<8:0> in Addresses 0x7A and 0x7B (Registers 5-35 - 5-36). The FIR_A<8:0> provides a maximum programmable decimation rate up to 512x using nine cascaded decimation stages.
- **MCP37D10-200:** (a) When DDC mode is not required, only FIR A is used; (b) When digital down-conversion (DDC) is used for I and Q data filtering, both FIR A and FIR B filters are used (see Figure 4-13). In this case, both are set to the same decimation rate. Note that stage 1A in FIR A is unused: the user must clear FIR_A<0> in Address 0x7A (Register 5-35).

The overall SNR performance can be improved with higher decimation rate. In theory, 3 dB improvement is expected with each successive stage of decimation (2x per stage), but the actual improvement is approximately 2.5 dB per stage due to finite attenuation in the FIR filters.

4.6.2.1 Output Data Rate and Clock Phase Control when Decimation is used

When decimation is used, it also reduces the output clock rate and output bandwidth by a factor equal to the decimation rate applied: the output clock rate is therefore no longer equal to the ADC sampling clock. The user needs to adjust the output clock and data rates in Address 0x02 (Register 5-3) based on the decimation applied. This allows the output data to be synchronized to the output data clock.

Phase shifts in the output clock can be achieved using DCLK_PHDLY_DEC<2:0> in Address 0x64 (Register 5-22). Only four output sampling phases are available when a 2x decimation rate is used, while all eight clock phases are available for other decimation rates. See **Section 4.9.8 "Output Data And Clock Rates"** for more details.

4.6.2.2 Using Decimation with Digital Down-Conversion (**MCP37D10-200**)

In the MCP37D10, the decimation feature can be used in conjunction with DDC. When DDC is enabled, the I and Q outputs can be decimated using I and Q channels. Since the half-band filter already includes a 2x decimation, the maximum possible decimation rate is 256x for each I and Q data using FIR A and FIR B filters (128x each from FIR A and B).

Note:	Digital Gain/Offset adjustment and DDC for I/Q data options occur prior to the decimation filters if they are enabled.

TABLE 4-12: DECIMATION RATE VS. SNR PERFORMANCE

Decimation Rate	SNR (dBFS)
1x	65.9
2x	67.8
4x	69.9
8x	71.3
16x	72.4
32x	73
64x	73.5
128x	
256x	73.7
512x	

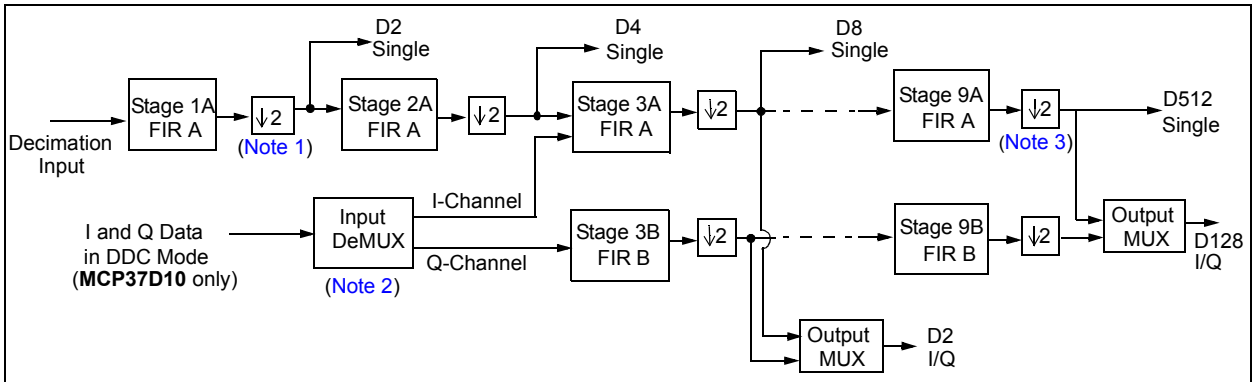
Note: The above data is valid with fs = 200 Msps, f_{IN} = 1 MHz, A_{IN} = -1 dBFS.

TABLE 4-13: REGISTER CONTROL PARAMETERS FOR USING DECIMATION FILTERS

Control Parameter	Register	Descriptions
Decimation Filter Settings		
FIR_A<8:0>	0x7A, 0x7B	FIR A configuration. I-Channel in I/Q-Channel mode
FIR_B<7:0>	0x7C	FIR B configuration for Q-Channel in I/Q-Channel mode
Output Data Rate and Clock Rate Settings(1)		
OUT_DATARATE<3:0>	0x02	Output data rate: Equal to decimation rate
OUT_CLKRATE<3:0>	0x02	Output clock rate: Equal to decimation rate
Output Clock Phase Control Settings(2)		
EN_PHDLY	0x64	Enable digital output phase delay when decimation filter is used
DCLK_PHDLY_DEC<2:0>	0x64	Digital output clock phase delay control

Note 1: The output data and clock rates must be updated when decimation rates are changed.

2: Output clock (DCLK) phase control is used when the output clock is divided by OUT_CLKRATE<3:0> bit settings.



Note 1: Stage 1A FIR is the first stage of the FIR A filter.

2: (a) Decimation Input (Not in DDC mode): Only FIR_A<8:0> is used.
(b) DDC Input for I/Q filtering in DDC mode: FIR_A<8:1> for I data and FIR_B<7:0> for Q data are used.

3: Maximum Decimation Rate:
(a) When DDC is not used: 512x.
(b) When DDC is used: 128x each for FIR A and FIR B.

FIGURE 4-13: *Simplified Block Diagram of Decimation Filters.*

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4.6.3 DIGITAL DOWN-CONVERSION (**MCP37D10-200** ONLY)

The Digital Down-Conversion (DDC) feature is available in MCP37D10-200. This feature can be combined with the decimation filter and used to:

- translate the input frequency spectrum to lower frequency band
- remove the unwanted out-of-band portion
- output the resulting signal as either I/Q data or a real signal centered at ¼ of the output data rate.

Figure 4-14 shows the DDC configuration. The DDC includes a 32-bit complex numerically controlled oscillator (NCO), a selectable (high/low) half-band filter, optional decimation and two output modes (I/Q or $f_S/8$).

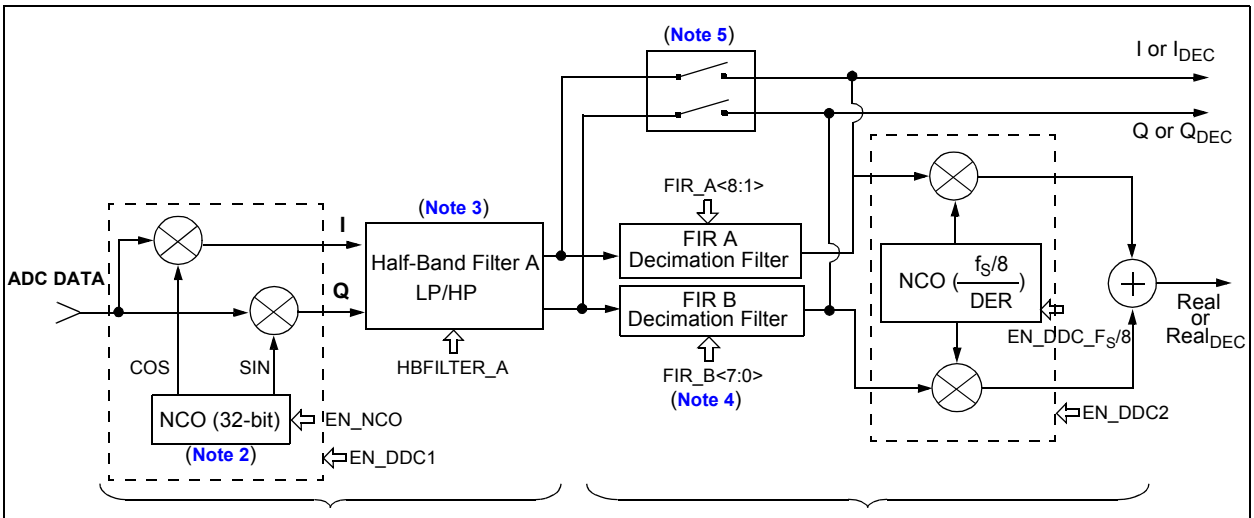
Frequency translation is accomplished with the NCO. The NCO frequency is programmable from 0 Hz to f_S. Phase and amplitude dither can be enabled to improve spurious performance of the NCO.

Each of the processing sub-blocks are individually controlled. Examples of setting registers for selected output type are shown in Tables 4-14 and 4-15 in **Section 4.6.4 "Examples of Register Settings for DDC and Decimation"**.

This DDC feature can be used in a variety of high-speed signal-processing applications, including digital radio, wireless base stations, radar, cable modems, digital video, MRI imaging, etc.

Example:

If the ADC is sampling an input at 200 Msps but the user is only interested in a 5 MHz span centered at 67 MHz, the digital down-conversion may be used to mix the sampled ADC data with 67 MHz to convert it to DC. The resulting signal can then be decimated by 16x such that the bandwidth of the ADC output is 6.25 MHz (200 Msps/16x decimation gives 12.5 Msps with 6.25 MHz Nyquist bandwidth). If $f_S/8$ mode is selected, then a single 25 Msps channel is output, where 6.25 MHz in the output data corresponds to 67 MHz at the ADC input. If I/Q mode is selected, then two 12.5 Msps channels are output, where DC corresponds to 67 MHz and the channels represent In-Phase (I) and Quadrature (Q) components of the down-conversion.



Note 1: See Addresses 0x80 - 0x81 (Registers 5-38 – 5-39) for the Control Parameters.
2: See Figure 4-15 for details of NCO control block.
3: Half-band Filter A includes a single-stage decimation filter.
4: See Figure 4-13 for details.
5: Switches are closed if decimation filter is not used and open if decimation filter is used.

FIGURE 4-14: *Simplified DDC Block Diagram for Single-Channel Mode. See Tables 4-14 and 4-15 for using this DDC Block.*

4.6.3.1 Numerically Controlled Oscillator (NCO)

The on-board Numerically Controlled Oscillator (NCO) provides the frequency reference for the In-Phase and Quadrature mixers in the digital down-converter (DDC).

The NCO serves as a quadrature local oscillator, capable of producing an NCO frequency of between 0 Hz and f_S with a resolution of $f_S/2^{32}$ where f_S is the ADC core sampling frequency.

Figure 4-15 shows the control signals associated with the NCO.

Note: The NCO is only used for DDC. It should be disabled when not in use.

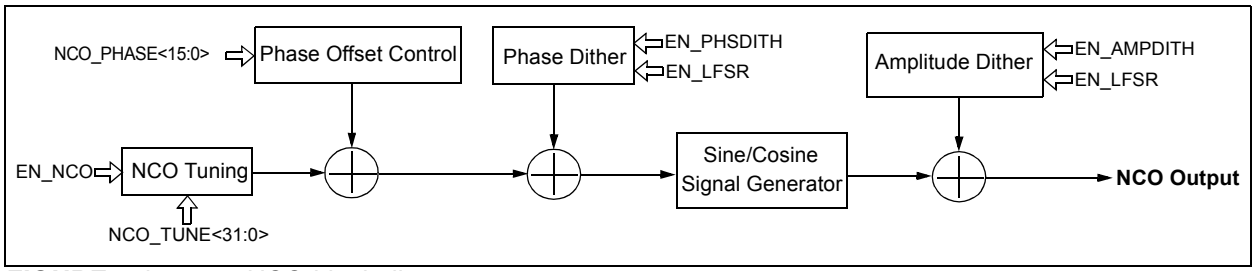


FIGURE 4-15: *NCO block diagram*

- **NCO Frequency Control:**

The NCO frequency is programmed from 0 Hz to f_S, using the 32-bit-wide unsigned register variable NCO_TUNE<31:0> in Addresses 0x82 – 0x85 (Registers 5-40 – 5-43).

The following equation is used to set the NCO_TUNE<31:0> register:

EQUATION 4-6: NCO FREQUENCY

$$NCO_TUNE<31:0> = round\left(2^{32} \times \frac{Mod(f_{NCO}, f_S)}{f_S}\right)$$

Where:

f_S = sampling frequency (Hz)

f_{NCO} = desired NCO frequency (Hz)

Mod (f_{NCO}, f_S) = gives the remainder of f_{NCO}/f_S

Mod() is a remainder function. For example, Mod(5, 2) = 1 and Mod(1.999, 2) = 1.999.

Example 1:

If f_{NCO} is 100 MHz and f_S is 200 MHz:

$$Mod(f_{NCO}, f_S) = Mod(100, 200) = 100$$

$$NCO_TUNE<31:0> = round\left(2^{32} \times \frac{Mod(100, 200)}{200}\right)$$

$$= 0x8000\ 0000$$

Example 2:

If f_{NCO} is 199.99999994 MHz and f_S is 200 MHz:

$$Mod(f_{NCO}, f_S) = Mod(199.99999994, 200) = 199.99999994$$

$$NCO_TUNE<31:0> = round\left(2^{32} \times \frac{Mod(199.99999994, 200)}{200}\right)$$

$$= 0xFFFF\ FFFF$$

4.6.3.2 NCO Amplitude and Phase Dither

The EN_AMPDITH and EN_PHSDITH parameters in Address 0x80 (Register 5-38) can be used for amplitude and phase dithering, respectively. In principle, these will dither the quantization error created by the use of digital circuits in the mixer and local oscillator, thus reducing spurs at the expense of noise. In practice, the DDC circuitry has been designed with sufficient noise and spurious performance for most applications. In the worst-case scenario, the NCO has an SFDR of greater than 116 dB when the amplitude dither is enabled and 112 dB when disabled. Although the SNR (≈ 93 dB) of the DDC is not significantly affected by the dithering option, using the NCO with dithering options enabled is always recommended for the best performance.

4.6.3.3 NCO for $f_S/8$ and $f_S/(8xDER)$

The output of the first down-conversion block (DDC1) is a complex signal (comprising I and Q data) which can then be optionally decimated further up to 128x to provide both a lower output data rate and input channel filtering. If $f_S/8$ mode is enabled, a second mixer stage (DDC2) will convert the I/Q signals from the DDC1 to a real signal centered at half of the current Nyquist frequency; i.e., if the current output data rate for I and Q is 25 Msps each (12.5 MHz Nyquist), then in $f_S/8$ mode the output data rate would be 50 Msps (25 Msps x2 for I and Q) and the resulting real signal after combining the two would be re-centered around 12.5 MHz. This second frequency translation by DDC2 is accomplished after the decimation filters (if used) as shown in Figure 4-14.

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When decimation is enabled, the I/Q outputs are up-converted by $f_S/(8xDER)$, where DER is the additional decimation rate added by the FIR decimation filters. This provides a decimated output signal centered at $f_S/8$ or $f_S/(8xDER)$ in the frequency domain.

4.6.3.4 NCO Phase Offset Control

The user can add phase offset to the NCO frequency using the NCO phase offset control registers (Addresses 0x86 to 0x87 – Registers 5-44 – 5-45). NCO_PHASE<15:0> is the 16-bit wide NCO phase offset control parameter. The phase offset can be controlled from 0° to 359.995° with 0.005° per step. The following equation is used to program the NCO phase offset register:

EQUATION 4-7: NCO PHASE OFFSET

$$NCO_PHASE<15:0> = 2^{16} \times \frac{Offset\ Value\ (\phi)}{360}$$

Where:

Offset Value (ϕ) = desired phase offset value in degrees

A decimal number is used for the binary contents of the NCO_PHASE<15:0>.

4.6.3.5 In-Phase and Quadrature Signals

When the first down-conversion is enabled, it produces In-phase (I) and Quadrature (Q) components given by:

EQUATION 4-8: I AND Q SIGNALS

$$I = ADC \times COS(2\pi f_{NCO} t + \phi)$$
$$Q = ADC \times SIN(2\pi f_{NCO} t + \phi)$$

where:

$$\phi = 360 \times \frac{NCO_PHASE<15:0>}{2^{16}}$$
$$= 0.005493164° \times NCO_PHASE<15:0>$$

where:

ADC = output of the ADC block

ϕ = NCO phase offset defined by NCO_PHASE<15:0> in Address 0x86

t = k/f_S, with k =1, 2, 3,..., n

f_{NCO} = NCO frequency

I and Q data are output in an interleaved fashion where I data is output on the rising edge of the WCK.

4.6.3.6 Half-Band Filter

The frequency translation is followed by a half-band digital filter, which is used to reduce the sample rate by a factor of two while rejecting aliases that fall into the band of interest.

The user can select a high- or low-pass half-band filter using the HBFILTER_A and HBFILTER_B bits in Address 0x80 (Register 5-38). These filters provide greater than 90 dB of attenuation in the attenuation band, and less than 1 mdB (10^{-3} dB) of ripple in the passband region of 20% of the input sampling rate. For example, for an ADC sample rate of 200 Msps, these filters provide less than 1 mdB of ripple over a bandwidth of 40 MHz.

The filter responses shown in Figures 4-16 and 4-17 indicate a ripple of 0.5 mdB and an alias rejection of 90 dB. The output of the half-band filter is a DC-centered complex signal (I and Q). This I and Q signal is then carried to the next down-conversion stage (DDC2) for frequency translation (up-conversion), if the DDC is enabled.

Note: The half-band filter delays the data output by 80 clock cycles: 2 (due to decimation) x 40 cycles (due to filter group delay)

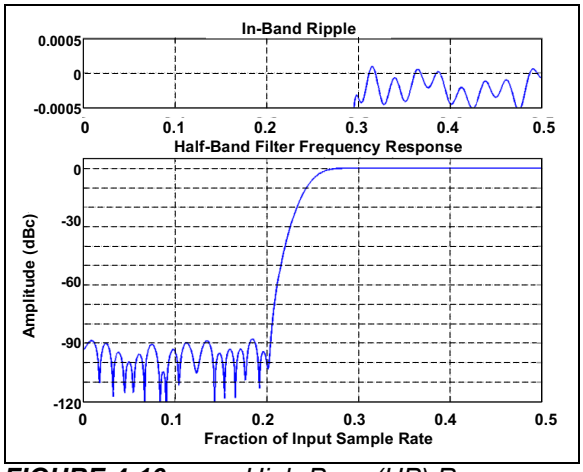

FIGURE 4-16: *High-Pass (HP) Response of Half-Band Filter.*

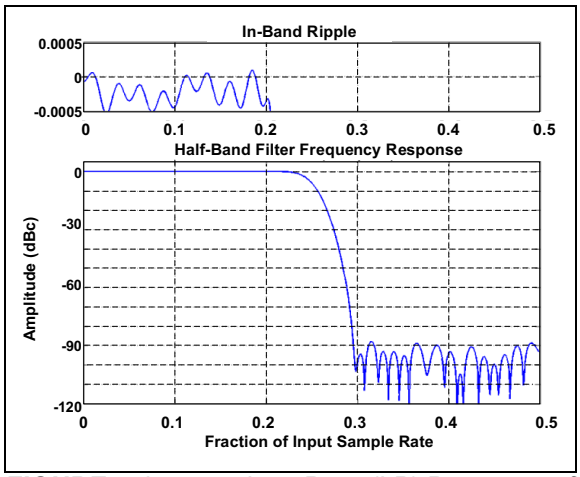

FIGURE 4-17: *Low-Pass (LP) Response of Half-Band Filter.*

4.6.4 EXAMPLES OF REGISTER SETTINGS FOR DDC AND DECIMATION

The following tables show examples of setting registers to use digital down-conversion (DDC) with decimation depending on the output type selection. This feature is available in the MCP37D10-200 device only.

TABLE 4-14: REGISTER SETTINGS FOR DDC AND DECIMATION OPTIONS – EXAMPLE

Decimation Rate (by FIR A and FIR B)(1)	DDC Mode	Address 0x02(2)	FIR A Filter		FIR B Filter	DDC1	DDC2	Output
			0x7A<6> (FIR_A<0>)	0x7B (FIR_A<8:1>)	0x7C (FIR_B<7:0>)	0x80<5,1,0>(3)	0x81<6>(4)	
0	Disabled	0x00	0	0x00	0x00	0,0,0	0	ADC
8	Disabled	0x33	1	0x03	0x00	0,0,0	0	ADC with decimation (÷8)
512	Disabled	0x99	1	0xFF	0x00	0,0,0	0	ADC with decimation (÷512)
0	I/Q	0x00(5)	0	0x00	0x00	1,0,1	0	I/Q Data
8	I/Q	0x33	0	0x07	0x07	1,0,1	0	Decimated I/Q (÷8)
0	f_S/8	0x11(6)	0	0x00	0x00	1,1,1	0	Real without additional decimation
8	f_S/8	0x44	0	0x07	0x07	1,0,1	1	Real with decimation (÷16)

Note 1: When DDC is used, the actual total decimation is 2x larger since 2x is included from the DDC Half-Band Filter. Example: Decimation = 8x with DDC-I/Q option actually has 16x decimation with 8x provided by the decimation filter and 2x from the DDC Half-Band Filter.

2: Output data and clock rate control register.

3: 0x80<5,1,0> = <EN_NCO, EN_DDC_FS/8, EN_DDC1>.

4: 0x81<6> = <EN_DDC2>.

5: Each of I/Q has 1/2 of f_S bandwidth. The combined bandwidth is the same as the f_S bandwidth. Therefore, the data rate adjustment is not needed.

6: The Half-Band Filter A includes decimation of 2.

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TABLE 4-15: OUTPUT TYPE VS. CONTROL PARAMETERS FOR DDC – EXAMPLE

Output Type	Control Parameter	Register	Descriptions
Complex: I and Q	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 0	0x80	NCO (f_S/8/DER) is disabled
	EN_DDC2 = 0	0x81	DDC2 is disabled
	FIR_A<8:1> = 0x00	0x7B	FIR A decimation filter is disabled
	FIR_B<7:0> = 0x00	0x7C	FIR B decimation filter is disabled
	OUT_CLKRATE<3:0>	0x02	Output clock rate is not affected (no need to change)
Decimated I and Q: I_{DEC}, Q_{DEC}	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 0	0x80	NCO (f_S/8/DER) is disabled
	EN_DDC2 = 0	0x81	DDC2 is disabled
	FIR_A<8:1>	0x7B	Program FIR A filter for extra decimation(1)
	FIR_B<7:0>	0x7C	Program FIR B filter for extra decimation(1)
	OUT_CLKRATE<3:0>	0x02	Adjust the output clock rate to the decimation rate
Real: $Real_A$ after DDC(f_S/8/DER) without using Decimation Filter	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 1	0x80	NCO (f_S/8/DER) is enabled. This translates the input signal from DC to f_S/8(2)
	EN_DDC2 = 1	0x81	DDC2 is enabled
	FIR_A<8:1> = 0x00	0x7B	Decimation filter FIR A is disabled
	FIR_B<7:0> = 0x00	0x7C	Decimation filter FIR B is disabled
	OUT_CLKRATE<3:0> = 0001	0x02	Adjust the output clock rate to divided by 2(3)
Decimated Real: $Real_{A_DEC}$ after Decimation Filter and DDC(f_S/8/DER)	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 1	0x80	NCO (f_S/8/DER) is enabled. This translates the input signal from DC to f_S/8/DER(2)
	EN_DDC2 = 1	0x81	DDC2 is enabled
	FIR_A<8:1>	0x7B	Program FIR B filter for extra decimation(4)
	FIR_B<7:0>	0x7C	Program FIR B filter for extra decimation(4)
	OUT_CLKRATE<3:0>	0x02	Adjust the output clock rate to the total decimation rate including the 2x decimation by the Half-Band Filter A

Note 1: For I/Q decimation, the maximum decimation rate for the FIR A and FIR B filters is 128x each since the input is already decimated by 2x in the Half-Band Filter. See Figure 4-13 for details.

2: DER is the decimation rate setting of the FIR A and FIR B filters.

3: The Half-Band Filter A includes decimation of 2.

4: When this filter is used, the up-conversion frequency is reduced by the extra decimation rates (DER).

4.7 Digital Offset and Digital Gain Settings

Figure 4-18 shows a simplified block diagram of the digital offset and gain settings. Offset is applied prior to the gain. Offset and gain adjustments occur prior to DDC or decimation when these features are used.

4.7.1 DIGITAL OFFSET SETTINGS

The offset can be controlled using two combined digital offset correction registers: DIG_OFFSET<15:0> in Addresses 0x66 - 0x67.

4.7.2 DIGITAL GAIN SETTINGS

The digital gain can be controlled using DIG_GAIN<7:0> in Addresses 0x96 - 0x9D. All DIG_GAIN<7:0> in Addresses 0x96 - 0x9D must be programmed with the same value.

When the device is first powered-up or has hardware reset, DIG_GAIN<7:0> is set with a default setting (‘0011-1100’). The user may program the DIG_GAIN<7:0> to ‘0011-1000’ for higher SNR performance (0.5 dB higher than the default setting).

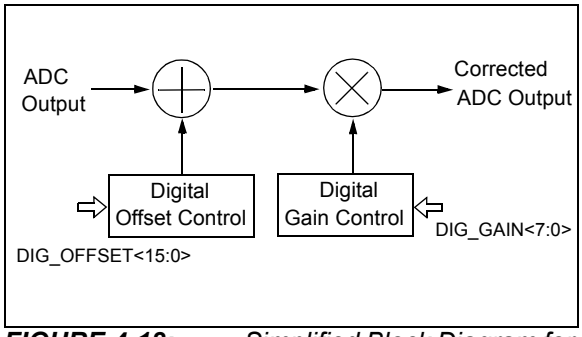

FIGURE 4-18: *Simplified Block Diagram for Digital Offset and Gain Settings.*

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4.8 Output Data format

The device can output the ADC data in offset binary or two's complement. The data format is selected by the DATA_FORMAT bit in Address 0x62 (Register 5-20).

Table 4-16 shows the relationship between the analog input voltage, the digital data output bits and the over-range bit. By default, the output data format is two's complement.

TABLE 4-16: ADC OUTPUT CODE VS. INPUT VOLTAGE

Input Range	Offset Binary (1)	Two's Complement (1)	Overrange (OVR)
$A_{IN} > A_{FS}$	1111-1111-1111	0111-1111-1111	1
$A_{IN} = A_{FS}$	1111-1111-1111	0111-1111-1111	0
$A_{IN} = A_{FS} – 1$ LSb	1111-1111-1110	0111-1111-1110	0
$A_{IN} = A_{FS} – 2$ LSb	1111-1111-1100	0111-1111-1100	0
	• • •		
$A_{IN} = A_{FS}/2$	1100-0000-0000	0100-0000-0000	0
$A_{IN} = 0$	1000-0000-0000	0000-0000-0000	0
$A_{IN} = -A_{FS}/2$	0011-1111-1111	1011-1111-1111	0
	• • •		
$A_{IN} = -A_{FS} + 2$ LSb	0000-0000-0010	1000-0000-0010	0
$A_{IN} = -A_{FS} + 1$ LSb	0000-0000-0001	1000-0000-0001	0
$A_{IN} = -A_{FS}$	0000-0000-0000	1000-0000-0000	0
$A_{IN} < -A_{FS}$	0000-0000-0000	1000-0000-0000	1

Note 1: MSb is sign bit.

4.9 Digital Output

The MCP37210-200 and MCP37D10-200 can operate in one of the following two digital output modes:

- Full-Rate CMOS
- Double-Data-Rate (DDR) LVDS

The outputs are powered by DV_{DD18} and GND. LVDS mode is recommended for data rates above 80 Msps. The digital output mode is selected by the OUTPUT_MODE<1:0> bits in Address 0x62 (Register 5-20). Figures 2-1 – 2-2 show the timing diagrams of the digital output.

4.9.1 FULL-RATE CMOS MODE

In full-rate CMOS mode, the data outputs (Q11 to Q0), over-range indicator (OVR), word clock (WCK) and the data output clock (DCLK+, DCLK–) have CMOS output levels. The WCK is disabled, except for the I/Q data output mode in the MCP37D10. The digital output should drive minimal capacitive loads. If the load capacitance is larger than 10 pF, a digital buffer should be used.

4.9.2 DOUBLE-DATA-RATE LVDS MODE

The Double-Data-Rate (DDR) LVDS mode is a parallel data stream which changes on each edge of the output clock. See Figure 2-2 for details.

In I/Q Data Output mode in the MCP37D10-200, I and Q data are clocked out sequentially with the WCK that is synchronized to I data. OVR and WCK are an LVDS pair.

The device outputs the following LVDS output pairs:

- Output data: Q5+/Q5- through Q0+/Q0-
- Output clock: DCLK+/DCLK-
- OVR/WCK

Note that WCK is logic '0' except in I/Q mode.

A 100Ω differential termination resistor is required for each LVDS output pin pair. The termination resistor should be located as close as possible to the LVDS receiver. By default, the outputs are standard LVDS levels: 3.5 mA output current with a 1.15V output common-mode voltage on 100Ω differential load. See Address 0x63 (Register 5-21) for more details of the LVDS mode control.

Note:	LVDS output polarity can be controlled independently for each LVDS pair. See POL_LVDS<5:0> setting in Address 0x65 (Register 5-23)

4.9.3 OVERRANGE BIT (OVR)

The input overrange status bit is asserted (logic high) when the analog input has exceeded the full-scale range of the ADC in either the positive or negative direction. The OVR bit has the same pipeline latency as the ADC data bits. See Address 0x68 (Register 5-26) for OVR control options.

If DSPP option is enabled, OVR pipeline latency will be unaffected; however, the data will incur additional delay. This has the effect of allowing the OVR indicator to precede the affected data.

4.9.3.1 OVR Bit in LVDS DDR Output Mode

(a) Normal ADC Output Mode:

The device outputs the OVR bit on the falling edge of the data output clock.

(b) I and Q Output Mode in MCP37D10-200:

The OVR bit is multiplexed with the word clock (WCK) output bit, such that OVR is output on the falling edge of the data output clock and WCK on the rising edge.

4.9.4 WORD CLOCK (WCK)

- MCP37210-200: WCK is disabled.
- MCP37D10-200: WCK is available in I/Q data output mode only. WCK is asserted coincidentally with the I data. See Address 0x68 (Register 5-26) for OVR and WCK control options.

4.9.5 LVDS OUTPUT POLARITY CONTROL

In LVDS mode, the output polarity can be controlled independently for each LVDS pair. Table 4-17 summarizes the LVDS output polarity control register bits.

TABLE 4-17: LVDS OUTPUT POLARITY CONTROL

Control Parameter	Register	Descriptions
POL_LVDS<5:0>	0x65	Control polarity of LVDS data pairs
POL_OVR_WCK	0x68	Control polarity of OVR and WCK bit pair

4.9.6 PROGRAMMABLE LVDS OUTPUT CURRENT

In LVDS mode, the default output driver current is 3.5 mA. This current can be adjusted by using the LVDS_IMODE<2:0> bit setting in Address 0x63 (Register 5-21). Available output drive currents are: 1.8 mA, 3.5 mA, 5.4 mA, and 7.2 mA.

4.9.7 OPTIONAL LVDS DRIVER INTERNAL TERMINATION

In most cases, using an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by setting the LVDS_LOAD bit in Address 0x63 (Register 5-21). The internal termination helps absorb any reflections caused by imperfect impedance termination at the receiver.

4.9.8 OUTPUT DATA AND CLOCK RATES

The user can reduce output data and output clock rates using Address 0x02 (Register 5-3). When decimation or digital down-conversion (DDC) is used, the output data rate has to be reduced to synchronize with the reduced output clock rate.

4.9.9 PHASE SHIFTING OF OUTPUT CLOCK (DCLK)

In full-rate CMOS mode, the data output bit transition occurs at the rising edge of DCLK+ so the falling edge of DCLK+ can be used to latch the output data.

In double-data-rate LVDS mode, the data transition occurs at both the rising and falling edges of DCLK+. For adequate setup and hold time when latching the data into the external host device, the user can shift the phase of the digital clock output (DCLK+/DCLK-) relative to the data output bits.

The output phase shift (delay) is controlled by each unique register depending on which timing source is used or if decimation is used. Table 4-18 shows the output clock phase control registers for each Configuration mode: (a) when DLL is used; (b) when decimation is used; and (c) when PLL is used.

Figure 4-19 shows an example of the output clock phase delay control using the DCLK_PHDLY_DLL<2:0> when DLL is used.

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TABLE 4-18: OUTPUT CLOCK (DCLK) PHASE CONTROL PARAMETERS

Control Parameter	Register	Operating Condition(1)
When DLL is used:		
EN_PHDLY	0x64	EN_PHDLY = 1: Enable output clock phase delay control
DCLK_PHDLY_DLL<2:0>	0x52	DCLK phase delay control when DLL is used. Decimation is not used.
When decimation is used:		
EN_PHDLY	0x64	EN_PHDLY = 1: Enable output clock phase delay control
DCLK_PHDLY_DEC<2:0>		DCLK phase delay control when decimation filter is used. The phase delay is controlled in digital clock output control block.
When PLL is used:		
DCLK_DLY_PLL<2:0>	0x6D	DCLK delay control when PLL is used

Note 1: See Figure 4-11 for details.

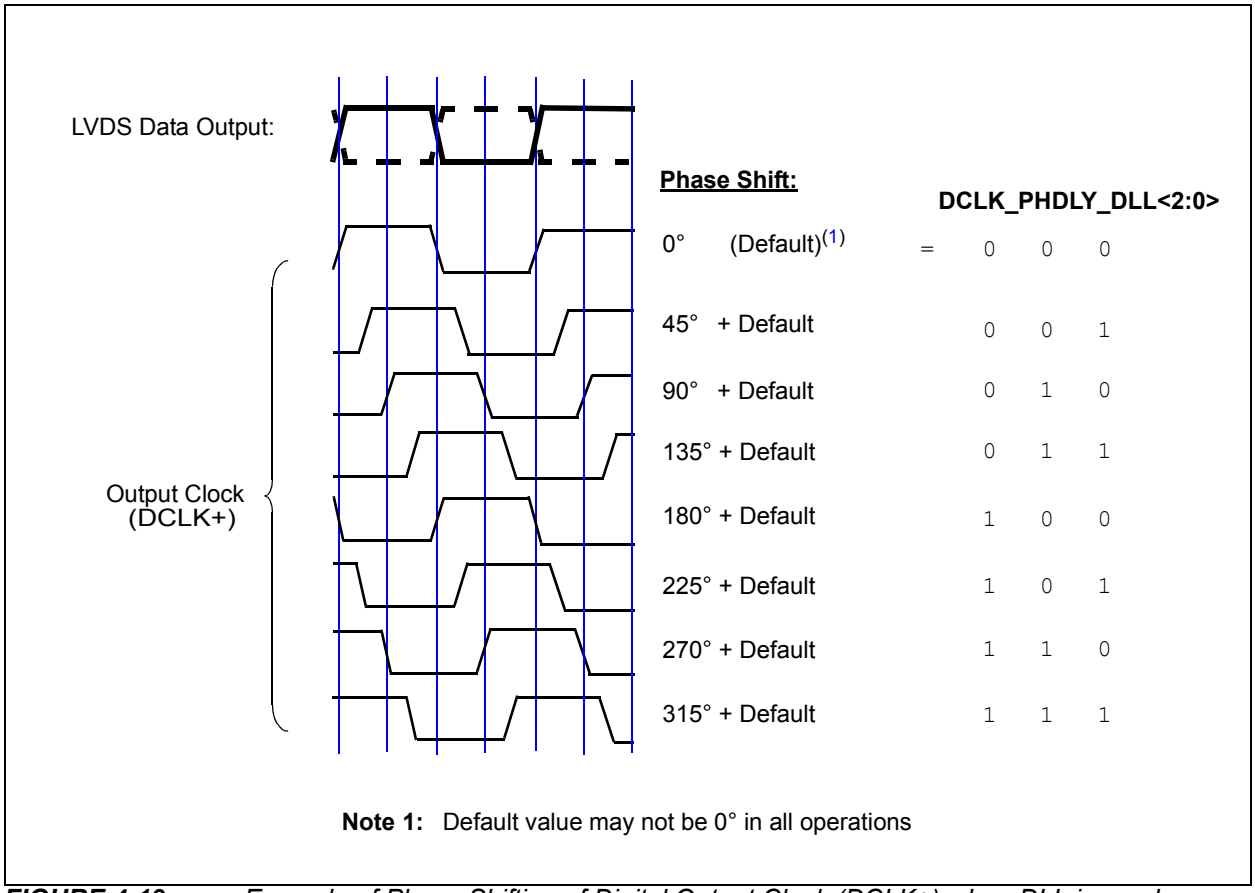

FIGURE 4-19: *Example of Phase Shifting of Digital Output Clock (DCLK+) when DLL is used.*

4.9.10 DIGITAL OUTPUT RANDOMIZER

Depending on PCB layout considerations and power supply coupling, SFDR may be improved by decorrelating the ADC input from the ADC digital output data. The device includes an output data randomizer option. When this option is enabled, the digital output is randomized by applying an exclusive-OR logic operation between the LSb (D0) and all other data output bits.

To decode the randomized data, the reverse operation is applied: an exclusive-OR operation is applied between the LSb (D0) and all other bits. The DCLK, OVR, WCK, and LSb (D0) outputs are not affected. Figure 4-20 shows the block diagram of the data randomizer and decoder logic. The output randomizer is enabled by setting the EN_OUT_RANDOM bit in Address 0x07 (Register 5-5).

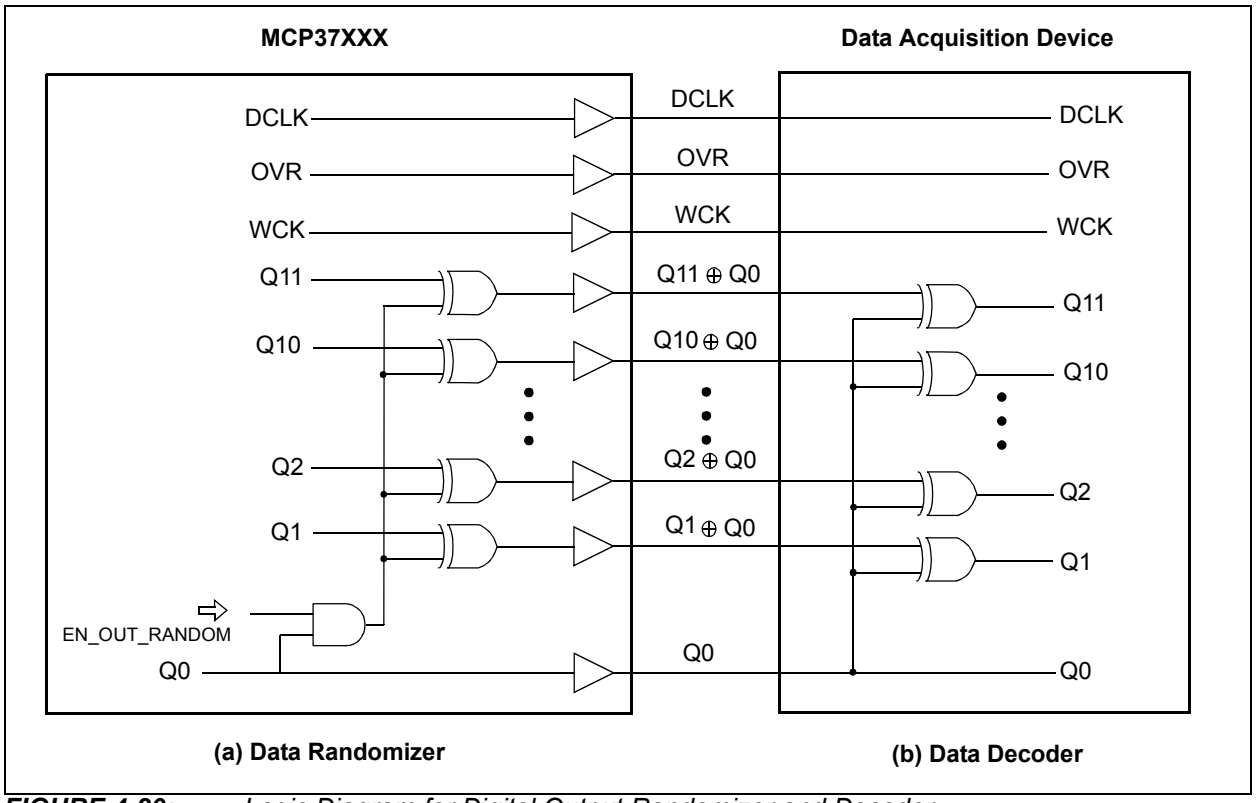

FIGURE 4-20: *Logic Diagram for Digital Output Randomizer and Decoder.*

4.9.11 OUTPUT DISABLE

The digital output can be disabled by setting OUTPUT_MODE<1:0> = 00 in Address 0x62 (Register 5-20). All digital outputs are disabled, including OVR, DCLK, etc.

4.9.12 OUTPUT TEST PATTERNS

To facilitate testing of the I/O interface, the device can produce various predefined or user-defined patterns on the digital outputs. See TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20) for the predefined test patterns. For the user-defined test patterns, Addresses 0x74 – 0x77 (Registers 5-29 – 5-32) can be used. When an output test mode is enabled, the ADC's analog section can still be operational but does not drive the digital outputs. The outputs are driven only with the selected test pattern.

Since the output test pins (TP, TP1 and TP2) can toggle during this test, always leave these test pins floating (not connected) to avoid contention and excess current draws.

4.9.12.1 Pseudo-Random Number (PN) Sequence Output

When TEST_PATTERNS<2:0> = 111, the device outputs a pseudo-random number (PN) sequence which is defined by the polynomial of degree 16, as shown in Equation 4-9. Figure 4-21 shows the block diagram of a 16-bit Linear Feedback Shift Register (LFSR) for the PN sequence.

EQUATION 4-9: POLYNOMIAL FOR PN

$$P(x) = 1 + x^4 + x^{13} + x^{15} + x^{16}$$

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The output PN[15:4] is directly applied to the output pins Qn[11:0]. In addition to the output at the Qn[11:0] pins, PN[15] is copied to OVR pin and PN[14] is copied to WCK pin. In CMOS output mode, the pattern is always applied to all CMOS I/O pins, regardless whether or not they are enabled. In LVDS output mode, the pattern is only applied to the LVDS pairs that are enabled.

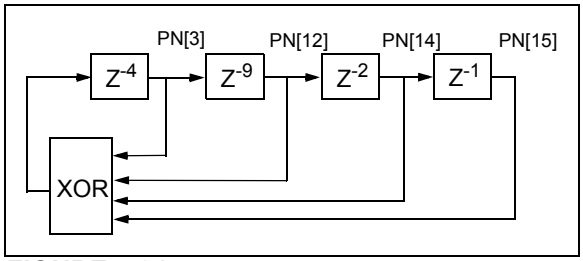

FIGURE 4-21: *Block Diagram of 16-bit LFSR for Pseudo-Random Number (PN) Sequence for Output Test Pattern.*

4.10 System Calibration

The built-in system calibration algorithm includes:

- Harmonic Distortion Correction (HDC)
- DAC Noise Cancellation (DNC)
- Dynamic Element Matching (DEM)

HDC and DNC correct the nonlinearity in the residue amplifier and DAC, respectively. The system calibration is performed by:

- Power-up calibration, which takes place during the Power-on Reset sequence (requires 3×2^{26} clock cycles)
- Background calibration, which takes place during normal operation (per 2^{30} clock cycles).

Background calibration time is invisible to the user and primarily affects the ADC's ability to track variations in ambient temperature.

The calibration status is monitored by CAL pin or the ADC_CAL_STAT bit in Address 0xC0 (Register 5-68). See also Address 0x07 (Register 5-5) and 0x1E (Register 5-6) for time delay control of the auto-calibration. Table 4-19 shows the calibration time for various ADC core sample rates.

TABLE 4-19: CALIBRATION TIME VS. ADC CORE SAMPLE RATE

f_S (Msps)	200	150	100	70	50
Power-Up Calibration Time (s)	1.01	1.34	2.01	2.88	4.03
Background Calibration Time (s)	5.37	7.16	10.73	15.34	21.48

4.10.1 RESET COMMAND

Although the background calibration will track changes in temperature or supply voltage, changes in clock frequency or register configuration should be followed by a recalibration of the ADC. This can be accomplished via either the Hard or the Soft Reset command. The recalibration time is the same as the power-up calibration time. Resetting the device is highly recommended when exiting from Shutdown or Standby mode after an extended amount of time. During the reset, the device has the following state:

- No ADC output
- No change in power-on condition of internal reference
- Most of the internal clocks are not distributed
- Contents of internal user registers:
  - Not affected by Soft Reset
  - Reset to default values by Hardware Reset
- Current consumption of the digital section is negligible, but no change in the analog section.

4.10.1.1 Hardware Reset

A hard reset is triggered by toggling the $\overline{\text{RESET}}$ pin. On the rising edge, all internal calibration registers and user registers are initialized to their default states and recalibration of the ADC begins. The recalibration time is the same as the power-up calibration time. See Figure 2-6 for the timing details of the hardware $\overline{\text{RESET}}$ pin.

4.10.1.2 Soft Reset

The user can issue a Soft Reset command for a fast recalibration of the ADC by setting the $\overline{\text{SOFT_RESET}}$ bit to '0' in Address 0x00 (Register 5-1). During Soft Reset, all internal calibration registers are initialized to their initial default states. User registers are unaffected. When exiting the Soft Reset (changing from '0' to '1'), an automatic device calibration takes place.

4.11 Power Dissipation and Power Savings

The power dissipation of the ADC core is proportional to the sample rate (f_S). The digital power dissipation of the CMOS outputs is determined primarily by the strength of the digital drivers and the load condition on each output pin. The maximum digital load current (I_{LOAD}) can be calculated as:

EQUATION 4-10: CMOS OUTPUT LOAD CURRENT

$$I_{LOAD} = DV_{DD1.8} \times f_{DCLK} \times N \times C_{LOAD}$$

Where:

N = Number of bits

C_{LOAD} = Capacitive load of output pin

The capacitive load presented at the output pins needs to be minimized to minimize digital power consumption. The output load current of the LVDS output is constant, since it is set by LVDS_IMODE<2:0> in Address 0x63 (Register 5-21).

4.11.1 POWER-SAVING MODES

This device has two power-saving modes:

- Shutdown
- Standby

They are set by the SHUTDOWN and STANDBY bits in Address 0x00 (Register 5-1).

In Shutdown mode, most of the internal circuitry, including the reference and clock, are turned off with the exception of the SPI interface. During Shutdown mode, the device consumes 25 mA (typical), primarily due to digital leakage. When exiting from Shutdown mode, issuing a Soft Reset at the same time is highly recommended. This will perform a fast recalibration of the ADC. The contents of the internal registers are not affected by the Soft Reset.

In Standby mode, most of the internal circuitry is disabled except for the reference, clock and SPI interface. If the device has been in standby for an extended period of time, the current calibration value may not be accurate. Therefore, when exiting from Standby mode, executing the device Soft Reset at the same time is highly recommended.

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5.0 SERIAL PERIPHERAL INTERFACE (SPI)

The user can configure the ADC for specific functions or optimized performance by setting the device's internal registers through the Serial Peripheral Interface (SPI). The SPI communication uses three pins: $\overline{CS}$, SCLK and SDIO. Table 5-1 summarizes the SPI pin functions. The SCLK is used as serial timing clock and can be used up to 50 MHz.

SDIO (Serial Data Input/Output) is a dual-purpose pin that allows data to be sent or read from the internal registers. The Chip Select ($\overline{CS}$) pin enables SPI communication when active-low. The falling edge of $\overline{CS}$ followed by a rising edge of SCLK determines the start of the SPI communication. When $\overline{CS}$ is tied to high, the SPI communication is disabled and SPI pins are placed in high-impedance mode. The internal registers are accessible by their address.

Figures 5-1 and 5-2 show the SPI data communication protocols for this device with MSb-first and LSb-first options, respectively. The communication protocol consists of:

- 16-bit wide instruction header + Data byte 1 + Data byte 2 +. . .+ Data Byte N

Table 5-2 summarizes the bit functions. The R/$\overline{W}$ bit of the instruction header indicates whether the command is a read ('1') or a write ('0'):

- If the R/$\overline{W}$ bit is '1', the SDIO pin changes direction from an input (SDI) to an output (SDO) after the 16-bit-wide instruction header.

By selecting the R/$\overline{W}$ bit, the user can write the register or read back the register contents. The W1 and W2 bits in the instruction header indicate the number of data bytes to transmit or receive in the following data frame.

A2 – A0 bits are the SPI device address bits. These bits are used when multiple devices are used in the same SPI bus. A2 is internally hard-coded to '0'. The A1 and A0 bits correspond to the logic level of ADR1 and ADR0 pins, respectively.

Note:	In VTLA-124 package, ADR1 is internally bonded to ground (logic '0').

The R9 – R0 bits represent the starting address of the configuration register to write or read. The data bytes following the instruction header are the register data. All register data is eight bits wide. Data can be sent in MSb-first mode (default) or in LSb-first mode, which is determined by the <LSB_ FIRST> bit setting in Address 0x00 (Register 5-1). In Write mode, the data is clocked in at the rising edge of the SCLK. In Read mode, the data is clocked out at the falling edge of the SCLK.

TABLE 5-1: SPI PIN FUNCTIONS

Pin Name	Descriptions
$\overline{CS}$	Chip Select pin. SPI mode is initiated at the falling edge. It needs to maintain active-low for the entire period of the SPI communication. The device exits the SPI communication at the rising edge.
SCLK	Serial clock input pin. • Writing to the device: Data is latched at the rising edge of SCLK • Reading from the device: Data is latched at the falling edge of SCLK
SDIO	Serial data input/output pin. This pin is initially an input pin (SDI) during the first 16-bit instruction header. After the instruction header, its I/O status can be changed depending on the R/$\overline{W}$ bit: • if R/$\overline{W}$ = 0: Data input pin (SDI) for writing • if R/$\overline{W}$ = 1: Data output pin (SDO) for reading

TABLE 5-2: SPI DATA PROTOCOL BIT FUNCTIONS

Bit Name	Descriptions
R/$\overline{W}$	1 = Read Mode 0 = Write Mode
W1, W0 (Data Length)	00 = Data for one register (1 byte) 01 = Data for two registers (2 bytes) 10 = Data for three registers (3 bytes) 11 = Continuous reading or writing by clocking SCLK(1)
A2 - A0	Device SPI Address for multiple devices in SPI bus. A2: Internally hard-coded to '0' A1: Logic level of ADR1 pin A0: Logic level of ADR0 pin
R9 - R0	Address of starting register.
D7 - D0	Register data. MSb or LSb first, depending on the LSB_FIRST bit setting in 0x00.

Note 1: The register address counter is incremented by one per step. The counter does not automatically reset to 0x00 after reaching the last address (0x15D). Be aware that the user-registers are not sequentially allocated.

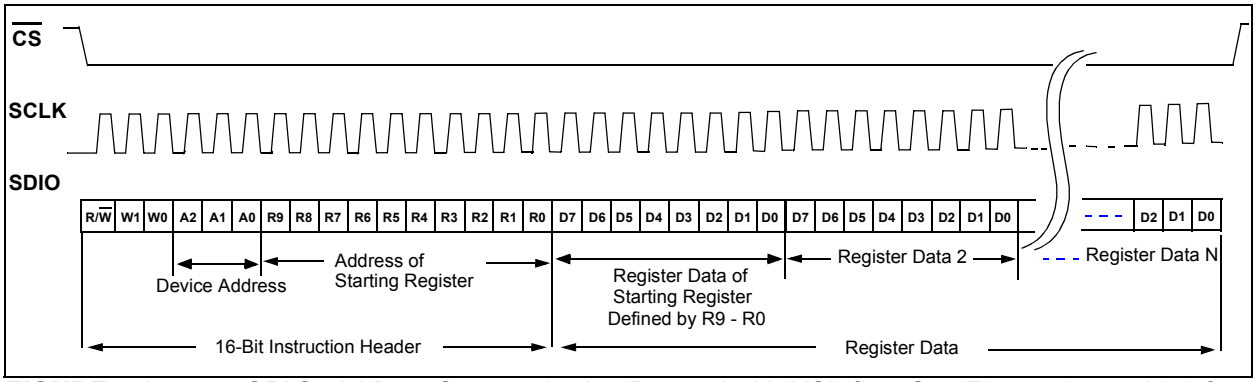

FIGURE 5-1: *SPI Serial Data Communication Protocol with MSb-first. See Figures 2-5 and 2-6 for Timing Specifications.*

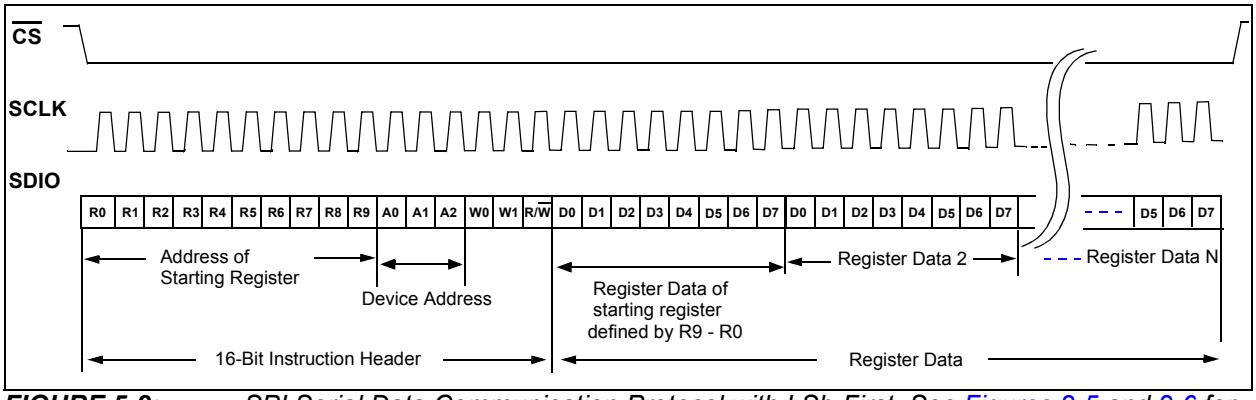

FIGURE 5-2: *SPI Serial Data Communication Protocol with LSb-First. See Figures 2-5 and 2-6 for Timing Specifications.*

5.1 Register Initialization

The internal configuration registers are initialized to their default values by two different ways:

- After 2^{20} clock cycles of delay from the Power-on Reset (POR).
- Reset by the hardware reset pin ($\overline{\text{RESET}}$).

Figures 2-5 and 2-6 show the timing details.

5.2 Configuration Registers

The internal registers are mapped from address 0x00 to 0x15D. These user registers are not sequentially located. Some user configuration registers include factory-controlled bits.

The factory-controlled register bits should not be overwritten by the user. All user configuration registers are read/write, except for the last four registers, which are read-only. Each register is made of an 8-bit-wide volatile memory bit, and their default values are loaded during the power-up sequence or by using the hardware $\overline{\text{RESET}}$ pin. All registers are accessible by the SPI command using the register address.

Table 5-3 shows the user-configuration memory map, and Registers 5-1 to 5-71 show the details of the register bit functions.

Note 1:	All addresses and bit locations that are not included in the following register map table should not be written or modified by the user.
2:	Some registers include factory-controlled bits (FCB). Do not overwrite these bits.

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TABLE 5-3: REGISTER MAP TABLE

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x00	SPI Bit Ordering and ADC Mode Selection	SHUTDOWN 1 = Shutdown	LSb-First 1 = LSb first 0 = MSb first	$\overline{\text{SOFT_RESET}}$ 0 = Soft Reset	STANDBY 1 = Standby	STANDBY 1 = Standby	$\overline{\text{SOFT_RESET}}$ 0 = Soft Reset	LSb-First 1 = LSb first 0 = MSb first	SHUTDOWN 1 = Shutdown	0x24
0x01	Independency Control of Output Data and Clock Divider	EN_DATCLK_IND	FCB<6:0> = 000 1111							0x0F
0x02	Output Data and Clock Rate Control	OUT_DATARATE<3:0>				OUT_CLKRATE<3:0>				0x00
0x04	SPI SDO Timing Control	SDO_TIME	FCB<6:0> = 001 1111							0x9F
0x07	Output Randomizer and WCK Polarity Control	POL_WCK	EN_AUTOCAL_TIMEDLY	FCB<4:0> = 10001					EN_OUT_RANDOM	0x62
0x1E	Auto-Calibration Time Delay Control	AUTOCAL_TIMEDLY<7:0>								0x80
0x52	DLL Control	EN_DUTY	DCLK_PHDLY_DLL<2:0>			EN_DLL_DCLK	EN_DLL	EN_CLK	$\overline{\text{RESET_DLL}}$	0x0A
0x53	Clock Source Selection	FCB<6:4>= 010			CLK_SOURCE	FCB<3:0>= 0101				0x45
0x54	PLL Reference Divider	PLL_REFDIV<7:0>								0x00
0x55	PLL Output and Reference Divider	PLL_OUTDIV<3:0>				FCB<1:0> = 10		PLL_REFDIV<9:8>		0x48
0x56	PLL Prescaler (LSB)	PLL_PRE (LSB)<7:0>								0x78
0x57	PLL Prescaler (MSB)	FCB<3:0> = 0100				PLL_PRE (MSB)<11:8>				0x40
0x58	PLL Charge Pump	FCB<2:0> = 000			PLL_BIAS	PLL_CHAGPUMP<3:0>				0x12
0x59	PLL Enable Control 1	U	FCB<4:3> = 10		EN_PLL_REFDIV	FCB<2:1> = 00		EN_PLL	FCB<0> = 1	0x41
0x5A	PLL Loop Filter Resistor	U	FCB<1:0> = 01		PLL_RES<4:0>					0x2F
0x5B	PLL Loop Filter Cap3	U	FCB<1:0> = 01		PLL_CAP3<4:0>					0x27
0x5C	PLL Loop Filter Cap1	U	FCB<1:0> = 01		PLL_CAP1<4:0>					0x27
0x5D	PLL Loop Filter Cap2	U	FCB<1:0> = 01		PLL_CAP2<4:0>					0x27
0x5F	PLL Enable Control 2	FCB<5:2> = 1111				EN_PLL_OUT	EN_PLL_BIAS	FCB<1:0> = 01		0xF1
0x62	Output Data Format and Output Test Pattern	U	FCB<0> = 0	DATA_FORMAT	OUTPUT_MODE<1:0>		TEST_PATTERNS<2:0>			0x10
0x63	LVDS Output Load and Driver Current Control	FCB<3:0> = 0000				LVDS_LOAD	LVDS_IMODE<2:0>			0x01
0x64	Output Clock Phase Control when Decimation Filter is used	EN_PHDLY	DCLK_PHDLY_DEC<2:0>			FCB<3:0> = 0011				0x03
0x65	LVDS Output Polarity Control	POL_LVDS<5:0>						NO EFFECT<1:0>		0x00
0x66	Digital Offset Correction - Lower Byte	DIG_OFFSET<7:0>								0x00

Legend: U = Unimplemented bit, read as '0'. FCB = Factory-Controlled bits. Do not program. 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Read-only register. Preprogrammed at the factory for internal use.

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TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x67	Digital Offset Correction - Upper Byte	DIG_OFFSET<15:8>								0x00
0x68	OVR and WCK Bit Control	FCB<5:2> = 0010				POL_OVR_WCK	EN_OVR_WCK	FCB<1:0> = 00		0x24
0x6B	PLL Calibration	FCB<6:2> = 00001					PLL_CAL_TRIG	FCB<1:0> = 00		0x08
0x6D	PLL Output and Output Clock Phase	U<1:0>		EN_PLL_CLK	FCB<1> = 0	DCLK_DLY_PLL<2:0>			FCB<0> = 0	0x00
0x74	User-Defined Output Pattern A - Lower Byte	PATTERN A<3:0>				Do not use (Leave these bits as '0000')				0x00
0x75	User-Defined Output Pattern A - Upper Byte	PATTERN A<11:4>								0x00
0x76	User-Defined Output Pattern B - Lower Byte	PATTERN B<3:0>				Do not use (Leave these bits as '0000')				0x00
0x77	User-Defined Output Pattern B - Upper Byte	PATTERN B<11:4>								0x00
0x78	Noise-Shaping Requantizer (NSR) Filter	NSR_RESET	NSR <6:0>							0x00
0x79	I/Q-Channel DSPP Control	EN_DSPP_I/Q	FCB<6:0> = 000 0000							0x00
0x7A	FIR_A0 Bit and Noise-Shaping Requantizer (NSR) Filter Selection	FCB<4> = 0	FIR_A<0>	FCB<3:0> = 0000				EN_NSR_11	EN_NSR_12	0x00
0x7B	FIR A Filter	FIR_A<8:1>								0x00
0x7C	FIR B Filter	FIR_B<7:0>								0x00
0x80	Digital Down-Converter Control 1	FCB<0> = 0	HBFILTER_A	EN_NCO	EN_AMPDITH	EN_PHSDITH	EN_LFSR	EN_DDC_FS/8	EN_DDC1	0x00
0x81	Digital Down-Converter Control 2	FCB<5> = 0	EN_DDC2	GAIN_HBF_DDC	FCB<4:0> = 00000					0x00
0x82	Numerically Controlled Oscillator (NCO) Tuning - Lower Byte	NCO_TUNE<7:0>								0x00
0x83	Numerically Controlled Oscillator (NCO) Tuning - Middle-Lower Byte	NCO_TUNE<15:8>								0x00
0x84	Numerically Controlled Oscillator (NCO) Tuning - Middle-Upper Byte	NCO_TUNE<23:16>								0x00
0x85	Numerically Controlled Oscillator (NCO) Tuning - Upper Byte	NCO_TUNE<31:24>								0x00
0x86	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0>								0x00

Legend: U = Unimplemented bit, read as '0'. FCB = Factory-Controlled bits. Do not program. 1 = bit is set 0 = bit is cleared x = bit is unknown
Note 1: Read-only register. Preprogrammed at the factory for internal use.

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TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x87	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8>								0x00
0x88	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x89	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x8A	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x8B	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x8C	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x8D	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x8E	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x8F	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x90	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x91	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x92	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x93	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x94	NCO Phase Offset in DDC Mode - Lower Byte	NCO_PHASE<7:0> - Repeat of Address 0x86								0x00
0x95	NCO Phase Offset in DDC Mode - Upper Byte	NCO_PHASE<15:8> - Repeat of Address 0x87								0x00
0x96	Digital Gain Control	DIG_GAIN<7:0>								0x3C
0x97	Digital Gain Control	DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C
0x98		DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C
0x99		DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C
0x9A		DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C
0x9B		DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C
0x9C		DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C
0x9D		DIG_GAIN<7:0> - Repeat of Address 0x96								0x3C

Legend: U = Unimplemented bit, read as '0'. FCB = Factory-Controlled bits. Do not program. 1 = bit is set 0 = bit is cleared x = bit is unknown
Note 1: Read-only register. Preprogrammed at the factory for internal use.

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TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0xC0	Calibration Status Indication (Read only)	ADC_CAL_STAT	FCB<6:0> = 000-0000							–
0xD1	PLL Calibration Status and PLL Drift Status Indication (Read only)	FCB<4:3> = xx		PLL_CAL_STAT	FCB<2:1> = xx		PLL_VCOL_STAT	PLL_VCOH_STAT	FCB<0> = x	–
0x15C	CHIP ID - Lower Byte[1] (Read only)	CHIP_ID<7:0>								–
0x15D	CHIP ID - Upper Byte[1] (Read only)	CHIP_ID<15:8>								–

Legend: U = Unimplemented bit, read as '0'. FCB = Factory-Controlled bits. Do not program. 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Read-only register. Preprogrammed at the factory for internal use.

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REGISTER 5-1: ADDRESS 0X00 – SPI BIT ORDERING AND ADC MODE SELECTION(1)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
SHUTDOWN	LSb_FIRST	$\overline{\text{SOFT_RESET}}$	STANDBY	STANDBY	$\overline{\text{SOFT_RESET}}$	LSb_FIRST	SHUTDOWN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SHUTDOWN**: Shutdown mode setting for power saving(2)
- 1 = ADC in Shutdown mode
- 0 = Not in Shutdown mode **(Default)**

bit 6 **LSB_FIRST**: Select SPI communication bit order
- 1 = Start SPI communication with LSb first
- 0 = Start SPI communication with MSb first **(Default)**

bit 5 **$\overline{\text{SOFT_RESET}}$:** Soft Reset control bit(3)
- 1 = Not in Soft Reset mode **(Default)**
- 0 = ADC in Soft Reset

bit 4 **STANDBY:** Send the device into a power-saving Standby mode(4)
- 1 = ADC in Standby mode
- 0 = Not in Standby mode **(Default)**

bit 3 **STANDBY:** Send the device into a power-saving Standby mode(4)
- 1 = ADC in Standby mode
- 0 = Not in Standby mode **(Default)**

bit 2 **$\overline{\text{SOFT_RESET}}$:** Soft Reset control bit(3)
- 1 = Not in Soft Reset mode **(Default)**
- 0 = ADC in Soft Reset

bit 1 **LSB_FIRST**: Select SPI communication bit order
- 1 = Start SPI communication with LSb first
- 0 = Start SPI communication with MSb first **(Default)**

bit 0 **SHUTDOWN**: Shutdown mode setting for power-saving(2)
- 1 = ADC in Shutdown mode
- 0 = Not in Shutdown mode **(Default)**

Note 1: Upper and lower nibble are mirrored, which makes the MSb- or LSb-first mode interchangeable. The lower nibble (bit <3:0>) has a higher priority when the mirrored bits have different values.

2: During Shutdown mode, most of the internal circuits including the reference and clock are turned-off except for the SPI interface. When exiting from shutdown (changing from '1' to '0'), executing the device Soft Reset simultaneously is highly recommended for a fast recalibration of the ADC. The internal user registers are not affected.

3: This bit forces the device into Soft Reset mode, which initializes the internal calibration registers to their initial default states. The user-registers are not affected. When exiting Soft Reset mode (changing from '0' to '1'), the device performs an automatic device calibration including PLL calibration if PLL is enabled. DLL is reset if enabled. During Soft Reset, the device has the following states:
- no ADC output
- no change in power-on condition of internal reference
- most of the internal clocks are not distributed.
- power consumption: (a) digital section - negligible, (b) analog section - no change.

4: During Standby mode, most of the internal circuits are turned off except for the reference, clock and SPI interface. When exiting from Standby mode (changing from '1' to '0') after an extended amount of time, executing Soft Reset simultaneously is highly recommended. The internal user registers are not affected.

REGISTER 5-2: ADDRESS 0X01 – INDEPENDENCY CONTROL OF OUTPUT DATA AND CLOCK DIVIDER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
EN_DATCLK_IND	FCB<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN_DATCLK_IND:** Enable data and clock divider independently(1)
1 = Enabled
0 = Disabled **(Default)**

bit 6-0 **FCB<6:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

Note 1: EN_DATCLK_IND = 1 enables OUT_CLKRATE<3:0> settings in Address 0x02 (Register 5-3).

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REGISTER 5-3: ADDRESS 0X02 – OUTPUT DATA AND CLOCK RATE CONTROL(Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUT_DATARATE<3:0>				OUT_CLKRATE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **OUT_DATARATE<3:0>**: Output data rate control bits
1111 = Output data is all 0's
1110 = Output data is all 0's
1101 = Output data is all 0's
1100 = Internal test only(2)
1011 = Internal test only(2)
1010 = Internal test only(2)
1001 = Full speed divided by 512
1000 = Full speed divided by 256
0111 = Full speed divided by 128
0110 = Full speed divided by 64
0101 = Full speed divided by 32
0100 = Full speed divided by 16
0011 = Full speed divided by 8
0010 = Full speed divided by 4
0001 = Full speed divided by 2
0000 = Full speed rate **(Default)**

bit 3-0 **OUT_CLKRATE<3:0>**: Output clock rate control bits(3, 4)
1111 = Full speed rate
1110 = No clock output
1101 = No clock output
1100 = No clock output
1011 = No clock output
1010 = No clock output
1001 = Full speed divided by 512
1000 = Full speed divided by 256
0111 = Full speed divided by 128
0110 = Full speed divided by 64
0101 = Full speed divided by 32
0100 = Full speed divided by 16
0011 = Full speed divided by 8
0010 = Full speed divided by 4
0001 = Full speed divided by 2
0000 = No clock output **(Default)**

Note 1: This register should be used when the decimation filter selection option (see Addresses 0x7B and 0x7C - Registers 5-36 and 5-37) or digital down-conversion (DDC) option (see Address 0x80 - Register 5-38) is used.
2: 1100 – 1010: Do not reprogram. These settings are used for the internal test only. If these bits are reprogrammed with different settings, the outputs will be in an undefined state.
3: Bits <3:0> become active if EN_DATCLK_IND = 1 in Address 0x01 (Register 5-2).
4: When no clock output is selected (Bits 1110 – 1010): clock output is not available at the DCLK+/DCLK- pins.

REGISTER 5-4: ADDRESS 0X04 – SPI SDO OUTPUT TIMING CONTROL

R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SDO_TIME	FCB<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SDO_TIME:** SPI SDO output timing control bit
1 = SDO output at the falling edge of clock **(Default)**
0 = SDO output at the rising edge of clock

bit 6-0 **FCB<6:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

REGISTER 5-5: ADDRESS 0X07 – OUTPUT RANDOMIZER AND WCK POLARITY CONTROL

R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
POL_WCK	EN_AUTOCAL_TIMEDLY	FCB<4:0>					EN_OUT_RANDOM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **POL_WCK**: WCK polarity control bit in DDC mode(1)
1 = Inverted
0 = Not inverted **(Default)**

bit 6 **EN_AUTOCAL_TIMEDLY**: Auto-calibration starter time delay counter control bit(2)
1 = Enabled **(Default)**
0 = Disabled

bit 5-1 **FCB<4:0>**: Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 0 **EN_OUT_RANDOM**: Output randomizer control bit
1 = Enabled: ADC data output is randomized
0 = Disabled **(Default)**

Note 1: Applicable in the MCP37D10-200 only. See Address 0x68 (Register 5-26) for OVR/WCK pair control.
2: This bit enables the AUTOCAL_TIMEDLY<7:0> settings. See Address 0x1E (Register 5-6).

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REGISTER 5-6: ADDRESS 0X1E – AUTOCAL TIME DELAY CONTROL(1)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AUTOCAL_TIMEDLY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **AUTOCAL_TIMEDLY<7:0>:** Auto-calibration start time delay control bits
1111-1111 = Maximum value
• • •
1000-0000 = **(Default)**
• • •
0000-0000 = Minimum value

Note 1: EN_AUTOCAL_TIMEDLY in Address 0x07 (Register 5-5) enables this register setting. This register controls the time delay before the auto-calibration starts. The value increases linearly with the bit settings, from minimum to maximum values.

REGISTER 5-7: ADDRESS 0X52 – DLL CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
EN_DUTY	DCLK_PHDLY_DLL<2:0>			EN_DLL_DCLK	EN_DLL	EN_CLK	$\overline{\text{RESET_DLL}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN_DUTY:** Enable DLL circuit for duty cycle correction (DCC) of input clock(1)
1 = Correction is ON
0 = Correction is OFF **(Default)**

bit 6-4 **DCLK_PHDLY_DLL<2:0>:** Select the phase delay of the digital clock output when using DLL(2)
111 = +315°phase-shifted from default
110 = +270° phase-shifted from default
• • •
010 = +90° phase-shifted from default
001 = +45° phase-shifted from default
000 = **(Default)**

bit 3 **EN_DLL_DCLK:** Enable DLL digital clock output
1 = Enabled **(Default)**
0 = Disabled: DLL digital clock is turned off. ADC output is not available when DLL is used.

bit 2 **EN_DLL:** Enable DLL circuitry to provide a selectable phase clock to digital output clock.
1 = Enabled
0 = Disabled. DLL block is disabled **(Default)**

bit 1 **EN_CLK:** Enable clock input buffer
1 = Enabled **(Default).**
0 = Disabled. No clock is available to the internal circuits, ADC output is not available.

bit 0 **$\overline{\text{RESET_DLL}}$:** DLL circuit reset control(3)
1 = DLL is active
0 = DLL circuit is held in reset **(Default)**

Note 1: Enable the DLL circuitry for the duty cycle correction.
2: These bits have an effect only if EN_PHDLY = 1 and decimation is not used.
3: DLL reset control procedure: Set this bit to '0' (reset) and then to '1'.

REGISTER 5-8: ADDRESS 0X53 – CLOCK SOURCE SELECTION

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
FCB<6:4>			CLK_SOURCE	FCB<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **FCB<6:4>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4 **CLK_SOURCE:** Select internal timing source
1 = PLL output is selected as timing source
0 = External clock input is selected as timing source **(Default)**

bit 3-0 **FCB<3:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

REGISTER 5-9: ADDRESS 0X54 – PLL REFERENCE DIVIDER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLL_REFDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PLL_REFDIV<7:0>:** PLL Reference clock divider control bits(1)
1111-1111 = PLL reference divided by 255 (if PLL_REFDIV<9:8> = 00)
1111-1110 = PLL reference divided by 254 (if PLL_REFDIV<9:8> = 00)
• • •
0000-0011 = PLL reference divided by 3 (if PLL_REFDIV<9:8> = 00)
0000-0010 = **Do not use (No effect)**
0000-0001 = PLL reference divided by 1 (if PLL_REFDIV<9:8> = 00)
0000-0000 = PLL reference not divided (if PLL_REFDIV<9:8> = 00) **(Default)**

Note 1: PLL_REFDIV is a 10-bit-wide setting. See Address 0x55 (Register 5-10) for the upper two bits and **Table 4-5** for PLL_REFDIV<9:0> bit settings. This setting controls the clock division ratio of the PLL reference clock (external clock input at the clock input pin) before the PLL phase-frequency detector circuitry. Note that the divider value of 2 is not supported. EN_PLL_REFDIV in Address 0x59 (Register 5-14) must be set.

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REGISTER 5-10: ADDRESS 0X55 – PLL OUTPUT AND REFERENCE DIVIDER

R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
PLL_OUTDIV<3:0>				FCB<1:0>		PLL_REFDIV<9:8>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **PLL_OUTDIV<3:0>:** PLL output divider control bits(1)
1111 = PLL output divided by 15
1110 = PLL output divided by 14
• • •
0100 = PLL output divided by 4 **(Default)**
0011 = PLL output divided by 3
0010 = PLL output divided by 2
0001 = PLL output divided by 1
0000 = PLL output not divided

bit 3-2 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 1-0 **PLL_REFDIV<9:8>:** Upper two MSb bits of PLL_REFDIV<9:0>(2)
00 = see Table 5-4. **(Default)**

Note 1: PLL_OUTDIV<3:0> controls the PLL output clock divider: VCO output is divided by the PLL_OUTDIV<3:0> setting.

2: See Address 0x54 (Register 5-9) and Table 5-4 for PLL_REFDIV<9:0> bit settings. EN_PLL_REFDIV in Address 0x59 (Register 5-14) must be set.

TABLE 5-4: Example – PLL Reference Divider Bit Settings Vs. PLL Reference Input Frequency

PLL_REFDIV<9:0>	PLL Reference Frequency
11-1111-1111	Reference frequency divided by 1023
11-1111-1110	Reference frequency divided by 1022
–	—
00-0000-0011	Reference frequency divided by 3
00-0000-0010	Do not use (Not supported)
00-0000-0001	Reference frequency divided by 1
00-0000-0000	Reference frequency divided by 1

REGISTER 5-11: ADDRESS 0X56 – PLL PRESCALER (LSB)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PLL_PRE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PLL_PRE<7:0>:** PLL prescaler selection(1)
1111-1111 = VCO clock divided by 255 (if PLL_PRE<11:8> = 0000)
• • •
0111-1000 = VCO clock divided by 120 (if PLL_PRE<11:8> = 0000) **(Default)**
• • •
0000-0010 = VCO clock divided by 2 (if PLL_PRE<11:8> = 0000)
0000-0001 = VCO clock divided by 1 (if PLL_PRE<11:8> = 0000)
0000-0000 = VCO clock not divided (if PLL_PRE<11:8> = 0000)

Note 1: PLL_PRE is a 12-bit-wide setting. The upper four bits (PLL_PRE<11:8>) are defined in Address 0x57. See Table 4-5 for the PLL_PRE<11:0> bit settings. The PLL Prescaler is used to divide down the VCO output clock in the PLL phase-frequency detector loop circuit.

REGISTER 5-12: ADDRESS 0X57 – PLL PRESCALER (MSB)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FCB<3:0>				PLL_PRE<11:8>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<3:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 3-0 **PLL_PRE<11:8>:** PLL prescaler selection(1)
1111 = 2^{12} - 1 (max), if PLL_PRE<7:0> = 0xFF
• • •
0000 = **(Default)**

Note 1: PLL_PRE is a 12-bit-wide setting. See the lower eight bit settings (PLL_PRE<7:0>) in Address 0x56 (Register 5-11). See Table 5-5 for the PLL_PRE<11:0> bit settings for PLL feedback frequency.

TABLE 5-5: Example: PLL Prescaler Bit Settings and PLL Feedback Frequency

PLL_PRE<11:0>	PLL Feedback Frequency
1111-1111-1111	VCO clock divided by 4095 (2^{12} - 1)
1111-1111-1110	VCO clock divided by 4094 (2^{12} - 2)
–	—
0000-0000-0011	VCO clock divided by 3
0000-0000-0010	VCO clock divided by 2
0000-0000-0001	VCO clock divided by 1
0000-0000-0000	VCO clock divided by 1

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REGISTER 5-13: ADDRESS 0X58 – PLL CHARGE PUMP

R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
FCB<2:0>:			PLL_BIAS	PLL_CHAGPUMP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **FCB<2:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4 **PLL_BIAS:** PLL charge pump bias source selection bit
1 = Self-biasing coming from AV_{DD} **(Default)**
0 = Bandgap voltage from the reference generator (1.2V)

bit 3-0 **PLL_CHAGPUMP<3:0>:** PLL charge pump bias current control bits(1)
1111 = Maximum current
• • •
0010 = **(Default)**
• • •
0000 = Minimum current

Note 1: PLL_CHAGPUMP<3:0> bits should be set based on the phase detector comparison frequency. The bias current amplitude increases linearly with increasing the bit setting values. The increase is from approximately 25 µA to 375 µA, 25 µA per step. See **Section 4.5.2.1 "PLL Output Frequency and Output Control Parameters"** for more details of the PLL block.

REGISTER 5-14: ADDRESS 0X59 – PLL ENABLE CONTROL 1

U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	FCB<4:3>		EN_PLL_REFDIV	FCB<2:1>		EN_PLL	FCB<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<4:3>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4 **EN_PLL_REFDIV:** Enable PLL Reference Divider (PLL_REFDIV<9:0>).
1 = Enabled
0 = Reference divider is bypassed **(Default)**

bit 3-2 **FCB<2:1>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 1 **EN_PLL:** Master enable bit for PLL circuit.
1 = Enabled
0 = Disabled **(Default)**

bit 0 **FCB<0>:** Factory-Controlled bit. This is not for the user. Do not change default setting.

REGISTER 5-15: ADDRESS 0X5A – PLL LOOP FILTER RESISTOR

U-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_RES<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4-0 **PLL_RES<4:0>:** Resistor value selection bits for PLL loop filter(1)

11111 = Maximum value
• • •
01111= **(Default)**
• • •
00000 = Minimum value

Note 1: PLL_RES<4:0> bits should be set based on the phase detector comparison frequency. The resistor value increases linearly with the bit settings, from minimum to maximum values. See the PLL loop filter section in **Section 4.5.2.1 "PLL Output Frequency and Output Control Parameters"**.

REGISTER 5-16: ADDRESS 0X5B – PLL LOOP FILTER CAP3

U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_CAP3<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4-0 **PLL_CAP3<4:0>:** Capacitor 3 value selection bits for PLL loop filter(1)

11111= Maximum value
• • •
00111= **(Default)**
• • •
00000= Minimum value

Note 1: This capacitor is in series with the shunt resistor, which is set by PLL_RES<4:0> bits. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

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REGISTER 5-17: ADDRESS 0X5C – PLL LOOP FILTER CAP1

U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_CAP1<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4-0 **PLL_CAP1<4:0>:** Capacitor 1 value selection bits for PLL loop filter(1)

11111= Maximum value

• • •

00111= **(Default)**

• • •

00000= Minimum value

Note 1: This capacitor is located between the charge pump output and ground, and in parallel with the shunt resistor which is defined by the PLL_RES<4:0>. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-18: ADDRESS 0X5D – PLL LOOP FILTER CAP2

U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_CAP2<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 4-0 **PLL_CAP2<4:0>:** Capacitor 2 value selection bits for PLL loop filter(1)

11111= Maximum value

• • •

00111= **(Default)**

• • •

00000= Minimum value

Note 1: This capacitor is located between the charge pump output and ground, and in parallel with CAP1 which is defined by the PLL_CAP1<4:0>. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-19: ADDRESS 0X5F – PLL ENABLE CONTROL 2(1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
FCB<5:2>				EN_PLL_OUT	EN_PLL_BIAS	FCB<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<5:2>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 3 **EN_PLL_OUT:** Enable PLL output.
1 = Enabled
0 = Disabled **(Default)**

bit 2 **EN_PLL_BIAS:** Enable PLL bias
1 = Enabled
0 = Disabled **(Default)**

bit 1-0 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

Note 1: To enable PLL output, EN_PLL_OUT, EN_PLL_BIAS and EN_PLL in Address 0x59 (Register 5-14) must be set.

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REGISTER 5-20: ADDRESS 0X62 – OUTPUT DATA FORMAT AND OUTPUT TEST PATTERN

U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
—	FCB<0>	DATA_FORMAT	OUTPUT_MODE<1:0>		TEST_PATTERNS<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6 **FCB<0>:** Factory-controlled bit. This is not for the user. Do not change default setting.

bit 5 **DATA_FORMAT**: Output data format selection
1 = Offset binary (unsigned)
0 = Two's complement **(Default)**

bit 4-3 **OUTPUT_MODE<1:0>**: Output mode selection(1)
11 = Do not use. Output is undefined
10 = Select DDR LVDS output mode with even bit first(2) **(Default)**
01 = Select CMOS output mode
00 = Output disabled

bit 2-0 **TEST_PATTERNS<2:0>**: Test output data pattern selection(3)
111 = Output data is pseudo-random number (PN) sequence(4)
110 = Sync Pattern for LVDS output
Output: '11111111 0000'
101 = Alternating Sequence for LVDS mode
Output: '01010101 1010'
100 = Alternating Sequence for CMOS mode
Output: '11111111 1111' alternating with '00000000 0000'
011 = Alternating Sequence for CMOS
Output: '01010101 0101' alternating with '10101010 1010'
010 = Ramp Pattern: Output (Q0) is incremented by1 LSb per 64 clock cycles
001 = Double Custom Patterns
Output: Alternating custom pattern A (see Addresses 0X74 - 0X75 – Registers 5-29 – 5-30) and custom pattern B (see Address 0X76 - 0X77 – Registers 5-31 – 5-32)(5)
000 = Normal Operation. Output: ADC data **(Default)**

Note 1: See Figures 2-1 – 2-2 for the timing diagrams.
2: Rising edge: Q10, Q8, Q6, Q4, Q2, Q0.
Falling edge: Q11, Q9, Q7, Q5, Q3, Q1.
3: See **Section 4.9.12 "Output Test Patterns"** for more details.
(a) In LVDS mode: only the active pins (per register settings) are active. Inactive output pins are High Z state.
(b) In CMOS mode: all data output pins (Q11-Q0), output test pins (TP, TP1, TP2), OVR and WCK pins are active, even if they are disabled by register settings. Since the output test pins (TP, TP1, TP2) can toggle during this test, the output test pins can draw extra current if they are connected to the supply pin or ground. To avoid the extra current draws, always leave the test pins floating (not connected).
4: Pseudo-random number (PN) code is generated by the linear feedback shift register (LFSR).
See **Section 4.9.12.1 "Pseudo-Random Number (PN) Sequence Output"** for more details.
5: Pattern A<11:0> and B<11:0> are applied to Q<11:0>. Q11 = OVR, Q10 = WCK.

REGISTER 5-21: ADDRESS 0X63 – LVDS OUTPUT LOAD AND DRIVER CURRENT CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
FCB<3:0>				LVDS_LOAD	LVDS_IMODE<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<3:0>**: Factory-controlled bits. This is not for the user. Do not change default settings.

bit 3 **LVDS_LOAD**: Enable internal LVDS load termination
1 = Enabled
0 = Disabled **(Default)**

bit 2-0 **LVDS_IMODE<2:0>**: LVDS driver current control bits
111 = 7.2 mA
011 = 5.4 mA
001 = 3.5 mA **(Default)**
000 = 1.8 mA
Do not use the following settings(1):
110, 101, 100, 010

Note 1: These settings can result in unknown outputs currents.

REGISTER 5-22: ADDRESS 0X64 – OUTPUT CLOCK PHASE CONTROL WHEN DECIMATION FILTER IS USED

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EN_PHDLY	DCLK_PHDLY_DEC<2:0>			FCB<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN_PHDLY:** Enable digital output clock phase delay control when DLL or decimation filter is used.
1 = Enabled
0 = Disabled **(Default)**

bit 6-4 **DCLK_PHDLY_DEC<2:0>**: Digital output clock phase delay control when decimation filter is used(1)
111 = +315° phase-shifted from default(2)
110 = +270° phase-shifted from default
101 = +225° phase-shifted from default(2)
100 = +180° phase-shifted from default
011 = +135° phase-shifted from default(2)
010 = +90° phase-shifted from default
001 = +45° phase-shifted from default(2)
000 = **Default**(3)

bit 3-0 **FCB<3:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

Note 1: These bits have an effect only if EN_PHDLY = 1. See Address 0x52 (Register 5-7) for the same feature when DLL is used.
2: Only available when the decimation filter setting is greater than 2. When FIR_A/B <8:1> = 0's (default) and FIR_A<6> = 0, only 4-phase shifts are available (+45°, +135°, +225°, +315°) from default. See Addresses 0x7A, 0x7B and 0x7C (Registers 5-35 –5-37). See address 0x6D and 0x52 for DCLK (Registers 5-28 and5-7) phase shift for other modes.
3: The phase delay for all other settings is referenced to this default phase.

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REGISTER 5-23: ADDRESS 0X65 – LVDS OUTPUT POLARITY CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL_LVDS<5:0>						NO EFFECT<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **POL_LVDS<5:0>:** Control polarity of LVDS data pairs **(Q_{5+}/Q_{5-} – Q_{0+}/Q_{0-})**
111111 = Invert all LVDS pairs
111110 = Invert all LVDS pairs except the LSb pair
• • •
100000 = Invert MSb LVDS pair
• • •
000001 = Invert LSb LVDS pair
000000 = No inversion of LVDS bit pairs (**Default)**

bit 1-0 **NO EFFECT<1:0>:** No effect bits.

REGISTER 5-24: ADDRESS 0X66 – DIGITAL OFFSET CORRECTION (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIG_OFFSET <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_OFFSET <7:0>:** Lower byte of DIG_OFFSET<15:0>(1)
0000-0000 = **Default**

Note 1: Offset is added to the ADC output. Setting is two's complement using two combined registers (16 bits wide).
- 0 LSb if DIG_OFFSET<15:0>=0x0000
- Step size: 0.25 LSb per each bit setting
- Setting Range: (-2^{15} to 2^{15} - 1) × 0.25 LSb or (-32768 to +32767) × 0.25 LSb

REGISTER 5-25: ADDRESS 0X67 – DIGITAL OFFSET CORRECTION (UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIG_OFFSET<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_OFFSET <15:8>:** Upper byte of DIG_OFFSET<15:0>(1)
0000-0000 = **Default**

Note 1: See **Note 1** in Address 0x66 (Register 5-24).

REGISTER 5-26: ADDRESS 0X68 – OVR AND WCK BIT CONTROL

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
FCB<5:2>				POL_OVR_WCK	EN_OVR_WCK	FCB<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<5:2>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 3 **POL_OVR_WCK**: Polarity control for OVR and WCK bit pair in LVDS mode
1 = Inverted
0 = Not inverted **(Default)**

bit 2 **EN_OVR_WCK**: Enable OVR and WCK output bit pair
1 = Enabled **(Default)**
0 = Disabled

bit 1-0 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

REGISTER 5-27: ADDRESS 0X6B – PLL CALIBRATION

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
FCB<6:2>					PLL_CAL_TRIG	FCB<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **FCB<6:2>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 2 **PLL_CAL_TRIG**: Manually force recalibration of the PLL at the state of bit transition(1)
Toggle from '1' to '0', or '0' to '1' = Start PLL calibration

bit 1-0 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

Note 1: See PLL_CAL_STAT in Address 0xD1 (Register 5-69) for calibration status indication.

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REGISTER 5-28: ADDRESS 0X6D – PLL OUTPUT AND OUTPUT CLOCK PHASE(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		EN_PLL_CLK	FCB<1>	DCLK_DLY_PLL<2:0>			FCB<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Not used

bit 5 **EN_PLL_CLK:** Enable PLL output clock
1 = PLL output clock is enabled to the ADC core
0 = PLL clock output is disabled **(Default)**

bit 4 **FCB<1>:** Factory-Controlled bit. This is not for the user. Do not change default setting.

bit 3-1 **DCLK_DLY_PLL<2:0>:** Output clock is delayed by the number of VCO clock cycles from the nominal PLL output(2)
111 = Delay of 15 cycles
110 = Delay of 14 cycles
• • •
001 = Delay of one cycle
000 = No delay **(Default)**

bit 0 **FCB<0>:** Factory-Controlled bit. This is not for the user. Do not change default setting.

Note 1: This register has effect only when the PLL clock is selected by CLK_SOURCE bit in Address 0x53 (Register 5-8) and PLL circuit is enabled by EN_PLL bit in Address 0x59 (Register 5-14).
2: This bit setting enables the output clock phase delay. This phase delay control option is applicable when PLL is used as the clock source and decimation is not used.

REGISTER 5-29: ADDRESS 0X74 – USER-DEFINED OUTPUT PATTERN A (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_A<3:0>				**Do not use (Leave these bits as '0000')**			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **PATTERN_A<3:0>:** Lower nibble of PATTERN_A<11:0>(1)

bit 3-0 **Do not use:** Leave these bits to default settings ('0000')(2)

Note 1: See PATTERN_A<11:4> in Address 0x75 (Register 5-30) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).
2: The output from these bit settings is on "Unused Output Pattern Test Pins", which are recommended to not be connected to the host device. Therefore, the effect of these bit settings is not monitored. Leave these bits at default settings ('0000') all the time.

REGISTER 5-30: ADDRESS 0X75 – USER-DEFINED OUTPUT PATTERN A (UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_A<11:4>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PATTERN_A<11:4>:** Upper byte of PATTERN_A<11:0>(1)

Note 1: See PATTERN_A<3:0> in Address 0x74 (Register 5-29) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

REGISTER 5-31: ADDRESS 0X76 – USER-DEFINED OUTPUT PATTERN B (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_B<3:0>				**Do not use (Leave these bits as '0000')**			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **PATTERN_B<3:0>:** Lower nibble of PATTERN_B<11:0>(1)

bit 3-0 **Do not use:** Leave these bits at default settings ('0000')(2)

Note 1: See PATTERN_B<11:4> in Address 0x77 (Register 5-32) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

2: The output from these bit settings is on "Unused Output Pattern Test Pins", which are recommended to not be connected to the host device. Therefore, the effect of these bit settings is not monitored. Leave these bits at default settings ('0000') all the time.

REGISTER 5-32: ADDRESS 0X77 – USER-DEFINED OUTPUT PATTERN B (UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_B<11:4>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PATTERN_B<11:4>:** Upper byte of PATTERN_B<15:0>(1)

Note 1: See PATTERN_B<3:0> in Address 0x76 (Register 5-31) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

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REGISTER 5-33: ADDRESS 0X78 – NOISE-SHAPING REQUANTIZER (NSR) FILTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSR_RESET	NSR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **NSR_RESET:** Toggling this bit causes a reset of the NSR filter.
- Toggle from '1' to '0' or from '0' to '1' = Reset of NSR filter.
- Otherwise = No effect **(Default)**

bit 6-0 **NSR<6:0>:** NSR filter setting. See Table 4-10 T and Table 4-11 for the NSR filter settings.

REGISTER 5-34: ADDRESS 0X79 – I/Q CHANNEL DIGITAL SIGNAL POST-PROCESSING CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EN_DSPP_I/Q	FCB<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EN_DSPP_I/Q:** Enable all digital signal post-processing functions for I/Q-channel operation.
1 = Enabled
0 = Disabled **(Default)**

bit 6-0 **FCB<6:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

REGISTER 5-35: ADDRESS 0X7A – FIR_A0 BIT AND NOISE-SHAPING REQUANTIZER (NSR) SELECTION

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FCB<4>	FIR_A<0>	FCB<3:0>				EN_NSR_11	EN_NSR_12
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FCB<4>:** Factory-Controlled bit. This is not for the user. Do not change default setting.

bit 6 **FIR_A<0>:** Enable the first 2x decimation (Stage 1A in FIR A)(1)
1 = Enabled
0 = Disabled **(Default)**

bit 5-2 **FCB<3:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

bit 1 **EN_NSR_11:** Enable 11-bit noise-shaping requantizer
1 = Enabled
0 = Disabled **(Default)**

bit 0 **EN_NSR_12:** Enable 12-bit noise-shaping requantizer
1 = Enabled
0 = Disabled **(Default)**

Note 1: Set FIR_A<0> = 0 for I and Q channels in DDC mode (MCP37D10-200). See Address 0x7B (Register 5-36) for FIR_A<8:1>.

REGISTER 5-36: ADDRESS 0X7B – FIR A FILTER(1, 4)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIR_A<8:1>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **FIR_A<8:1>:** Decimation Filter FIR A settings(2)

Normal Decimation Operation:

FIR_A<8:0> =

1-1111-1111 = Enabled stage 1 - 9 filters (decimation rate: 512)
0-1111-1111 = Enabled stage 1 - 8 filters
0-0111-1111 = Enabled stage 1 - 7 filters
0-0011-1111 = Enabled stage 1 - 6 filters
0-0001-1111 = Enabled stage 1 - 5 filters
0-0000-1111 = Enabled stage 1 - 4 filters
0-0000-0111 = Enabled stage 1 - 3 filters (decimation rate = 8)
0-0000-0011 = Enabled stage 1 - 2 filters (decimation rate = 4)
0-0000-0001 = Enabled stage 1 filter (decimation rate = 2)
0-0000-0000 = Disabled all FIR A filters. **(Default)**

In-Phase (I) Data Channel in DDC Mode (MCP37D10-200):(3)

FIR_A<8:0> =

1-1111-1100 = Enabled stage 3 - 9 filters (decimation rate: 128)
0-1111-1100 = Enabled stage 3 - 8 filters
0-0111-1100 = Enabled stage 3 - 7 filters
0-0011-1100 = Enabled stage 3 - 6 filters
0-0001-1100 = Enabled stage 3 - 5 filters
0-0000-1100 = Enabled stage 3 - 4 filters
0-0000-0100 = Enabled stage 3 filter (decimation rate = 2)
0-0000-0000 = Disabled all FIR A filters. **(Default)**

Note 1: The register values are thermometer encoded.

2: FIR_A<0> is placed in Address 0x7A (Register 5-35).

3: In I and Q channel operation, it starts with the 3rd stage filter.

4: SNR is improved by approximately 2.5 dB per each filter stage, but output data rate is reduced by a factor of 2 per stage. The data and clock rates in Address 0X02 (Register 5-3) need to be updated accordingly when this register is updated. Address 0x64 (Register 5-22) setting is also affected. The maximum decimation factor is 512, and 128 for the I and Q channel operation in DDC mode (MCP37D10).

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REGISTER 5-37: ADDRESS 0X7C – FIR B FILTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIR_B<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **FIR_B<7:0>:**Decimation Filter FIR B settings for Quadrature (Q) data channel
1111-1111 = Enabled stage 3 - 9 filters (decimation rate: 128)
0111-1111 = Enabled stage 3 - 8 filters
0011-1111 = Enabled stage 3 - 7 filters
0001-1111 = Enabled stage 3 - 6 filters
0000-1111 = Enabled stage 3 - 5 filters
0000-0111 = Enabled stage 3 - 4 filters
0000-0011 = Enabled stage 3 filter (decimation rate = 2)
0000-0001 = No effect
0000-0000 = Disabled all FIR B filters. **(Default)**

Note 1: This register is used only for Q data channel in DDC mode (MCP37D10-200). The register values are thermometer encoded.

REGISTER 5-38: ADDRESS 0X80 – DIGITAL DOWN-CONVERTER CONTROL 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FCB<0>	HBFILTER_A	EN_NCO	EN_AMPDITH	EN_PHSDITH	EN_LFSR	EN_DDC_FS/8	EN_DDC1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FCB<0>:** Factory-Controlled bit. This is not for the user. Do not change default setting.

bit 6 **HBFILTER_A:** Select half-bandwidth filter at DDC output of channel A(1)
1 = Select High-Pass filter at DDC output
0 = Select Low-Pass filter at DDC output **(Default)**

bit 5 **EN_NCO:** Enable NCO of DDC1
1 = Enabled
0 = Disabled **(Default)**

bit 4 **EN_AMPDITH:** Enable amplitude dithering for NCO(2, 3)
1 = Enabled
0 = Disabled **(Default)**

bit 3 **EN_PHSDITH:** Enable phase dithering for NCO(2, 3)
1 = Enabled
0 = Disabled **(Default)**

bit 2 **EN_LFSR:** Enable linear feedback shift register (LFSR) for amplitude and phase dithering for NCO
1 = Enabled
0 = Disabled **(Default)**

bit 1 **EN_DDC_FS/8:** Enable NCO for the DDC2 to center the DDC output signal to be around $f_S/8/DER$(4)
1 = Enabled
0 = Disabled **(Default)**

bit 0 **EN_DDC1:** Enable digital down-converter 1 (DDC1)
1 = Enabled(5)
0 = Disabled **(Default)**

Note 1: This filter includes a decimation of 2.
2: This requires the LFSR to be enabled: <EN_LFSR>=1
3: EN_AMPDITH = 1 and EN_PHSDITH = 1 are recommended for the best performance.
4: DER is the decimation rate defined by FIR A or FIR B filter. If up-converter is disabled, output is I/Q data.
5: DDC and NCO are enabled. For DDC function, bits 0, 2 and 5 need to be enabled together.

REGISTER 5-39: ADDRESS 0X81 – DIGITAL DOWN-CONVERTER CONTROL 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FCB<5>	EN_DDC2	GAIN_HBF_DDC	FCB<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **FCB<5>:** Factory-Controlled bit. This is not for the user. Do not change default setting.

bit 6 **EN_DDC2:** Enable DDC2 after the digital half-band filter (HBF) in DDC
1 = Enabled
0 = Disabled **(Default)**

bit 5 **GAIN_HBF_DDC:** Gain select for the output of the digital half-band filter (HBF) in DDC
1 = x2
0 = x1 **(Default)**

bit 4-0 **FCB<4:0>:** Factory-Controlled bits. This is not for the user. Do not change default settings.

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REGISTER 5-40: ADDRESS 0X82 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE <7:0>:** Lower byte of NCO_TUNE<31:0>[(1)]
0000-0000 = DC (0 Hz) when NCO_TUNE<31:0> = 0x00000000 **(Default)**

Note 1: See **Note 1** and **Note 2** in Address 0x85 (Register 5-43).

REGISTER 5-41: ADDRESS 0X83 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (MIDDLE-LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE<15:8>:** Middle-lower byte of NCO_TUNE<31:0>[(1)]
0000-0000 = **Default**

Note 1: See **Note 1** and **Note 2** in Address 0x85 (Register 5-43).

REGISTER 5-42: ADDRESS 0X84 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (MIDDLE-UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE<23:16>:** Middle-upper byte of NCO_TUNE<31:0>[(1)]
0000-0000 = **Default**

Note 1: See **Note 1** and **Note 2** in Address 0x85 (Register 5-43).

REGISTER 5-43: ADDRESS 0X85 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<31:24>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE<31:24>:** Upper byte of NCO_TUNE<31:0>(2)
1111-1111 = f_S if NCO_TUNE<31:0> = 0xFFFF FFFF
• • •
0000-0000 = **Default**

Note 1: This register is used only when DDC is enabled: EN_DDC1 = 1 in Address 0x80 (Register 5-38). See **Section 4.6.3.1 "Numerically Controlled Oscillator (NCO)"** for the details of NCO.
2: NCO frequency = (NCO_TUNE<31:0>/2^{32}) × f_S, where f_S is the ADC core sampling frequency.

REGISTER 5-44: ADDRESS 0X86 – NCO PHASE OFFSET IN DDC MODE (LOWER BYTE)(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(2)
1111-1111 = 1.4° when NCO_PHASE<15:0> = 0x00FF
• • •
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: This register has effect only when DDC mode is used in MCP37D10-200.
2: NCO_PHASE_OFFSET<15:0> = 2^{16} × Phase Offset Value/360.
3: When this register is used, the same setting must be repeated in Addresses 0x88, 0x8A, 0x8C, 0x8E, 0x90, 0x92 and 0x94.

REGISTER 5-45: ADDRESS 0X87 – NCO PHASE OFFSET IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(2)
1111-1111 = 359.995° when NCO_PHASE<15:0> = 0xFFFF
• • •
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See **Note 1** and **Note 2** in Register 5-44.
2: When this register is used, the same setting must be repeated in Addresses 0x89, 0x8B, 0x8D, 0x8F, 0x91, 0x93, and 0x95.

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REGISTER 5-46: ADDRESS 0X88 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-47: ADDRESS 0X89 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

REGISTER 5-48: ADDRESS 0X8A – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-49: ADDRESS 0X8B – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

REGISTER 5-50: ADDRESS 0X8C – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-51: ADDRESS 0X8D – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

REGISTER 5-52: ADDRESS 0X8E – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-53: ADDRESS 0X8F – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

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REGISTER 5-54: ADDRESS 0X90 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-55: ADDRESS 0X91 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

REGISTER 5-56: ADDRESS 0X92 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-57: ADDRESS 0X93 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000-0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

REGISTER 5-58: ADDRESS 0X94 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (LOWER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<7:0>:** Lower byte of NCO_PHASE<15:0>(1)
0000–0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x86.

REGISTER 5-59: ADDRESS 0X95 – NCO PHASE OFFSET (REPEAT) IN DDC MODE (UPPER BYTE)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_PHASE<15:8>:** Upper byte of NCO_PHASE<15:0>(1)
0000–0000 = 0° when NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-44. Keep this register setting the same as in Address 0x87.

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REGISTER 5-60: ADDRESS 0X96 – DIGITAL GAIN CONTROL(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)

1111-1111 = -0.03125
1111-1110 = -0.0625
1111-1101 = -0.09375
1111-1100 = -0.125
• • •
1000-0011 = -3.90625
1000-0010 = -3.9375
1000-0001 = -3.96875
1000-0000 = -4
0111-1111 = 3.96875 (MAX)
0111-1110 = 3.9375
0111-1101 = 3.90625
0111-1100 = 3.875
• • •
0011-1100 = 1.875 **(Default)**
0011-1011 = 1.84375
0011-1010 = 1.8125
0011-1001 = 1.78125
0011-1000 = 1.75 **(Optimum)**(3)

• • •
0000-0011 = 0.09375
0000-0010 = 0.0625
0000-0001 = 0.03125
0000-0000 = 0.0

Note 1: When this setting is updated, the same setting must be repeated in Addresses 0x97 - 0x9D.

2: Max = 0x7F(3.96875), Min = 0x80 (-4), Step size = 0x01 (0.03125). Bit range from 0x81-0xFF is two's complementary of 0x00-0x80. Negative gain setting inverts output.

3: This setting improves SNR by 0.5 dB from the default setting. This setting is recommended for optimum SNR performance.

REGISTER 5-61: ADDRESS 0X97 – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

REGISTER 5-62: ADDRESS 0X98 – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

REGISTER 5-63: ADDRESS 0X99 – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

REGISTER 5-64: ADDRESS 0X9A – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

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REGISTER 5-65: ADDRESS 0X9B – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

REGISTER 5-66: ADDRESS 0X9C – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

REGISTER 5-67: ADDRESS 0X9D – DIGITAL GAIN CONTROL (REPEAT)(1,2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_GAIN<7:0>:** Digital gain setting(3)
0011-1100 = 1.875 **(Default)**

Note 1: Keep this register setting the same as in Address 0x96. See Notes 1 - 3 in Register 5-60.

REGISTER 5-68: ADDRESS 0XC0 – CALIBRATION STATUS INDICATION

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ADC_CAL_STAT	FCB<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADC_CAL_STAT:** Power-Up auto-calibration status indication flag bit
1 = Device power-up calibration is completed
0 = Device power-up calibration is not completed

bit 6-0 **FCB<6:0>:** Factory-Controlled bits. These bits are readable and have no meaning for the user.

REGISTER 5-69: ADDRESS 0XD1 – PLL CALIBRATION STATUS AND PLL DRIFT STATUS INDICATION

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FCB<4:3>		PLL_CAL_STAT	FCB<2:1>		PLL_VCOL_STAT	PLL_VCOH_STAT	FCB<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **FCB<4:3>:** Factory-Controlled bits. These bits are read only and have no meaning for the user.

bit 5 **PLL_CAL_STAT:** PLL auto-calibration status indication flag bit(1)
1 = Complete: PLL auto-calibration is completed
0 = Incomplete: PLL auto-calibration is not completed

bit 4-3 **FCB<2:1>:** Factory-Controlled bits. These bits are read only and have no meaning for the user.

bit 2 **PLL_VCOL_STAT:** PLL drift status indication bit
1 = PLL drifts out of lock with low VCO frequency
0 = PLL operates as normal

bit 1 **PLL_VCOH_STAT:** PLL drift status indication bit
1 = PLL drifts out of lock with high VCO frequency
0 = PLL operates as normal

bit 0 **FCB<0>:** Factory-Controlled bit. This bit is read only and has no meaning for the user.

Note 1: See PLL_CAL_TRIG bit setting in Address 0x6B (Register 5-27).

REGISTER 5-70: ADDRESS 0X15C – CHIP ID (LOWER BYTE)(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
CHIP_ID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **CHIP_ID<7:0>:** Chip ID of the device: Lower byte of the CHIP ID<15:0>

Note 1: Read-only register. Preprogrammed at the factory for internal use.
Example: MCP37210-200: '0001000000110000'
MCP37D10-200: '0001001000110000'

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REGISTER 5-71: ADDRESS 0X15D – CHIP ID (UPPER BYTE)(1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
CHIP_ID<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CHIP_ID<15:8>:** Chip ID of the device: Upper byte of the CHIP_ID<15:0>

Note 1: Read-only register. Preprogrammed at the factory for internal use.

Example: MCP37210-200: '0001000000110000’

MCP37D10-200: '0001001000110000’

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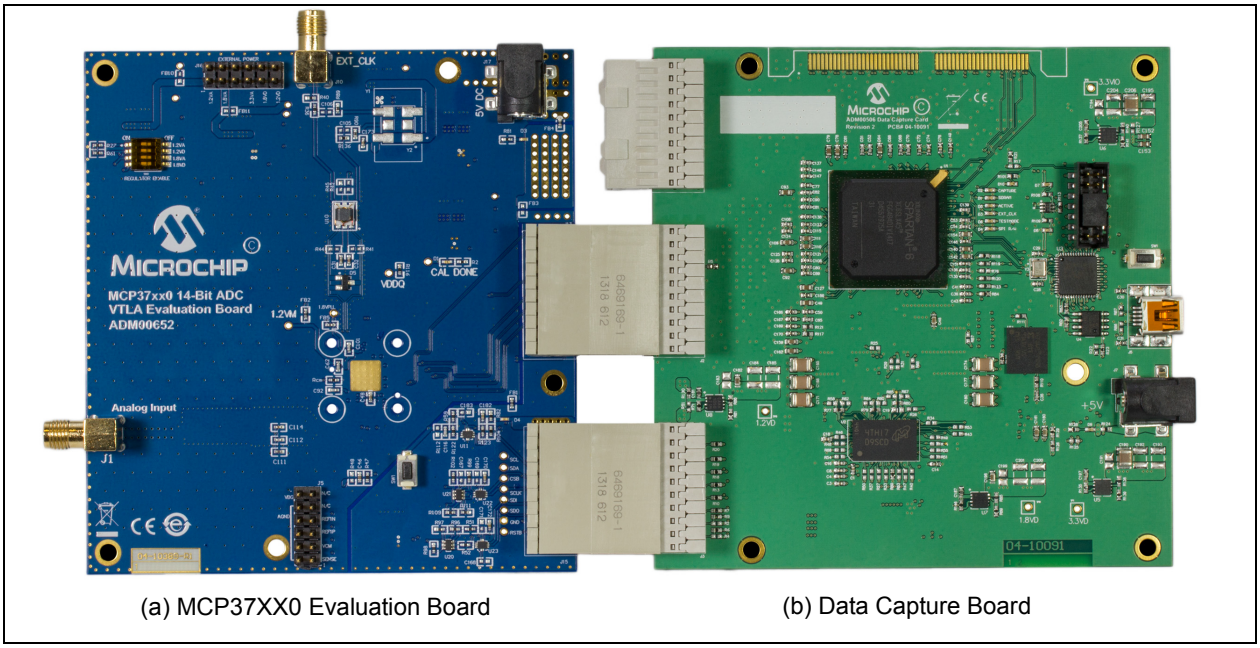
6.0 DEVELOPMENT SUPPORT

Microchip offers a high-speed ADC evaluation platform which can be used to evaluate Microchip's high-speed ADC products. The platform consists of an MCP37XX0-200 evaluation board, an FPGA-based data capture card board and PC-based Graphical User Interface (GUI) software for ADC and evaluation.

Figure 6-1 and Figure 6-2 show this evaluation tool. This evaluation platform allows users to quickly evaluate the ADC's performance for their specific application requirements. More information is available at http://www.microchip.com.



(a) MCP37XX0 Evaluation Board (b) Data Capture Board

FIGURE 6-1: *MCP37XX0 Evaluation Kit.*

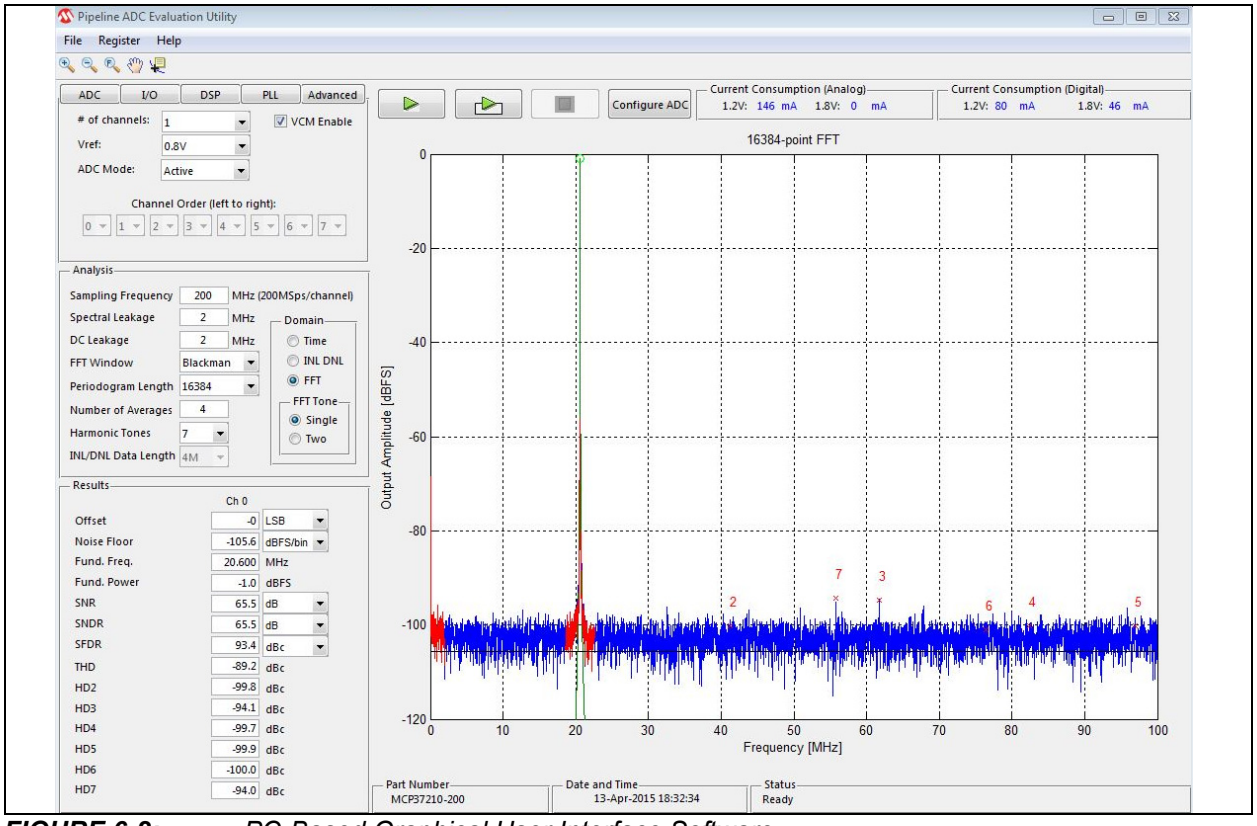


FIGURE 6-2: *PC-Based Graphical User Interface Software.*

Notes:

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7.0 TERMINOLOGY

Analog Input Bandwidth (Full-Power Bandwidth)

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay or Sampling Delay

This is the time delay between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty

The sample-to-sample variation in aperture delay.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal-to-noise ratio due to the jitter alone will be:

EQUATION 7-1:

$$SNR_{JITTER} = -20log(2\pi \times f_{IN} \times t_{JITTER})$$

Calibration Algorithms

This device utilizes two patented analog and digital calibration algorithms, Harmonic Distortion Correction (HDC) and DAC Noise Cancellation (DNC), to improve the ADC performance. The algorithms compensate various sources of linear impairments such as capacitance mismatch, charge injection error and finite gain of operational amplifiers. These algorithms execute in both power-up sequence (foreground) and background mode:

- Power-Up Calibration: The calibration is conducted within the first 3×2^{26} clock cycles after power-up. The user needs to wait this Power-Up Calibration period after the device is powered-up for an accurate ADC performance.
- Background Calibration: This calibration is conducted in the background while the ADC is performing conversions. The update rate is about once every 2^{30} clock cycles.

Pipeline Delay (LATENCY)

LATENCY is the number of clock cycles between the initiation of conversion and when that data is presented to the output pins. Data for any given input sample is available after the pipeline delay plus the output delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay plus the output delay. Latency is increased if digital signal post-processing is used.

Clock Pulse Width and Duty Cycle

The clock duty cycle is the ratio of the time the clock signal remains at a logic high (clock pulse width) to one clock period. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSb apart. DNL is the deviation from this ideal value. No missing codes to 12-bit resolution indicates that all 4096 codes must be present over all the operating conditions.

Integral Nonlinearity (INL)

INL is the maximum deviation of each individual code from an ideal straight line drawn from negative full scale through positive full scale.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), below the Nyquist frequency and excluding the power at DC and the first nine harmonics.

EQUATION 7-2:

$$SNR = 10log\left(\frac{P_S}{P_N}\right)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D) below the Nyquist frequency, but excluding DC:

EQUATION 7-3:

$$SINAD = 10log\left(\frac{P_S}{P_D + P_N}\right)$$
$$= -10log\left[10^{-\frac{SNR}{10}} - 10^{-\frac{THD}{10}}\right]$$

SINAD is given in either units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

EQUATION 7-4:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Gain Error

Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Gain error is usually expressed in LSb or as a percentage of full-scale range (%FSR).

Gain-Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

Offset Error

The major carry transition should occur for an analog value of ½ LSb below $A_{IN}+ = A_{IN}-$. Offset error is defined as the deviation of the actual transition from that point.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (+25°C) value to the value across the T_{MIN} to T_{MAX} range.

Maximum Conversion Rate

The maximum clock rate at which parametric testing is performed.

Minimum Conversion Rate

The minimum clock rate at which parametric testing is performed.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier) or dBFS.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the summed power of the first 13 harmonics (P_D).

$$THD = 10log\left(\frac{P_S}{P_D}\right)$$

THD is typically given in units of dBc (dB to carrier). THD is also shown by:

EQUATION 7-5:

$$THD = -20log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_1^2}$$

Where:

V_1 = RMS amplitude of the fundamental frequency

V_1 through V_n = Amplitudes of the second through n^{th} harmonics

Two-Tone Intermodulation Distortion (Two-Tone IMD, IMD3)

Two-tone IMD is the ratio of the power of the fundamental (at frequencies f_{IN1} and f_{IN2}) to the power of the worst spectral component at either frequency $2f_{IN1} - f_{IN2}$ or $2f_{IN2} - f_{IN1}$. Two-tone IMD is a function of the input amplitudes and frequencies (f_{IN1} and f_{IN2}). It is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the ADC full-scale range.

Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both sides of a differential input pair. The common-mode signal can be an AC or DC signal or a combination of the two. CMRR is measured using the ratio of the differential signal gain to the common-mode signal gain and expressed in dB with the following equation:

EQUATION 7-6:

$$CMRR = 20log\left(\frac{A_{DIFF}}{A_{CM}}\right)$$

Where:

A_{DIFF} = ΔOutput Code/ΔDifferential Voltage

A_{DIFF} = ΔOutput Code/ΔCommon Mode Voltage

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NOTES:

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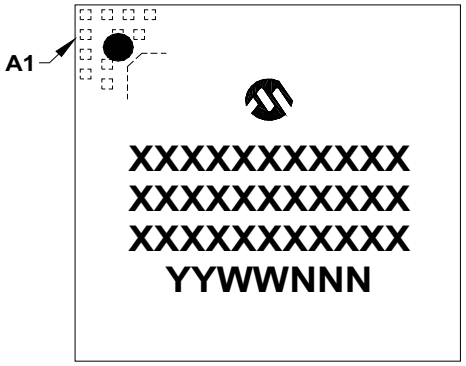
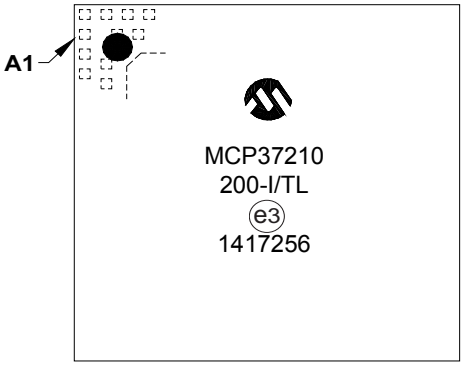
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

124-Lead VTLA (9x9x0.9 mm)



Example

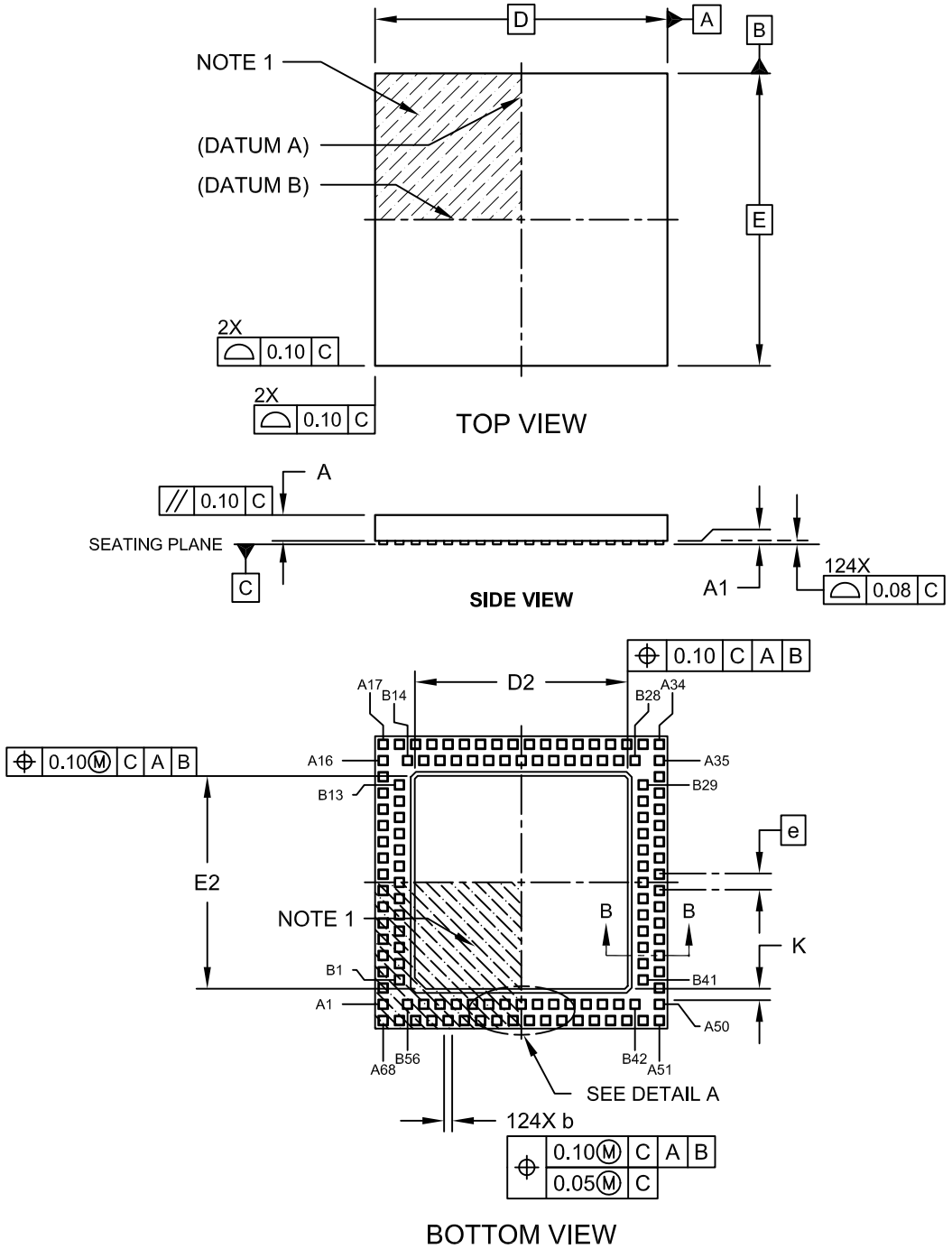


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-193A Sheet 1 of 2

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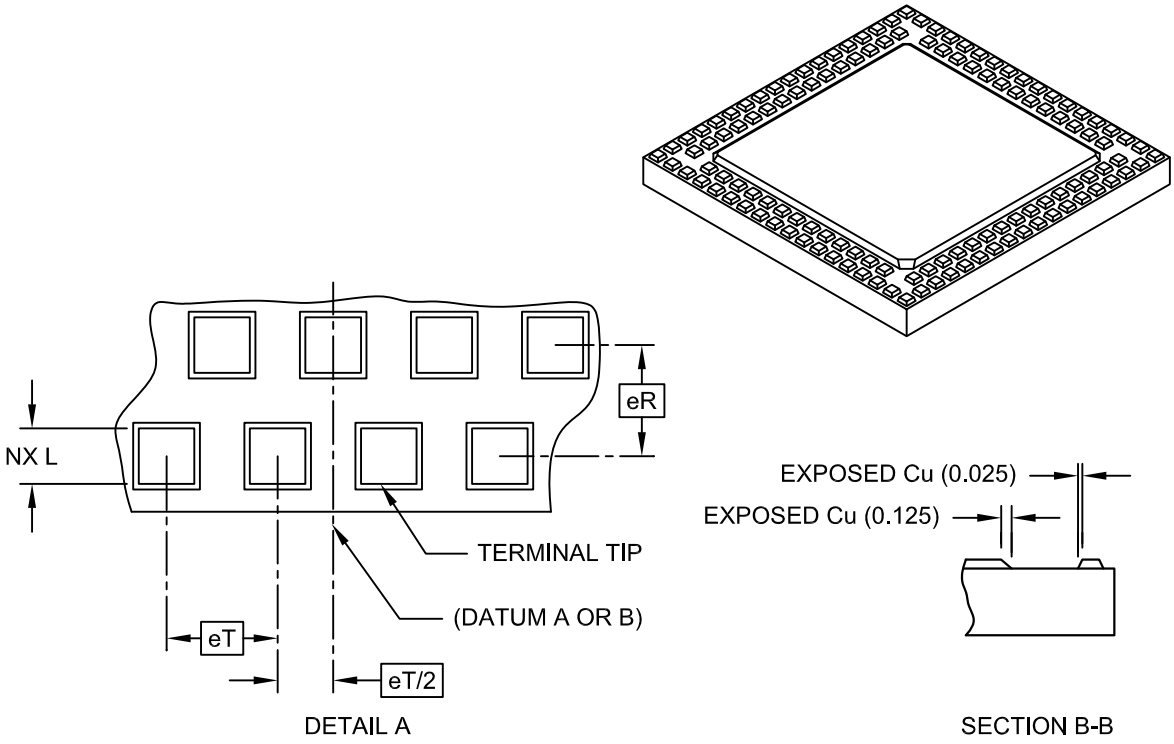
124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		124	
Pitch	eT		0.50 BSC	
Pitch (Inner to outer terminal ring)	eR		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	6.40	6.55	6.70
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	6.40	6.55	6.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

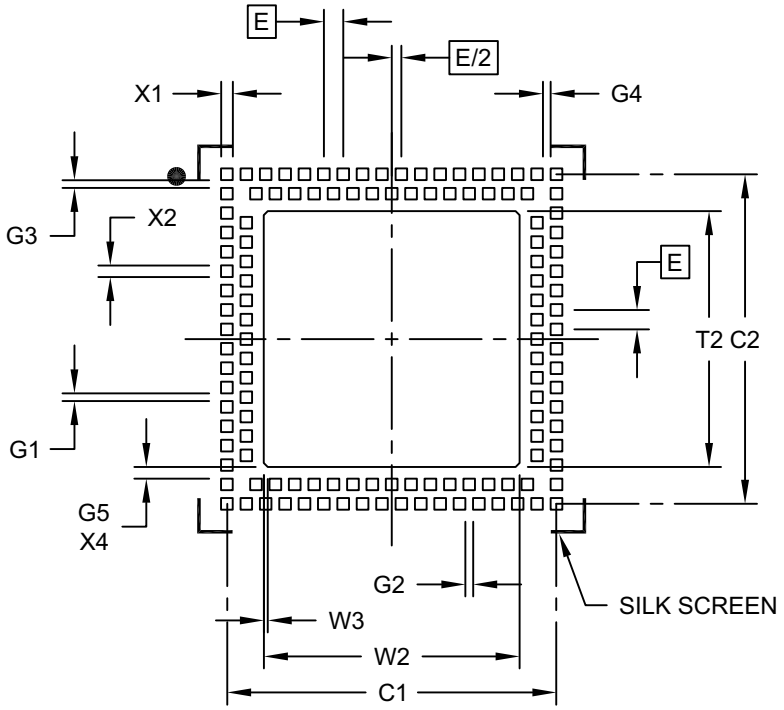
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A

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APPENDIX A: REVISION HISTORY

Revision A (April 2015)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XXX	X	/XX
Device	Tape and Reel Option	Sample Rate	Temperature Range	Package

Device:	MCP37210-200:	12-Bit Low-Power Single-Channel ADC
	MCP37D10-200:	12-Bit Low-Power Single-Channel ADC with digital down-converter option
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Sample Rate	200 =	200 Msps
Temperature Range:	I =	-40°C to +85°C (Industrial)
Package:	TL =	Terminal Very Thin Leadless Array Package - 9x9x0.9 mm Body (VTLA), 124-Lead
	TE* =	Ball Plastic Thin Profile Fine Pitch Ball Grid Array - 8x8x1.08 mm Body (TFBGA), 121-Lead

* Contact Microchip Technology Inc. for availability.

Examples:

a) MCP37210-200I/TL: Industrial temperature, 124LD VTLA, 200 Msps

b) MCP37210T-200I/TL: Tape and Reel, Industrial temperature, 124LD VTLA, 200 Msps

c) MCP37210T-200I/TE*: Tape and Reel, Industrial temperature, 121LD TFBGA, 200 Msps

a) MCP37D10I-200I/TL: Industrial temperature, 124LD VTLA, 200 Msps

b) MCP37D10IT-200I/TL: Tape and Reel, Industrial temperature, 124LD VTLA, 200 Msps

c) MCP37D10I/TE*: Industrial temperature, 121LD TFBGA, 200 Msps

* Contact Microchip Technology Inc. for availability.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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