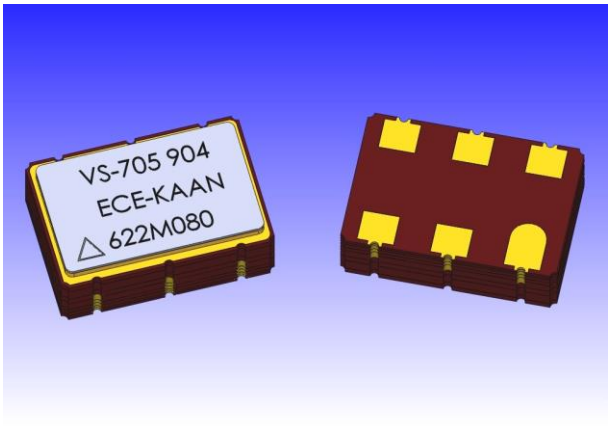
VS-705
Single Frequency VCSO



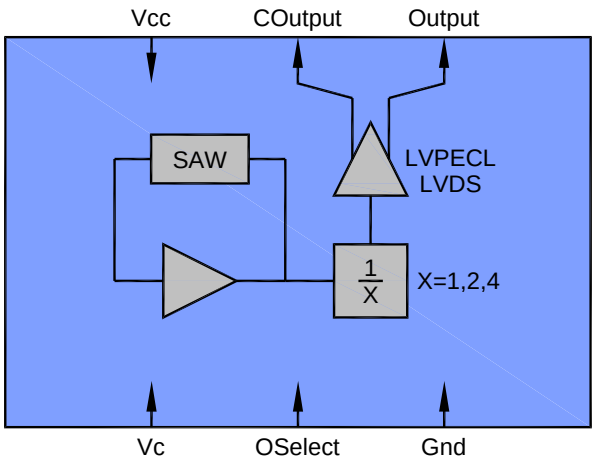
Features

- Industry Standard Package, 5.0 x 7.5 x 2.5 mm
- 5th Generation ASIC Technology for Ultra Low Jitter
  120 fs-rms (f_N = 622.08 MHz, 12 kHz to 20 MHz)
  105 fs-rms (f_N = 622.08 MHz, 50 kHz to 80 MHz)
- Output Frequencies from 122.88 MHz to 1.00 GHz
- Spurious Suppression, 90 dBc Typical
- 2.5V or 3.3V Supply Voltage
- LVPECL or LVDS Output Configurations
- Tri-State Output Select (OD, OS, OE)
- Compliant to EC RoHS Directive

Applications

PLL circuits for Clock Smoothing and Frequency Translation

Description	Standard
• SONET / SDH	GR-253-CORE
• OTN (Optical Transport Network)	ITU-T G.709/Y.1331
• 10 GbE (Gigabit Ethernet)	IEEE 802.3ae
• 10 GFC (Gigabit Fibre Channel)	INCITS 364-2003
• 40 GbE & 100 GbE	IEEE 802.3ba
• Synchronous Ethernet	ITU-T G.8261
• WiMax	IEEE 802.16



Description

The VS-705 is a Voltage Controlled SAW Oscillator that operates at the fundamental frequency of the internal SAW filter. The SAW filter is a high-Q Quartz device that enables the circuit to achieve low phase jitter performance over a wide operating temperature range. A divider circuit is deployed for output frequencies less than 491.52 MHz. The oscillator is housed in a hermetically sealed leadless surface mount package and offered on tape and reel. It has a tri-state Output Select function that provides one of three conditions: Output Disable, Output Set, or Output Enable.

Electrical Performance: 3.3V LV-PECL

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Nominal Frequency	f_N	120		1000	MHz	1,2,3
Absolute Pull Range	APR	±50			ppm	1,2,3,9
Linearity	Lin		±7		%	2,4,9
Gain Transfer	K_V		+445		ppm/V	2,9
Temperature Stability	f_{STAB}		±100		ppm	1,7
Supply						
Voltage (± 10%)	V_{CC}	2.97	3.3	3.63	V	2,3
Current (Typical 50Ω Load)	I_{CC}		73		mA	3
Current (No Load)	I_{CC}		60	75	mA	3
Outputs						
Mid Level		V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	mV	2,3
Single Ended Swing			750		mV-pp	2,3
Differential Swing			1.5		V-pp	2,3
Current	I_{OUT}			20	mA	7
Rise Time	t_R		180	250	ps-pp	6,7
Fall Time	t_F		180	250	ps-pp	6,7
Symmetry	SYM	45	50	55	%	2,3
Spurious Suppression		85	90		dBc	7
Jitter (>491.52 MHz to <1000.0 MHz)	ϕJ		150		fs-rms	7,8
Jitter (>245.76 MHz to <491.52 MHz)	ϕJ		190		fs-rms	7,8
Jitter (>122.88 MHz to <245.76 MHz)	ϕJ		280		fs-rms	7,8
Control Voltage						
Input Impedance (Output Enabled)	Z_C		123		kΩ	7
Input Impedance (Output Disabled)	Z_C		472		kΩ	7
Modulation Bandwidth	BW		200		kHz	7
Operating Temperature	T_{OP}	-40		+85	°C	1,3
Package Size		5.0 x 7.5 x 2.5			mm	

1. See Standard Frequencies and Ordering Information (Pg 8).
2. Parameters are tested with production test circuit (Pg 3).
3. Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4. Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5. The Vc Model is described below (Fig 1).
6. Parameters are described with waveform diagram below (Fig 2).
7. Not tested in production, guaranteed by design, verified at qualification.
8. For Frequencies >491.52 MHz, Jitter is Integrated across 50 kHz to 80 MHz.
   For Frequencies <491.52 MHz, Jitter is Integrated across 12 kHz to 20 MHz. (Both per GR-253-CORE Issue3).
9. Tested with Vc = 0.3V to 3.0V.

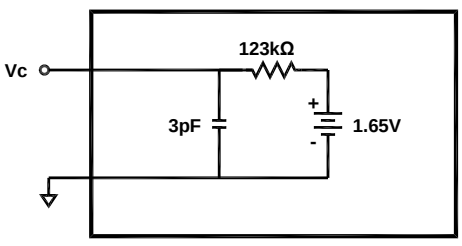


Figure 1. Vc Model – Output Enabled

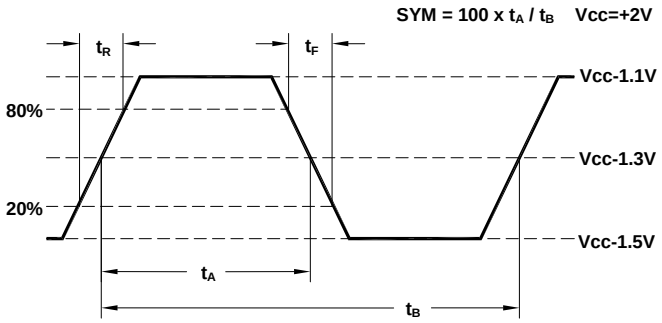


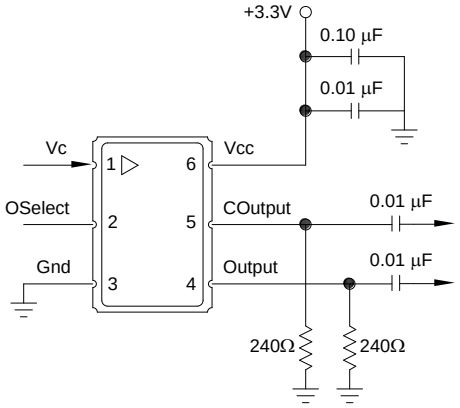
Figure 2. 10K LV-PECL Waveform

Absolute Maximum Ratings

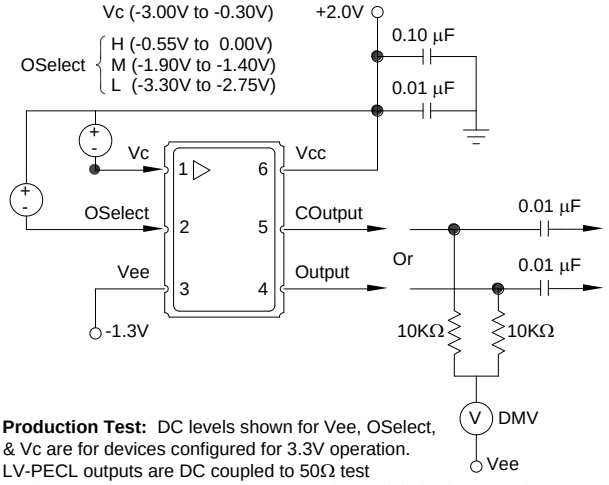
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Output Select	OSelect	0 to V_{CC}	V
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 40	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input (Vc or OS) draws >100 mA.

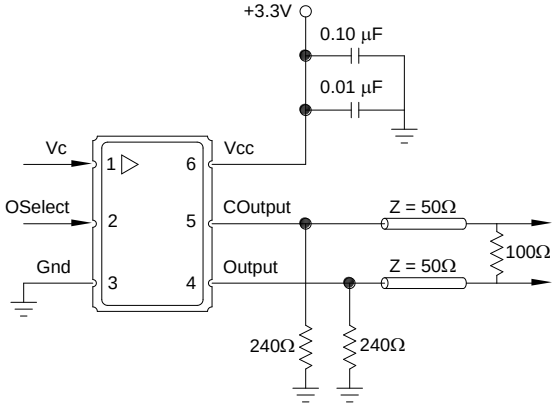
Test Circuits & Output Load Configurations



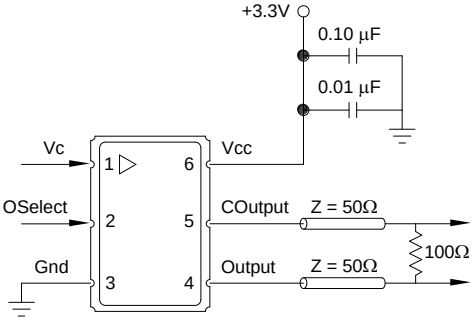
Functional Test: Allows use of standard power supply biasing configuration. Pull down resistors are used for LV-PECL outputs and are removed for with LVDS outputs. Since the LVDS outputs are AC coupled, the output DC levels cannot be measured.



Production Test: DC levels shown for Vee, OSelect, & Vc are for devices configured for 3.3V operation. LV-PECL outputs are DC coupled to 50Ω test equipment. LVDS outputs are connected to a digital volt meter, then AC coupled to the test equipment. The digitial volt meter allows for Mid Level & Swing measurements.

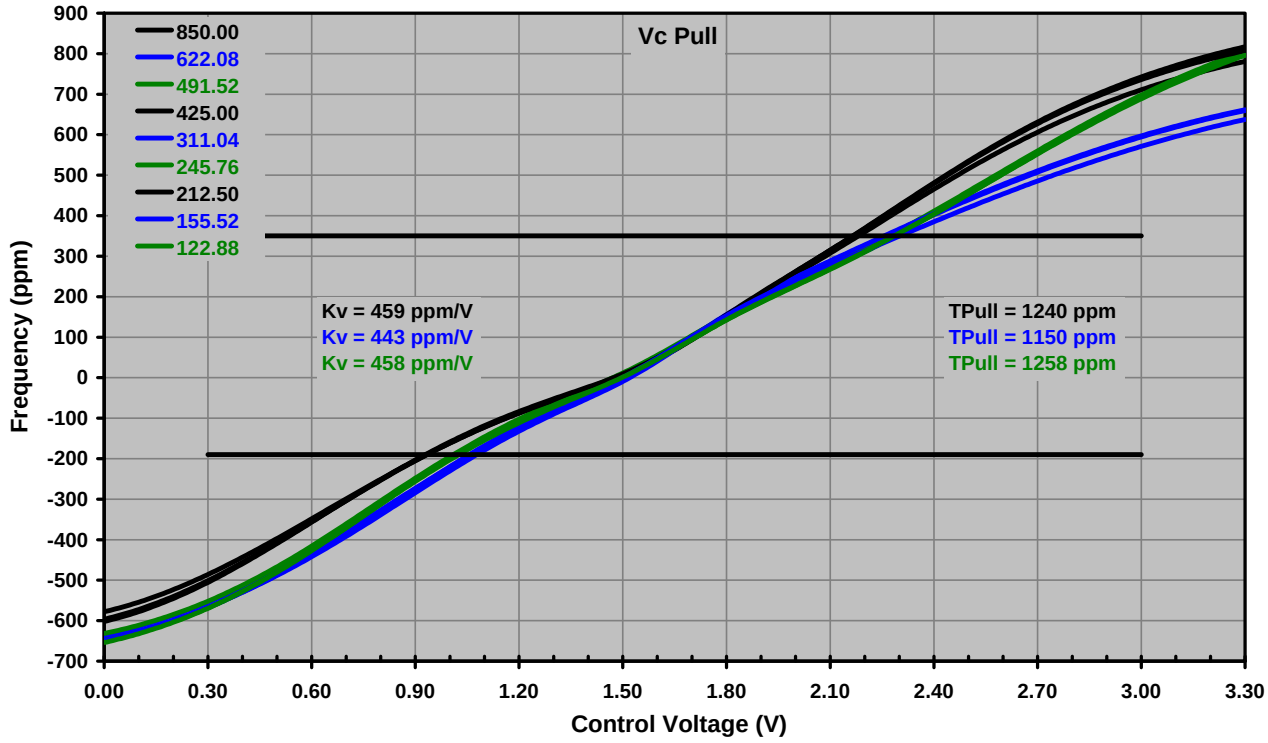


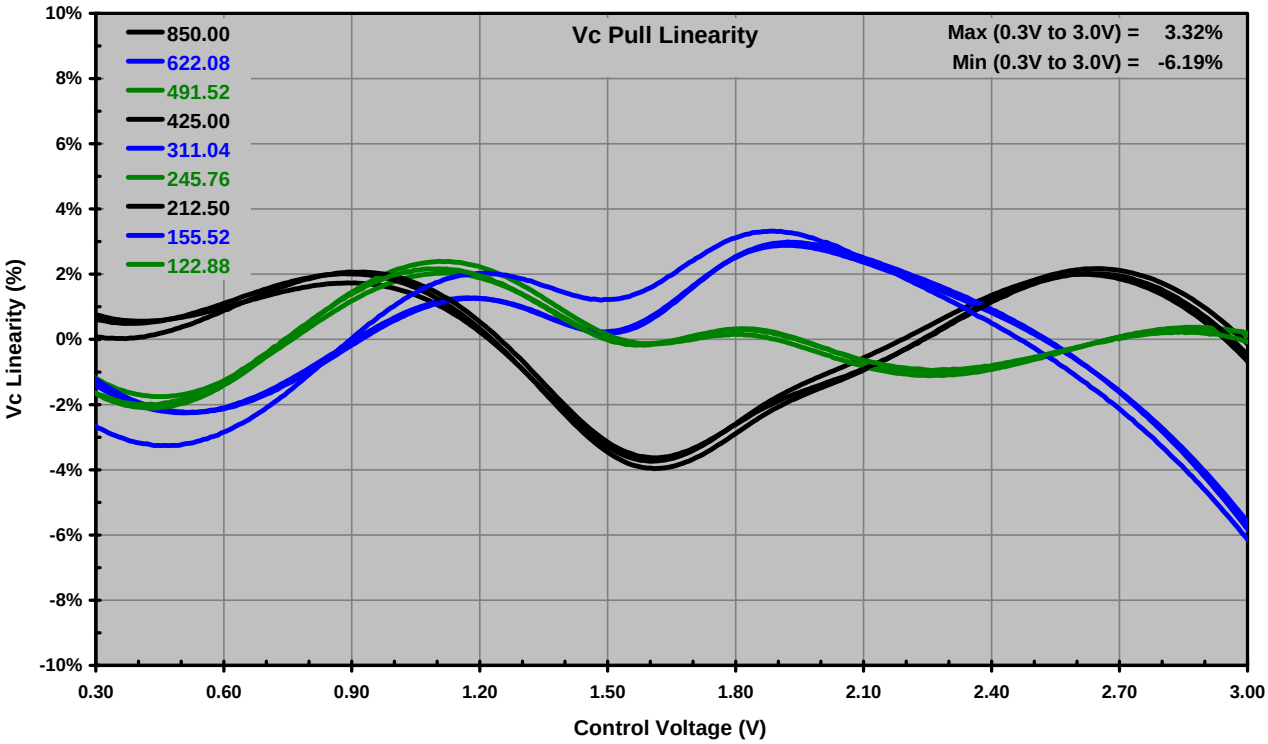
LV-PECL to LV-PECL: For short transmission lengths, the pull down resistor values shown provide reasonable power consumption and waveform performance.



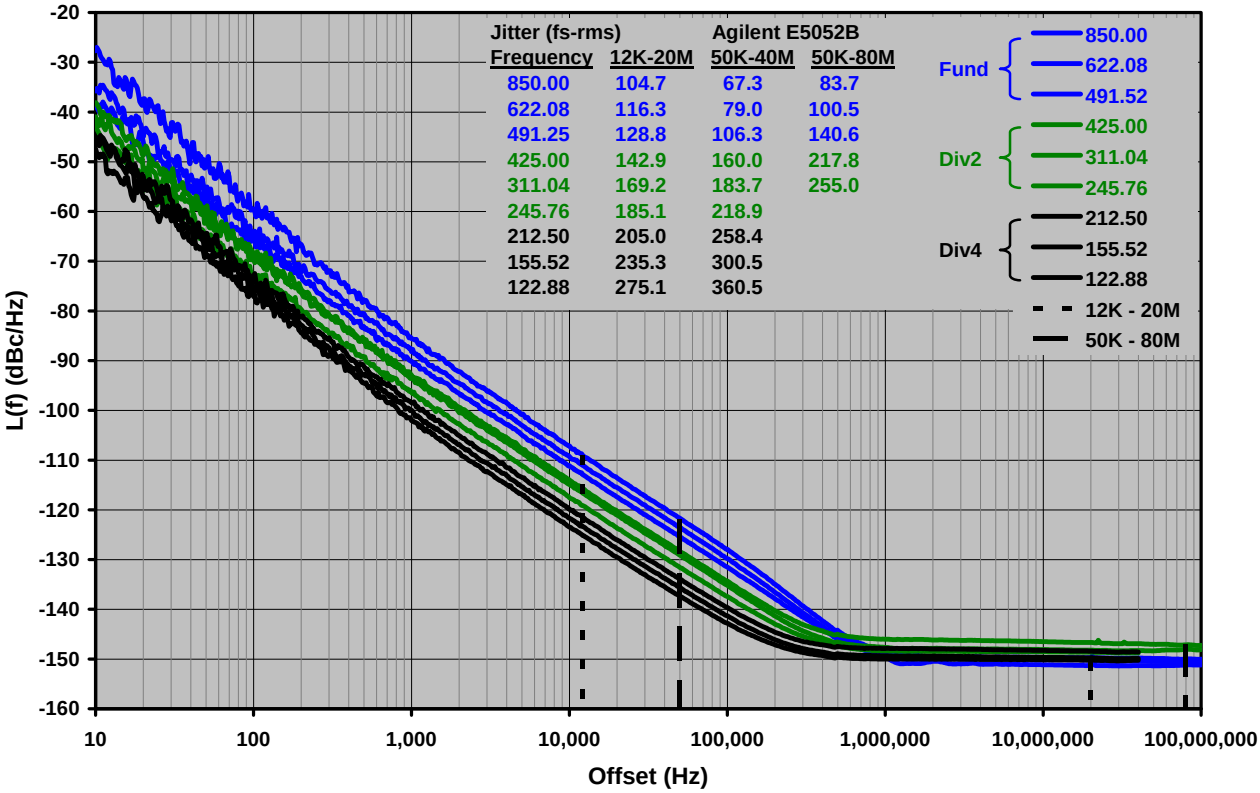
LVDS to LVDS: The 100Ω resistor should be removed if this load is provided internally within the LVDS receiver.

Typical Characteristics: Vc Pull & Vc Pull Linearity





Typical Characteristics: Phase Noise & Jitter



Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-705 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002 B
Mechanical Vibration	MIL-STD-883, Method 2007 A
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/JEDEC J-STD-020, MSL1

Handling Precautions

Although ESD protection circuitry has been designed into the VS-705 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

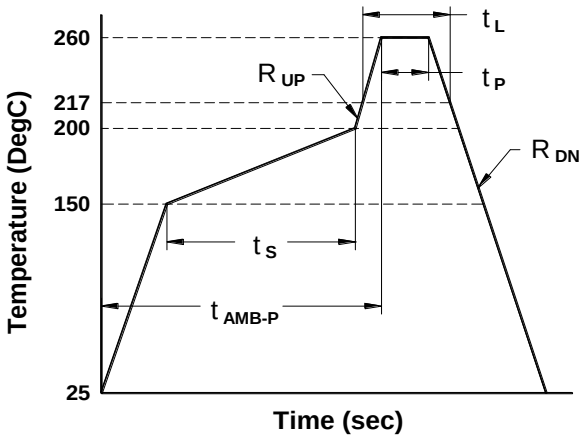
Model	Minimum	Conditions
Human Body Model	2000 V	MIL-STD 883, Method 3015
Charged Device Model	1000 V	JEDEC, JESD22-C101
Machine Model	200 V	JEDEC, JESD22-A115-A

Reflow Profile (IPC/JEDEC J-STD-020)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

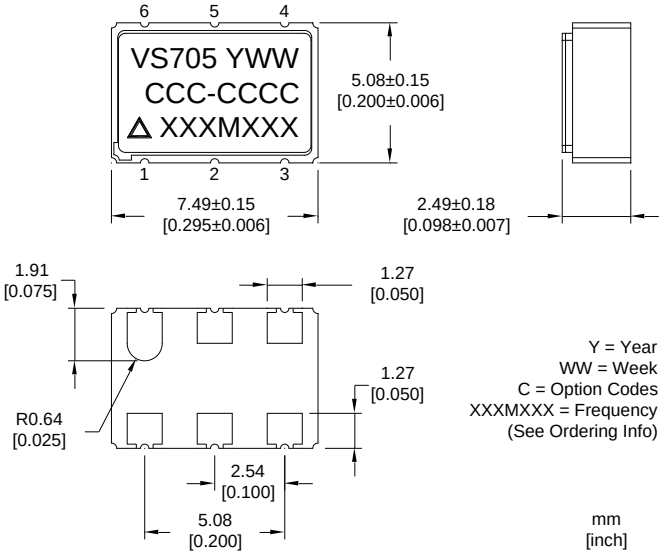
The VS-705 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-705 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electroless Ni > 1.90 μm
Electroless Au > 1.50 μm

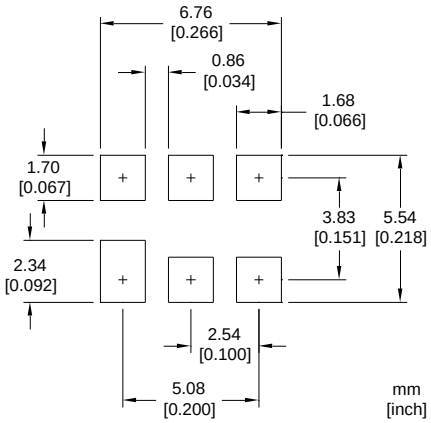


VS-705 Single Frequency VCSO

Outline & Marking Diagram



Suggested Pad Layout



Pin Out

Pin	Symbol	Function
1	V_C	Control Voltage
2	OSelect	Output Select
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{CC}	Power Supply Voltage

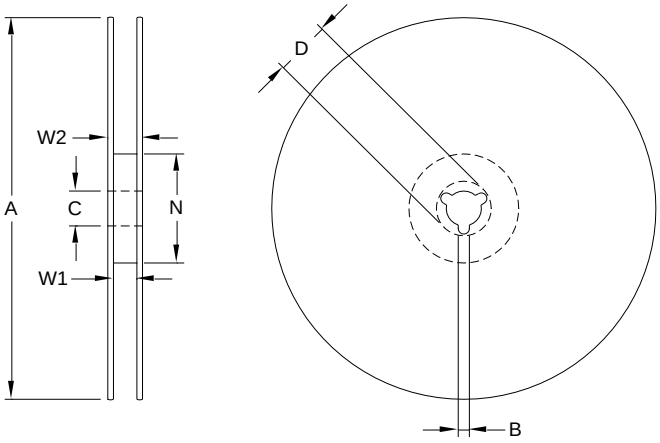
Floating OSelect Always Results In OE

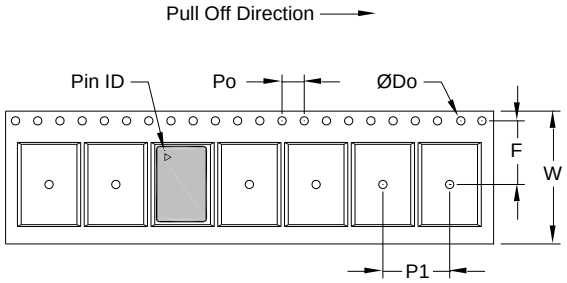
Output Select (Tri-State LV-CMOS)

Option	OS	Voltage Range	Result
A	H	(5V_{CC} / 6) to V_{CC}	OE
	M	(V_{CC} / 2) ± 15%(V_{CC} / 2)	OS
	L	Gnd to (V_{CC} / 6)	OD
C	H	(5V_{CC} / 6) to V_{CC}	OD
	M	(V_{CC} / 2) ± 15%(V_{CC} / 2)	OS
	L	Gnd to (V_{CC} / 6)	OE

OD = Outputs Disabled
OS = Outputs Set (Output = H, COutput = L)
OE = Outputs Enabled

Tape and Reel (EIA-481-2-A)





Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	**Reel**
VS-705	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

VS-705 Single Frequency VCSO

Standard Frequencies (MHz)

122.880000	125.000000	155.520000	156.250000	160.000000	161.132813	166.628572
167.331646	168.040678	173.370748	173.437500	184.320000	200.000000	212.500000
245.760000	307.200000	315.000000	320.000000	368.640000	400.000000	425.000000
491.520000	500.000000	531.250000	614.400000	622.080000	625.000000	627.329620
644.531250	657.421875	666.514286	669.326582	672.000000	699.517493	715.538900
716.800000	718.863800	737.280000	739.200000	768.000000	777.600000	800.000000
819.200000	834.640000	877.968756	983.040000	1000.00000		

Other Frequencies Available Upon Request.

Ordering Information

VS - 705 - E C E - K A A N – xxxMxxxxxx

Product Family
VS: VCSO

Package
705: 5.1 x 7.5 x 2.5 mm

Supply Voltage
E: 3.3V
H: 2.5V

Output Type
C: LVPECL
D: LVDS

Operating Temperature
E: -40°C to 85°C

Frequency (See Above)
122M880000 –

Other (Future Use)
N: N/A

Oscillator Gain
A: Standard
B: Low

Control Logic (Tri-State)
A: L = OD, M = OS, H = OE
C: L = OE, M = OS, H = OD

Absolute Pull Range
K: ± 50 ppm
S: ± 100 ppm

Example: VS-705-ECE-KAAN-983M040000

Contact Information:

EUROPE: Potsdamer Straße 18, D-14513 Teltow, Germany
Tel: +49 (0) 3328 4784 17 • Fax: +49 (0) 3328 4784 30

EUROPE: Landstrasse, D-74924, Neckarbischofsheim, Germany
Tel: +49 (0) 7268 8010 • Fax: +49 (0) 7268 801281

USA: Vectron International • 267 Lowell Road, Suite 102, Hudson, NH 03051
Tel: 1.888.328.7661 • Fax: 1.888.329.8328

ASIA: 68 Yin Cheng Road (C), 22nd Floor,
One LuJiaZui, Pudong, Shanghai, 200120 China
Tel : +86.21.6194.6886 • Fax : +86.21.6194.6699

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Revision History

Date	Approved	Description
15Apr2008	JM, BW	Release
30May2008	JM, BW	Corrected Production Test Circuit on Pg3.
29July2008	JM, BW	Max Operating Frequency extended to 985 MHz. Standard Frequency List updated.
23Oct2008	JM,BW	Standard Frequency List updated.
08Mar2010	JM	Updated rendering, application section, frequency range, environmental compliance, frequencies, and ordering codes.
23Jul2010	CH	Standard Frequency List updated.
03Mar2014	MK	Vectron Logo changed, Vectron Address Shanghai changed

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9