



# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

## General Description

The MAX6889/MAX6890/MAX6891 EEPROM-configurable, multivoltage supply sequencers/supervisors monitor several voltage detector inputs and general-purpose logic inputs and feature programmable outputs for highly configurable power-supply sequencing applications. The MAX6889 features eight voltage detector inputs and ten programmable outputs. The MAX6890 features six voltage detector inputs and eight programmable outputs, while the MAX6891 features four voltage detector inputs and five programmable outputs. Manual reset and margin disable inputs offer additional flexibility.

All voltage detectors offer a configurable threshold for undervoltage detection. High-voltage input IN1 monitors voltages from 2.5V to 13.2V in 50mV increments, or from 1.25V to 7.625V in 25mV increments. Inputs IN2–IN7 monitor voltages from 1V to 5.5V in 20mV increments or from 0.5V to 3.05V in 10mV increments. High-voltage input IN8 monitors voltages from 2.5V to 15.25V in 50mV increments, or from 1.25V to 7.625V in 25mV increments.

Programmable output stages control power-supply sequencing or system resets/interrupts. Programmable output options include: active-high, active-low, open drain, and weak pullup. Programmable timing delay blocks configure each output to wait between 25µs and 1600ms before deasserting.

The MAX6889/MAX6890/MAX6891 feature a watchdog timer for added flexibility. Program the watchdog timer to assert one or more programmable outputs. The initial and normal watchdog timeout periods are independently programmable from 6.25ms to 102.4s.

An SMBus™/I²C-compatible, 2-wire serial data interface programs and communicates with the configuration EEPROM, the configuration registers, and the internal 512-bit user EEPROM.

The MAX6889/MAX6890/MAX6891 are available in 5mm x 5mm x 0.8mm thin QFN packages and are specified to operate over the extended temperature range (-40°C to +85°C).

## Applications

Telecommunication/Central Office Systems  
Networking Systems  
Servers/Workstations  
Base Stations  
Storage Equipment  
Multi-Microprocessor/Voltage Systems

## Features

- ◆ Eight (MAX6889), Six (MAX6890), or Four (MAX6891) Configurable Input Voltage Detectors
  - High-Voltage Input (1.25V to 7.625V or 2.5V to 13.2V)
  - Six (MAX6889), Five (MAX6890), or Three (MAX6891) Voltage Inputs (0.5V to 3.05V or 1V to 5.5V)
  - Additional (MAX6889) High-Voltage Input (1.25V to 7.625V or 2.5V to 15.25V)
- ◆ Four (MAX6889/MAX6890) or Three (MAX6891) General-Purpose Logic Inputs
- ◆ Configurable Watchdog Timer
- ◆ Ten (MAX6889), Eight (MAX6890), or Five (MAX6891) Programmable Outputs
  - Active-High, Active-Low, Open Drain, Weak Pullup
  - Timing Delays from 25µs to 1600ms
- ◆ Margining Disable and Manual Reset Controls
- ◆ 512-Bit Internal User EEPROM
  - Endurance: 100,000 Erase/Write Cycles
  - Data Retention: 10 Years
- ◆ I²C/SMBus-Compatible Serial Configuration/Communication Interface
- ◆ ±1% Threshold Accuracy

## Ordering Information

| PART       | TEMP RANGE     | PIN-PACKAGE     |
|------------|----------------|-----------------|
| MAX6889ETJ | -40°C to +85°C | 32 Thin QFN-EP* |
| MAX6890ETI | -40°C to +85°C | 28 Thin QFN-EP* |
| MAX6891ETP | -40°C to +85°C | 20 Thin QFN-EP* |

\*EP = Exposed pad.

Pin Configurations and Typical Operating Circuit appear at end of data sheet.

SMBus is a trademark of Intel Corp.



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## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

|                                                               |               |
|---------------------------------------------------------------|---------------|
| IN2–IN7, V <sub>CC</sub> , SDA, SCL, A0, A1, GPI <sub>–</sub> |               |
| $\overline{\text{MR}}$ , $\overline{\text{MARGIN}}$           | –0.3V to +6V  |
| IN1, PO <sub>–</sub>                                          | –0.3V to +14V |
| IN8                                                           | –0.3V to +20V |
| DBP                                                           | –0.3V to +3V  |
| Input/Output Current (all pins)                               | ±20mA         |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)         |               |
| 20-Pin Thin QFN (derate 21.3mW/°C above +70°C)                | 1702mW        |

|                                                |                 |
|------------------------------------------------|-----------------|
| 28-Pin Thin QFN (derate 21.3mW/°C above +70°C) | 1702mW          |
| 32-Pin Thin QFN (derate 21.3mW/°C above +70°C) | 1702mW          |
| Operating Temperature Range                    | –40°C to +85°C  |
| Maximum Junction Temperature                   | +150°C          |
| Storage Temperature Range                      | –65°C to +150°C |
| Lead Temperature (soldering, 10s)              | +300°C          |

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>IN1</sub> = 6.5V to 13.2V, V<sub>IN2</sub>–V<sub>IN7</sub> = 2.7V to 5.5V, V<sub>IN8</sub> = 10V, GPI<sub>–</sub> = GND,  $\overline{\text{MARGIN}}$  =  $\overline{\text{MR}}$  = DBP, T<sub>A</sub> = –40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 1, 2, 3)

| PARAMETER                        | SYMBOL            | CONDITIONS                                                                                            | MIN   | TYP  | MAX   | UNITS |
|----------------------------------|-------------------|-------------------------------------------------------------------------------------------------------|-------|------|-------|-------|
| Operating Voltage Range (Note 4) | V <sub>IN1</sub>  | Voltage on IN1 to ensure the device is fully operational, IN2–IN8 = GND                               | 4.0   |      | 13.2  | V     |
|                                  |                   | Voltage on any one of IN2–IN5 or V <sub>CC</sub> to ensure the device is fully operational, IN1 = GND | 2.7   |      | 5.5   |       |
| IN1 Supply Voltage (Note 4)      | V <sub>IN1P</sub> | Minimum voltage on IN1 to guarantee that the device is powered through IN1                            |       |      | 6.5   | V     |
| Undervoltage Lockout             | V <sub>UVLO</sub> | Minimum voltage on one of IN2–IN5 to guarantee the device is EEPROM configured                        |       |      | 2.5   | V     |
| Digital Bypass Voltage           | V <sub>DBP</sub>  | No load                                                                                               | 2.48  | 2.55 | 2.67  | V     |
| Supply Current                   | I <sub>CC</sub>   | V <sub>IN1</sub> = 13.2V, IN2–IN8 = GND, no load                                                      |       | 1    | 1.2   | mA    |
|                                  |                   | Writing to configuration registers or EEPROM, no load                                                 |       | 1.1  | 1.5   | mA    |
| Threshold Voltage Range          | V <sub>TH</sub>   | V <sub>IN1</sub> (50mV increments)                                                                    | 2.5   |      | 13.2  | V     |
|                                  |                   | V <sub>IN1</sub> (25mV increments)                                                                    | 1.25  |      | 7.625 |       |
|                                  |                   | V <sub>IN2</sub> –V <sub>IN7</sub> (20mV increments)                                                  | 1.0   |      | 5.5   |       |
|                                  |                   | V <sub>IN2</sub> –V <sub>IN7</sub> (10mV increments)                                                  | 0.50  |      | 3.05  |       |
|                                  |                   | V <sub>IN8</sub> (50mV increments)                                                                    | 2.50  |      | 15.25 |       |
|                                  |                   | V <sub>IN8</sub> (25mV increments)                                                                    | 1.250 |      | 7.625 |       |
|                                  |                   | V <sub>IN2</sub> –V <sub>IN8</sub> (high-Z mode in 3.3mV increments)                                  | 0.167 |      | 1.017 |       |

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MAX6889/MAX6890/MAX6891

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN1}$  = 6.5V to 13.2V,  $V_{IN2}$ – $V_{IN7}$  = 2.7V to 5.5V,  $V_{IN8}$  = 10V,  $GPI_{-}$  = GND,  $\overline{MARGIN} = \overline{MR} = DBP$ ,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Notes 1, 2, 3)

| PARAMETER                          | SYMBOL        | CONDITIONS                                                    |                                                                                 | MIN    | TYP | MAX    | UNITS      |
|------------------------------------|---------------|---------------------------------------------------------------|---------------------------------------------------------------------------------|--------|-----|--------|------------|
| IN2–IN7 Threshold Accuracy         |               | $T_A$ = +25°C to +85°C<br>( $V_{IN_{-}}$ falling)             | $V_{IN_{-}}$ = 2.5V to 5.5V<br>(20mV increments)                                | -1     |     | +1     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 1V to 2.5V<br>(20mV increments)                                  | -25    |     | +25    | mV         |
|                                    |               |                                                               | $V_{IN_{-}}$ = 1.25V to 3.05V<br>(10mV increments)                              | -1     |     | +1     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 0.5V to 1.25V<br>(10mV increments)                               | -12.5  |     | +12.5  | mV         |
|                                    |               | $T_A$ = -40°C to +85°C<br>( $V_{IN_{-}}$ falling)             | $V_{IN_{-}}$ = 2.5V to 5.5V<br>(20mV increments)                                | -2     |     | +2     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 1V to 2.5V<br>(20mV increments)                                  | -50    |     | +50    | mV         |
|                                    |               |                                                               | $V_{IN_{-}}$ = 1.25V to 3.05V<br>(10mV increments)                              | -2     |     | +2     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 0.5V to 1.25V<br>(10mV increments)                               | -25    |     | +25    | mV         |
| IN1/IN8 Threshold Accuracy         |               | $T_A$ = +25°C to +85°C<br>( $V_{IN_{-}}$ falling)             | $V_{IN_{-}}$ = 6.25V to 13.2V<br>(6.25V to 15.25V for IN8)<br>(50mV increments) | -1     |     | +1     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 2.5V to 6.25V<br>(50mV increments)                               | -62.5  |     | +62.5  | mV         |
|                                    |               |                                                               | $V_{IN_{-}}$ = 3.125V to 7.625V<br>(25mV increments)                            | -1     |     | +1     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 1.25V to 3.125V<br>(25mV increments)                             | -31.25 |     | +31.25 | mV         |
|                                    |               | $T_A$ = -40°C to +85°C<br>( $V_{IN_{-}}$ falling)             | $V_{IN_{-}}$ = 6.25V to 13.2V<br>(6.25V to 15.25V for IN8)<br>(50mV increments) | -2     |     | +2     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 2.5V to 6.25V<br>(50mV increments)                               | -125   |     | +125   | mV         |
|                                    |               |                                                               | $V_{IN_{-}}$ = 3.125V to 7.625V<br>(25mV increments)                            | -2     |     | +2     | %          |
|                                    |               |                                                               | $V_{IN_{-}}$ = 1.25V to 3.125V<br>(25mV increments)                             | -62.5  |     | +62.5  | mV         |
| IN <sub>-</sub> Threshold Accuracy |               | IN <sub>-</sub> = 0.6V in high-Z mode ( $V_{IN_{-}}$ falling) | $T_A$ = +25°C to +85°C                                                          | -1     |     | +1     | %          |
|                                    |               |                                                               | $T_A$ = -40°C to 85°C                                                           | -2     |     | +2     |            |
| Threshold Hysteresis               | $V_{TH-HYST}$ |                                                               |                                                                                 | 0.3    |     |        | % $V_{TH}$ |

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN1}$  = 6.5V to 13.2V,  $V_{IN2}$ – $V_{IN7}$  = 2.7V to 5.5V,  $V_{IN8}$  = 10V,  $GPI_{-}$  = GND,  $\overline{MARGIN}$  =  $\overline{MR}$  = DBP,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Notes 1, 2, 3)

| PARAMETER                                                       | SYMBOL                    | CONDITIONS                                           |     | MIN   | TYP    | MAX   | UNITS            |
|-----------------------------------------------------------------|---------------------------|------------------------------------------------------|-----|-------|--------|-------|------------------|
| Reset-Threshold Temperature Coefficient                         | $\Delta V_{TH}/^{\circ}C$ |                                                      |     | 10    |        |       | ppm/ $^{\circ}C$ |
| Threshold-Voltage Differential Nonlinearity                     | $V_{TH}$ DNL              |                                                      |     | -1    |        | +1    | LSB              |
| IN1 Input Leakage Current                                       | $I_{LIN1}$                | For $V_{IN1}$ < the highest of $V_{IN2}$ – $V_{IN5}$ |     | 100   |        | 140   | $\mu A$          |
| IN2–IN7 Input Impedance                                         | $R_{IN2}$ to $R_{IN7}$    | $V_{IN1} > 6.5V$                                     |     | 290   | 400    | 555   | k $\Omega$       |
| IN8 Input Impedance                                             | $R_{IN8}$                 |                                                      |     | 730   | 1000   | 1400  | k $\Omega$       |
| IN2–IN8 Input Leakage Current                                   | $I_{LIN2-LIN8}$           | IN2–IN8 in high-Z mode, $V_{IN-} = 1.017V$           |     | -50   |        | +50   | nA               |
| Power-Up Delay                                                  | $t_{PU}$                  | $V_{CC} \geq V_{UVLO}$                               |     |       |        | 3     | ms               |
| IN_ to PO_ Delay                                                | $t_{DPO}$                 | $V_{IN-}$ falling or rising, 100mV overdrive         |     | 20    |        |       | $\mu s$          |
| PO_ Timeout Period                                              | $t_{RP}$                  | Register contents (Table 19)                         | 000 | 8     | 25     | 80    | $\mu s$          |
|                                                                 |                           |                                                      | 001 | 1.406 | 1.5625 | 1.719 | ms               |
|                                                                 |                           |                                                      | 010 | 5.625 | 6.25   | 6.875 |                  |
|                                                                 |                           |                                                      | 011 | 22.5  | 25     | 27.5  |                  |
|                                                                 |                           |                                                      | 100 | 45    | 50     | 55    |                  |
|                                                                 |                           |                                                      | 101 | 180   | 200    | 220   |                  |
|                                                                 |                           |                                                      | 110 | 360   | 400    | 440   |                  |
|                                                                 |                           |                                                      | 111 | 1440  | 1600   | 1760  |                  |
| PO_ Output Low                                                  | $V_{OL}$                  | $I_{SINK} = 4mA$ , output asserted                   |     | 0.4   |        |       | V                |
| PO_ Output Initial Pulldown Current                             | $I_{PD}$                  | $V_{CC} \leq V_{UVLO}$ , $V_{PO} = 0.8V$             |     | 10    |        | 40    | $\mu A$          |
| PO_ Output Open-Drain Leakage Current                           | $I_{LKG}$                 | Output high impedance                                |     | -1    |        | +1    | $\mu A$          |
| PO_ Output Pullup Resistance                                    | $R_{PU}$                  | $V_{PO-} = 2V$                                       |     | 6.6   | 10     | 15.0  | k $\Omega$       |
| $\overline{MR}$ , $\overline{MARGIN}$ , $GPI_{-}$ Input Voltage | $V_{IL}$                  |                                                      |     | 0.6   |        |       | V                |
|                                                                 | $V_{IH}$                  |                                                      |     | 1.4   |        |       |                  |
| $\overline{MR}$ Input Pulse Width                               | $t_{MR}$                  |                                                      |     | 1     |        |       | $\mu s$          |
| $\overline{MR}$ Glitch Rejection                                |                           |                                                      |     | 100   |        |       | ns               |
| $\overline{MR}$ to PO_ Delay                                    | $t_{DMR}$                 |                                                      |     | 2     |        |       | $\mu s$          |
| $\overline{MR}$ to DBP Pullup Current                           | $I_{MR}$                  | $V_{\overline{MR}} = 1.4V$                           |     | 5     | 10     | 15    | $\mu A$          |
| $\overline{MARGIN}$ to DBP Pullup Current                       | $I_{MARGIN}$              | $V_{\overline{MARGIN}} = 1.4V$                       |     | 5     | 10     | 15    | $\mu A$          |
| $GPI_{-}$ Input Hysteresis                                      |                           |                                                      |     | 100   |        |       | mV               |
| $GPI_{-}$ to PO_ Delay                                          | $t_{DGPI_{-}}$            |                                                      |     | 200   |        |       | ns               |
| $GPI_{-}$ Pulldown Current                                      | $I_{GPI_{-}}$             | $V_{GPI_{-}} = 0.6V$                                 |     | 5     | 10     | 15    | $\mu A$          |
| Watchdog Input Pulse Width                                      | $t_{WDI}$                 | $GPI_{-}$ configured as a watchdog input             |     | 50    |        |       | ns               |

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN1}$  = 6.5V to 13.2V,  $V_{IN2}$ – $V_{IN7}$  = 2.7V to 5.5V,  $V_{IN8}$  = 10V,  $GPI_{-}$  = GND,  $\overline{MARGIN} = \overline{MR} = DBP$ ,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Notes 1, 2, 3)

| PARAMETER                                 | SYMBOL           | CONDITIONS                      |     | MIN   | TYP    | MAX    | UNITS |
|-------------------------------------------|------------------|---------------------------------|-----|-------|--------|--------|-------|
| Watchdog Timeout Period                   | tWD              | Register contents<br>(Table 21) | 000 | 5.625 | 6.25   | 6.875  | ms    |
|                                           |                  |                                 | 001 | 22.5  | 25     | 27.5   |       |
|                                           |                  |                                 | 010 | 90    | 100    | 110    |       |
|                                           |                  |                                 | 011 | 360   | 400    | 440    |       |
|                                           |                  |                                 | 100 | 1.44  | 1.60   | 1.76   | s     |
|                                           |                  |                                 | 101 | 5.76  | 6.40   | 7.04   |       |
|                                           |                  |                                 | 110 | 23.04 | 25.60  | 28.16  |       |
|                                           |                  |                                 | 111 | 92.16 | 102.40 | 112.64 |       |
| SERIAL INTERFACE LOGIC (SDA, SCL, A0, A1) |                  |                                 |     |       |        |        |       |
| Logic-Input Low Voltage                   | V <sub>IL</sub>  |                                 |     |       | 0.8    | V      |       |
| Logic-Input High Voltage                  | V <sub>IH</sub>  |                                 | 2.0 |       |        | V      |       |
| Input Leakage Current                     | I <sub>LKG</sub> |                                 | -1  |       | +1     | μA     |       |
| Output Low Voltage                        | V <sub>OL</sub>  | I <sub>SINK</sub> = 3mA         |     |       | 0.4    | V      |       |
| Input/Output Capacitance                  | C <sub>I/O</sub> |                                 |     | 10    |        | pF     |       |

## SERIAL INTERFACE TIMING CHARACTERISTICS (Figure 3)

( $IN1$  = GND,  $V_{IN2}$ – $V_{IN7}$  = 2.7V to 5.5V,  $V_{IN8}$  = 10V,  $GPI_{-}$  = GND,  $\overline{MARGIN} = \overline{MR} = DBP$ ,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C.) (Notes 1, 2, 3)

| PARAMETER                         | SYMBOL       | CONDITIONS        | MIN                        | TYP                       | MAX | UNITS |
|-----------------------------------|--------------|-------------------|----------------------------|---------------------------|-----|-------|
| Serial Clock Frequency            | $f_{SCL}$    |                   |                            |                           | 400 | kHz   |
| Clock Low Period                  | $t_{LOW}$    |                   | 1.3                        |                           |     | μs    |
| Clock High Period                 | $t_{HIGH}$   |                   | 0.6                        |                           |     | μs    |
| Bus-Free Time                     | $t_{BUF}$    |                   | 1.3                        |                           |     | μs    |
| START Setup Time                  | $t_{SU:STA}$ |                   | 0.6                        |                           |     | μs    |
| START Hold Time                   | $t_{HD:STA}$ |                   | 0.6                        |                           |     | μs    |
| STOP Setup Time                   | $t_{SU:STO}$ |                   | 0.6                        |                           |     | μs    |
| Data In Setup Time                | $t_{SU:DAT}$ |                   | 100                        |                           |     | ns    |
| Data In Hold Time                 | $t_{HD:DAT}$ |                   | 30                         |                           | 900 | ns    |
| Receive SCL/SDA Minimum Rise Time | $t_R$        | (Note 5)          |                            | $20 + 0.1 \times C_{BUS}$ |     | ns    |
| Receive SCL/SDA Maximum Rise Time | $t_R$        | (Note 5)          |                            | 300                       |     | ns    |
| Receive SCL/SDA Minimum Fall Time | $t_F$        | (Note 5)          |                            | $20 + 0.1 \times C_{BUS}$ |     | ns    |
| Receive SCL/SDA Maximum Fall Time | $t_F$        | (Note 5)          |                            | 300                       |     | ns    |
| Transmit SDA Fall Time            | $t_F$        | $C_{BUS} = 400pF$ | $20 + 0.04 \times C_{BUS}$ |                           | 300 | ns    |

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## SERIAL INTERFACE TIMING CHARACTERISTICS (Figure 3) (continued)

(IN1 = GND, VIN2–VIN7 = 2.7V to 5.5V, VIN8 = 10V, GPI\_ = GND, MARGIN = MR = DBP, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Notes 1, 2, 3)

| PARAMETER                       | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--------|------------|-----|-----|-----|-------|
| Pulse Width of Spike Suppressed | tSP    | (Note 6)   |     | 50  |     | ns    |
| EEPROM Byte Write Cycle Time    | tWR    | (Note 7)   |     |     | 11  | ms    |

**Note 1:** 100% production tested at TA = +25°C and TA = +85°C. Specifications at TA = -40°C are guaranteed by design.

**Note 2:** Specifications are guaranteed for the stated global conditions. The device also meets the parameters specified when 0 < VIN1 < 6.5V and at least one of VIN2–VIN5 is between 2.7V and 5.5V, while the remaining VIN2–VIN5 are between 0 and 5.5V. Specifications are also guaranteed if VCC is externally supplied.

**Note 3:** Device may be supplied from any one of IN1 to IN5, or VCC (see the *Powering the MAX6889/MAX6890/MAX6891* section).

**Note 4:** The internal supply voltage, measured at VCC, equals the maximum of IN2 to IN5 if VIN1 = 0V, or equals 5.4V if VIN1 > 6.5V. For 4V < VIN1 < 6.5V and VIN2–VIN5 > 2.7V, the input that powers the device cannot be determined.

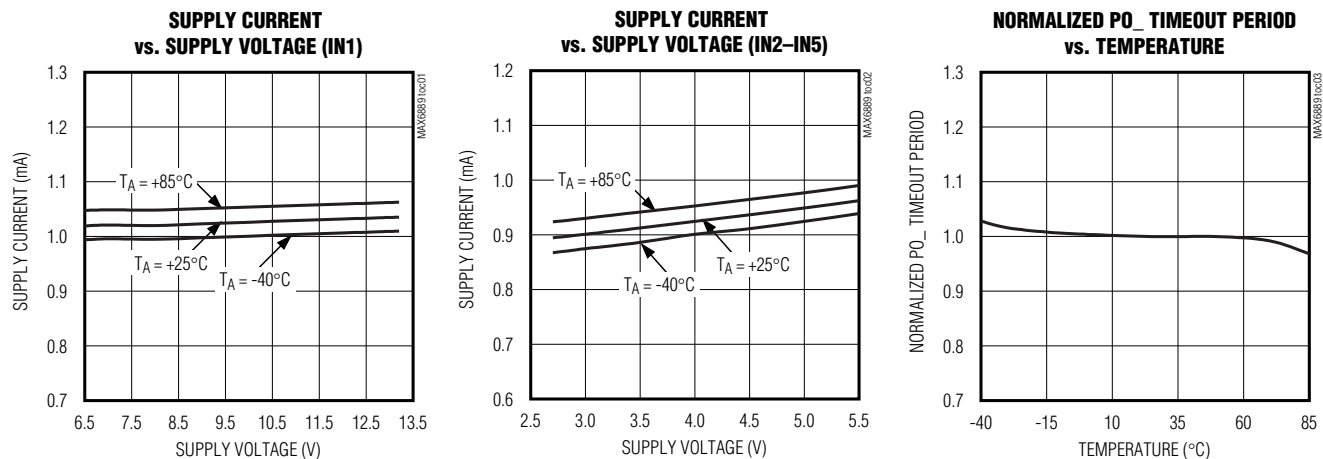
**Note 5:** CBUS = total capacitance of one bus line in pF. Rise and fall times are measured between 0.1 × VBUS and 0.9 × VBUS.

**Note 6:** Input filters on SDA, SCL, A0, and A1 suppress noise spikes < 50ns.

**Note 7:** An additional cycle is required when writing to configuration memory for the first time.

## Typical Operating Characteristics

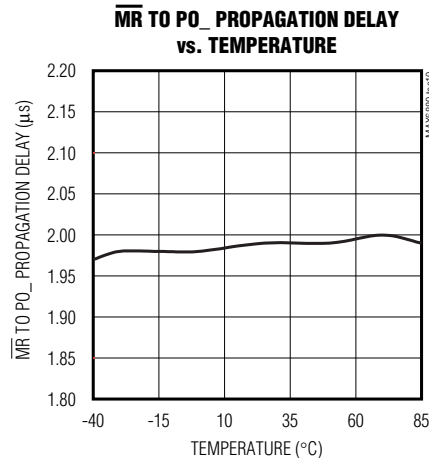
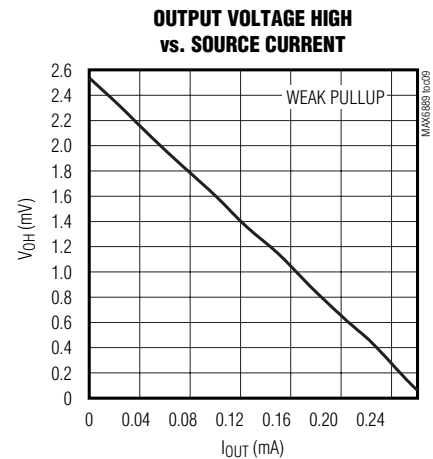
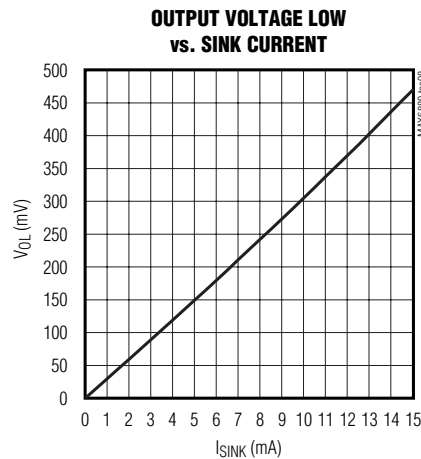
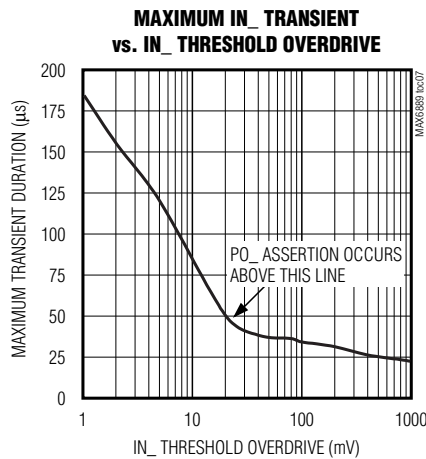
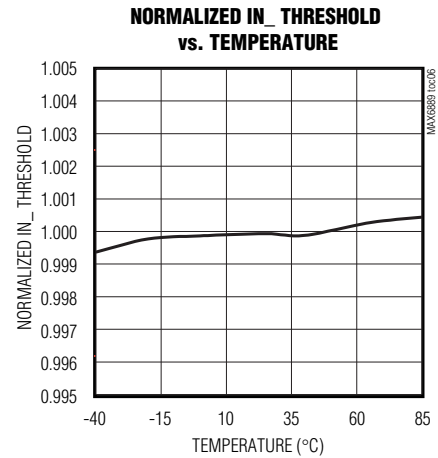
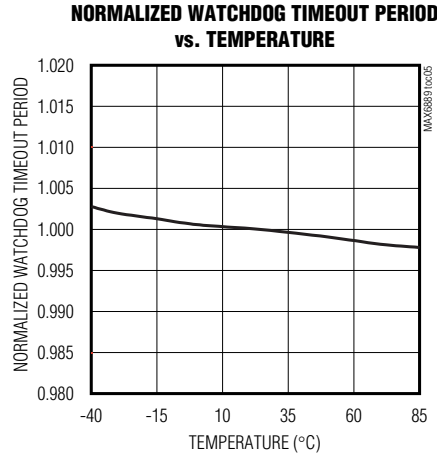
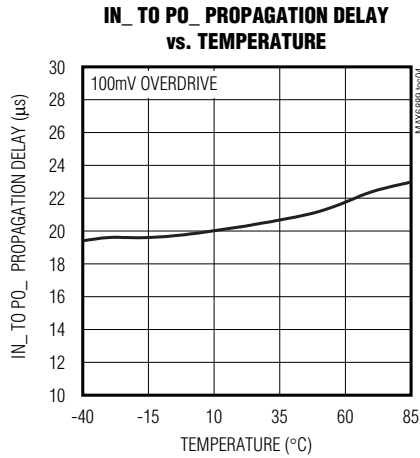
(VIN1 = 6.5V to 13.2V, VIN8 = 10V, VIN\_ = 2.7V to 5.5V, GPI\_ = GND, MARGIN = MR = DBP, TA = +25°C, unless otherwise noted.)



# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

## Typical Operating Characteristics (continued)

( $V_{IN1} = 6.5V$  to  $13.2V$ ,  $V_{IN8} = 10V$ ,  $V_{IN\_} = 2.7V$  to  $5.5V$ ,  $GPI\_ = GND$ ,  $\overline{MARGIN} = \overline{MR} = DBP$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

## Pin Description

| PIN     |         |         | NAME                       | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                            |
|---------|---------|---------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX6889 | MAX6890 | MAX6891 |                            |                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1       | 1       | 1       | PO2                        | Programmable Output 2. Configurable, active-high, active-low, open-drain, or weak pullup output. PO2 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO2 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 2       | 2       | 2       | PO3                        | Programmable Output 3. Configurable, active-high, active-low, open-drain, or weak pullup output. PO3 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO3 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 3       | 3       | 3       | PO4                        | Programmable Output 4. Configurable, active-high, active-low, open-drain, or weak pullup output. PO4 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO4 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 4       | 4       | 4       | GND                        | Ground                                                                                                                                                                                                                                                                                                                                                                                              |
| 5       | 5       | 5       | PO5                        | Programmable Output 5. Configurable, active-high, active-low, open-drain, or weak pullup output. PO5 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO5 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 6       | 6       | —       | PO6                        | Programmable Output 6. Configurable, active-high, active-low, open-drain, or weak pullup output. PO6 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO6 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 7       | 7       | —       | PO7                        | Programmable Output 7. Configurable, active-high, active-low, open-drain, or weak pullup output. PO7 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO7 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 8       | 8       | —       | PO8                        | Programmable Output 8. Configurable, active-high, active-low, open-drain, or weak pullup output. PO8 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO8 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                      |
| 9       | —       | —       | PO9                        | Programmable Output 9. Configurable, active-high, active-low, open-drain, or weak pullup output. PO9 pulls low with a 10µA internal current sink for $+1V < V_{CC} < V_{UVLO}$ . PO9 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                     |
| 10      | —       | —       | PO10                       | Programmable Output 10. Configurable, active-high, active-low, open-drain, or weak pullup output. PO10 pulls low with a 10µA internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO10 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V.                                                                                                   |
| 11      | 9       | 6       | $\overline{\text{MARGIN}}$ | Margin Input. $\overline{\text{MARGIN}}$ holds PO <sub>n</sub> in its existing state when $\overline{\text{MARGIN}}$ is driven low. Leave $\overline{\text{MARGIN}}$ unconnected or connect to DBP if unused. $\overline{\text{MARGIN}}$ overrides $\overline{\text{MR}}$ if both assert at the same time. $\overline{\text{MARGIN}}$ is internally pulled up to DBP through a 10µA current source. |

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## Pin Description (continued)

| PIN     |         |         | NAME                   | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                            |
|---------|---------|---------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX6889 | MAX6890 | MAX6891 |                        |                                                                                                                                                                                                                                                                                                                                                                                                     |
| 12      | 10      | 7       | $\overline{\text{MR}}$ | Manual Reset Input. $\overline{\text{MR}}$ is configurable to either assert $\text{PO}_\text{L}$ into a programmed state or to have no effect on $\text{PO}_\text{L}$ when driving $\overline{\text{MR}}$ low (see Table 6). Leave $\overline{\text{MR}}$ unconnected or connect to DBP if unused. $\overline{\text{MR}}$ is internally pulled up to DBP through a 10 $\mu\text{A}$ current source. |
| 13      | 11      | 8       | SDA                    | Serial Data Input/Output (Open Drain). SDA requires an external pullup resistor.                                                                                                                                                                                                                                                                                                                    |
| 14      | 12      | 9       | SCL                    | Serial Clock Input. SCL requires an external pullup resistor.                                                                                                                                                                                                                                                                                                                                       |
| 15      | 13      | 10      | A0                     | Address Input 0. Address inputs allow up to four (MAX6889/MAX6890) or two (MAX6891) connections on one common bus. Connect A0 to GND or to the serial-interface power supply.                                                                                                                                                                                                                       |
| 16      | 14      | —       | A1                     | Address Input 1. Address inputs allow up to four MAX6889/MAX6890 connections on one common bus. Connect A1 to GND or to the serial-interface power supply.                                                                                                                                                                                                                                          |
| 17      | 15      | —       | GPI4                   | General-Purpose Logic Input 4. An internal 10 $\mu\text{A}$ current source pulls GPI4 to GND. Configure GPI4 to control watchdog timer functions or the programmable outputs.                                                                                                                                                                                                                       |
| 18      | 16      | 11      | GPI3                   | General-Purpose Logic Input 3. An internal 10 $\mu\text{A}$ current source pulls GPI3 to GND. Configure GPI3 to control watchdog timer functions or the programmable outputs.                                                                                                                                                                                                                       |
| 19      | 17      | 12      | GPI2                   | General-Purpose Logic Input 2. An internal 10 $\mu\text{A}$ current source pulls GPI2 to GND. Configure GPI2 to control watchdog timer functions or the programmable outputs.                                                                                                                                                                                                                       |
| 20      | 18      | 13      | GPI1                   | General-Purpose Logic Input 1. An internal 10 $\mu\text{A}$ current source pulls GPI1 to GND. Configure GPI1 to control watchdog timer functions or the programmable outputs.                                                                                                                                                                                                                       |
| 21      | 19      | 14      | VCC                    | Internal Power-Supply Voltage. Bypass VCC to GND with a 1 $\mu\text{F}$ ceramic capacitor. VCC supplies power to the internal circuitry. VCC is internally powered from the highest of the monitored IN1–IN5 voltages. Do not use VCC to supply power to external circuitry. To externally supply VCC, see the <i>Powering the MAX6889/MAX6890/MAX6891</i> section.                                 |
| 22      | 20      | 15      | DBP                    | Internal Digital Power-Supply Voltage. Bypass DBP to GND with a 1 $\mu\text{F}$ ceramic capacitor. DBP supplies power to the EEPROM memory, the internal logic circuitry, and the programmable outputs. Do not use DBP to supply power to external circuitry.                                                                                                                                       |
| 23      | —       | —       | IN8                    | High-Voltage Input 8. Configure IN8 to detect voltage thresholds from 2.5V to 15.25V in 50mV increments, or 1.25V to 7.625V in 25mV increments. For improved noise immunity, bypass IN8 to GND with a 0.1 $\mu\text{F}$ capacitor installed as close to the device as possible.                                                                                                                     |
| 24      | —       | —       | IN7                    | Voltage Input 7. Configure IN7 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN7 to GND with a 0.1 $\mu\text{F}$ capacitor installed as close to the device as possible.                                                                                                                            |

MAX6889/MAX6890/MAX6891

# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

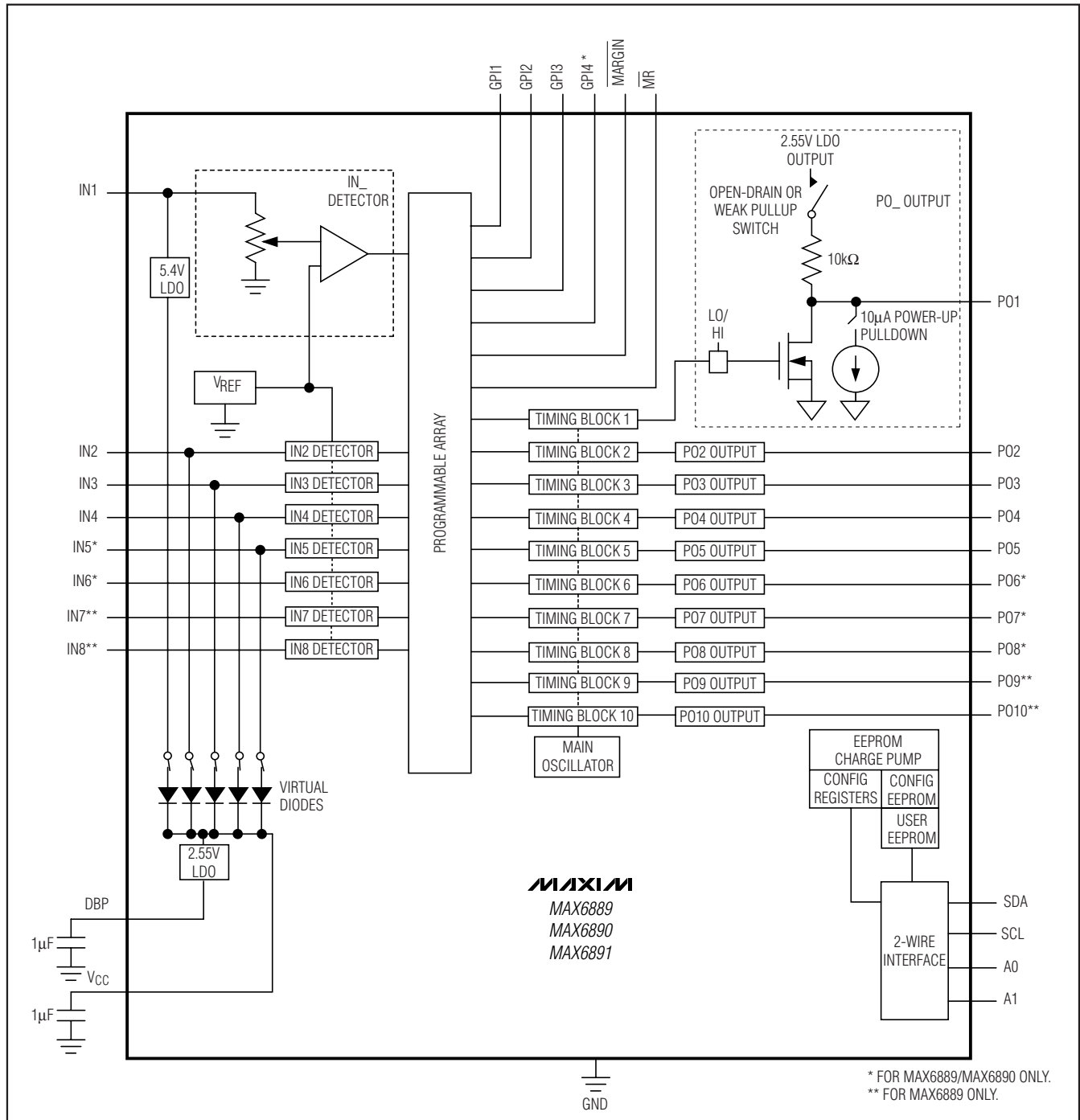
## Pin Description (continued)

| PIN     |         |         | NAME | FUNCTION                                                                                                                                                                                                                                                                                             |
|---------|---------|---------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX6889 | MAX6890 | MAX6891 |      |                                                                                                                                                                                                                                                                                                      |
| 25      | 21      | —       | IN6  | Voltage Input 6. Configure IN6 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN6 to GND with a 0.1 $\mu$ F capacitor installed as close to the device as possible.                                   |
| 26      | 22      | —       | IN5  | Voltage Input 5. Configure IN5 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN5 to GND with a 0.1 $\mu$ F capacitor installed as close to the device as possible.                                   |
| 27      | 23      | 16      | IN4  | Voltage Input 4. Configure IN4 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN4 to GND with a 0.1 $\mu$ F capacitor installed as close to the device as possible.                                   |
| 28      | 24      | 17      | IN3  | Voltage Input 3. Configure IN3 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN3 to GND with a 0.1 $\mu$ F capacitor installed as close to the device as possible.                                   |
| 29      | 25      | 18      | IN2  | Voltage Input 2. Configure IN2 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN2 to GND with a 0.1 $\mu$ F capacitor installed as close to the device as possible.                                   |
| 30      | 26      | 19      | IN1  | High-Voltage Input 1. Configure IN1 to detect voltage thresholds from 2.5V to 13.2V in 50mV increments, or 1.25V to 7.625V in 25mV increments. For improved noise immunity, bypass IN1 to GND with a 0.1 $\mu$ F capacitor installed as close to the device as possible.                             |
| 31      | 27      | —       | N.C. | No Connection. Not internally connected.                                                                                                                                                                                                                                                             |
| 32      | 28      | 20      | PO1  | Programmable Output 1. Configurable, active-high, active-low, open-drain, or weak pullup output. PO1 pulls low with a 10 $\mu$ A internal current sink for $1V < V_{CC} < V_{UVLO}$ . PO1 assumes its programmed conditional output state when $V_{CC}$ exceeds undervoltage lockout (UVLO) of 2.5V. |
| EP      | EP      | EP      | GND  | Exposed Paddle. Internally connected to GND. Connect exposed paddle to GND or leave floating.                                                                                                                                                                                                        |

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## Functional Diagram

MAX6889/MAX6890/MAX6891



# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

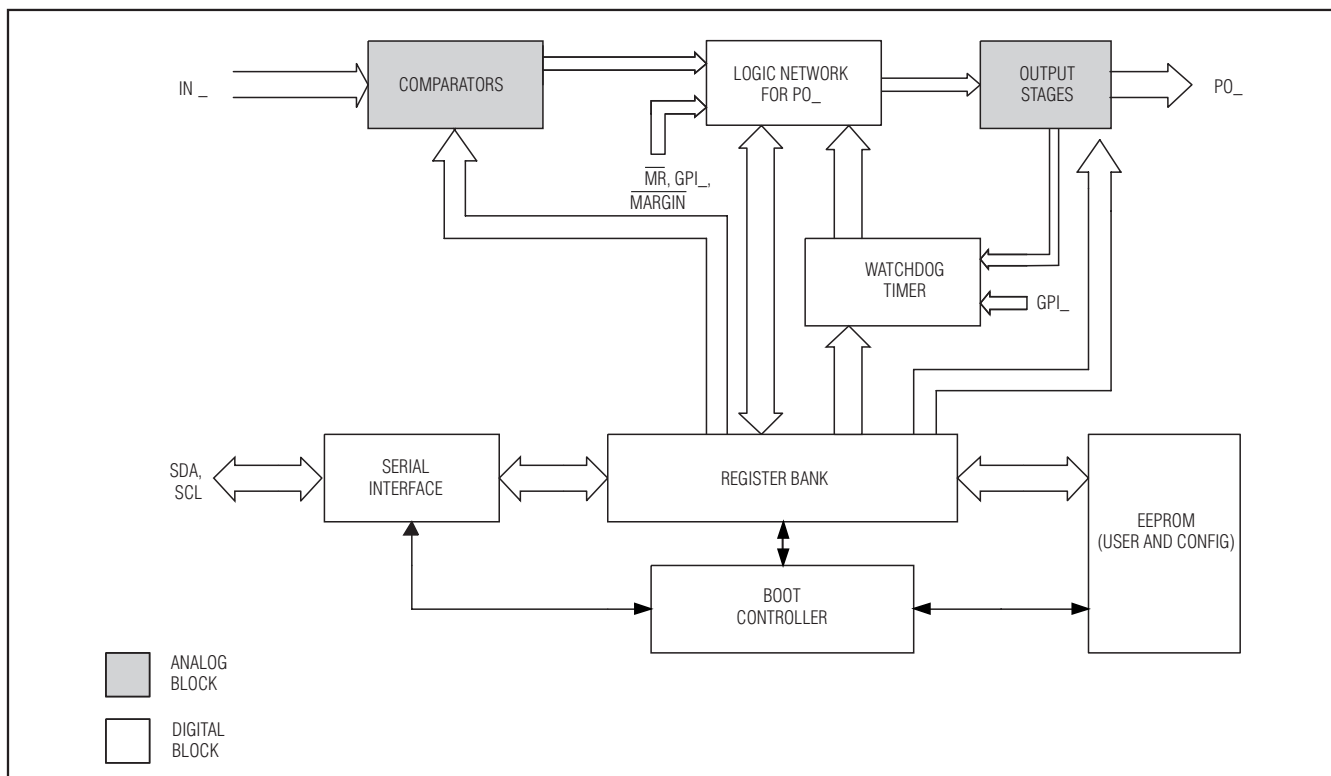


Figure 1. Top-Level Block Diagram

## Detailed Description

The MAX6889/MAX6890/MAX6891 EEPROM-configurable, multivoltage supply sequencers/supervisors monitor several voltage detector inputs and general-purpose logic inputs, and feature programmable outputs for highly-configurable power-supply sequencing applications. The MAX6889 features eight voltage detector inputs and ten programmable outputs. The MAX6890 features six voltage detector inputs and eight programmable outputs, while the MAX6891 features four voltage detector inputs and five programmable outputs. Manual reset and margin disable inputs simplify board-level testing during the manufacturing process.

All voltage detectors provide configurable thresholds for undervoltage detection. The high-voltage input (IN1) monitors voltages from 1.25V to 7.625V in 25mV increments, or 2.5V to 13.2V in 50mV increments. Inputs (IN2–IN7) monitor voltages from 0.5V to 3.05V in 10mV increments, or 1.0V to 5.5V in 20mV increments. An additional high-voltage input (IN8, MAX6889 only) monitors voltages from 1.25V to 7.625V in 25mV increments, or 2.5V to 15.25V in 50mV increments. To

monitor thresholds from 0.1667V to 1.0167V in 3.3mV increments, the respective input voltage detector must be programmed for high impedance (high-Z) and an external voltage-divider must be connected.

The host controller communicates with the MAX6889/MAX6890/MAX6891s' internal 512-bit user EEPROM, configuration EEPROM, and configuration registers through an SMBus/I<sup>2</sup>C-compatible serial interface (see Figure 1).

Programmable output options include active-high, active-low, open drain, and weak pullup. Program each output to assert on any voltage detector input, general-purpose logic input, watchdog timer, or manual reset. Programmable timing delay blocks configure each output to wait between 25μs and 1600ms before deasserting.

The MAX6889/MAX6890/MAX6891 feature a watchdog timer for added flexibility. Program the watchdog timer to assert one or more programmable outputs. Program the watchdog timer to clear on a combination of one GPI<sub>L</sub> input and one programmable output, one of the GPI<sub>L</sub> inputs only, or one of the programmable outputs only. The initial and normal watchdog timeout periods are independently programmable from 6.25ms to 102.4s.

# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

MAX6889/MAX6890/MAX6891

**Table 1. Programmable Features**

| FEATURE                                                                                | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| High-Voltage Input IN1                                                                 | <ul style="list-style-type: none"> <li>2.5V to 13.2V threshold in 50mV increments.</li> <li>1.25V to 7.625V threshold in 25mV increments.</li> </ul>                                                                                                                                                                                                                                                                                                               |
| Positive Voltage Input<br>IN2–IN7 (MAX6889)<br>IN2–IN6 (MAX6890)<br>IN2–IN4 (MAX6891)  | <ul style="list-style-type: none"> <li>1V to 5.5V threshold in 20mV increments.</li> <li>0.5V to 3.05V threshold in 10mV increments.</li> <li>0.1667V to 1.0167V threshold in 3.3mV increments in high-Z mode.</li> </ul>                                                                                                                                                                                                                                          |
| High-Voltage Input IN8<br>(MAX6889)                                                    | <ul style="list-style-type: none"> <li>2.5V to 15.25V threshold in 50mV increments.</li> <li>1.25V to 7.625V threshold in 25mV increments.</li> <li>0.1667V to 1.0167V threshold in 3.3mV increments in high-Z mode.</li> </ul>                                                                                                                                                                                                                                    |
| Programmable Outputs<br>PO1–PO10 (MAX6889)<br>PO1–PO8 (MAX6890)<br>PO1–PO5 (MAX6891)   | <ul style="list-style-type: none"> <li>Active-high or active-low.</li> <li>Open-drain or weak pullup output.</li> <li>Dependent on <math>\overline{MR}</math>, <math>\overline{MARGIN}</math>, <math>IN_{-}</math>, <math>GPI_{-}</math>, and <math>WD</math>.</li> <li>Programmable reset timeout periods of 25<math>\mu</math>s, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s.</li> </ul>                                                                 |
| General-Purpose Logic Inputs:<br>GPI1–GPI4<br>(MAX6889–MAX6890)<br>GPI1–GPI3 (MAX6891) | <ul style="list-style-type: none"> <li>Active-high or active-low logic levels.</li> <li>Configure <math>GPI_{-}</math> as inputs to the watchdog timer or the programmable output stages.</li> </ul>                                                                                                                                                                                                                                                               |
| Watchdog Timer                                                                         | <ul style="list-style-type: none"> <li>Clear dependent on any combination of one <math>GPI_{-}</math> input and one programmable output, a <math>GPI_{-}</math> input only, or a programmable output only.</li> <li>Initial watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s.</li> <li>Normal watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s.</li> <li>Watchdog enable/disable.</li> </ul> |
| Manual Reset Input ( $\overline{MR}$ )                                                 | <ul style="list-style-type: none"> <li>Forces <math>PO_{-}</math> into the active output state when <math>\overline{MR} = GND</math>.</li> <li><math>PO_{-}</math> deassert after <math>\overline{MR}</math> releases high and the <math>PO_{-}</math> timeout period expires.</li> </ul>                                                                                                                                                                          |
| VCC Power Mode                                                                         | Programs whether the device is powered from the highest $IN_{-}$ input or from an external supply connected to $V_{CC}$ .                                                                                                                                                                                                                                                                                                                                          |
| Write Disable                                                                          | Locks user EEPROM based on $PO_{-}$ .                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Configuration Lock                                                                     | Locks configuration registers and EEPROM.                                                                                                                                                                                                                                                                                                                                                                                                                          |

## Powering the MAX6889/MAX6890/MAX6891

The MAX6889/MAX6890/MAX6891 derive power from the voltage detector inputs: IN1–IN5 (MAX6889/MAX6890), IN1–IN4 (MAX6891), or an external  $V_{CC}$  supply. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). IN1 must be at least 4V, or one of IN2–IN5 (MAX6889/MAX6890)/IN2–IN4 (MAX6891) must be at least 2.7V to ensure device operation. An internal LDO regulates IN1 down to 5.4V.

The highest input voltage on IN2–IN5 (MAX6889/MAX6890)/IN2–IN4 (MAX6891) supplies power to the device, unless  $V_{IN1} > 6.5V$ , in which case IN1 supplies power to the device. For  $4V < V_{IN1} < 6.5V$  and one of

$V_{IN2}–V_{IN5} > 2.7V$ , the input power source cannot be determined due to the dropout voltage of the LDO. Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

$V_{CC}$  powers the analog circuitry. Bypass  $V_{CC}$  to GND with a 1 $\mu$ F ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at  $V_{CC}$ , equals the maximum of IN2–IN5 if  $V_{IN1} = 0V$ , or equals 5.4V when  $V_{IN1} > 6.5V$ . Do not use the internally generated  $V_{CC}$  to provide power to external circuitry. Power cannot be supplied through high-impedance voltage detector inputs. To externally supply power through  $V_{CC}$ :

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- 1) Apply a voltage between 2.7V and 5.5V to one of V<sub>CC</sub> or IN2–IN5.
- 2) Program the internal/external V<sub>CC</sub> power EEPROM at AEh, Bit[2] = 1 (see Table 22).
- 3) Power down the device.

Subsequent power-ups and software reboots require an externally supplied V<sub>CC</sub> to ensure the device is fully operational.

The MAX6889/MAX6890/MAX6891 also generate a digital supply voltage (DBP) for the internal logic circuitry and the EEPROM. Bypass DBP to GND with a 1μF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is 2.55V. Do not use DBP to provide power to external circuitry.

## Inputs

The MAX6889/MAX6890/MAX6891 contain multiple logic and voltage detector inputs. Each voltage detector input is monitored for undervoltage thresholds. Table 1 summarizes these various inputs. Set the threshold voltage for each voltage detector input with registers 00h–07h. Each threshold voltage is an undervoltage threshold. Set the threshold range for each voltage detector with register 08h.

### High-Voltage Input (IN1)

IN1 offers threshold voltages of 2.5V to 13.2V in 50mV increments, or 1.25V to 7.625V in 25mV increments. Use the following equations to set the threshold voltages for IN1:

$$x = \frac{V_{TH} - 2.5V}{0.05V} \text{ for 2.5V to 13.2V range}$$

$$x = \frac{V_{TH} - 1.25V}{0.025V} \text{ for 1.25V to 7.625V range}$$

where V<sub>TH</sub> is the desired threshold voltage and x is the decimal code for the desired threshold (Table 2). For the 2.5V to 13.2V range, x must equal 214 or less; otherwise

the threshold exceeds the maximum operating voltage of IN1.

### IN2–IN7

The IN2–IN7 positive voltage detectors monitor voltages from 1V to 5.5V in 20mV increments, 0.5V to 3.05V in 10mV increments, or 0.1667V to 1.0167V in 3.3mV increments in high-Z mode. Use the following equations to set the threshold voltages for IN<sub>x</sub>:

$$x = \frac{V_{TH} - 1V}{0.02V} \text{ for 1V to 5.5V range}$$

$$x = \frac{V_{TH} - 0.5V}{0.1V} \text{ for 0.5V to 3.05V range}$$

$$x = \frac{V_{TH} - 0.1667V}{0.0033V} \text{ for 0.1667V to 1.0167V high-Z range}$$

where V<sub>TH</sub> is the desired threshold voltage and x is the decimal code for the desired threshold (Table 3). For the 1V to 5.5V range, x must equal 225 or less; otherwise the threshold exceeds the maximum operating voltage of IN2–IN7.

### High-Voltage Input (IN8)

Configure IN8 to detect positive thresholds from 2.5V to 15.25V in 50mV increments, 1.25V to 7.625V in 25mV increments, or 0.1667V to 1.0167V in 3.3mV increments in high-Z mode. Use the following equations to set the threshold voltages for IN8:

$$x = \frac{V_{TH} - 2.5V}{0.05V} \text{ for 2.5V to 15.25V range}$$

$$x = \frac{V_{TH} - 1.25V}{0.025V} \text{ for 1.25V to 7.625V range}$$

$$x = \frac{V_{TH} - 0.1667V}{0.0033V} \text{ for 0.1667V to 1.0167V high-Z range}$$

where V<sub>TH</sub> is the desired threshold voltage and x is the decimal code for the desired threshold (Table 4).

**Table 2. IN1 Threshold Settings**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                                    |
|------------------|-----------------------|-----------|----------------------------------------------------------------------------------------------------------------|
| 00h              | 80h                   | [7:0]     | IN1 undervoltage detector threshold (V1) (see equations in the <i>Inputs</i> section)                          |
| 08h              | 88h                   | [0]       | IN1 range selection. 0 = 2.5V to 13.2V range in 50mV increments. 1 = 1.25V to 7.625V range in 25mV increments. |
| 09h              | 89h                   | [0]       | Must be set to "0" for normal operation                                                                        |

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MAX6889/MAX6890/MAX6891

Table 3. IN2–IN7 Threshold Settings

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                                                     |
|------------------|-----------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------|
| 01h              | 81h                   | [7:0]     | IN2 undervoltage detector threshold (V2) (see equations in the <i>Inputs</i> section)                                           |
| 02h              | 82h                   | [7:0]     | IN3 undervoltage detector threshold (V3) (see equations in the <i>Inputs</i> section)                                           |
| 03h              | 83h                   | [7:0]     | IN4 undervoltage detector threshold (V4) (see equations in the <i>Inputs</i> section)                                           |
| 04h              | 84h                   | [7:0]     | IN5 (MAX6889/MAX6890 only) undervoltage detector threshold (V5) (see equations in the <i>Inputs</i> section)                    |
| 05h              | 85h                   | [7:0]     | IN6 (MAX6889/MAX6890 only) undervoltage detector threshold (V6) (see equations in the <i>Inputs</i> section)                    |
| 06h              | 86h                   | [7:0]     | IN7 (MAX6889 only) undervoltage detector threshold (V7) (see equations in the <i>Inputs</i> section)                            |
| 08h              | 88h                   | [1]       | IN2 range selection, 0 = 1V to 5.5V range in 20mV increments, 1 = 0.5V to 3.05V range in 10mV increments                        |
|                  |                       | [2]       | IN3 range selection, 0 = 1V to 5.5V range in 20mV increments, 1 = 0.5V to 3.05V range in 10mV increments                        |
|                  |                       | [3]       | IN4 range selection, 0 = 1V to 5.5V range in 20mV increments, 1 = 0.5V to 3.05V range in 10mV increments                        |
|                  |                       | [4]       | IN5 (MAX6889/MAX6890 only) range selection, 0 = 1V to 5.5V range in 20mV increments, 1 = 0.5V to 3.05V range in 10mV increments |
|                  |                       | [5]       | IN6 (MAX6889/MAX6890 only) range selection, 0 = 1V to 5.5V range in 20mV increments, 1 = 0.5V to 3.05V range in 10mV increments |
|                  |                       | [6]       | IN7 (MAX6889 only) range selection, 0 = 1V to 5.5V range in 20mV increments, 1 = 0.5V to 3.05V range in 10mV increments         |
|                  |                       | [7]       | Not used                                                                                                                        |
| 09h              | 89h                   | [1]       | IN2 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.                     |
|                  |                       | [2]       | IN3 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.                     |
|                  |                       | [3]       | IN4 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.                     |
|                  |                       | [4]       | IN5 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.                     |
|                  |                       | [5]       | IN6 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.                     |
|                  |                       | [6]       | IN7 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.                     |

## GPI1–GPI4

The GPI1–GPI4 (General-Purpose Input) programmable logic inputs control power-supply sequencing (programmable outputs), reset/interrupt signaling, and watchdog functions (see the *Configuring the Watchdog Timer* section). Configure GPI1–GPI4 for active-low or active-high logic (Table 5). GPI1–GPI4 internally pull down to GND through a 10μA current sink.

## $\overline{MR}$

The manual reset ( $\overline{MR}$ ) input initiates a reset condition. See Table 6 to program the PO\_ outputs to assert when  $\overline{MR}$  is low. All affected programmable outputs remain asserted (see the *Programmable Outputs* section) for their PO\_ timeout periods after  $\overline{MR}$  releases high. An internal 10μA current source pulls  $\overline{MR}$  to DBP. Leave  $\overline{MR}$  unconnected or connect to DBP if unused.

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Table 4. IN8 Threshold Settings

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                                           |
|------------------|-----------------------|-----------|-----------------------------------------------------------------------------------------------------------------------|
| 07h              | 87h                   | [7:0]     | IN8 undervoltage detector threshold (V8) (see equations in the <i>Inputs</i> section)                                 |
| 08h              | 88h                   | [7]       | IN8 range selection.<br>0 = 2.5V to 15.25V range in 50mV increments.<br>1 = 1.25V to 7.625V range in 25mV increments. |
| 09h              | 89h                   | [7]       | IN8 input impedance. 0 = normal mode. 1 = high-Z mode, with a 0.1667V to 1.0167V range in 3.3mV increments.           |

Table 5. GPI1–GPI4 Active Logic States

| REGISTER ADDRESS | EEPROM ADDRESS | BIT RANGE | DESCRIPTION                                                   |
|------------------|----------------|-----------|---------------------------------------------------------------|
| 28h              | A8h            | [0]       | GPI1. 0 = active-low, 1 = active-high.                        |
|                  |                | [1]       | GPI2. 0 = active-low, 1 = active-high.                        |
|                  |                | [2]       | GPI3. 0 = active-low, 1 = active-high.                        |
|                  |                | [3]       | GPI4 (MAX6889/MAX6890 only). 0 = active-low, 1 = active-high. |

**MARGIN** allows system-level testing while power supplies exceed the normal ranges. Driving **MARGIN** low forces the programmable outputs to hold the last state while system-level testing occurs. Leave **MARGIN** unconnected or connect to **DBP** if unused. An internal 10μA current source pulls **MARGIN** to **DBP**. The state of each programmable output does not change while **MARGIN** = **GND**. **MARGIN** overrides **MR** if both assert at the same time.

## Programmable Outputs

The MAX6889 features ten programmable outputs, the MAX6890 features eight programmable outputs, and the MAX6891 features five programmable outputs. Selectable output stage configurations include: active-low or active-high, open drain, or weak pullup. During power-up, the programmable outputs pull to **GND** with an internal 10μA current sink for  $1V < V_{CC} < V_{UVLO}$ . The programmable outputs remain in their active states until their respective **PO** timeout period expires, and all of the programmed conditions are met for each output. Any output programmed to depend on no condition always remains in its active state (Table 17). An output

configured as active-high is considered asserted when that output is logic-high.

The voltage monitors generate fault signals (logical 0) to the MAX6889/MAX6890/MAX6891s' logic array when an input voltage is below the programmed undervoltage threshold. For example, the **PO3** (Table 9) programmable output may depend on the **IN1** undervoltage threshold, and the state of **GPI1**. Write "1"s to **R10h[0]** and **R11h[1]** to configure as indicated. **IN1** must be above the undervoltage threshold (Table 2) and **GPI1** must be inactive (Table 5) to be a logic "1," then **PO3** deasserts. The logic state of **PO3**, in this example, is equivalent to the logical statement: " $V1 \cdot GPI1$ ."

Registers 0Ah through 27h configure each of the programmable outputs. Programmable timing blocks set the **PO\_** timeout period from 25μs to 1600ms for each programmable output. See Table 17 to set the active state (active-high or active-low) for each programmable output and Tables 18 and 19 to select the output stage types, and **PO\_** timeout periods for each output. Each programmable output allows a different set of conditions to assert each output as shown in Tables 7–16.

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**Table 6. Programmable Output Behavior and  $\overline{MR}$**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                                      |
|------------------|-----------------------|-----------|------------------------------------------------------------------------------------------------------------------|
| 0Bh              | 8Bh                   | [5]       | PO1. 0 = PO1 independent of $\overline{MR}$ , 1 = PO1 asserts when $\overline{MR}$ = low.                        |
| 0Eh              | 8Eh                   | [5]       | PO2. 0 = PO2 independent of $\overline{MR}$ , 1 = PO2 asserts when $\overline{MR}$ = low.                        |
| 11h              | 91h                   | [5]       | PO3. 0 = PO3 independent of $\overline{MR}$ , 1 = PO3 asserts when $\overline{MR}$ = low.                        |
| 14h              | 94h                   | [5]       | PO4. 0 = PO4/PO2 independent of $\overline{MR}$ , 1 = PO4 asserts when $\overline{MR}$ = low.                    |
| 17h              | 97h                   | [5]       | PO5. 0 = PO5 independent of $\overline{MR}$ , 1 = PO5 asserts when $\overline{MR}$ = low.                        |
| 1Ah              | 9Ah                   | [5]       | PO6 (MAX6889/MAX6890 only). 0 = PO6 independent of $\overline{MR}$ , 1 = PO6 asserts when $\overline{MR}$ = low. |
| 1Dh              | 9Dh                   | [5]       | PO7 (MAX6889/MAX6890 only). 0 = PO7 independent of $\overline{MR}$ , 1 = PO7 asserts when $\overline{MR}$ = low. |
| 20h              | A0h                   | [5]       | PO8 (MAX6889/MAX6890 only). 0 = PO8 independent of $\overline{MR}$ , 1 = PO8 asserts when $\overline{MR}$ = low. |
| 23h              | A3h                   | [5]       | PO9 (MAX6889 only). 0 = PO9 independent of $\overline{MR}$ , 1 = PO9 asserts when $\overline{MR}$ = low.         |
| 26h              | A6h                   | [5]       | PO10 (MAX6889 only). 0 = PO10 independent of $\overline{MR}$ , 1 = PO10 asserts when $\overline{MR}$ = low.      |

**Table 7. PO1 Output Dependency**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                              |
|------------------|-----------------------|-------|------------------------------------------------------------------------------------------|
| 0Ah              | 8Ah                   | [0]   | 1 = PO1 assertion depends on IN1 undervoltage threshold (Table 2)                        |
|                  |                       | [1]   | 1 = PO1 assertion depends on IN2 undervoltage threshold (Table 3)                        |
|                  |                       | [2]   | 1 = PO1 assertion depends on IN3 undervoltage threshold (Table 3)                        |
|                  |                       | [3]   | 1 = PO1 assertion depends on IN4 undervoltage threshold (Table 3)                        |
|                  |                       | [4]   | 1 = PO1 assertion depends on IN5 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO1 assertion depends on IN6 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO1 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3)         |
|                  |                       | [7]   | 1 = PO1 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4)         |
| 0Bh              | 8Bh                   | [0]   | 1 = PO1 assertion depends on watchdog (Table 20)                                         |
|                  |                       | [1]   | 1 = PO1 assertion depends on GPI1 (Table 5)                                              |
|                  |                       | [2]   | 1 = PO1 assertion depends on GPI2 (Table 5)                                              |
|                  |                       | [3]   | 1 = PO1 assertion depends on GPI3 (Table 5)                                              |
|                  |                       | [4]   | 1 = PO1 assertion depends on GPI4 (MAX6889/MAX6890 only) (Table 5)                       |
|                  |                       | [5]   | 1 = PO1 asserts when $\overline{MR}$ = low (Table 6)                                     |
|                  |                       | [7:6] | Not used                                                                                 |

**Note:** Table 7 only applies to PO1. Write a "0" to a bit to make the PO1 output independent of the respective signal (IN\_ thresholds, WD, GPI\_, or  $\overline{MR}$ ).

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Table 8. PO2 Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                              |
|------------------|-----------------------|-------|------------------------------------------------------------------------------------------|
| 0Dh              | 8Dh                   | [0]   | 1 = PO2 assertion depends on IN1 undervoltage threshold (Table 2)                        |
|                  |                       | [1]   | 1 = PO2 assertion depends on IN2 undervoltage threshold (Table 3)                        |
|                  |                       | [2]   | 1 = PO2 assertion depends on IN3 undervoltage threshold (Table 3)                        |
|                  |                       | [3]   | 1 = PO2 assertion depends on IN4 undervoltage threshold (Table 3)                        |
|                  |                       | [4]   | 1 = PO2 assertion depends on IN5 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO2 assertion depends on IN6 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO2 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3)         |
|                  |                       | [7]   | 1 = PO2 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4)         |
| 0Eh              | 8Eh                   | [0]   | 1 = PO2 assertion depends on watchdog (Table 20)                                         |
|                  |                       | [1]   | 1 = PO2 assertion depends on GPI1 (Table 5)                                              |
|                  |                       | [2]   | 1 = PO2 assertion depends on GPI2 (Table 5)                                              |
|                  |                       | [3]   | 1 = PO2 assertion depends on GPI3 (Table 5)                                              |
|                  |                       | [4]   | 1 = PO2 assertion depends on GPI4 (MAX6889/MAX6890 only) (Table 5)                       |
|                  |                       | [5]   | 1 = PO2 asserts when $\overline{MR}$ = low (Table 6)                                     |
|                  |                       | [7:6] | Not used                                                                                 |

**Note:** Table 8 only applies to PO2. Write a "0" to a bit to make the PO2 output independent of the respective signal (IN\_ thresholds, WD, GPI\_, or  $\overline{MR}$ ).

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Table 9. PO3 Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                              |
|------------------|-----------------------|-------|------------------------------------------------------------------------------------------|
| 10h              | 90h                   | [0]   | 1 = PO3 assertion depends on IN1 undervoltage threshold (Table 2)                        |
|                  |                       | [1]   | 1 = PO3 assertion depends on IN2 undervoltage threshold (Table 3)                        |
|                  |                       | [2]   | 1 = PO3 assertion depends on IN3 undervoltage threshold (Table 3)                        |
|                  |                       | [3]   | 1 = PO3 assertion depends on IN4 undervoltage threshold (Table 3)                        |
|                  |                       | [4]   | 1 = PO3 assertion depends on IN5 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO3 assertion depends on IN6 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO3 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3)         |
|                  |                       | [7]   | 1 = PO3 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4)         |
| 11h              | 11h                   | [0]   | 1 = PO3 assertion depends on watchdog (Table 20)                                         |
|                  |                       | [1]   | 1 = PO3 assertion depends on GPI1 (Table 5)                                              |
|                  |                       | [2]   | 1 = PO3 assertion depends on GPI2 (Table 5)                                              |
|                  |                       | [3]   | 1 = PO3 assertion depends on GPI3 (Table 5)                                              |
|                  |                       | [4]   | 1 = PO3 assertion depends on GPI4 (MAX6889/MAX6890 only) (Table 5)                       |
|                  |                       | [5]   | 1 = PO3 asserts when $\overline{MR}$ = low (Table 6)                                     |
|                  |                       | [7:6] | Not used                                                                                 |

**Note:** Table 9 only applies to PO3. Write a "0" to a bit to make the PO3 output independent of the respective signal ( $IN_+$  thresholds,  $WD$ ,  $GPI_+$ , or  $\overline{MR}$ ).

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Table 10. PO4 Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                              |
|------------------|-----------------------|-------|------------------------------------------------------------------------------------------|
| 13h              | 93h                   | [0]   | 1 = PO4 assertion depends on IN1 undervoltage threshold (Table 2)                        |
|                  |                       | [1]   | 1 = PO4 assertion depends on IN2 undervoltage threshold (Table 3)                        |
|                  |                       | [2]   | 1 = PO4 assertion depends on IN3 undervoltage threshold (Table 3)                        |
|                  |                       | [3]   | 1 = PO4 assertion depends on IN4 undervoltage threshold (Table 3)                        |
|                  |                       | [4]   | 1 = PO4 assertion depends on IN5 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO4 assertion depends on IN6 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO4 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3)         |
|                  |                       | [7]   | 1 = PO4 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4)         |
| 14h              | 14h                   | [0]   | 1 = PO4 assertion depends on watchdog (Table 20)                                         |
|                  |                       | [1]   | 1 = PO4 assertion depends on GPI1 (Table 5)                                              |
|                  |                       | [2]   | 1 = PO4 assertion depends on GPI2 (Table 5)                                              |
|                  |                       | [3]   | 1 = PO4 assertion depends on GPI3 (Table 5)                                              |
|                  |                       | [4]   | 1 = PO4 assertion depends on GPI4 (MAX6889/MAX6890 only) (Table 5)                       |
|                  |                       | [5]   | 1 = PO4 asserts when $\overline{MR}$ = low (Table 6)                                     |
|                  |                       | [7:6] | Not used                                                                                 |

**Note:** Table 10 only applies to PO4. Write a "0" to a bit to make the PO4 output independent of the respective signal (IN<sub>n</sub> thresholds, WD, GPI<sub>n</sub>, or  $\overline{MR}$ ).

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Table 11. PO5 Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                              |
|------------------|-----------------------|-------|------------------------------------------------------------------------------------------|
| 16h              | 96h                   | [0]   | 1 = PO5 assertion depends on IN1 undervoltage threshold (Table 2)                        |
|                  |                       | [1]   | 1 = PO5 assertion depends on IN2 undervoltage threshold (Table 3)                        |
|                  |                       | [2]   | 1 = PO5 assertion depends on IN3 undervoltage threshold (Table 3)                        |
|                  |                       | [3]   | 1 = PO5 assertion depends on IN4 undervoltage threshold (Table 3)                        |
|                  |                       | [4]   | 1 = PO5 assertion depends on IN5 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO5 assertion depends on IN6 (MAX6889/MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO5 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3)         |
|                  |                       | [7]   | 1 = PO5 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4)         |
| 17h              | 17h                   | [0]   | 1 = PO5 assertion depends on watchdog (Table 20)                                         |
|                  |                       | [1]   | 1 = PO5 assertion depends on GPI1 (Table 5)                                              |
|                  |                       | [2]   | 1 = PO5 assertion depends on GPI2 (Table 5)                                              |
|                  |                       | [3]   | 1 = PO5 assertion depends on GPI3 (Table 5)                                              |
|                  |                       | [4]   | 1 = PO5 assertion depends on GPI4 (MAX6889/MAX6890 only) (Table 5)                       |
|                  |                       | [5]   | 1 = PO5 asserts when $\overline{MR}$ = low (Table 6)                                     |
|                  |                       | [7:6] | Not used                                                                                 |

**Note:** Table 11 only applies to PO5. Write a "0" to a bit to make the PO5 output independent of the respective signal (IN<sub>n</sub> thresholds, WD, GPI<sub>n</sub>, or  $\overline{MR}$ ).

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**Table 12. PO6 (MAX6889/MAX6890 Only) Output Dependency**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                      |
|------------------|-----------------------|-------|----------------------------------------------------------------------------------|
| 19h              | 99h                   | [0]   | 1 = PO6 assertion depends on IN1 undervoltage threshold (Table 2)                |
|                  |                       | [1]   | 1 = PO6 assertion depends on IN2 undervoltage threshold (Table 3)                |
|                  |                       | [2]   | 1 = PO6 assertion depends on IN3 undervoltage threshold (Table 3)                |
|                  |                       | [3]   | 1 = PO6 assertion depends on IN4 undervoltage threshold (Table 3)                |
|                  |                       | [4]   | 1 = PO6 assertion depends on IN5 undervoltage threshold (Table 3)                |
|                  |                       | [5]   | 1 = PO6 assertion depends on IN6 undervoltage threshold (Table 3)                |
|                  |                       | [6]   | 1 = PO6 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [7]   | 1 = PO6 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4) |
| 1Ah              | 9Ah                   | [0]   | 1 = PO6 assertion depends on watchdog (Table 20)                                 |
|                  |                       | [1]   | 1 = PO6 assertion depends on GPI1 (Table 5)                                      |
|                  |                       | [2]   | 1 = PO6 assertion depends on GPI2 (Table 5)                                      |
|                  |                       | [3]   | 1 = PO6 assertion depends on GPI3 (Table 5)                                      |
|                  |                       | [4]   | 1 = PO6 assertion depends on GPI4 (Table 5)                                      |
|                  |                       | [5]   | 1 = PO4 asserts when $\overline{MR}$ = low (Table 6)                             |
|                  |                       | [7:6] | Not used                                                                         |

**Note:** Table 12 only applies to PO6 (MAX6889/MAX6890 only). Write a "0" to a bit to make the PO6 output independent of the respective signal (IN\_ thresholds, WD, GPL, or MR).

**Table 13. PO7 (MAX6889/MAX6890 Only) Output Dependency**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                      |
|------------------|-----------------------|-------|----------------------------------------------------------------------------------|
| 1Ch              | 9Ch                   | [0]   | 1 = PO7 assertion depends on IN1 undervoltage threshold (Table 2)                |
|                  |                       | [1]   | 1 = PO7 assertion depends on IN2 undervoltage threshold (Table 3)                |
|                  |                       | [2]   | 1 = PO7 assertion depends on IN3 undervoltage threshold (Table 3)                |
|                  |                       | [3]   | 1 = PO7 assertion depends on IN4 undervoltage threshold (Table 3)                |
|                  |                       | [4]   | 1 = PO7 assertion depends on IN5 undervoltage threshold (Table 3)                |
|                  |                       | [5]   | 1 = PO7 assertion depends on IN6 undervoltage threshold (Table 3)                |
|                  |                       | [6]   | 1 = PO7 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [7]   | 1 = PO7 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4) |
| 1Dh              | 9Dh                   | [0]   | 1 = PO7 assertion depends on watchdog (Table 20)                                 |
|                  |                       | [1]   | 1 = PO7 assertion depends on GPI1 (Table 5)                                      |
|                  |                       | [2]   | 1 = PO7 assertion depends on GPI2 (Table 5)                                      |
|                  |                       | [3]   | 1 = PO7 assertion depends on GPI3 (Table 5)                                      |
|                  |                       | [4]   | 1 = PO7 assertion depends on GPI4 (Table 5)                                      |
|                  |                       | [5]   | 1 = PO7 asserts when $\overline{MR}$ = low (Table 6)                             |
|                  |                       | [7:6] | Not used                                                                         |

**Note:** Table 13 only applies to PO7 (MAX6889/MAX6890 only). Write a "0" to a bit to make the PO7 output independent of the respective signal (IN\_ thresholds, WD, GPL, or MR).

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**Table 14. PO8 (MAX6889/MAX6890 Only) Output Dependency**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                                      |
|------------------|-----------------------|-------|----------------------------------------------------------------------------------|
| 1Fh              | 9Fh                   | [0]   | 1 = PO8 assertion depends on IN1 undervoltage threshold (Table 2)                |
|                  |                       | [1]   | 1 = PO8 assertion depends on IN2 undervoltage threshold (Table 3)                |
|                  |                       | [2]   | 1 = PO8 assertion depends on IN3 undervoltage threshold (Table 3)                |
|                  |                       | [3]   | 1 = PO8 assertion depends on IN4 undervoltage threshold (Table 3)                |
|                  |                       | [4]   | 1 = PO8 assertion depends on IN5 undervoltage threshold (Table 3)                |
|                  |                       | [5]   | 1 = PO8 assertion depends on IN6 undervoltage threshold (Table 3)                |
|                  |                       | [6]   | 1 = PO8 assertion depends on IN7 (MAX6890 only) undervoltage threshold (Table 3) |
|                  |                       | [7]   | 1 = PO8 assertion depends on IN8 (MAX6890 only) undervoltage threshold (Table 4) |
| 20h              | A0h                   | [0]   | 1 = PO8 assertion depends on watchdog (Table 20)                                 |
|                  |                       | [1]   | 1 = PO8 assertion depends on GPI1 (Table 5)                                      |
|                  |                       | [2]   | 1 = PO8 assertion depends on GPI2 (Table 5)                                      |
|                  |                       | [3]   | 1 = PO8 assertion depends on GPI3 (Table 5)                                      |
|                  |                       | [4]   | 1 = PO8 assertion depends on GPI4 (Table 5)                                      |
|                  |                       | [5]   | 1 = PO8 asserts when $\overline{MR}$ = low (Table 6)                             |
|                  |                       | [7:6] | Not used                                                                         |

**Note:** Table 14 only applies to PO8 (MAX6889/MAX6890 only). Write a "0" to a bit to make the PO8 output independent of the respective signal (IN\_ thresholds, WD, GPL\_, or  $\overline{MR}$ ).

**Table 15. PO9 (MAX6889 Only) Output Dependency**

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                       |
|------------------|-----------------------|-------|-------------------------------------------------------------------|
| 22h              | A2h                   | [0]   | 1 = PO9 assertion depends on IN1 undervoltage threshold (Table 2) |
|                  |                       | [1]   | 1 = PO9 assertion depends on IN2 undervoltage threshold (Table 3) |
|                  |                       | [2]   | 1 = PO9 assertion depends on IN3 undervoltage threshold (Table 3) |
|                  |                       | [3]   | 1 = PO9 assertion depends on IN4 undervoltage threshold (Table 3) |
|                  |                       | [4]   | 1 = PO9 assertion depends on IN5 undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO9 assertion depends on IN6 undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO9 assertion depends on IN7 undervoltage threshold (Table 3) |
|                  |                       | [7]   | 1 = PO9 assertion depends on IN8 undervoltage threshold (Table 4) |
| 23h              | A3h                   | [0]   | 1 = PO9 assertion depends on watchdog (Table 20)                  |
|                  |                       | [1]   | 1 = PO9 assertion depends on GPI1 (Table 5)                       |
|                  |                       | [2]   | 1 = PO9 assertion depends on GPI2 (Table 5)                       |
|                  |                       | [3]   | 1 = PO9 assertion depends on GPI3 (Table 5)                       |
|                  |                       | [4]   | 1 = PO9 assertion depends on GPI4 (Table 5)                       |
|                  |                       | [5]   | 1 = PO9 asserts when $\overline{MR}$ = low (Table 6)              |
|                  |                       | [7:6] | Not used                                                          |

**Note:** Table 15 only applies to PO9 (MAX6889 only). Write a "0" to a bit to make the PO9 output independent of the respective signal (IN\_ thresholds, WD, GPL\_, or  $\overline{MR}$ ).

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Table 16. PO10 (MAX6889 Only) Output Dependency

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT   | OUTPUT ASSERTION CONDITIONS                                        |
|------------------|-----------------------|-------|--------------------------------------------------------------------|
| 25h              | A5h                   | [0]   | 1 = PO10 assertion depends on IN1 undervoltage threshold (Table 2) |
|                  |                       | [1]   | 1 = PO10 assertion depends on IN2 undervoltage threshold (Table 3) |
|                  |                       | [2]   | 1 = PO10 assertion depends on IN3 undervoltage threshold (Table 3) |
|                  |                       | [3]   | 1 = PO10 assertion depends on IN4 undervoltage threshold (Table 3) |
|                  |                       | [4]   | 1 = PO10 assertion depends on IN5 undervoltage threshold (Table 3) |
|                  |                       | [5]   | 1 = PO10 assertion depends on IN6 undervoltage threshold (Table 3) |
|                  |                       | [6]   | 1 = PO10 assertion depends on IN7 undervoltage threshold (Table 3) |
|                  |                       | [7]   | 1 = PO10 assertion depends on IN8 undervoltage threshold (Table 4) |
| 26h              | A6h                   | [0]   | 1 = PO10 assertion depends on watchdog (Table 20)                  |
|                  |                       | [1]   | 1 = PO10 assertion depends on GPI1 (Table 5)                       |
|                  |                       | [2]   | 1 = PO10 assertion depends on GPI2 (Table 5)                       |
|                  |                       | [3]   | 1 = PO10 assertion depends on GPI3 (Table 5)                       |
|                  |                       | [4]   | 1 = PO10 assertion depends on GPI4 (Table 5)                       |
|                  |                       | [5]   | 1 = PO10 asserts when $\overline{MR}$ = low (Table 6)              |
|                  |                       | [7:6] | Not used                                                           |

**Note:** Table 16 only applies to PO10 (MAX6890 only). Write a "0" to a bit to make the PO10 output independent of the respective signal (IN\_ thresholds, WD, GPL\_, or  $\overline{MR}$ ).

Table 17. Programmable Output Active States

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | AFFECTED OUTPUT | DESCRIPTION                                            |
|------------------|-----------------------|-----------|-----------------|--------------------------------------------------------|
| 0Ch              | 8Ch                   | [1]       | PO1             | 0 = active-low, 1 = active-high                        |
| 0Fh              | 8Fh                   | [1]       | PO2             | 0 = active-low, 1 = active-high                        |
| 12h              | 92h                   | [1]       | PO3             | 0 = active-low, 1 = active-high                        |
| 15h              | 95h                   | [1]       | PO4             | 0 = active-low, 1 = active-high                        |
| 18h              | 98h                   | [1]       | PO5             | 0 = active-low, 1 = active-high                        |
| 1Bh              | 9Bh                   | [1]       | PO6             | MAX6889/MAX6890 only. 0 = active-low, 1 = active-high. |
| 1Eh              | 9Eh                   | [1]       | PO7             | MAX6889/MAX6890 only. 0 = active-low, 1 = active-high. |
| 21h              | A1h                   | [1]       | PO8             | MAX6889/MAX6890 only. 0 = active-low, 1 = active-high. |
| 24h              | A4h                   | [1]       | PO9             | MAX6889 only. 0 = active-low, 1 = active-high.         |
| 27h              | A7h                   | [1]       | PO10            | MAX6889 only. 0 = active-low, 1 = active-high.         |

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## Output Stage Configurations

Independently configure each programmable output as active-high or active-low (Table 17). Additionally, configure each programmable output as open drain or weak pullup (Table 18). Finally, set the PO\_ timeout period for each programmable output (Table 19). The programmable outputs can sink up to 4mA.

## Weak Pullup Output Configuration

The MAX6889/MAX6890/MAX6891s' programmable outputs have a pullup resistance (10k $\Omega$ , typ) connected to the internal 2.55V LDO output to provide weak pullup outputs.

## Open-Drain Output Configuration

Connect an external pullup resistor from the programmable output to an external voltage when configured as an open-drain output. Open-drain configured outputs may be pulled up to 13.2V. Choose the pullup resistor depending on the number of devices connected to the open-drain output and the allowable current consumption. The open-drain output configuration allows wire-ORed connections, and provides flexibility in setting the pullup current.

## Configuring the Watchdog Timer (Registers 29h–2Ah)

A watchdog timer monitors microprocessor software execution for a stalled condition and resets the microprocessor if it stalls. The output of the watchdog timer (one of the programmable outputs) connects to the reset input or a nonmaskable interrupt of the microprocessor.

Registers 29h–2Ah configure the watchdog functionality of the MAX6889/MAX6890/MAX6891. Program the watchdog timer to assert one or more programmable outputs (see Tables 7–16). Program the watchdog timer to reset on one of the GPI\_ inputs, one of the programmable outputs, or a combination of one GPI\_ input and one programmable output.

The watchdog timer features independent initial and normal watchdog timeout periods. The initial watchdog timeout period applies immediately after power-up, after a software reboot, after a reset event takes place, or after enabling the watchdog timer. The initial watchdog timeout period allows the microprocessor to per-

form its initialization process. If no pulse occurs during the initial watchdog timeout period, the microprocessor is taking too long to initialize, indicating a potential problem.

The normal watchdog timeout period applies after the initial watchdog timeout period occurs. The normal watchdog timeout period monitors a pulsed output of the microprocessor that indicates when normal processor behavior occurs. If no pulse occurs during the normal watchdog timeout period, this indicates that the processor has stopped operating or is stuck in an infinite execution loop.

Register 2Ah programs the initial and normal watchdog timeout periods, and enables or disables the watchdog timer. See Tables 20 and 21 for a summary of the watchdog behavior.

## Configuration Lock

Lock the configuration register bank and configuration EEPROM contents after initial programming by setting the lock bit high (see Table 22). Locking the configuration prevents write operations to all registers except the configuration lock register. Clear the lock bit to reconfigure the device.

## Internal/External VCC Power

The MAX6889/MAX6890/MAX6891 can generate an internal VCC, or VCC can be externally supplied (see Table 22). To internally generate VCC from the highest voltage on IN1–IN5 set register 2Eh and EEPROM address AEh Bit[2] = 0. To use an externally supplied, always-on VCC ensure register 2Eh and EEPROM address AEh Bit[2] = 1 (see the *Powering the MAX6889/MAX6890/MAX6891* section).

## Write Disable

A unique write-disable feature protects the MAX6889/MAX6890/MAX6891 from inadvertent user-EEPROM writes. As input voltages that power the serial interface, a microprocessor, or any other writing-devices fall, unintentional data may be written onto the data bus. The user-EEPROM write-disable function (see Table 23) ensures that unintentional data does not corrupt the MAX6889/MAX6890/MAX6891 EEPROM data.

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Table 18. Programmable Output Stage Options

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | AFFECTED OUTPUT | DESCRIPTION                                            |
|------------------|-----------------------|-----------|-----------------|--------------------------------------------------------|
| 0Ch              | 8Ch                   | [0]       | PO1             | 0 = weak pullup, 1 = open drain                        |
| 0Fh              | 8Fh                   | [0]       | PO2             | 0 = weak pullup, 1 = open drain                        |
| 12h              | 92h                   | [0]       | PO3             | 0 = weak pullup, 1 = open drain                        |
| 15h              | 95h                   | [0]       | PO4             | 0 = weak pullup, 1 = open drain                        |
| 18h              | 98h                   | [0]       | PO5             | 0 = weak pullup, 1 = open drain                        |
| 1Bh              | 9Bh                   | [0]       | PO6             | MAX6889/MAX6890 only. 0 = weak pullup, 1 = open drain. |
| 1Eh              | 9Eh                   | [0]       | PO7             | MAX6889/MAX6890 only. 0 = weak pullup, 1 = open drain. |
| 21h              | A1h                   | [0]       | PO8             | MAX6889/MAX6890 only. 0 = weak pullup, 1 = open drain. |
| 24h              | A4h                   | [0]       | PO9             | MAX6889 only. 0 = weak pullup, 1 = open drain.         |
| 27h              | A7h                   | [0]       | PO10            | MAX6889 only. 0 = weak pullup, 1 = open drain.         |

Table 19. PO\_ Timeout Periods

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | AFFECTED OUTPUTS      | DESCRIPTION                                                                                                            |
|------------------|-----------------------|-----------|-----------------------|------------------------------------------------------------------------------------------------------------------------|
| 0Ch              | 8Ch                   | [4:2]     | PO1                   | 000 = 25μs<br>001 = 1.5625ms<br>010 = 6.25ms<br>011 = 25ms<br>100 = 50ms<br>101 = 200ms<br>110 = 400ms<br>111 = 1600ms |
| 0Fh              | 8Fh                   | [4:2]     | PO2                   |                                                                                                                        |
| 12h              | 92h                   | [4:2]     | PO3                   |                                                                                                                        |
| 15h              | 95h                   | [4:2]     | PO4                   |                                                                                                                        |
| 18h              | 98h                   | [4:2]     | PO5                   |                                                                                                                        |
| 1Bh              | 9Bh                   | [4:2]     | PO6 (MAX6889/MAX6890) |                                                                                                                        |
| 1Eh              | 9Eh                   | [4:2]     | PO7 (MAX6889/MAX6890) |                                                                                                                        |
| 21h              | A1h                   | [4:2]     | PO8 (MAX6889/MAX6890) |                                                                                                                        |
| 24h              | A4h                   | [4:2]     | PO9 (MAX6889 only)    |                                                                                                                        |
| 27h              | A7h                   | [4:2]     | PO10 (MAX6889 only)   |                                                                                                                        |

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Table 20. Watchdog Inputs

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                                                                                                                                                                                                                                                        |
|------------------|-----------------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29h              | A9h                   | [1:0]     | Watchdog Input Selection:<br>00 = GPI1 input<br>01 = GPI2 input<br>10 = GPI3 input<br>11 = GPI4 input (MAX6889/MAX6890 only). Selects GPI3 on MAX6891.                                                                                                                                                                             |
|                  |                       | [5:2]     | Watchdog Internal Input Selection:<br>0000 = PO1<br>0001 = PO2<br>0010 = PO3<br>0011 = PO4<br>0100 = PO5<br>0101 = PO6 (MAX6889/MAX6890 only)<br>0110 = PO7 (MAX6889/MAX6890 only)<br>0111 = PO8 (MAX6889/MAX6890 only)<br>1000 = PO9 (MAX6889 only)<br>1001 = PO10 (MAX6889 only)<br>[1011] to [1111] = WD is not affected by PO_ |
|                  |                       | [7:6]     | Watchdog Dependency on Inputs:<br>00 = Watchdog not dependent on any input<br>01 = Watchdog clear depends on selected GPI_ input only<br>01 = Watchdog clear depends on selected PO_ input only<br>11 = Watchdog clear depends on both selected GPI_ and PO_ inputs                                                                |

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Table 21. Watchdog Timeout Period Selection

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                                                                                                                                                 |
|------------------|-----------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2Ah              | AAh                   | [2:0]     | Normal Watchdog Timeout Period:<br>000 = 6.25ms<br>001 = 25ms<br>010 = 100ms<br>011 = 400ms<br>100 = 1.6s<br>101 = 6.4s<br>110 = 25.6s<br>111 = 102.4s                                                                      |
|                  |                       | [5:3]     | Initial Watchdog Timeout Period (immediately following power-up, reset event, or enabling watchdog):<br>000 = 6.25ms<br>001 = 25ms<br>010 = 100ms<br>011 = 400ms<br>100 = 1.6s<br>101 = 6.4s<br>110 = 25.6s<br>111 = 102.4s |
|                  |                       | [6]       | Watchdog Enable<br>0 = Disables watchdog timer<br>1 = Enables watchdog timer                                                                                                                                                |
|                  |                       | [7]       | Not used                                                                                                                                                                                                                    |

Table 22. Configuration Lock and Internal/External VCC Power Register

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                                 |
|------------------|-----------------------|-----------|---------------------------------------------------------------------------------------------|
| 2Eh              | AEh                   | [0]       | 0 = Configuration unlocked<br>1 = Configuration locked                                      |
|                  |                       | [1]       | Not used                                                                                    |
|                  |                       | [2]       | Internal/External VCC Power:<br>0 = VCC internally generated<br>1 = VCC externally supplied |
|                  |                       | [7:3]     | Not used                                                                                    |

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Table 23. Write Disable Register

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | BIT RANGE | DESCRIPTION                                                                     |
|------------------|-----------------------|-----------|---------------------------------------------------------------------------------|
| 2Ch              | ACh                   | [0]       | 0 = Write is not disabled if PO1 asserts<br>1 = Write disabled if PO1 asserts   |
|                  |                       | [1]       | 0 = Write is not disabled if PO2 asserts<br>1 = Write disabled if PO2 asserts   |
|                  |                       | [2]       | 0 = Write is not disabled if PO3 asserts<br>1 = Write disabled if PO3 asserts   |
|                  |                       | [3]       | 0 = Write is not disabled if PO4 asserts<br>1 = Write disabled if PO4 asserts   |
|                  |                       | [4]       | 0 = Write is not disabled if PO5 asserts<br>1 = Write disabled if PO5 asserts   |
|                  |                       | [5]       | 0 = Write is not disabled if PO6 asserts<br>1 = Write disabled if PO6 asserts   |
|                  |                       | [6]       | 0 = Write is not disabled if PO7 asserts<br>1 = Write disabled if PO7 asserts   |
|                  |                       | [7]       | 0 = Write is not disabled if PO8 asserts<br>1 = Write disabled if PO8 asserts   |
| 2Dh              | ADh                   | [0]       | 0 = Write is not disabled if PO9 asserts<br>1 = Write disabled if PO9 asserts   |
|                  |                       | [1]       | 0 = Write is not disabled if PO10 asserts<br>1 = Write disabled if PO10 asserts |
|                  |                       | [7:2]     | Not used                                                                        |

## Configuring the MAX6889/MAX6890/MAX6891

The MAX6889/MAX6890/MAX6891 factory-default configuration sets all registers to 0h, except bits in Tables 17 and 18, which are set to 1h. Factory-default configuration sets all PO\_'s as active-high, open drain (all outputs are high impedance until the device is configured by the user). Each device requires configuration before full power is applied to the system. To configure the MAX6889/MAX6890/MAX6891, first apply an input voltage to IN1, or one of IN2–IN5 or VCC (see the *Powering the MAX6889/MAX6890/MAX6891* section).  $V_{IN1} > 4V$ , or one of  $V_{IN2}$ – $V_{IN5}$  or  $V_{CC} > 2.7V$  to ensure device operation. Next, transmit data through the serial interface. Use the block write protocol to quickly configure the device. Write to the configuration registers first to ensure the device is configured properly. After completing the setup procedure, use the read word or block read protocol to read back the data from the configuration registers. Lastly, use the write byte or block

write protocol to write this data to the EEPROM registers. After completing the EEPROM register configuration, apply full power to the system to begin normal operation. The nonvolatile EEPROM stores the latest configuration upon removal of power. Write 0s to all EEPROM registers to clear the memory.

### Software Reboot

A software reboot allows the user to restore the EEPROM configuration to the volatile registers without cycling the power supplies. Use the send byte command with data byte C4h to initiate a software reboot. The 3ms (max) power-up delay also applies after a software reboot.

### Configuration EEPROM

The configuration EEPROM addresses range from 80h to AEh. Write data to the configuration EEPROM to automatically set up the MAX6889/MAX6890/MAX6891 upon power-up. Data is transferred from the configuration EEPROM to the configuration registers when VCC exceeds UVLO during power-up or after a software

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reboot. After  $V_{CC}$  exceeds UVLO, an internal 1MHz clock starts after a 5 $\mu$ s delay, and data transfer begins. Data transfer disables access to the configuration registers and EEPROM. The data transfer from EEPROM to configuration registers takes 3ms (max). Read configuration EEPROM data at any time after power-up or software reboot. Write commands to the configuration EEPROM are allowed at any time after power-up or software reboot, unless the configuration lock bit is set (see Table 22). The maximum cycle time to write a single byte is 11ms (max).

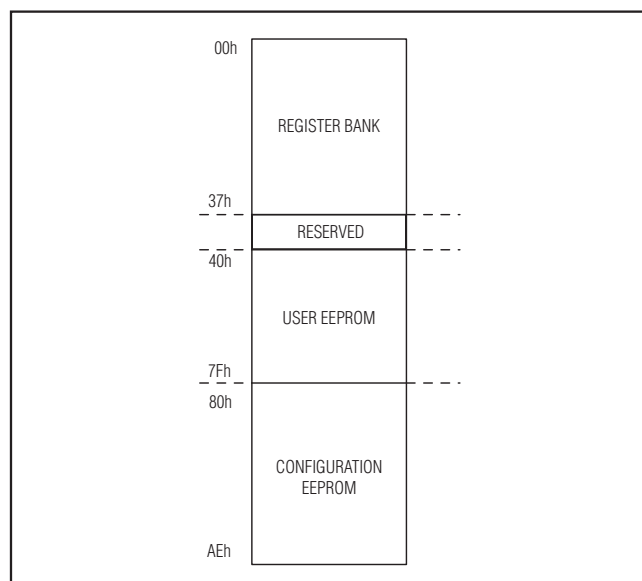


Figure 2. Memory Map

## User EEPROM

The 512-bit, user-EEPROM addresses range from 40h to 7Fh (see Figure 2). Store software revision data, board revision data, and other data in these registers. The maximum cycle time to write a single byte is 11ms (max).

## Configuration Register Bank and EEPROM

The configuration registers can be directly modified through the serial interface without modifying the EEPROM, after the power-up procedure terminates and the configuration EEPROM data has been loaded into the configuration register bank. Use the write byte or block write protocols to write directly to the configuration registers. Changes to the configuration registers take effect immediately and are lost upon power removal.

At device power-up, the register bank loads configuration data from the EEPROM. Configuration data may be directly altered in the register bank during application development, allowing maximum flexibility. Transfer the new configuration data byte-by-byte to the configuration EEPROM with the write protocol. The next device power-up or software reboot automatically loads the new configuration.

## SMBus/I<sup>2</sup>C-Compatible Serial Interface

The MAX6889/MAX6890/MAX6891 feature an I<sup>2</sup>C/SMBus-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX6889/MAX6890/MAX6891 and the master device at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX6889/MAX6890/MAX6891 are transmit/receive slave-only devices, relying upon a

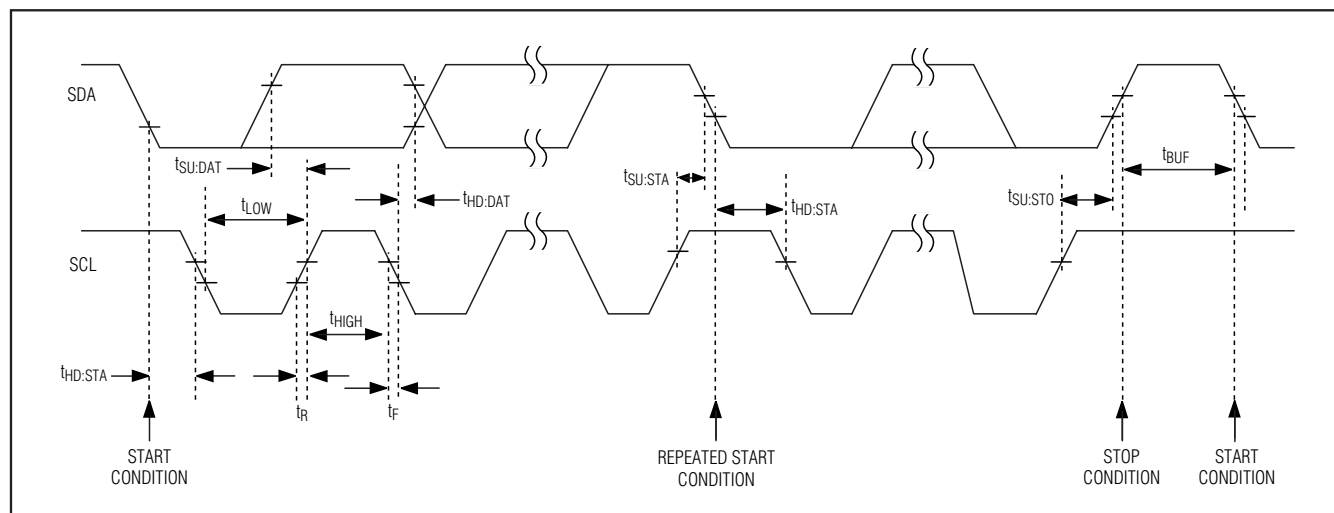


Figure 3. Serial-Interface Timing Details

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master device to generate a clock signal. The master device (typically a microcontroller) generates SCL and initiates data transfer on the bus.

A master device communicates to the MAX6889/MAX6890/MAX6891 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is an open-drain input/output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7k $\Omega$  resistors for most applications.

## Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 4), otherwise the MAX6889/MAX6890/MAX6891 register a START or STOP condition (Figure 5) from the master. SDA and SCL idle high when the bus is not busy.

## Start and Stop Conditions

A master device signals the beginning of a transmission with a START (S) condition (Figure 5) by transitioning SDA from high to low while SCL is high. The master device issues a STOP (P) condition (Figure 5) by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the read byte or block read protocol (see Figure 8). Both SCL and SDA are high when the bus is not busy.

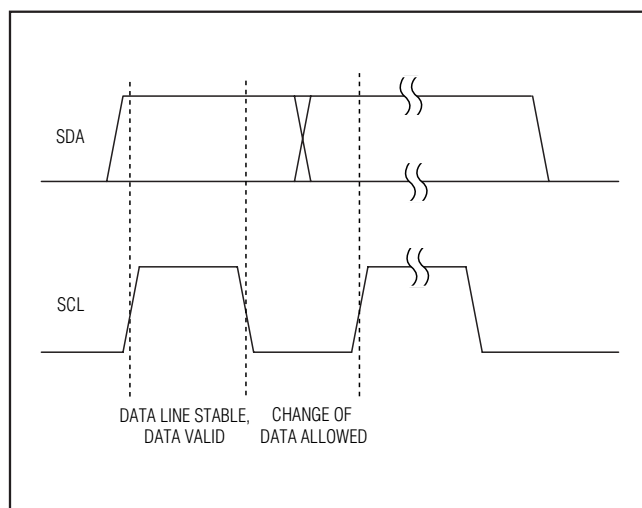


Figure 4. Bit Transfer

## Early STOP Conditions

The MAX6889/MAX6890/MAX6891 recognize a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I<sup>2</sup>C format. At least one clock pulse must separate any START and STOP condition.

## Repeated START Conditions

A REPEATED START (SR) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 8). SR may also be used when the bus master is writing to several I<sup>2</sup>C devices and does not want to relinquish control of the bus. The MAX6889/MAX6890/MAX6891 serial interface supports continuous write operations with or without an SR condition separating them. Continuous read operations require SR conditions because of the change in direction of data flow.

## Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX6889/MAX6890/MAX6891 generate an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 6). When transmitting data, such as when the master device reads data back from the MAX6889/MAX6890/MAX6891, the MAX6889/MAX6890/MAX6891 wait for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful

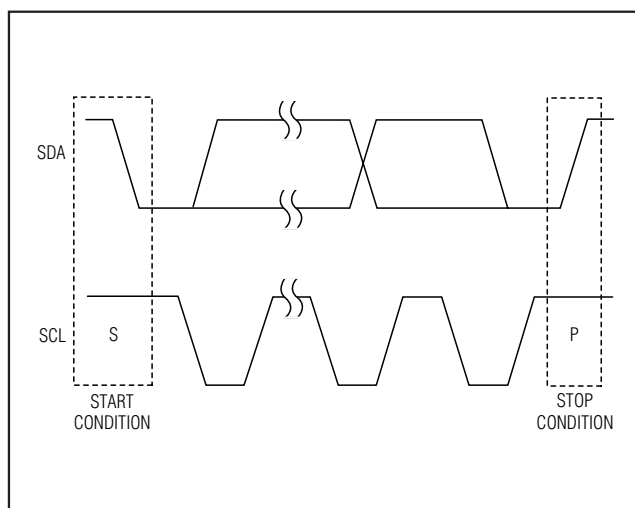


Figure 5. Start and Stop Conditions

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data transfer, the bus master should reattempt communication at a later time. The MAX6889/MAX6890/MAX6891 generate a NACK after the command byte during a software reboot, while writing to the EEPROM, or when receiving an illegal memory address.

## Slave Address

SA7 through SA4 represent the standard 2-wire interface address (1010) for devices with EEPROM. SA3 and SA2 correspond to the A1 and A0 address inputs of the MAX6889/MAX6890/MAX6891 (hardwired as logic-low or logic-high). SA0 is a read/write flag bit (0 = write, 1 = read).

The A0 and A1 address inputs allow up to four MAX6889/MAX6890 to connect to one bus, while the A0 address input allows up to two MAX6891s to con-

nect to one bus. Connect A0 and A1 to GND or to the 2-wire serial-interface power supply (see Figure 7).

The MAX6889/MAX6890 slave address conforms to the following table:

| SA7 (MSB) | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 (LSB) |
|-----------|-----|-----|-----|-----|-----|-----|-----------|
| 1         | 0   | 1   | 0   | A1  | A0  | X   | R/W       |

X = Don't Care

The MAX6891 slave address conforms to the following table:

| SA7 (MSB) | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 (LSB) |
|-----------|-----|-----|-----|-----|-----|-----|-----------|
| 1         | 0   | 1   | 0   | 0   | A0  | X   | R/W       |

X = Don't Care

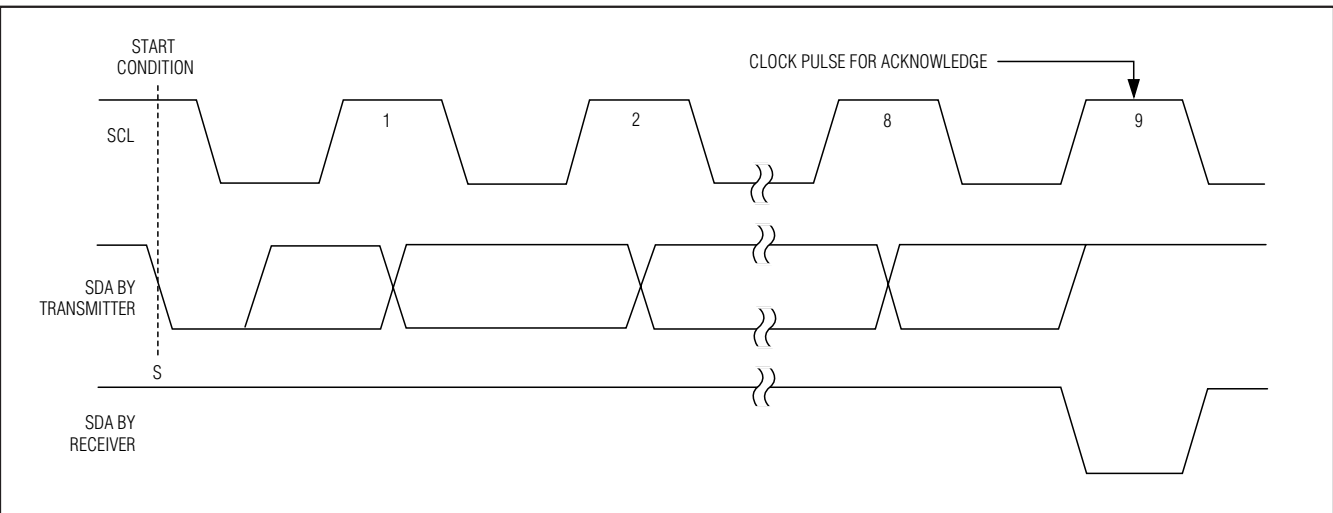


Figure 6. Acknowledge

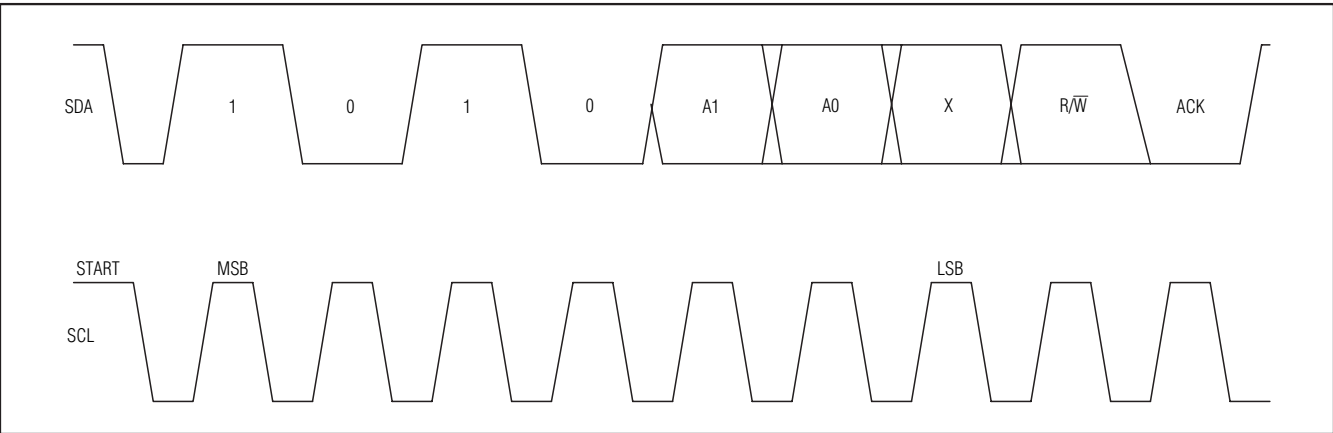


Figure 7. Slave Address

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### Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 8). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed or if the device is writing data to EEPROM or is booting. If the master sends C0h, the data is ACK. This could be the start of the block write protocol, and the slave expects the following data bytes. If the master sends a Stop condition, the internal address pointer does not change. If the master sends C1h, this signifies that the block read protocol is expected, and a repeated Start condition should follow. The device reboots if the master sends C4h. The send byte procedure follows:

- 1) The master sends a Start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends an 8-bit data byte.
- 5) The addressed slave asserts an ACK on SDA.
- 6) The master sends a Stop condition.

### Write Byte

The write byte protocol allows the master device to write a single byte in the register bank or in the EEPROM (configuration or user) (see Figure 8). The Write Byte procedure follows:

- 1) The master sends a Start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends an 8-bit command code.
- 5) The addressed slave asserts an ACK on SDA.
- 6) The master sends an 8-bit data byte.
- 7) The addressed slave asserts an ACK on SDA.
- 8) The master sends a Stop condition.

In order to write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The command code must be in the range of

00h to 2Eh. The data byte is written to the register bank if the command code is valid. The slave generates a NACK at step 5 if the command code is invalid or any internal operations are ongoing.

In order to write a single byte of data to the user or configuration EEPROM, the 8-bit command code and a single 8-bit data byte are sent. The following 8-bit data byte is written to the addressed EEPROM location.

### Block Write

The block write protocol allows the master device to write a block of data (1 to 16 bytes) to the EEPROM or to the register bank (see Figure 8). The destination address must already be set by the send byte protocol and the command code must be C0h. If the number of bytes to be written causes the address pointer to exceed 2Fh for the configuration register or B7h for the configuration EEPROM, the address pointer stops incrementing, overwriting the last memory address with the remaining bytes of data. Only the last data byte sent is stored in B7h (as 2Fh is read only and a write causes no change in the content). If the number of bytes to be written exceeds the address pointer 7Fh for the user EEPROM, the address pointer stops incrementing and continues writing exceeding data to the last address. Only the last data is actually written to 7Fh. The block write procedure follows:

- 1) The master sends a Start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.
- 4) The master sends the 8-bit command code for block write (C0h).
- 5) The addressed slave asserts an ACK on SDA.
- 6) The master sends the 8-bit byte count (1 to 16 bytes) N.
- 7) The addressed slave asserts an ACK on SDA.
- 8) The master sends 8 bits of data.
- 9) The addressed slave asserts an ACK on SDA.
- 10) Repeat steps 8 and 9 N – 1 times.
- 11) The master generates a Stop condition.

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## Read Byte

The read byte protocol allows the master device to read the register or an EEPROM location (user or configuration) content of the MAX6889/MAX6890/MAX6891 (see Figure 8). The read byte procedure follows:

- 1) The master sends a Start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on the data line.
- 4) The master sends 8 data bits.
- 5) The active slave asserts an ACK on the data line.
- 6) The master sends a repeated Start condition.
- 7) The master sends the 7-bit slave ID plus a read bit (high).
- 8) The addressed slave asserts an ACK on the data line.
- 9) The slave sends 8 data bits.
- 10) The master asserts a NACK on the data line.
- 11) The master generates a Stop condition.

Note that once the read has been done, the internal pointer is increased by one, unless a memory boundary is hit.

If the device is busy or if the address is not an allowed one, the command code is NACKed and the internal address pointer is not altered. The master must then interrupt the communication issuing a STOP condition.

## Block Read

The block read protocol allows the master device to read a block of 16 bytes from the EEPROM or register bank (see Figure 8). Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. Previous actions through the serial interface predetermines the first source address. It is suggested to use a send byte protocol, before the block read, to set the initial read address. The block read protocol is initiated with a command code of C1h. The block read procedure follows:

- 1) The master sends a Start condition.
- 2) The master sends the 7-bit slave address and a write bit (low).
- 3) The addressed slave asserts an ACK on SDA.

- 4) The master sends 8 bits of the block read command (C1h).
- 5) The slave asserts an ACK on SDA, unless busy.
- 6) The master generates a repeated Start condition.
- 7) The master sends the 7-bit slave address and a read bit (high).
- 8) The slave asserts an ACK on SDA.
- 9) The slave sends the 8-bit byte count (16).
- 10) The master asserts an ACK on SDA.
- 11) The slave sends 8 bits of data.
- 12) The master asserts an ACK on SDA.
- 13) Repeat steps 8 and 9 15 times.
- 14) The master generates a Stop condition.

## Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 00h to 2Fh. Register addresses outside of this range result in a NACK being issued from the MAX6889/MAX6890/MAX6891. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 2Fh. If the address pointer is already 2Fh, and more data bytes are being sent, these subsequent bytes overwrite address 2Fh repeatedly. No data will be left in 2Fh as this is a read-only address.

For the configuration EEPROM, valid address pointers range from 80h to B7h (even if they are only meaningful up to AEh). When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at B7h. If the address pointer is already B7h, and more data bytes are being sent, these subsequent bytes overwrite address B7h repeatedly, leaving only the last sent data byte stored at this register address.

For the user EEPROM, valid address pointers range from 40h to 7Fh. As for the configuration EEPROM, block write and block read protocols can also be used. The internal address pointer will auto-increment up to the user-EEPROM boundary 7Fh where the pointer will stop incrementing. When writing, only the last data written will be stored in 7Fh.

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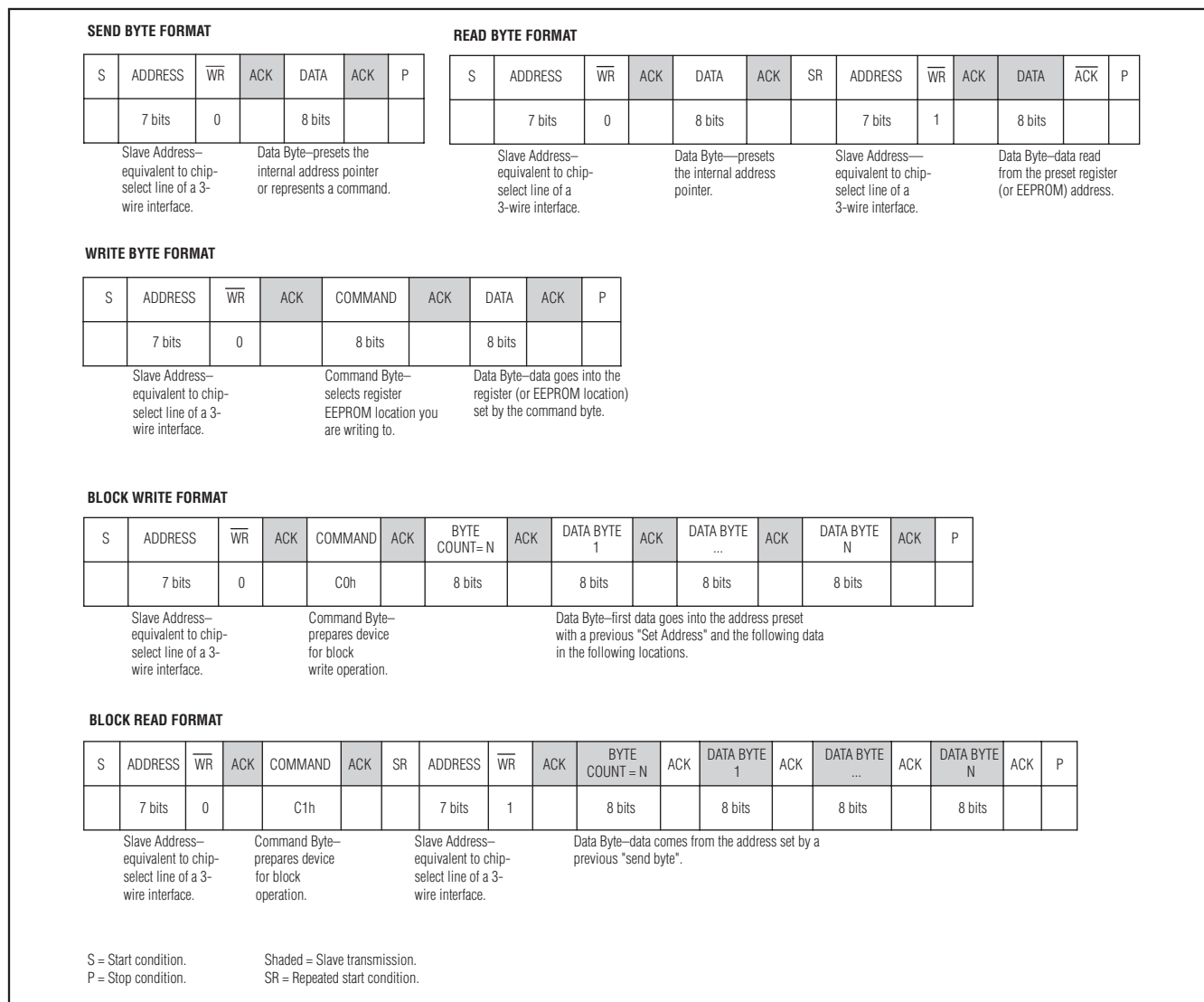


Figure 8. SMBus/I<sup>2</sup>C Protocols

## Applications Information

### Configuration Download at Power-up

The configuration of the MAX6889/MAX6890/MAX6891 (undervoltage thresholds, PO<sub>1</sub> timeout periods, watchdog behavior, programmable output conditions and configurations, etc.) depends on the contents of the EEPROM. The EEPROM is comprised of buffered latches that store the configuration. The local volatile memory latches lose their contents at power-down. Therefore, at power-up, the device configuration must be restored by downloading the contents of the EEPROM (non-

volatile memory) to the local latches. This download occurs in a number of steps:

- 1) Programmable outputs go high impedance with no power applied to the device.
- 2) When V<sub>CC</sub> exceeds 1V, all programmable outputs are weakly pulled to GND through a 10μA current sink.
- 3) When V<sub>CC</sub> exceeds UVLO, the configuration EEPROM starts to download its contents to the volatile configuration registers. The programmable outputs assume their programmed conditional output state when V<sub>CC</sub> exceeds UVLO.

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- 4) Any attempt to communicate with the device prior to this download completion results in a NACK being issued from the MAX6889/MAX6890/MAX6891.

## Forcing Programmable Outputs High During Power-up

A weak, 10 $\mu$ A pulldown current holds all programmable outputs low during power-up until V<sub>CC</sub> exceeds the undervoltage-lockout (UVLO) threshold. Applications requiring a guaranteed high programmable output for V<sub>CC</sub> down to GND require external pullup resistors to maintain the logic state until V<sub>CC</sub> exceeds UVLO. Use 20k $\Omega$  resistors for most applications.

## Uses for General-Purpose Inputs (GPI\_)

### Watchdog Timer

Program GPI\_ as an input to the watchdog timer in the MAX6889/MAX6890/MAX6891. The GPI\_ input must toggle within the watchdog timeout period; otherwise any programmable output dependent on the watchdog timer will assert.

### Additional Manual Reset Functions

The programmable outputs allow a set of conditions to assert the output. Program the set of conditions to depend on one of the GPI\_ inputs. Any output that depends on GPI\_ asserts when GPI\_ is held in its active state, effectively acting as a manual reset input.

## Other Fault Signals from $\mu$ C

Connect a general-purpose output from a  $\mu$ C to one of the GPI\_ inputs to allow interrupts to assert any output of the MAX6889/MAX6890/MAX6891. Configure one of the programmable outputs to assert on whichever GPI\_ input connects to the general-purpose output of the  $\mu$ C.

## Layout and Bypassing

For better noise immunity, bypass each of the voltage detector inputs to GND with 0.1 $\mu$ F capacitors installed as close to the device as possible. Bypass V<sub>CC</sub> and DBP to GND with 1 $\mu$ F capacitors installed as close to the device as possible. V<sub>CC</sub> (when not externally supplied) and DBP are internally generated voltages and should not be used to supply power to external circuitry.

## Configuration Latency Period

A delay of less than 5 $\mu$ s occurs between writing to the configuration registers and the time when these changes actually take place, unless when changing one of the voltage detector's thresholds. Changing a voltage detector threshold typically takes 150 $\mu$ s. When changing EEPROM contents, a software reboot or cycling of power is required for these changes to transfer to volatile memory.

## Chip Information

PROCESS: BiCMOS

## Register Map

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | READ/ WRITE | DESCRIPTION                                                                                         |
|------------------|-----------------------|-------------|-----------------------------------------------------------------------------------------------------|
| 00h              | 80h                   | R/W         | IN1 undervoltage detector threshold (Table 2)                                                       |
| 01h              | 81h                   | R/W         | IN2 undervoltage detector threshold (Table 3)                                                       |
| 02h              | 82h                   | R/W         | IN3 undervoltage detector threshold (Table 3)                                                       |
| 03h              | 83h                   | R/W         | IN4 undervoltage detector threshold (Table 3)                                                       |
| 04h              | 84h                   | R/W         | IN5 undervoltage detector threshold (MAX6889/MAX6890 only) (Table 3)                                |
| 05h              | 85h                   | R/W         | IN6 undervoltage detector threshold (MAX6889/MAX6890 only) (Table 3)                                |
| 06h              | 86h                   | R/W         | IN7 undervoltage detector threshold (MAX6889 only) (Table 3)                                        |
| 07h              | 87h                   | R/W         | IN8 undervoltage detector threshold (MAX6889 only) (Table 4)                                        |
| 08h              | 88h                   | R/W         | Threshold range selection (Tables 2, 3, and 4)                                                      |
| 09h              | 89h                   | R/W         | High-Z mode selection (Tables 2, 3, and 4)                                                          |
| 0Ah              | 8Ah                   | R/W         | PO1 input selection (Table 7)                                                                       |
| 0Bh              | 8Bh                   | R/W         | PO1 input selection (Table 7)                                                                       |
| 0Ch              | 8Ch                   | R/W         | PO1 timeout period, programmable output polarity, and output type selection (Tables 17, 18, and 19) |
| 0Dh              | 8Dh                   | R/W         | PO2 input selection (Table 8)                                                                       |
| 0Eh              | 8Eh                   | R/W         | PO2 input selection (Table 8)                                                                       |

# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

MAX6889/MAX6890/MAX6891

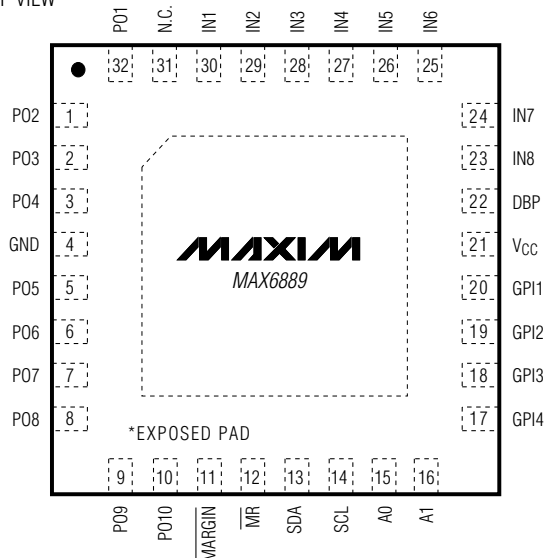
Register Map (continued)

| REGISTER ADDRESS | EEPROM MEMORY ADDRESS | READ/ WRITE | DESCRIPTION                                                                            |
|------------------|-----------------------|-------------|----------------------------------------------------------------------------------------|
| 0Fh              | 8Fh                   | R/W         | PO2 timeout period and output type selection (Tables 17, 18, and 19)                   |
| 10h              | 90h                   | R/W         | PO3 input selection (Table 9)                                                          |
| 11h              | 91h                   | R/W         | PO3 input selection (Table 9)                                                          |
| 12h              | 92h                   | R/W         | PO3 timeout period and output type selection (Tables 17, 18, and 19)                   |
| 13h              | 93h                   | R/W         | PO4 input selection (Table 10)                                                         |
| 14h              | 94h                   | R/W         | PO4 input selection (Table 10)                                                         |
| 15h              | 95h                   | R/W         | PO4 timeout period and output type selection (Tables 17, 18, and 19)                   |
| 16h              | 96h                   | R/W         | PO5 input selection (Table 11)                                                         |
| 17h              | 97h                   | R/W         | PO5 input selection (Table 11)                                                         |
| 18h              | 98h                   | R/W         | PO5 timeout period and output type selection (Tables 17, 18, and 19)                   |
| 19h              | 99h                   | R/W         | PO6 (MAX6889/MAX6890) input selection (Table 12)                                       |
| 1Ah              | 9Ah                   | R/W         | PO6 (MAX6889/MAX6890) input selection (Table 12)                                       |
| 1Bh              | 9Bh                   | R/W         | PO6 (MAX6889/MAX6890) timeout period and output type selection (Tables 17, 18, and 19) |
| 1Ch              | 9Ch                   | R/W         | PO7 (MAX6889/MAX6890) input selection (Table 13)                                       |
| 1Dh              | 9Dh                   | R/W         | PO7 (MAX6889/MAX6890) input selection (Table 13)                                       |
| 1Eh              | 9Eh                   | R/W         | PO7 (MAX6889/MAX6890) timeout period and output type selection (Tables 17, 18, and 19) |
| 1Fh              | 9Fh                   | R/W         | PO8 (MAX6889/MAX6890) input selection (Table 14)                                       |
| 20h              | A0h                   | R/W         | PO8 (MAX6889/MAX6890) input selection (Table 14)                                       |
| 21h              | A1h                   | R/W         | PO8 (MAX6889/MAX6890) timeout period and output type selection (Tables 17, 18, and 19) |
| 22h              | A2h                   | R/W         | PO9 (MAX6889 only) input selection (Table 15)                                          |
| 23h              | A3h                   | R/W         | PO9 (MAX6889 only) input selection (Table 15)                                          |
| 24h              | A4h                   | R/W         | PO9 (MAX6889 only) timeout period and output type selection (Tables 17, 18, and 19)    |
| 25h              | A5h                   | R/W         | PO10 (MAX6889 only) input selection (Table 16)                                         |
| 26h              | A6h                   | R/W         | PO10 (MAX6889 only) input selection (Table 16)                                         |
| 27h              | A7h                   | R/W         | PO10 (MAX6889 only) timeout period and output type selection (Tables 17, 18, and 19)   |
| 28h              | A8h                   | R/W         | GPL_ input polarity selection                                                          |
| 29h              | A9h                   | R/W         | WD input selection and clear dependency (Table 20)                                     |
| 2Ah              | AAh                   | R/W         | WD initial and normal timeout duration and disable (Table 21)                          |
| 2Bh              | ABh                   | —           | Reserved. Should not be overwritten.                                                   |
| 2Ch              | ACH                   | R/W         | User EEPROM write disable (Table 23)                                                   |
| 2Dh              | ADh                   | R/W         | User EEPROM write disable (Table 23)                                                   |
| 2Eh              | A Eh                  | R/W         | Configuration lock and internal/external V <sub>CC</sub> power (Table 22)              |

# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

## Pin Configurations

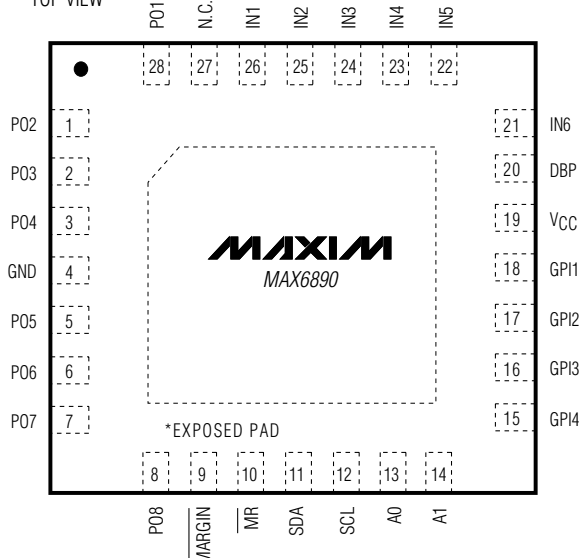
TOP VIEW



(5mm x 5mm THIN QFN)

\*EXPOSED PAD INTERNALLY CONNECTED TO GND.

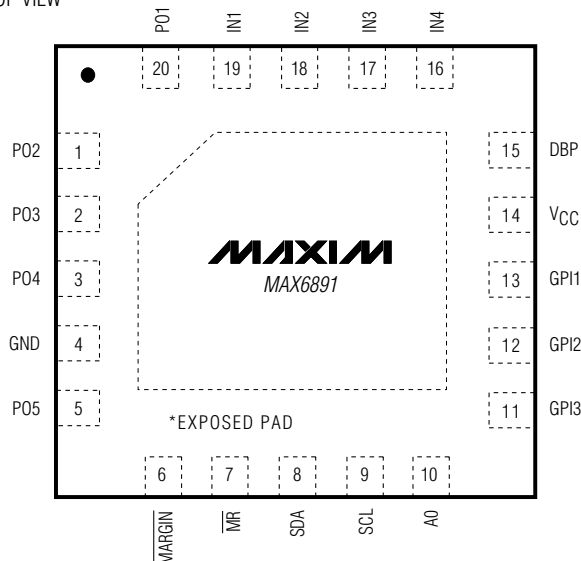
TOP VIEW



(5mm x 5mm THIN QFN)

\*EXPOSED PAD INTERNALLY CONNECTED TO GND.

TOP VIEW

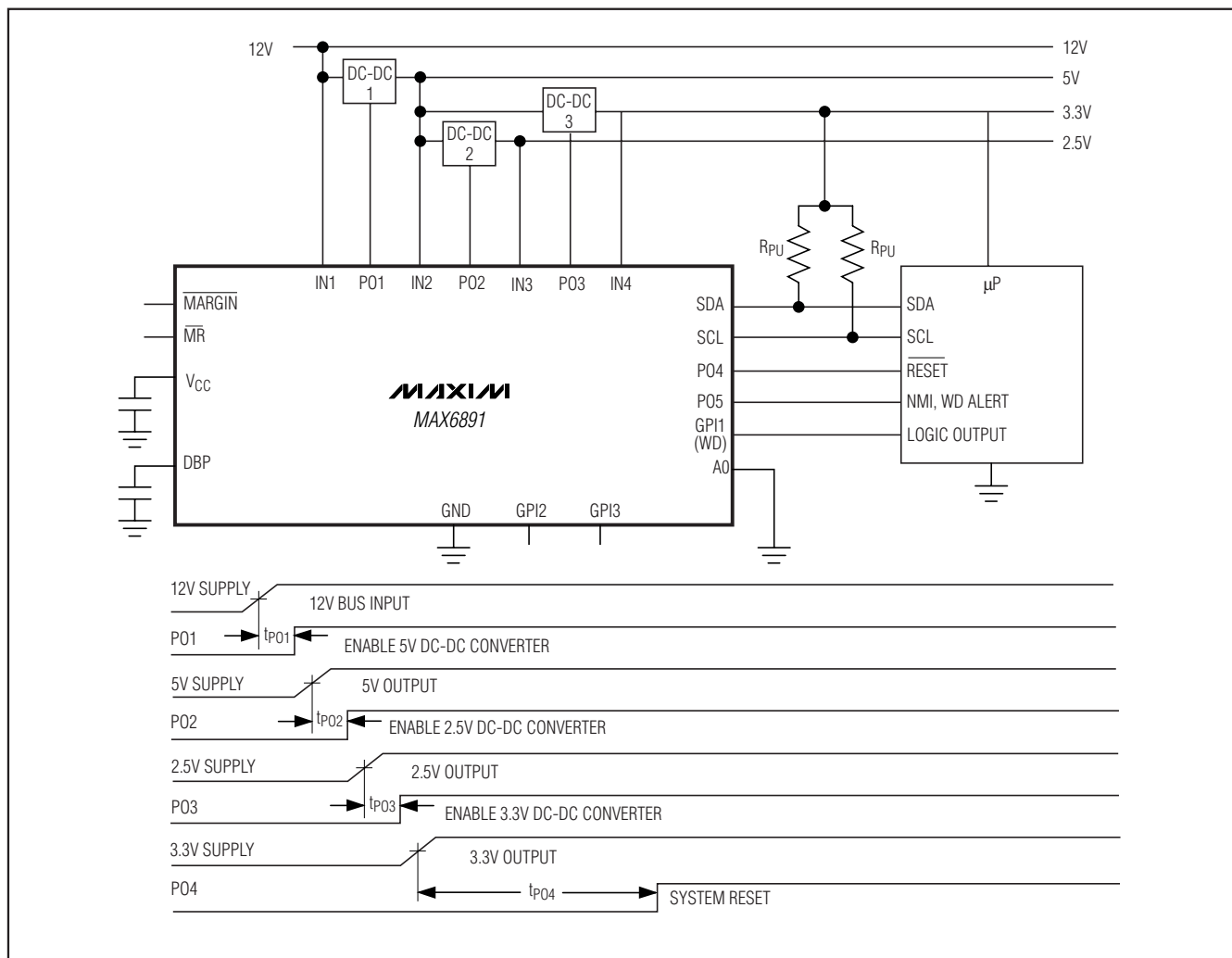


(5mm x 5mm THIN QFN)

\*EXPOSED PAD INTERNALLY CONNECTED TO GND.

# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

## Typical Operating Circuit



MAX6889/MAX6890/MAX6891

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 20 TQFN      | T2055-5      | <a href="#">21-0140</a> |
| 28 TQFN      | T2855-8      | <a href="#">21-0140</a> |
| 32 TQFN      | T3255-4      | <a href="#">21-0140</a> |

# EEPROM-Programmable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION                                                 | PAGES<br>CHANGED |
|--------------------|------------------|-------------------------------------------------------------|------------------|
| 0                  | 2/05             | Initial release                                             | —                |
| 1                  | 9/08             | Added specifications to <i>Electrical Characteristics</i> . | 4                |

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