



BUK6D120-40E

40 V, N-channel Trench MOSFET

29 April 2019

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range $T_j = 175\text{ °C}$
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection $> 1\text{ kV HBM}$ (class H1C)
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

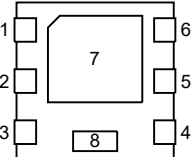
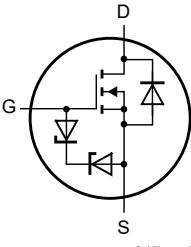
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	40	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$	-	-	5.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	7.5	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 2.9\text{ A}; T_j = 25\text{ °C}$	-	85	120	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view DFN2020MD-6 (SOT1220)	 017aaa255
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6D120-40E	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6D120-40E	5F

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	40	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C		-	5.7	A
		V _{GS} = 10 V; T _{sp} = 100 °C		-	3.6	A
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	2.9	A
I _{DM}	peak drain current	T _{sp} = 25 °C; single pulse; t _p ≤ 10 μs		-	23	A
P _{tot}	total power dissipation	T _{sp} = 25 °C		-	7.5	W
		T _{amb} = 25 °C	[1]	-	2	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{sp} = 25 °C		-	5.7	A
		T _{amb} = 25 °C	[1]	-	2	A
I _{SM}	peak source current	single pulse; t _p ≤ 10 μs; T _{sp} = 25 °C		-	23	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[2]	-	1000	V
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = 0.26 A; DUT in avalanche (unclamped)		-	5.8	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

[2] Measured between all pins.

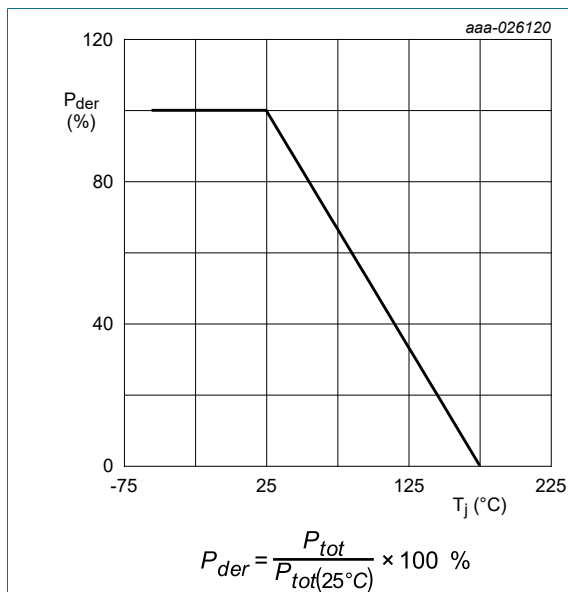


Fig. 1. Normalized total power dissipation as a function of junction temperature

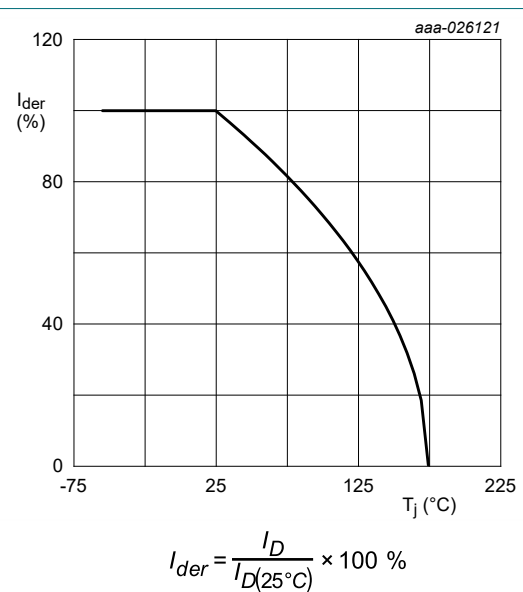
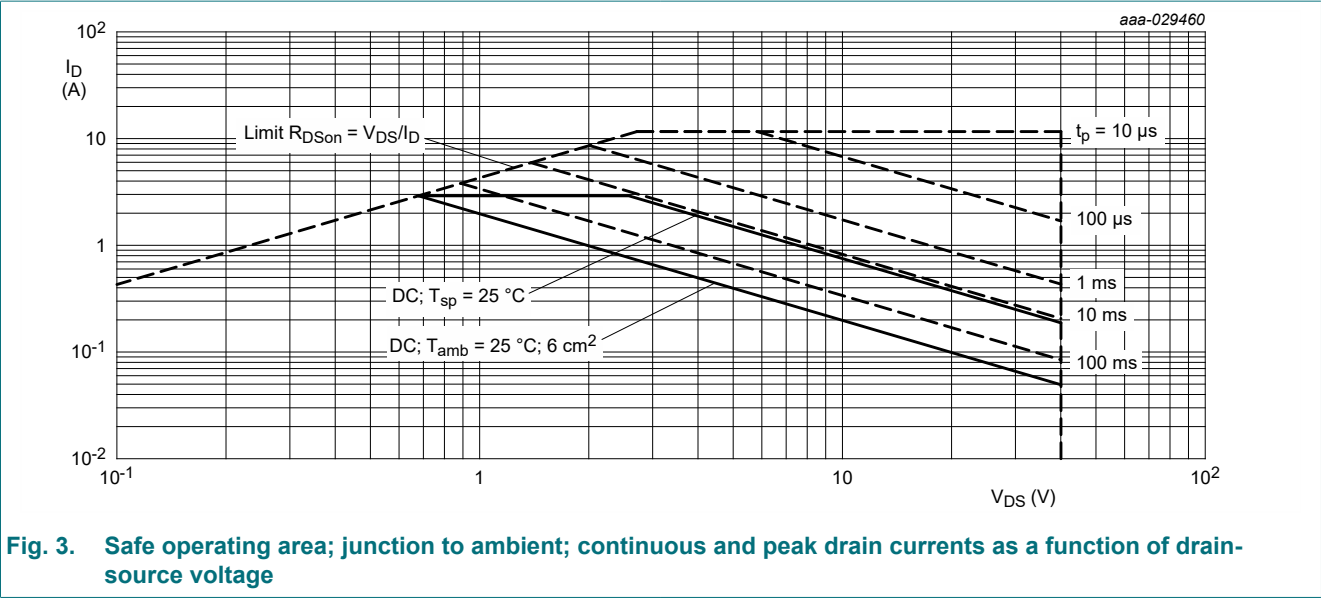


Fig. 2. Normalized continuous drain current as a function of junction temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	66	76	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

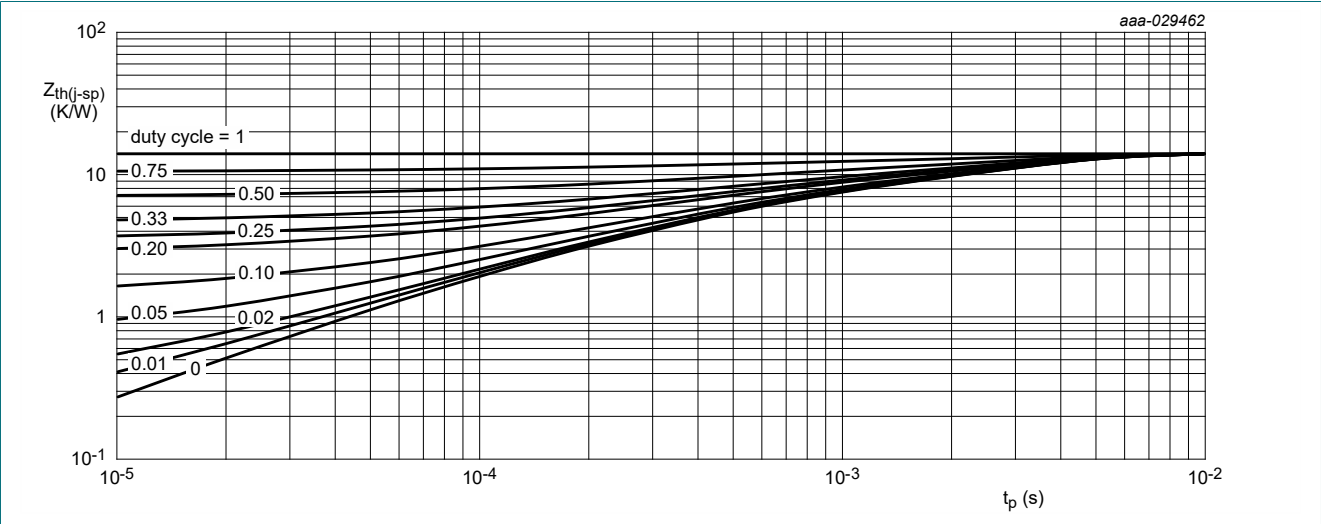


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values

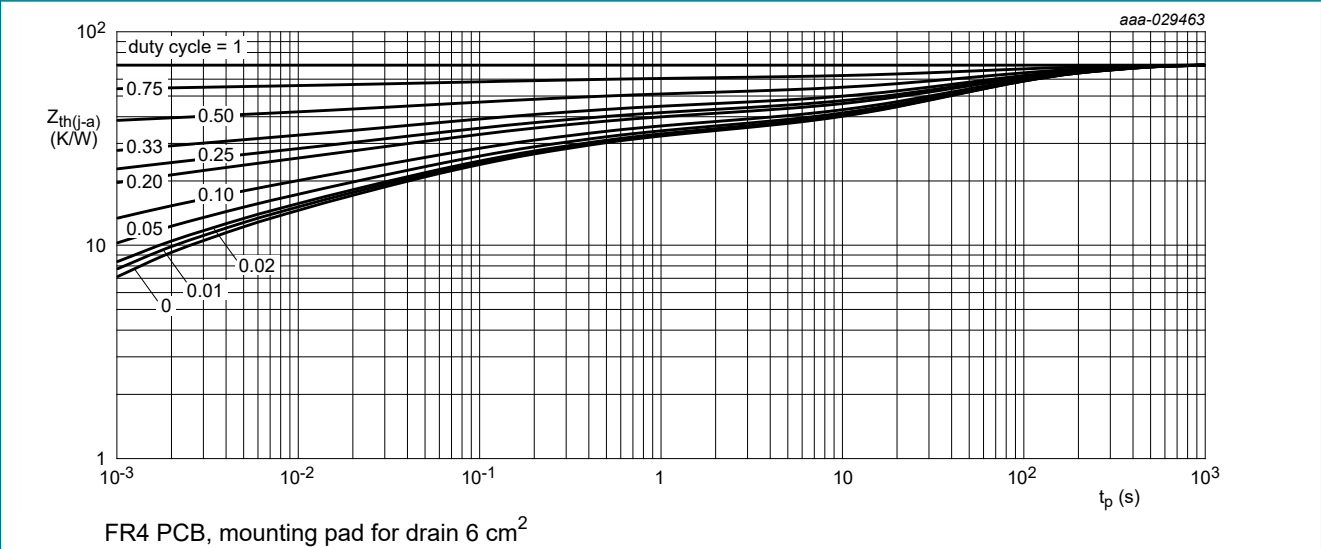


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		40	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		1	1.6	2.5	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 125 °C		-	-	4	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 2.9 A; T _j = 25 °C		-	85	120	mΩ
		V _{GS} = 10 V; I _D = 2.9 A; T _j = 175 °C		-	165	233	mΩ
		V _{GS} = 4.5 V; I _D = 2.5 A; T _j = 25 °C		-	112	160	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 2 A; T _j = 25 °C		-	4.5	-	S
R _G	gate resistance	f = 1 MHz		-	28	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 20 V; I _D = 2.9 A; V _{GS} = 10 V; T _j = 25 °C		-	2.4	3.6	nC
Q _{GS}	gate-source charge			-	0.3	-	nC
Q _{GD}	gate-drain charge			-	0.4	-	nC
C _{iss}	input capacitance	V _{DS} = 20 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	113	-	pF
C _{oss}	output capacitance			-	27	-	pF
C _{rss}	reverse transfer capacitance			-	14	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; I _D = 2.9 A; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	8	-	ns
t _{d(off)}	turn-off delay time			-	11	-	ns
t _f	fall time			-	3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 2 A; V _{GS} = 0 V; T _j = 25 °C		-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 1 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C		-	7.2	-	ns
Q _r	recovered charge			-	3	-	nC

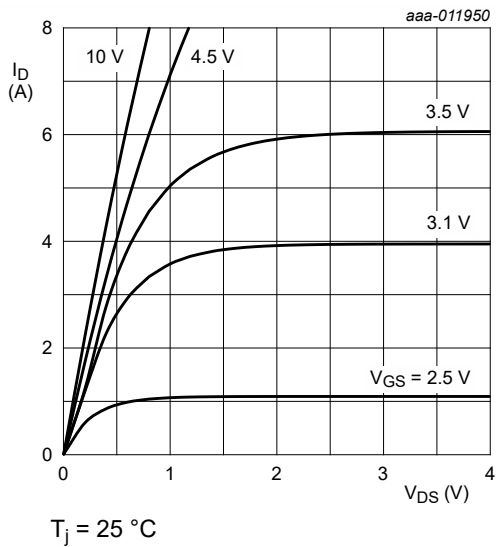


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

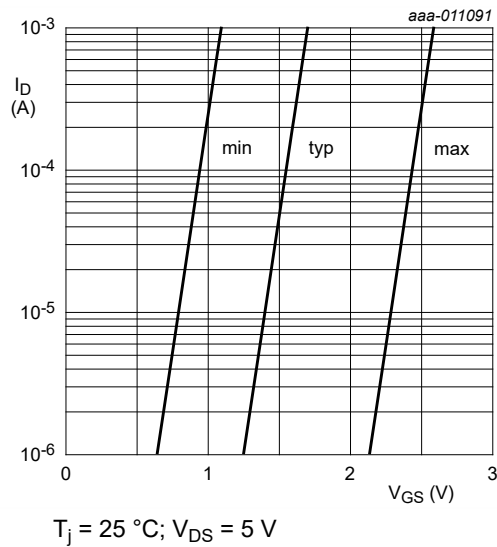


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

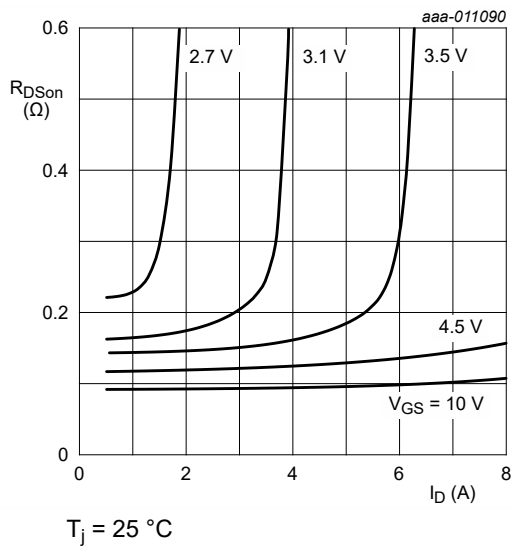


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

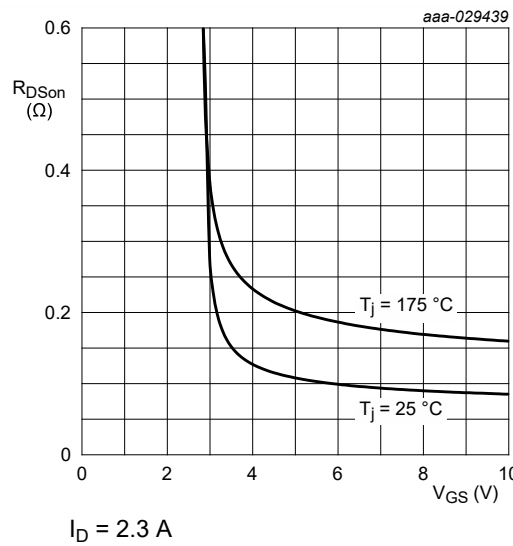


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

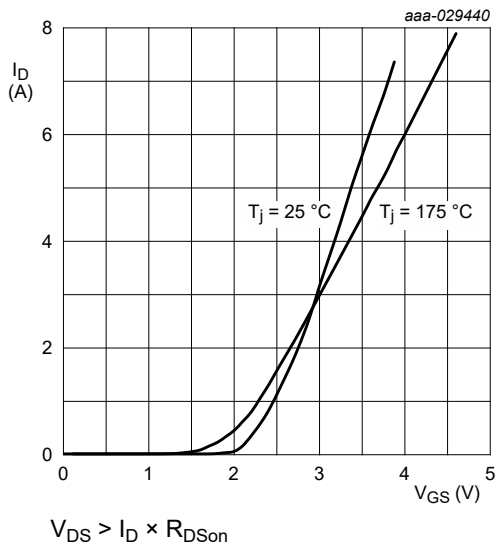


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

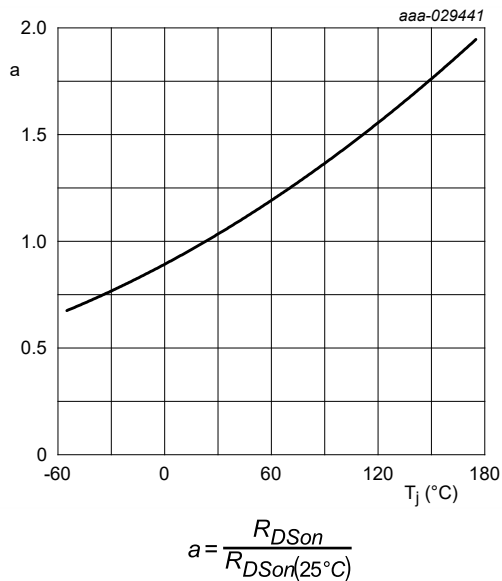


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

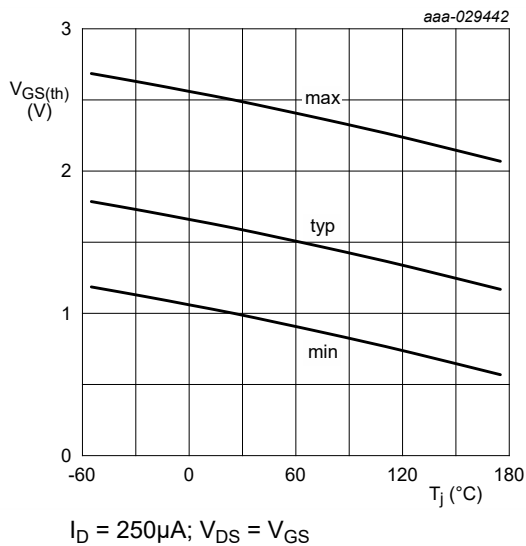


Fig. 12. Gate-source threshold voltage as a function of junction temperature

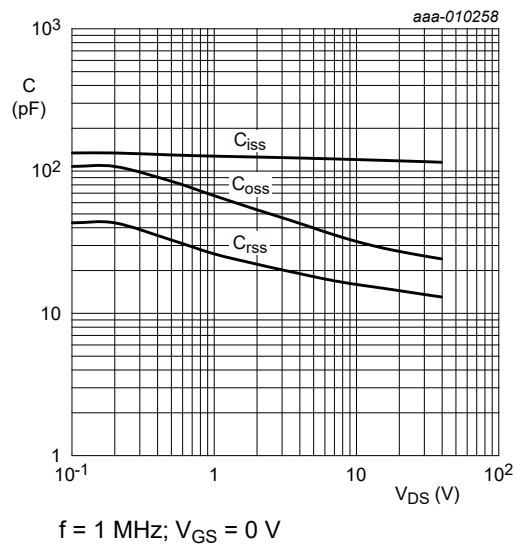


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

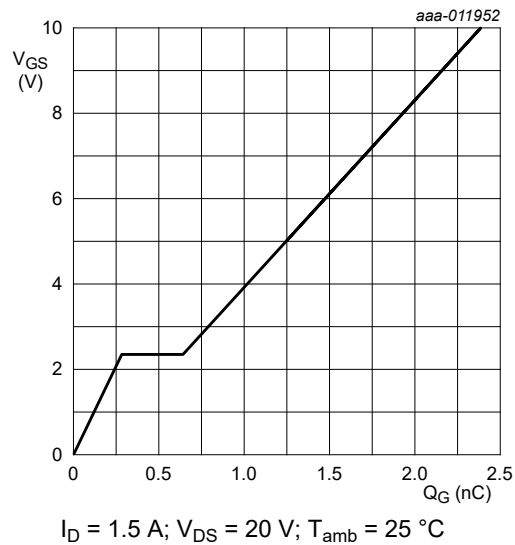


Fig. 14. Gate-source voltage as a function of gate charge; typical values

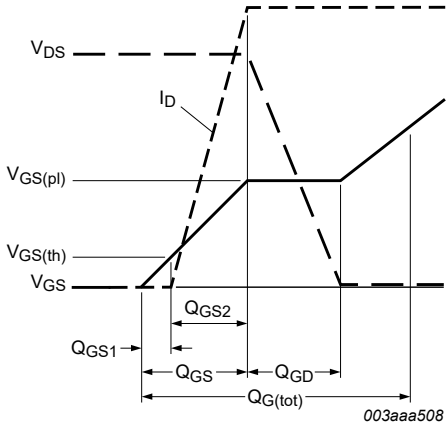


Fig. 15. Gate charge waveform definitions

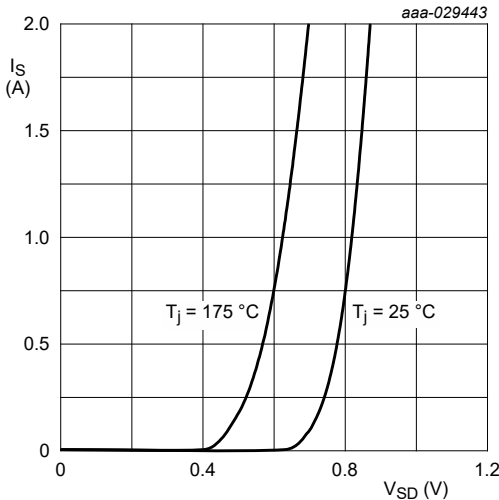


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information



Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

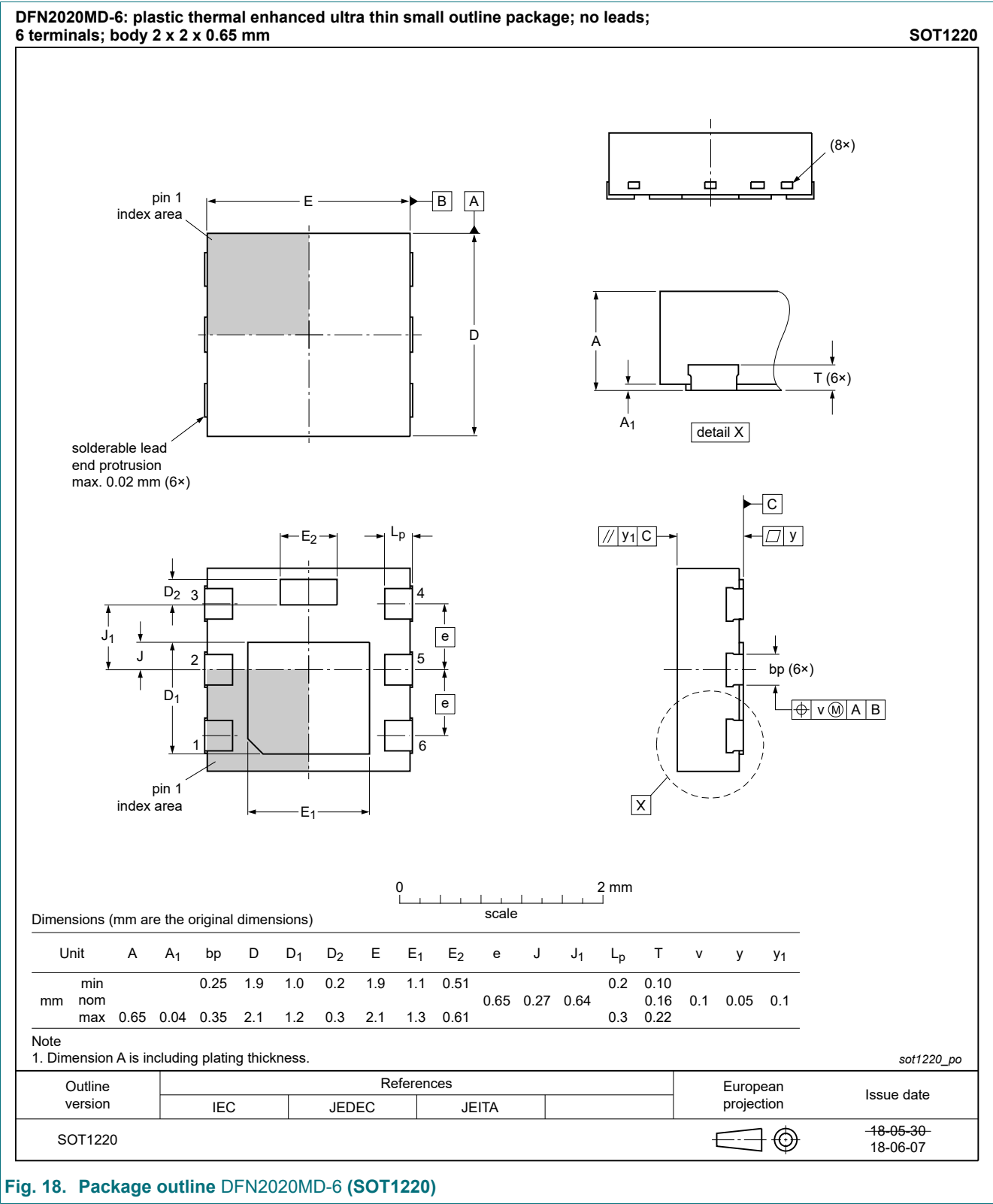


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

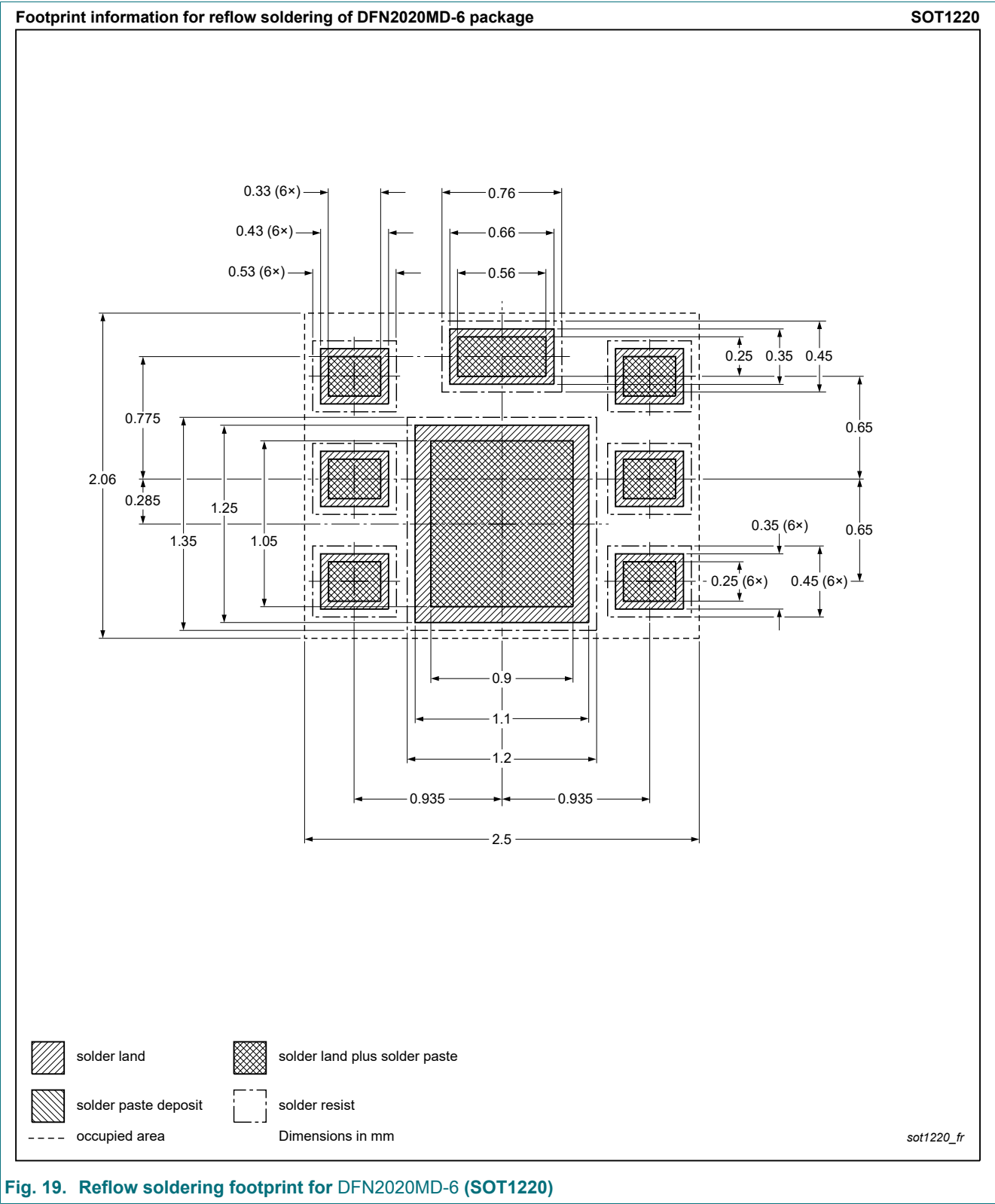


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6D120-40E v.1	20190429	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 29 April 2019

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