MIC2111B

High-Performance, Multi-Mode, Step-Down Controller

General Description

Micrel's MIC2111B is a programmable-frequency, valley-current/voltage-mode PWM controller that provides the control and protection features necessary for power devices and drivers that use current sensing across the inductor. The MIC2111B can provide single tri-state PWM logic signal to work with either power-stage modules or discrete driver and MOSFETs. The device has precision enable and power-good (PG) functions for sequencing of multiple power supplies. In addition, the solution is compatible with intelligent power stages in a high-current, step-down DC/DC converter.

To optimize system size and system efficiency, the MIC2111B frequency can be programmed from 200kHz to 2MHz. The device operates in power-saving mode at light loads by reducing frequency. Optional outside audio range operation is possible when the power-stage is configured in light load mode. The solution uses differential current sensing for better current-limit accuracy and a dedicated differential amplifier for remote output sensing for accurate output voltage control. The MIC2111B has a high-gain transconductance amplifier for loop compensation. External slope compensation can be added through a resistor to avoid sub-harmonic oscillations. Other features include programmable OCP, output OVP, and thermal OTP protections. The MIC2111B offers Micrel's proprietary bi-directional, single wire fault communication for total system protection.

The MIC2111B is available in a 20-pin 3mm × 3mm TQFN package and has a junction temperature range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

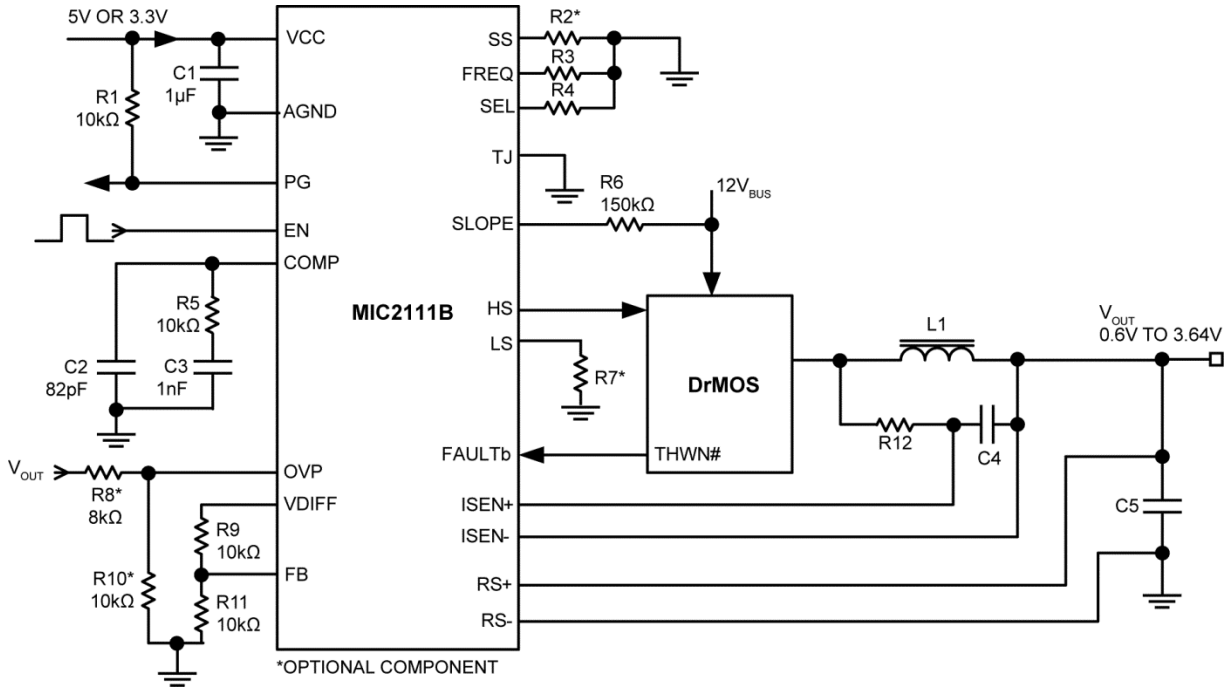
Features

- Single 3.3V or 5V supply
- Supports load currents up to 40A
- Programmable valley-current/voltage-mode PWM architecture
- 3.3V logic PWM output compatible with power-stage modules and DrMOS modules
- Single tri-state PWM output
- Programmable switching frequency: 200kHz to 2MHz.
- Differential remote sensing for output voltage and inductor current
- 0.6V reference voltage with total ±1% accuracy for output
- Adjustable soft-start/soft-stop and pre-biased safe startup.
- Supports light load and outside audio modes
- Programmable slope compensation and loop compensation
- Enable input, power-good (PG) output for sequencing
- Programmable OCP, output OVP, thermal OTP, and dedicated FAULTb pin for system safe startup/stop
- Internal thermal shutdown and UVLO
- –40°C to +125°C junction temperature range
- Available in 20-pin 3mm × 3mm TQFN package

Applications

- Servers and work stations
- Routers, switches, networking/telecom infrastructure
- Printers, scanners, graphics and video cards
- High current, high-performance POLs

Typical Application

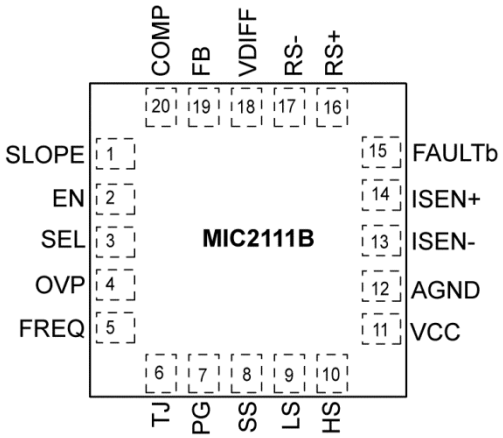


MIC2111B and DrMOS for a 25A Synchronous Buck Converter

Ordering Information

Part Number	Switching Frequency	Junction Temperature Range	Current-Sense Gain	Power Stage	Package	Lead Finish
MIC2111BYMT	200kHz to 2MHz	–40°C to +125°C	30V/V	DrMOS	20-Pin 3mm × 3mm TQFN	Pb-Free

Pin Configuration



20-Pin 3mm × 3mm TQFN (MT)
(Top View)

Pin Description

Pin Number	I/O	Pin Name	Pin Name
1	I	SLOPE	Valley Current Mode: Slope compensation can be adjusted by adding a resistor from this pin to VIN (input power supply). Voltage Mode: Artificial ramp controlled by SLOPE resistor
2	I	EN	Enable (Input): A logic signal to enable or disable the controller. The EN pin is CMOS compatible. Logic high = enable, logic low = disable or shutdown. Do not leave floating.
3	I	SEL	Control-Mode Selection Pin: Connect this pin to AGND for valley current-mode operation. Leave this pin open for voltage mode control operation.
4	I	OVP	Output OVP programming pin. Connect a resistive divider to set OVP.OVP pin has 0.6V reference (see *Functional Description* for more details).
5	I	FREQ	Switching Frequency Adjust (Input): Connect a resistor from this pin to GND to set the switching frequency.
6	I	TJ	Power Module Temperature Sense Pin. Connect resistor divider to program TJ. TJ comparator has 0.6V reference (see *Functional Description* for more details).
7	O	PG	Power Good (Output): Open drain output, an external resistor to V_{OUT} is required for pull-up.
8	I	SS	Soft-start pin for limiting inrush current. A resistor from this pin to ground sets the soft-start time. If enabled, soft-stop time is same as soft-start. Contact factory for soft stop.

Pin Description (Continued)

Pin Number	I/O	Pin Name	Pin Name
9	I/O	LS	Low-Side Logic Output. Connect this pin to module-mode pin for outside audio operation. Leave this pin open if outside audio (>25kHz) operation is not required. Current limit can be adjusted by connecting a resistor from LS to AGND (see Table 1 for details).
10	O	HS	High-Side Logic of Power Module Top FET. Connect this pin to the PWM pin of power module. This pin has tri-state capability.
11	P	VCC	5V Supply Input. A 1µF ceramic capacitor from VCC to AGND is required for decoupling.
12	P	AGND	Analog Ground.
13	I	ISEN–	Negative pin of the inductor current-sense input.
14	I	ISEN+	Positive pin of the inductor current-sense input.
15	I/O	FAULTb	Bi-Directional Pin. This pin goes low if controller or module is not ready. This pin goes low if V_{CC} is less than UVLO, or if a TJ or OVP fault is triggered. Either VCC cycling or EN cycling is required to clear the fault. This pin has an internal 100kΩ pull-up resistor to VCC
16	I	RS+	The non-inverting input of the remote sensing amplifier. Remote sense for output voltage.
17	I	RS-	The inverting input of the remote sensing amplifier. Remote sense for GND.
18	O	VDIFF	Output of differential amplifier. Connect a resistor divider from VDIFF to set output voltage
19	I	FB	The inverting input of the error amplifier.
20	I/O	COMP	Transconductance Amplifier Output. Connect compensation network from COMP node for frequency response.

Absolute Maximum Ratings[1]

V_{CC} to AGND ..... –0.3V to +6.0V
$V_{EN/SS}$, V_{FREQ} to AGND..... –0.3V to (V_{CC} +0.3V)
V_{OVP}, V_{TJ}, V_{FAULTb} to AGND ..... –0.3V to (V_{CC} + 0.3V)
$V_{RS±}$, $V_{HS/LS}$, $V_{ISEN±}$, V_{FB} to AGND ..... –0.3V to (V_{CC} + 0.3V)
V_{SLOPE} to AGND..... –0.3V to 20V
Junction Temperature ..... +150°C
Storage Temperature (T_S)..... –65°C to +150°C
Lead Temperature (soldering, 10s)..... 260°C
ESD
Human Body Model[3] 2kV
Machine Model 200V

Operating Ratings[2]

Supply Voltage (V_{CC})..... 3.135V to 5.5V
Enable Input (V_{EN})..... 0V to V_{CC}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
20-Pin 3mm × 3mm TQFN (θ_{JA}) ..... 60°C/W
20-Pin 3mm × 3mm TQFN (θ_{JC}) ..... 10°C/W

Electrical Characteristics[4]

V_{CC} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input (VCC)					
VCC Input Voltage Range	Valley current mode, voltage mode	**3.135**		**5.5**	V
VCC UVLO Threshold	V_{CC} rising	**2.75**	2.85	**2.95**	V
VCC UVLO Hysteresis			100		mV
Quiescent Supply Current	No switching, V_{FB} >0.8V		2.1		mA
Shutdown Supply Current	V_{EN} = 0V			**10**	µA
Output Voltage					
Output Voltage		**0.6**		**3.46**	V
Minimum V_{CC}-to-Output Set Point	Minimum V_{CC} – V_{OUT} headroom required			**1.3**	V
Voltage Accuracy	(RS+) - (RS-)	**0.594**	0.6	**0.606**	V
Remote Sense Amplifier Gain	V_{DIFF}/[(V_{RS+}) – ($V_{RS–}$)], $V_{RS–}$ = 0V ; V_{RS+} = 3.6V	0.997	1.000	1.003	V/V
Remote Sense Amplifier Source/Sink Current		**550**			µA
RS+ Input Impedance			175		kΩ
RS– Input Impedance			87		kΩ
RS+/RS– Common-Mode Voltage		**100**			mV
FB Bias Current	V_{FB} = 0.6V		5	**100**	nA
Transconductance Error Amplifier					
Error Amplifier Transconductance	FB-to-COMP g_m		2		mS
Error Amplifier Source/Sink Current		175	220		µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside operating range
3. Devices are ESD sensitive. Handling precautions recommended. Human body model is 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Electrical Characteristics[4] (Continued)

V_{CC} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Enable/Soft-Start/Soft-Stop					
EN Threshold Voltage	EN rising, point at which the output is enabled	**1.0**	1.2	**1.3**	V
EN Hysteresis			50		mV
Soft-Start time	R_{SS} = Floating		2		ms
Soft-Stop Time[5]	R_{SS} = Floating		2		ms
Oscillator and PWM					
Switching Frequency	R_{FREQ} = 49.9kΩ	**1.6**	2	**2.4**	MHz
	R_{FREQ} = 100kΩ	**0.85**	1	**1.15**	
	R_{FREQ} = 499kΩ	**0.16**	0.2	**0.24**	
Minimum Duty Cycle	V_{FB} = 0.8V		0		%
Minimum Off-Time	CCM		100		ns
Minimum On-Time	CCM		40		ns
HS, LS Logic High Voltage	I_{LOAD} = 50mA	**4**			V
HS, LS Logic Low Voltage	I_{LOAD} = 50mA			**0.8**	V
HS Tri-State Leakage Current	V_{HS} = 1.5V	**-1**		**1**	µA
LS Tri-State Leakage Current	V_{LS} = 1.5V	**-1**		**1**	µA
HS, LS Rise/Fall Time	C_{LOAD}= 20pF		1		ns
Outside Audio DCM time	No Load		32		µs
Current-Sense Amplifier					
Current Amplifier Gain			30		V/V
Current Amplifier Bandwidth	3dB bandwidth		10		MHz
Current-Limit Threshold	LS = 0.5V	**15**	18.3	**22.5**	mV
	LS = 0.7V	**20**	23.3	**27.5**	
ISEN+I_{SEN}-Input Bias Current			0.01	**0.1**	µA
Slope Compensation					
V_{SLOPE} Common-Mode Range		**0.6**		**3.46**	V
SLOPE Sink Current	Valley Current Mode			**280**	µA
Power Good (PG)					
Power Good Threshold Voltage	FB rising	**90**	92	**95**	%VOUT
Power Good Hysteresis			2		%VOUT
Power Good Delay	FB rising, delay from FB high to PG high		200		µs
Power Good Low Voltage	V_{FB} < 90% × V_{NOM}, I_{PG} = 1mA		12	**200**	mV

Note:

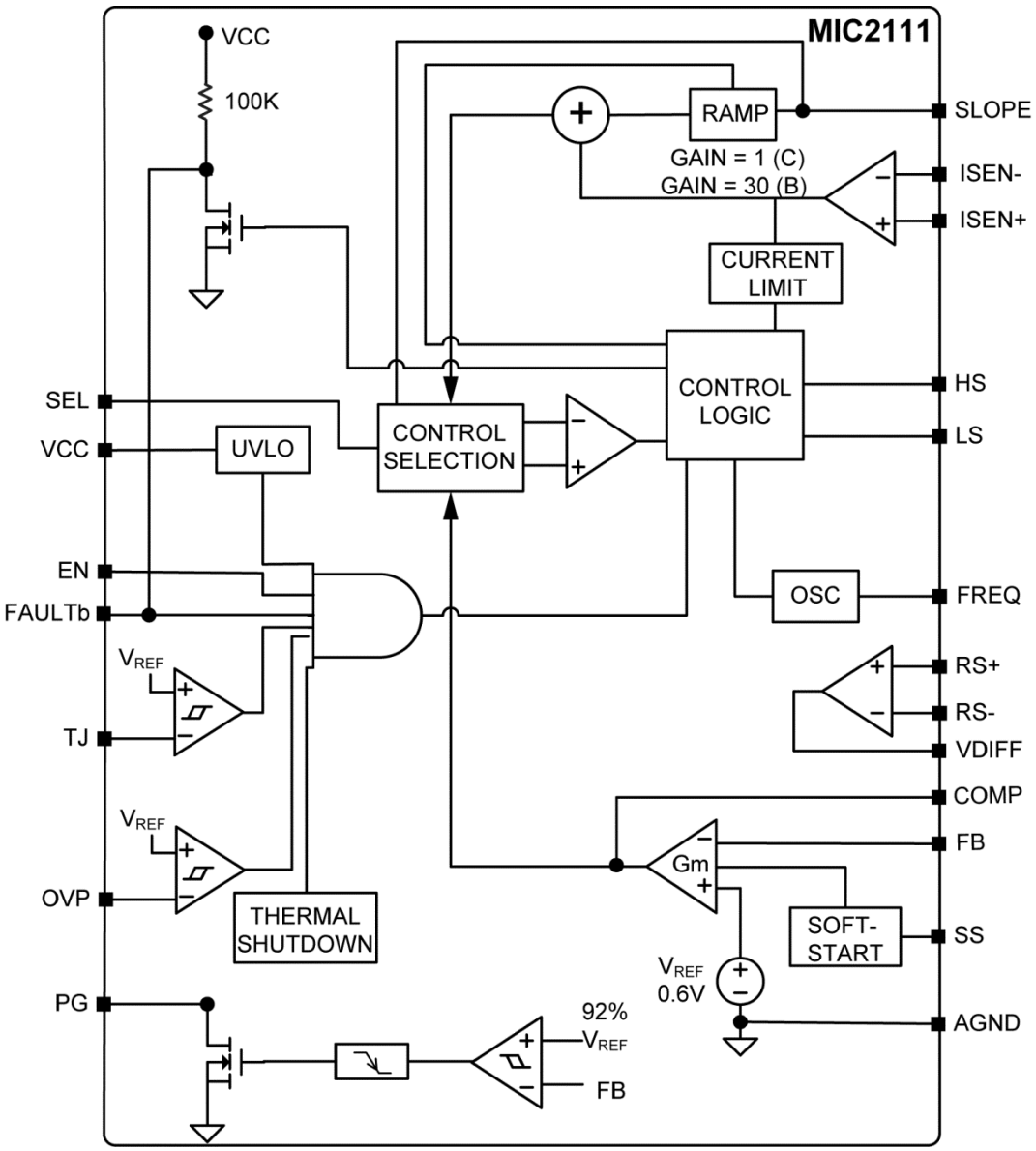
5. Soft-stop is disabled by default. Contact factory to enable soft-stop.

Electrical Characteristics[4] (Continued)

V_{CC} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C

Parameter	Condition	Min.	Typ.	Max.	Units
FAULTb					
FAULTb Threshold Voltage	FAULTb rising	**2**	3.1		V
FAULTb Hysteresis			1.1		V
FAULTb Low Voltage	I_{LOAD} = 500µA		10	**50**	mV
FAULTb Leakage Current				**1**	µA
OVP					
OVP Threshold Voltage	OVP rising	0.585	0.6	0.615	V
OVP Hysteresis			20		mV
Thermal Shutdown					
TJThreshold Voltage	TJ_J rising	0.585	0.6	0.615	V
TJ Hysteresis			50		mV
Internal Thermal Shutdown	Temperature rising		155		°C
Internal Thermal Shutdown Hysteresis			20		°C

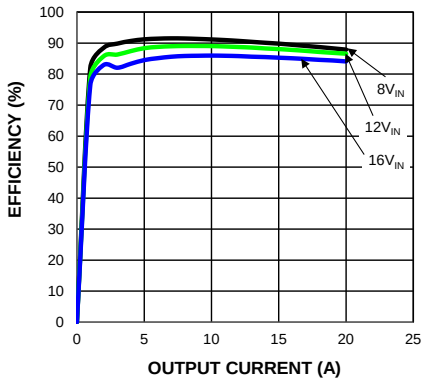
Functional Block Diagram



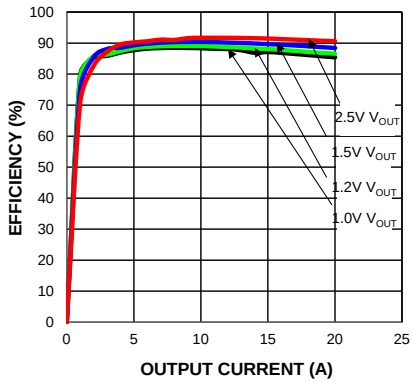
Typical Characteristics

Refer to *Typical Application Schematic*.

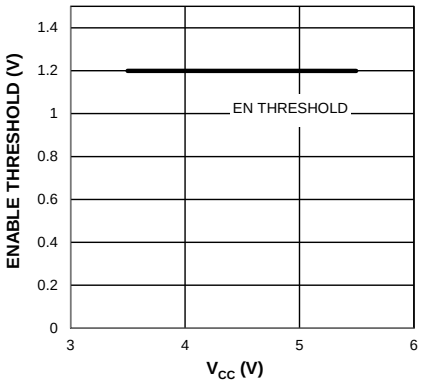
Efficiency vs. Output Current (V_{OUT} = 1.2V)



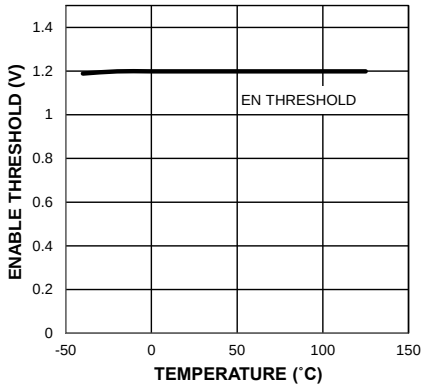
Efficiency vs. Output Current (V_{IN} = 12V)



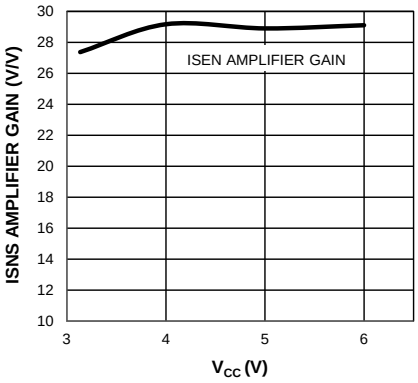
EN Threshold vs. V_{CC} Change



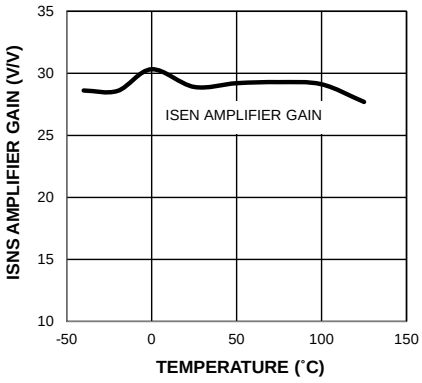
EN Threshold vs. Temperature



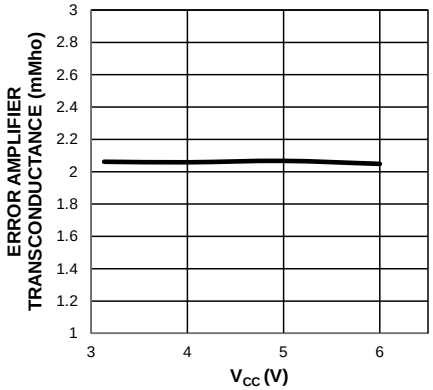
ISEN Amplifier Gain vs. V_{CC} (MIC2111B)



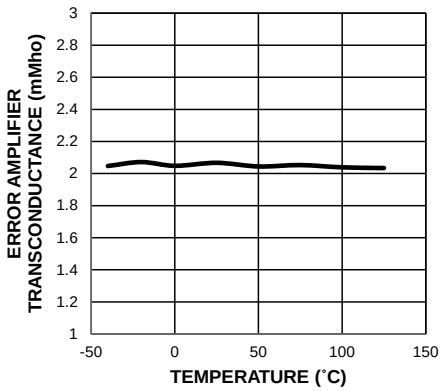
ISEN Amplifier Gain vs. Temperature (MIC2111B)



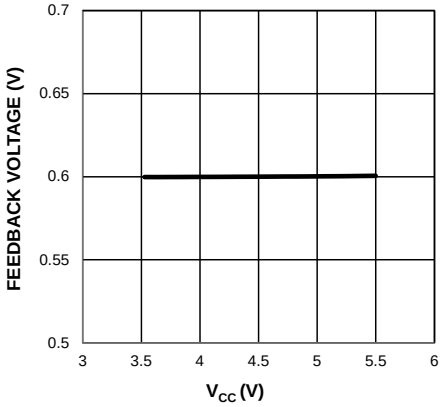
Error Amplifier Transconductance vs. V_{CC} (T = 25°C)



Error Amplifier Transconductance vs. Temperature (V_{CC} = 5V)

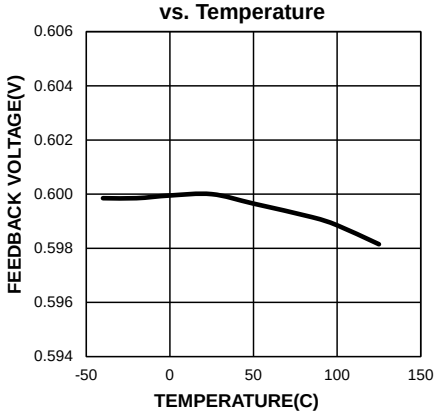


Feedback Voltage vs. V_{CC}

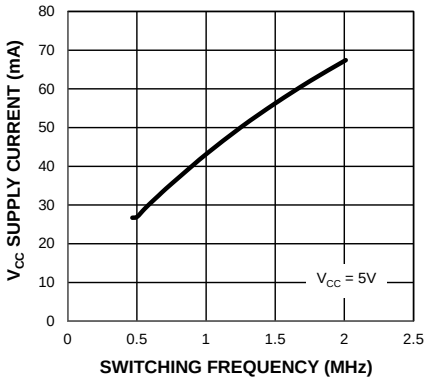


Typical Characteristics (Continued)

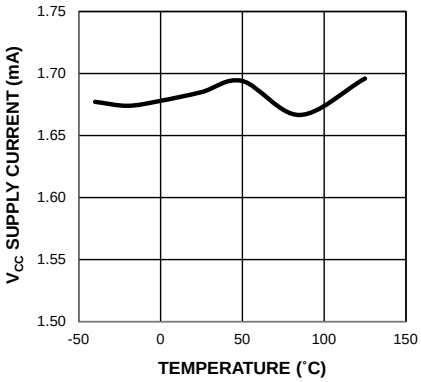
Feedback Voltage vs. Temperature



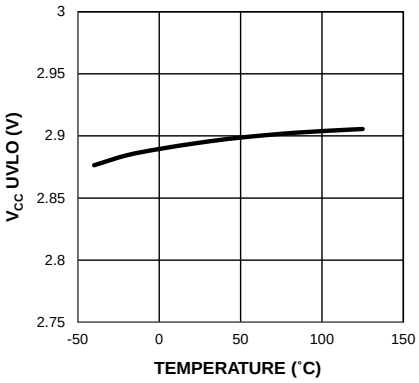
V_{CC} Supply Current vs. Switching Frequency



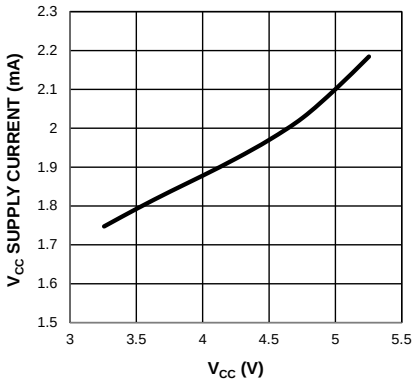
V_{CC} Supply Current vs. Temperature



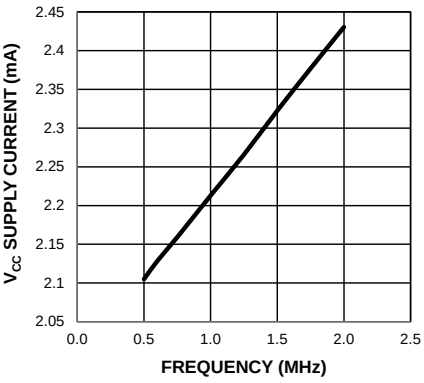
V_{CC} UVLO vs. Temperature



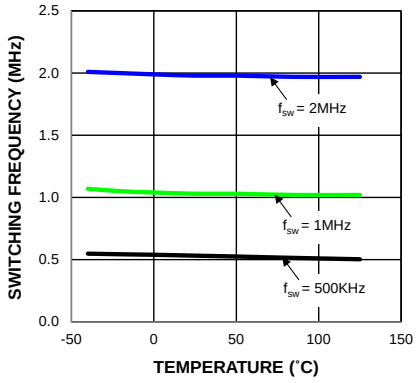
V_{CC} Quiescent Current vs. V_{CC} Voltage



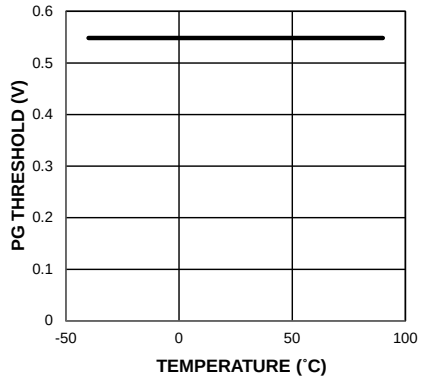
V_{CC} Quiescent Current vs. Frequency



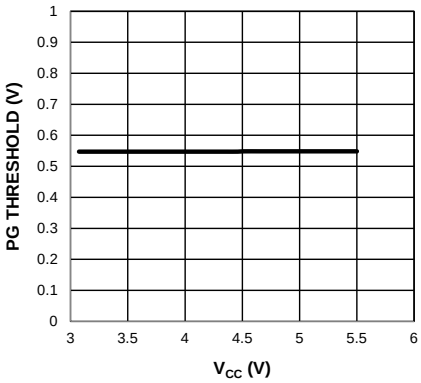
Switching Frequency vs. Temperature



PG Threshold vs. Temperature

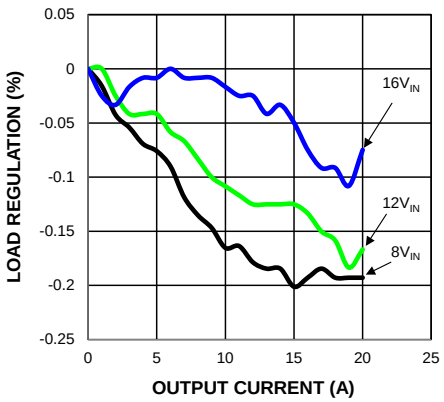


PG Threshold vs. V_{CC}

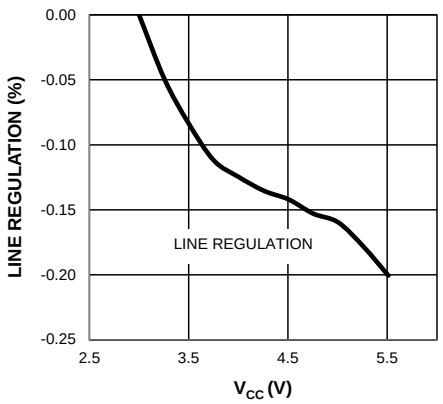


Typical Characteristics (Continued)

Load Regulation vs. Output Current



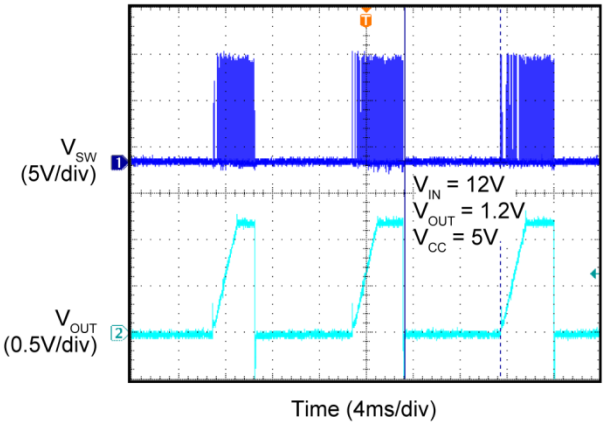
Line Regulation vs. V_{CC} (V_{IN} = 12V, V_{OUT} = 1.2V, 5A Load)



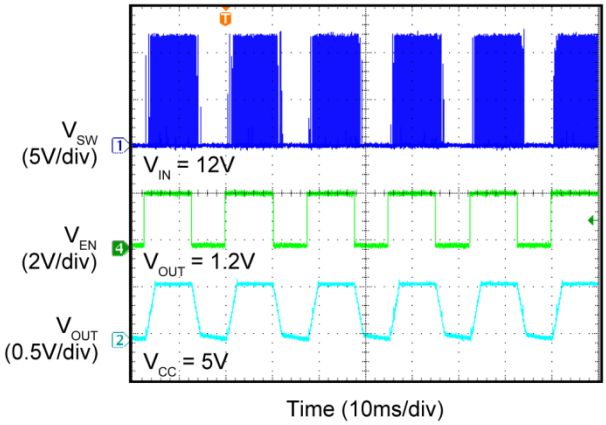
Functional Characteristics

Refer to *Typical Application Schematic*.

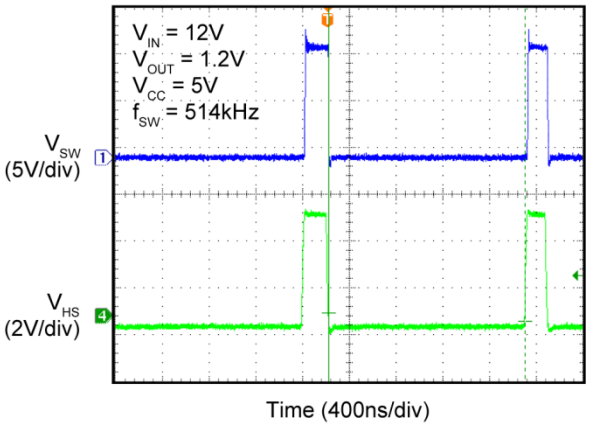
Short Circuit



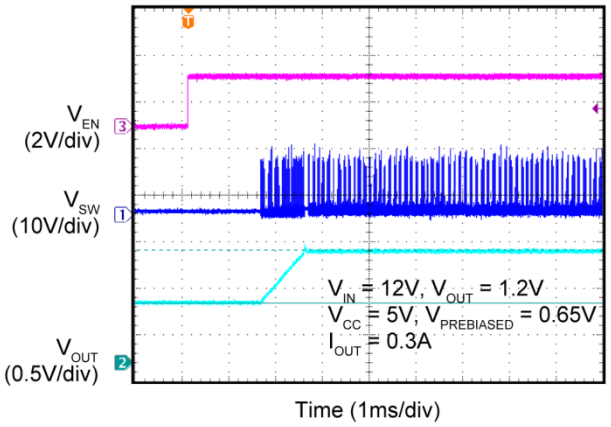
Enable Start and Disable Toggling



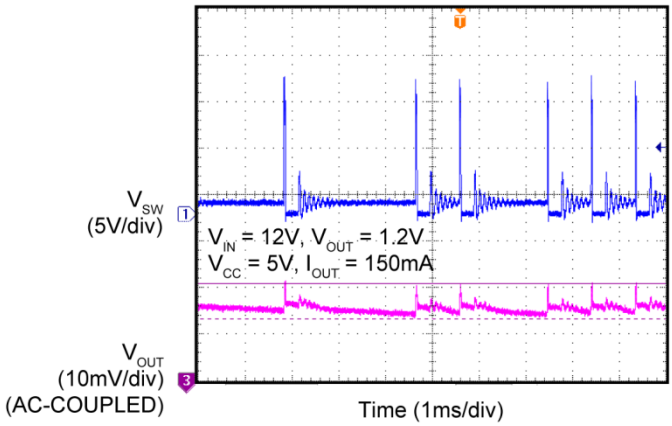
Switching Waveforms



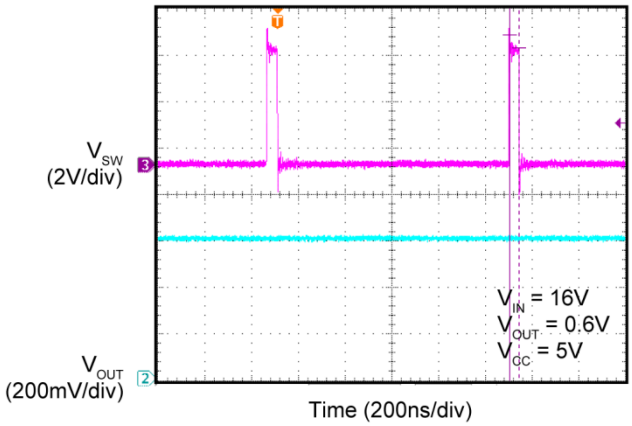
Prebiased Start-Up



Switching Waveforms (Light Load Conditions)



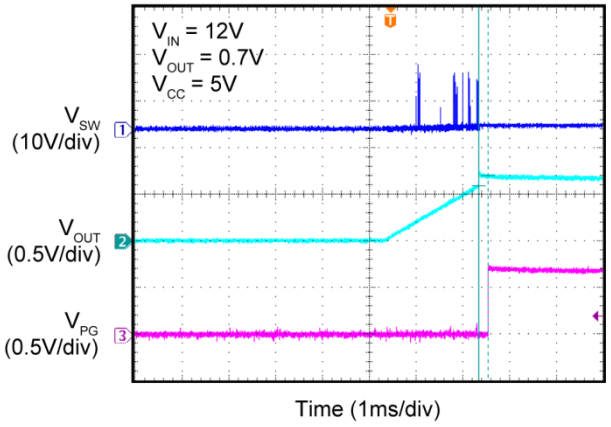
Minimum On-Time



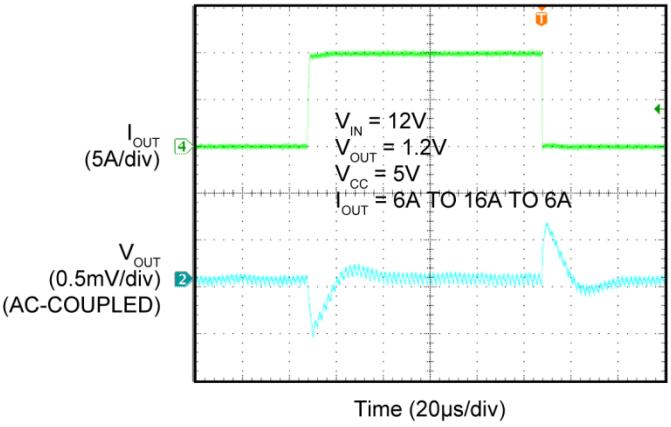
Functional Characteristics (Continued)

Refer to *Typical Application Schematic*.

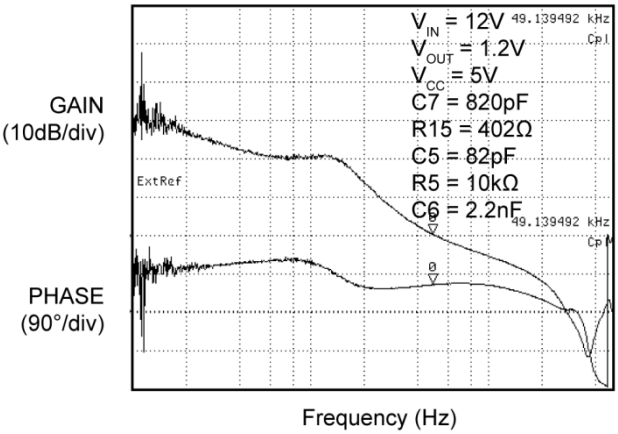
Start-Up Condition



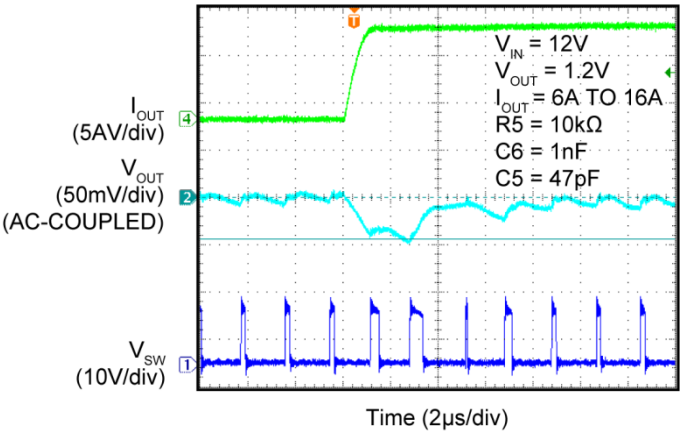
Transient Condition (Voltage Mode)



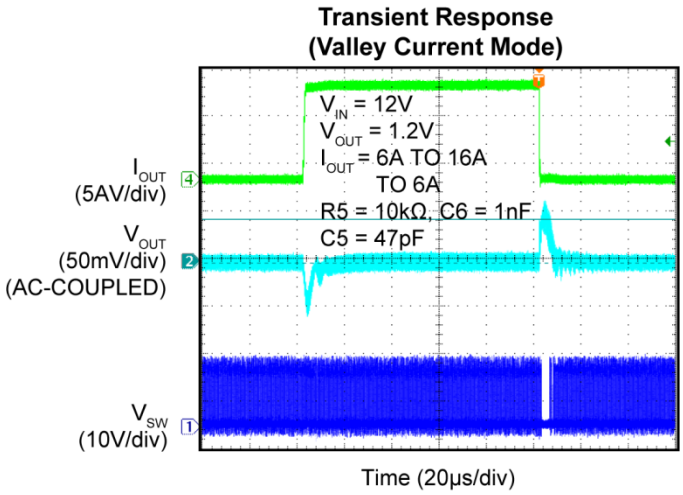
Bode Plot (Voltage Mode)



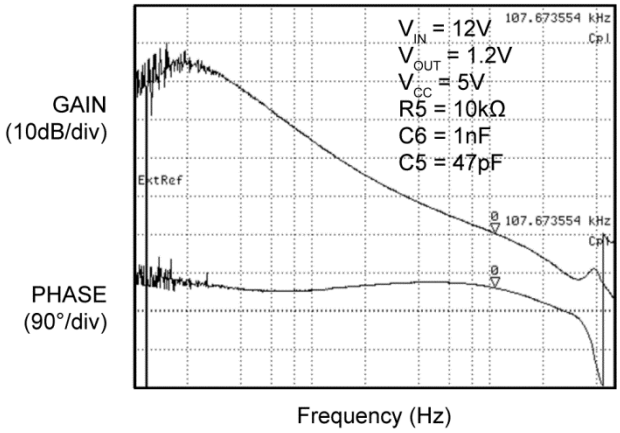
Transient Response (Valley Current Mode)



Transient Response (Valley Current Mode)



Bode Plot (Valley Current Mode)



Functional Description

The MIC2111B is a pin-programmable control-mode, single-phase PWM buck controller. The control mode can be programmed to either valley current mode or voltage mode through a single pin. The device provides the control and protection features necessary for driving intelligent power stages in high-current, step-down, DC/DC converters. The MIC2111B is also compatible with DrMOS power stages and drivers that use current sensing across the inductor. The MIC2111B provides a single tri-state, PWM logic signal that works with either power-stage modules or discrete-driver MOSFETs. It has precision enable and power good (PG) functions for sequencing of multiple power supplies and its frequency can be programmed from 200kHz to 2MHz thereby optimizing system size and system efficiency.

The device supports power-saving mode at light loads when the MODE pin of the power stage is connected to GND. Optional outside audio range operation is also possible when the power stage is configured in light load mode. The MIC2111B uses differential current sensing for better current-limit accuracy. It also uses a dedicated differential amplifier for remote output sensing to achieve accurate output voltage control. The MIC2111B has a high-gain transconductance amplifier for easier loop compensation. External slope compensation can be added through a resistor to avoid sub-harmonic oscillations. The MIC2111B has programmable OCP, output OVP and thermal OTP protections and offers Micrel's proprietary bi-directional, single-wire fault communication for total system protection.

Control Architecture

The MIC2111B is a pin-programmable multi-mode, single-phase PWM buck controller that can be operated under valley-current-mode and voltage-mode control architectures.

Valley Current Mode

When MIC2111B is programmed to a fixed-frequency, valley current mode control architecture, the inductor current is sensed by the voltage drop measured across the DCR of the inductor (MIC2111B). The current is sensed during the off period of the switching cycle and is conditioned with the internal current sense amplifier. The gain of the current sense amplifier is 30 V/V. The output signal of the current sense amplifier is compared with the current programmed by the error amplifier to determine the correct duty cycle. Slope compensation is added via a resistor between V_{IN} and the SLOPE pin. The MIC2111B generates a (V_{IN} –V_{OUT}) proportional current and passes it through a capacitor to generate the slope compensation ramp.

This slope compensation ramp is then added to comp signal to avoid sub-harmonic oscillations for duty cycles of less than 50%.

Calculation of R_{SLOPE} can be found in the *Application Information* section.

Voltage Mode

The MIC2111B can also be configured as voltage-mode control scheme for noise sensitive applications. Control-loop compensation is external for providing maximum flexibility in choosing the operating frequency and output LC filter components. Ramp is generated by connecting a resistor between VIN and SLOPE. An internal transconductance error amplifier produces an integrated error voltage at COMP that helps to provide higher DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. On the rising edge of an internal clock, the PWM turns on. During this ON time, inductor current ramps up. Internal comparator turn OFF PWM once appropriate duty cycle is reached. During this time inductor releases the stored energy as the inductor current ramps down, providing current to the output.

Oscillator Frequency

The MIC2111B has an internal oscillator wherein the frequency can be set through an external resistor at the FREQ pin. The switching frequency can be programmed from 200kHz to 2MHz using Equation 1:

$$R_{FREQ} = 10^{11}/F_{SW}\ [\Omega] \qquad \text{Eq. 1}$$

Where:

F_{SW} = Desired switching frequency in Hz.

PWM Modes and Logic Levels

There are multiple versions of power stages currently on the market that support different load currents. These include DrMOS and other intelligent power-stages. All these power stages contain a MOSFET driver, high-side and low-side MOSFETs. These power stages require a single tri-stated PWM control signal for control and protection (Table 1).

Table 1. PWM Truth Table

LS	HS	High-Side FET	Low-Side FET	Switch Node
0	0	OFF	ON to OFF	Diode Emulation
0	1	ON	OFF	High
X	Tri-State	OFF	OFF	Tri-State (Pre-Bias/ Fault Shutdown)
1	0	OFF	ON	Low
1	1	ON	OFF	High

The MIC2111B will output a PWM signal on the HS pin with levels of 0 (turn on the low-side driver) and 1 (turn on the high-side driver). HS will be turned high-impedance (tri-state) when a fault condition exists which should be interpreted by the power stage to turn-off both the high-side driver and low-side driver. MIC2111B supports 3.3V logic-compatible PWM thresholds on HS. These levels can found in the "Oscillator and PWM" section within the *Electrical Characteristics.*

Programmable Current-Limit and Hiccup Mode

MIC2111B has a dedicated current-sense amplifier and can support high load currents up to 40A in single-phase configuration. The MIC2111B also features differential current sense input pins (ISEN+ and ISEN–).

With the MIC2111B, it is possible to sense current across inductor DCRs for low-cost applications. As the DCR of the inductor will be less than 1mΩ for a high-current application, the MIC2111B features a current-sense amplifier with a gain of 30V/V. This amplified signal is used for control and cycle-by-cycle current limit. These high-current applications need thermal compensation from the current-sense signal because of DCR variation with temperature. External thermal compensation could be provided using a NTC resistor in series with the RC across the inductor. See *Application Information* for more details about thermal compensation and filter calculations.

Current limit can be programmed through an external resistor connected at the LS pin. The MIC2111B provides two selectable current-limit thresholds. During start-up, a current source of 8µA is injected into the external resistor connected between the LS pin and GND. The voltage developed across the resistor is measured as part of the power-up sequence and the current threshold determined as illustrated in Table 2.

Once the voltage has been measured, the current source is turned off. If LS is connected to the MODE pin of DrMOS, current-limit setting resistance must be adjusted for the input resistance of the MODE pin.

Many high-current applications require hiccup mode protection for current limit because they can see peak load currents for a very short duration. The MIC2111B uses a proprietary hiccup current-limit algorithm to avoid inductor saturation. An internal counter increments by two in each cycle over current is detected, and decrements by one each cycle when the current is not over the limit. When the counter reaches 16, the part will shut down and wait for 8ms before restarting again (Figure 2 and Figure 3).

E24 Range Resistance	MIC2111B Current-Limit Threshold
88kΩ	23.3mV
63kΩ	18.3mV

Table 2. Fault Handling

Parameter	Fault Flag	Action While Flagged with Intelligent Power Stage	Release
T_J	When TJ pin goes above 0.6V flag FAULTb immediately.	Turn off high- and low-side FETs, i.e., tri-state.	Release Fault when T_J falls below 0.6V (50mV hysteresis)
Internal T_{SD}	When 155°C is detected, flag FAULTb immediately.	Turn off high- and low-side FETs, i.e., tri-state.	Release FAULTb when temperature falls below 130°C.
OVP	When OVP pin goes above 0.6V flag FAULTb immediately.	Turn off high- and low-side FETs, i.e., tri-state.	Enable or V_{CC} cycling.
UVLO	When UVLO, FAULTb is flagged.	Turn off high- and low-side FETs, i.e., tri-state.	Release when not UVLO.
Current Limit	FAULTb is not flagged. Enter into hiccup current mode.	8 consecutive current-limit cycles will enter hiccup mode. Wait for 8ms before retry.	No Flag/No release.
Pre-Bias Above Nominal V_{OUT}	Flag FAULTb immediately	Turn off high- and low-side FETs, i.e., tri-state.	Enable or V_{CC} cycling.

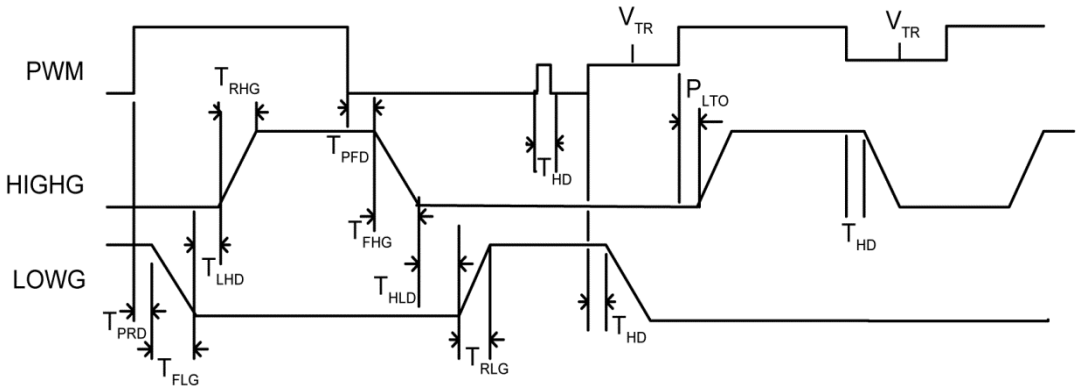


Figure 1. PWM Timing Diagram (all delays shown are assumed as a part of power stage operation)

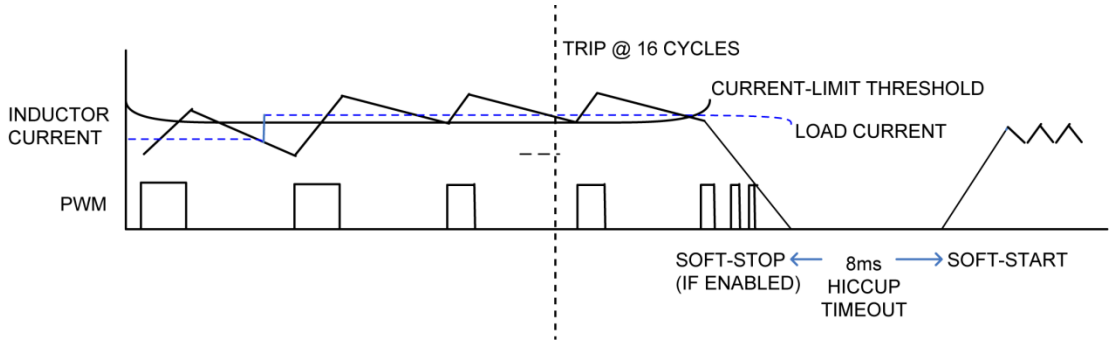


Figure 2. Cycle-by-Cycle Current Limit (MIC2111B)

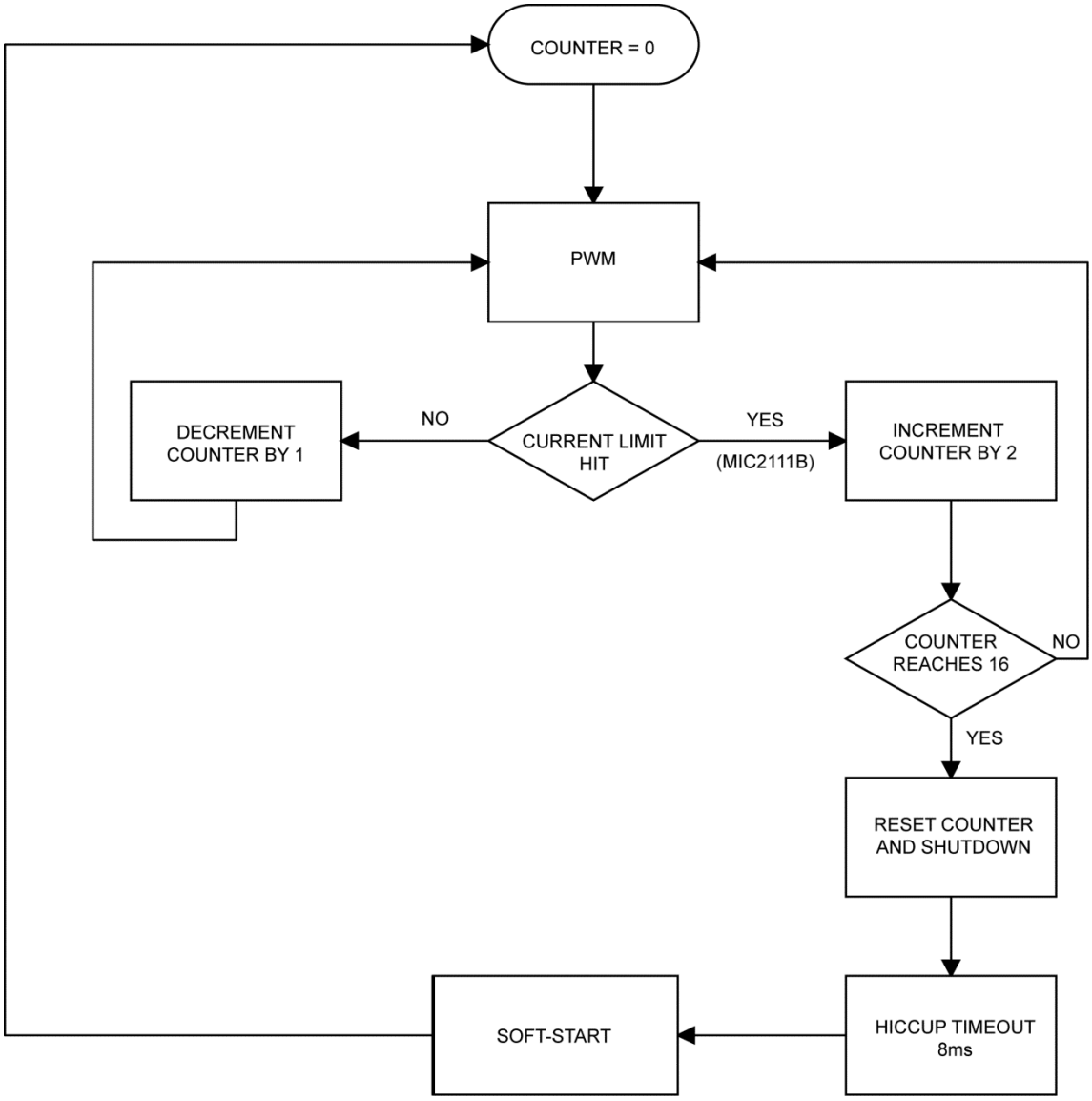


Figure 3. Hiccup Limit Flow Chart

VCC Undervoltage Lockout (UVLO)

The MIC2111B operates from a single 3.3V or 5V supply and has only 2mA of quiescent current. When bias voltage at V_{CC} is less than the under-voltage lockout (UVLO) level of 2.85V, HS will be high impedance to drive both MOSFETs to tri-state. UVLO has 100mV hysteresis to avoid an undesirable turn-on. If the same supply voltage is used for the power module and the MIC2111B, it is recommended to use a series RC filter (1Ω and 1µF) for MIC2111B bypassing.

Enable/Disable (EN) Control

The precision EN pin is used to enable or disable the MIC2111B. The typical threshold is 1.2V. When the voltage at EN rises above the threshold, the controller is enabled and starts normal operation after initialization of the internal oscillator, references, current-limit settings, and the soft-start period. The MIC2111B has initialization delay of 250µs before the PWM output starts.

When the voltage at EN drops 100mV or more (hysteresis) below the threshold voltage, then the internal controller circuits in the MIC2111B are turned off. It is possible to use the EN pin for sequencing multiple power supplies along with power-good (PG) pin. Do not float the EN pin. An external RC delay may be added to achieve sequencing.

Power Good (PG)

The power-good (PG) pin is an open-drain output. External pull-up resistance is required between PG and an external voltage. When the feedback voltage, V_{FB}, rises above the PG threshold the PG output is pulled high after a delay of 200µs (contact Micrel for other PG delays).

Bi-Directional Fault Communication (FAULTb)

The MIC2111B adopts Micrel's proprietary fault (FAULTb) communication protocol. There are multiple system faults possible in a high-current environment. The MIC2111B features internal pull-up of 100kΩ between the VCC and FAULTb pin.

Soft-Start/Soft-Stop (SS)

The MIC2111B has digital soft-start/soft-stop (SS) to avoid high inrush current in the input supply lines. Soft-start time can be programmed with an external resistor connected from the SS pin to GND. Table 3 illustrates resistor values and soft start time. Soft-stop time is the same as the programmed soft-start time (contact Micrel for instructions on enabling soft-stop).

Table 3. Soft-Start Programming

E96 Range Resistance	Soft-Start	E96 Range Resistance	Soft-Start
6.19kΩ	64µs	105kΩ	3072µs
19.1kΩ	128µs	118kΩ	4096µs
30.9kΩ	256µs	130kΩ	6144µs
44.2kΩ	512µs	143kΩ	8192µs
56.2kΩ	768µs	154kΩ	16384µs
68.1kΩ	1024µs	169kΩ	24576µs
80.6kΩ	1536µs	182kΩ	32768µs
93.1kΩ	2048µs	Open	2048µs

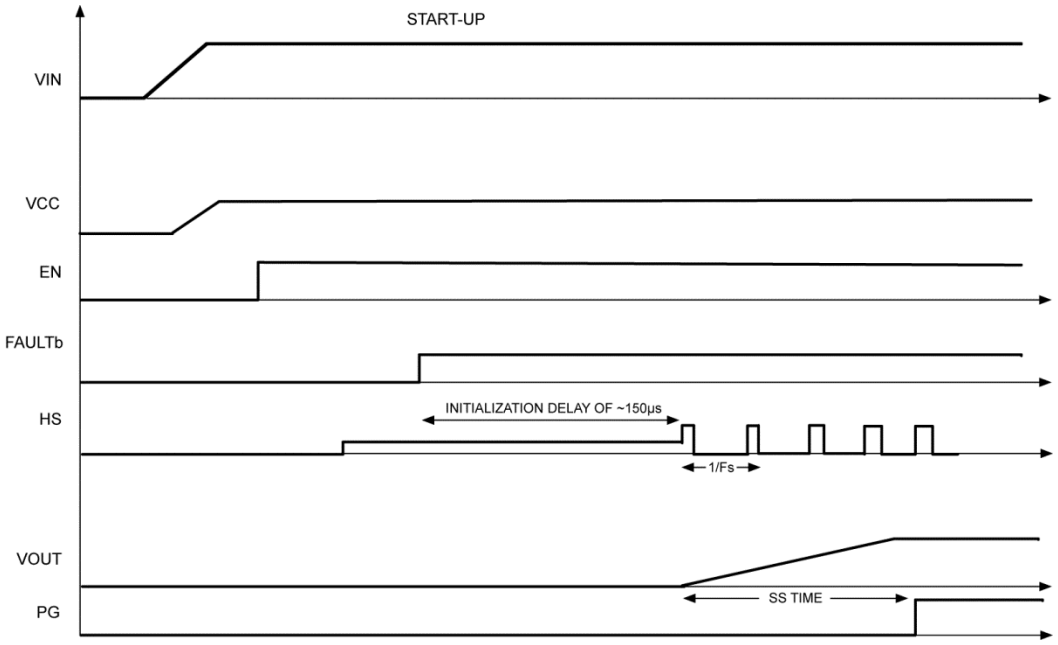


Figure 4. Typical System Soft-Start

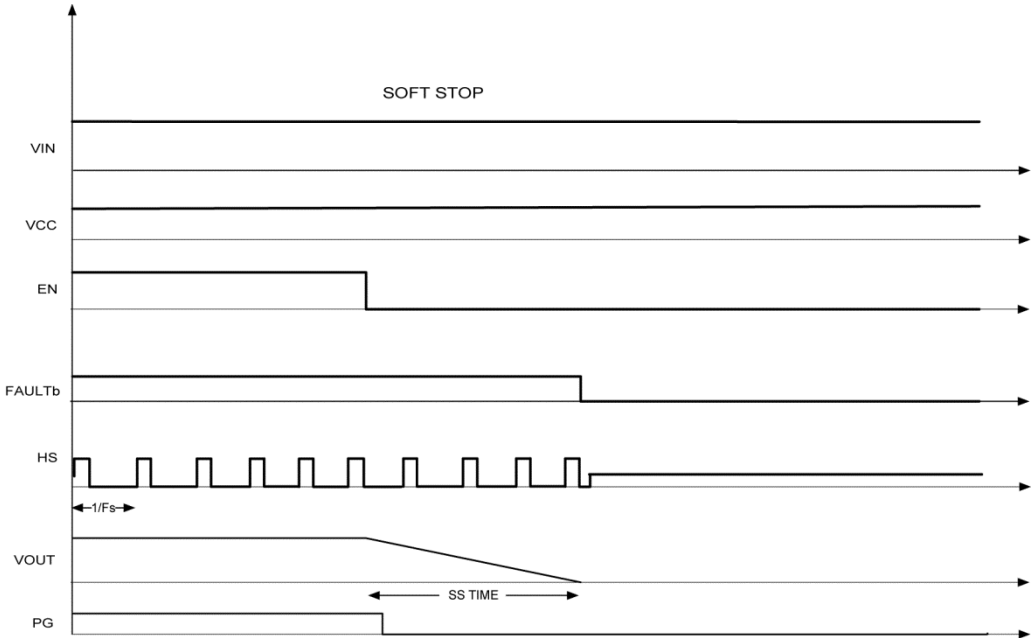


Figure 5. Typical Soft-Stop

Light Load Operation (DCM)

The MIC2111B supports pulse-skip mode for good light efficiency. Connecting the MODE or SMOD# pin of the power module to GND is required to enable the light-load mode. To avoid discharging the output during light-load mode, the power module zero current detector disables the low-side FET once inductor current reaches zero. The MIC2111B generates the next PWM signal based on COMP voltage. This will cause discontinuous conduction mode at the switch node as shown below.

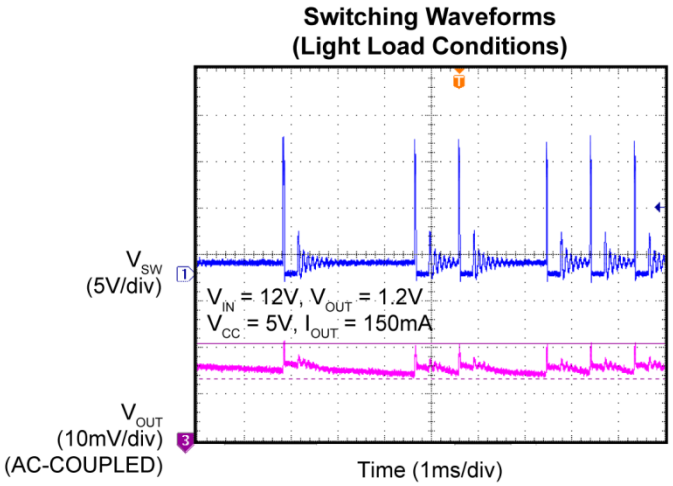


Figure 6. Light Load Operation (DCM)

Outside Audio Operation

Some systems require outside audio operation during light-load mode. When the system load reduces during light-load mode, the system will change from CCM to DCM and, as the load reduces further, the switching frequency reduces as well. If the effective switching frequency reduces below a certain threshold, the MIC2111B will enter outside audio mode, attempting to maintain the effective switching frequency above the audio band. For the outside audio mode to function, the LS output of the MIC2111B must be connected to the MODE pin of the DrMOS. While in this mode, if the MIC2111B detects that the period between HS pulses is longer than 32µs it forces LS a logic-1, which turns on the low-side driver. This results in current flowing from the output capacitor through the inductor and low-side MOSFET. This can cause the output voltage to fall and initiate a PWM cycle with HS going high and LS going low.

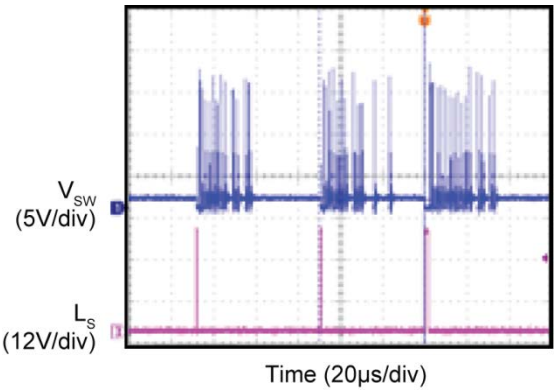


Figure 7. Outside Audio Waveform

Output Overvoltage Protection (OVP)

The MIC2111B has a dedicated pin for overvoltage protection (OVP). The OVP pin senses the output voltage through a voltage divider. If this voltage is higher than the reference voltage, the overvoltage protection engages and FAULTb is pulled low.

This OVP function typically protects against open feedback loop or V_{FB} short-to-GND. This will protect the costly load from being damaged by the DC/DC converter.

The OVP level can be programmed through a resistive divider at the OVP pin as follows. Select R4 same as lower feedback resistor. R1 can be calculated based upon required OVP level as illustrated in Equation 1 and Figure 8.

$$R_1 = R_4 \times \left[\frac{V_{OUT} - 0.6V}{0.6V}\right] \quad \text{Eq. 1}$$

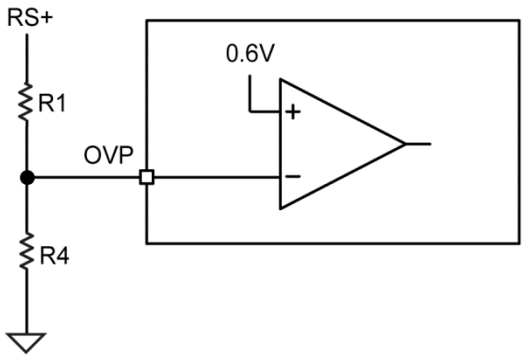


Figure 8. OVP Programming

After the OVP fault is triggered, the system will be shut down and latched off. It is required to cycle either VCC or EN for enabling the converter.

Temperature Sense Input

The MIC2111B has a dedicated input for thermal sense from intelligent power stages. The temperature sense pin (TJ) senses the voltage divided from thermal sense signal and sends it to the comparator. If this voltage is higher than the reference voltage, the thermal shutdown engages and FAULTb is pulled low. Thermal shutdown threshold can be programmed through a resistive divider from TJ.

$$R_1 = R_4 \times \left[\frac{V_{TSENSE} - 0.6V}{0.6V} \right] \quad \text{Eq. 2}$$

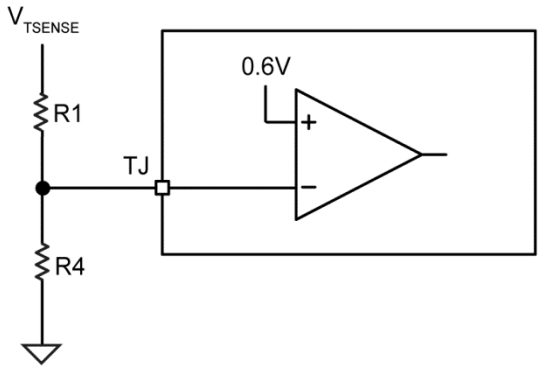


Figure 9. Thermal-Shutdown Programming

Output will be turned off by pulling FAULTb low after TJ fault is triggered. The fault will be released after hysteresis of 50mV is achieved.

Application Information

Programming Output Voltage with RS Amplifier Diagram

The output voltage is set using a resistive voltage divider from the output of differential amplifier to FB (Figure 10). For R1, use a 1kΩ to 10kΩ resistor. Choose R4 to set the output voltage by using Equation 3.

$$R_4 = R_1 \times \left[\frac{V_{FB}}{V_{OUT} - V_{FB}} \right] \quad \text{Eq. 3}$$

Where V_{FB} = 0.6V.

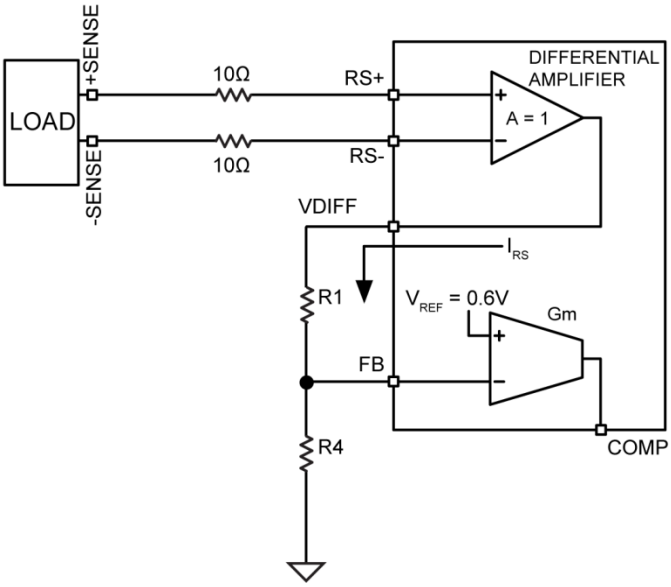


Figure 10. Programming Output Voltage

Current Sensing and Current Limit

MIC2111B has differential current-sense input with a dedicated current-sense amplifier. MIC2111BThe MIC2111B has current-sense amplifier gain of 30V/V and uses lossless inductor current sensing. This offers the advantage of lower power loss and lower cost over using a discrete resistor in series with the inductor.

The inductor sense circuit is shown in Figure 11. It extracts the voltage drop across the inductor's DC winding resistance.

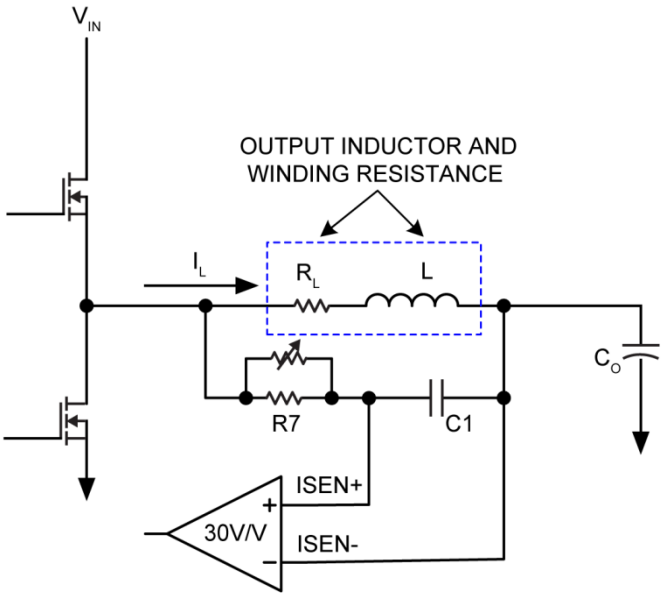


Figure 11. MIC2111B Current Sensing

The voltage across capacitor C1 is illustrated in Equation 4:

$$V_S = I_L \times R_L \left[\frac{\frac{sL}{R_L} + 1}{sC1 \times R7 + 1} \right] \quad \text{Eq. 4}$$

If the R7 x C1 time constant is equal to the L/R_L time constant, then the voltage across capacitor C1 equals R_L x I_L. Figure 12 is a plot of Equation 4. It assumes an inductance of 1.5µH, R_L = 0.01Ω (–40dB), C1 = 0.1µF and R7 = 1.5kΩ. The time constants are equal and diverge at the same rate. The overall impedance, H(s), equals R_L for all frequencies.

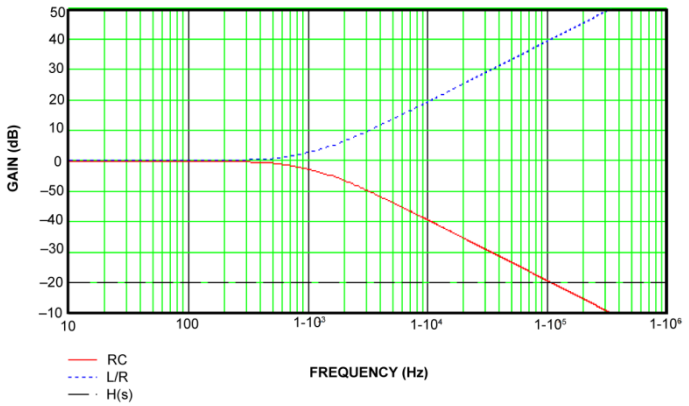


Figure 12. Current-Sense Gain/Phase Plot

For a system employing the MIC2111B with inductor current sensing, the absolute current-limit threshold is:

$$I_{LIM} = \frac{V_{THRESH}}{R_{DCR}} \quad \text{Eq. 7}$$

Here, R_{DCR} is the inductor DC resistance. For R_{DCR} = 1mΩ and a 23.3mV current-limit voltage threshold, the absolute current limit would be:

$$I_{LIM} = \frac{V_{THRESH}}{R_{DCR}} = 0.0233V / (1m\Omega) = 23.3A \quad \text{Eq. 8}$$

For compensating the inductor's DCR variation with temperature, an NTC is placed in parallel with the resistor (R7) in Figure 11.

Slope Compensation

Slope compensation is required in most conditions for current-mode PWM controllers. The MIC2111B applies slope compensation dependent on the system input voltage, output voltage and inductance by a single resistor. The resistor is connected between VIN and the SLOPE pin.

In VCM, 1x slope compensation is implemented by selecting the following resistor value:

R_{SLOPE} = K_{SLOPE} × L / [($A_{ISENAMP}$ × R_{SENSE})]

K_{SLOPE} = 1.33 × 10^{10}Ω/s

L = Inductor value

$A_{ISENAMP}$ = Internal current amplifier gain (30 in MIC2111B)

R_{SENSE} = External current-sense gain

For low-frequency applications (less than 500kHz) and noisy systems, increasing the slope compensation by a factor of 2 is recommended.

Because slope compensation is not needed in voltage mode, the SLOPE pin is used to generate the sawtooth ramp. A 1V peak-to-peak ramp at the PWM comparator input is implemented by selecting the following resistor value:

R_{SLOPE} = $K_{SLOPE} \times T \times (V_{IN} - V_{OUT})$

K_{SLOPE} = 1.33×10^{10} Ω/s

T = Switching period (1/switching frequency)

V_{IN} = System input voltage

V_{OUT} = Output voltage

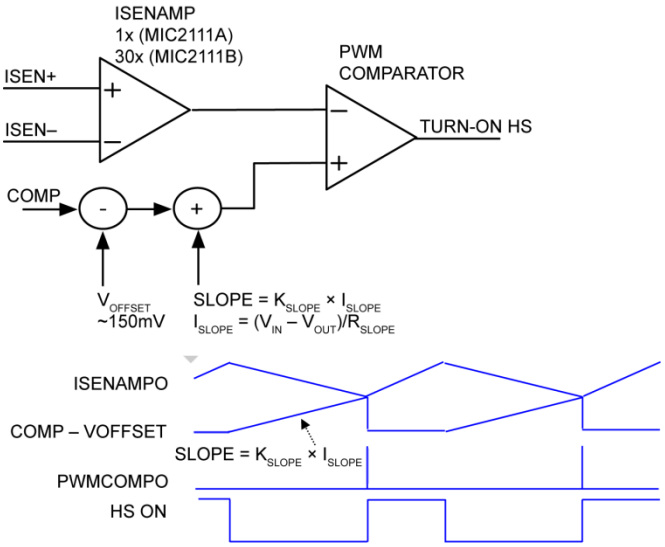


Figure 13. Valley Current Mode Compensation

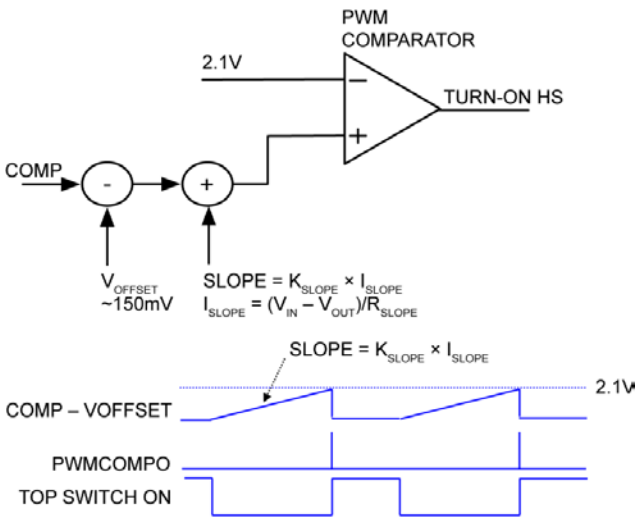


Figure 14. Voltage Mode Ramp Generation

Loop Compensation

Current Mode (Type II Method)

The MIC2111B uses an internal transconductance error amplifier wherein the output compensates the control loop. The external inductor, output capacitor, slope compensation resistor and compensation network all determine the loop stability. The inductor and output capacitors are chosen based on performance, size, and cost. The MIC2111B is configured in a valley current-mode control scheme when the SEL pin is connected to AGND. In this mode, the MIC2111B regulates the output voltage by forcing the required current through the external inductor. Current-mode control eliminates the double pole in the feedback loop which is caused by the inductor and output capacitor. This will result in a smaller phase shift and requires less elaborate error-amplifier compensation than voltage-mode control. A simple series R_C and C_C is all that is needed to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a non-ceramic output-capacitor loop, one would need to add another compensation capacitor from COMP to GND as it cancels this ESR to zero. The basic regulator loop is modeled as a power modulator, an output feedback divider and an error amplifier.

The power modulator has DC gain ($A_{MOD(DC)}$), is set by R_L, (output load, equivalent resistance) with a pole and zero pair set by R_L, the output capacitor (C_{OUT}) and its equivalent series resistance (R_{ESR}). Equation 9 defines the power modulator (Figure 16)

$$A_{MOD(DC)} = \frac{1}{A_{CS}} \frac{R_L}{1 + \frac{R_L}{R_{SLOPE}}} \quad \text{Eq. 9}$$

$A_{CS} = A_{ISENAMP} \times R_{SENSE}$

As current-mode control separates the complex LC double pole, a pole is formed by load resistance and output capacitance.

$$f_{PO} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

$$f_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad \text{Eq. 10}$$

The feedback voltage-divider has a gain of $A_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is equal to 0.6V.The transconductance error amplifier has a DC gain, $A_{EA(DC)} = g_{mEA} \times R_O$, where g_{mEA} is the error-amplifier transconductance, which is equal to 2ms, and R_O is the output resistance of the error amplifier, which is 50MΩ. A dominant pole (f_{pdEA}) is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and the compensation resistor (R_C); a zero (f_{zEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_{Cf} and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C):

$$f_{pdEA} = \frac{1}{2\pi \times (R_O + R_C) \times C_C}$$

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C} \quad \text{Eq. 11}$$

$$f_{pEA} = \frac{1}{2\pi \times R_C \times C_{Cf}}$$

$$f_{pdEA} = \frac{1}{2\pi \times (R_O + R_C) \times C_C}$$

The crossover frequency, f_O, should be much higher than the power-modulator pole f_{PO}. Also, f_C should be less than or equal to 1/5 the switching frequency:

$$f_{PO} << f_O \leq \frac{f_{SW}}{5} \quad \text{Eq. 12}$$

Choosing a lower cross-over frequency reduces the effects of noise pickup into the feedback loop, such as jittery duty cycle.

At the crossover frequency, the total loop gain must equal 1, and is expressed as:

$$A_{MOD(fo)} \times A_{EA(fo)} \times A_{FB} = 1 \quad \text{Eq. 13}$$

Mid-band gain is decided by the g_m and R_C:

$$A_{EA(fo)} = g_m \times R_C \quad \text{Eq. 14}$$

Where g_m = 2ms.

$$A_{MOD(fo)} = A_{MOD(DC)} \times \frac{f_{PO}}{f_O} \quad \text{Eq. 15}$$

Then R_C and C_C can be calculated as:

$$R_C = \frac{A_{FB}}{g_m \times A_{MOD(f_O)}} \quad \text{Eq. 16}$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{PO}} \quad \text{Eq. 17}$$

For high-current applications, it is recommended to place C_{Cf} to cancel the effect of ESR zero:

$$C_{Cf} = \frac{1}{2\pi \times R_C \times f_{PO}} \quad \text{Eq. 18}$$

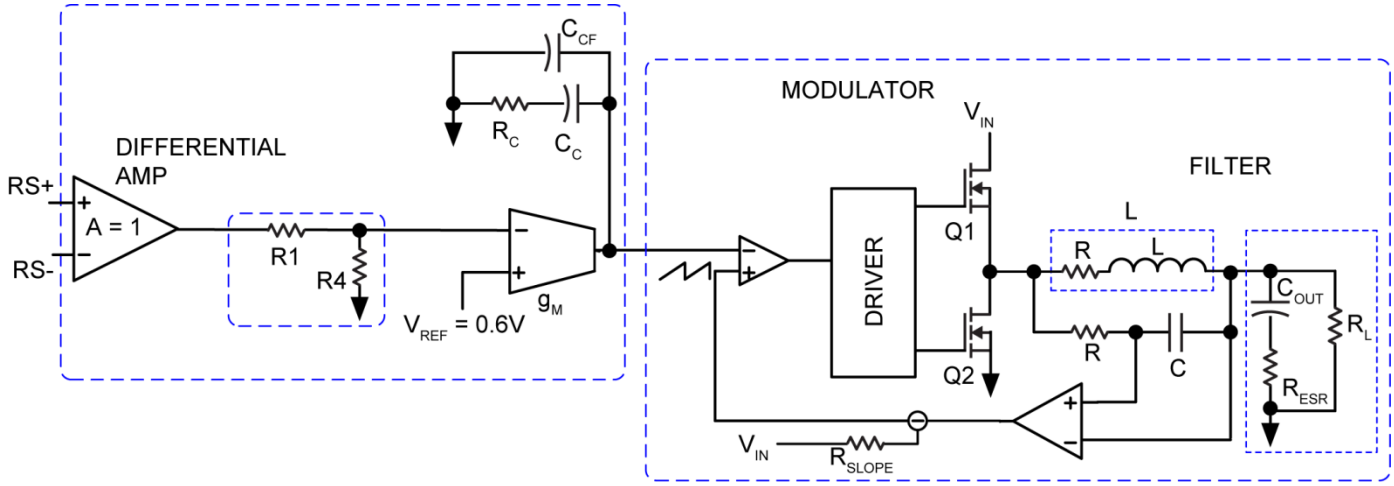


Figure 15. Valley Current Mode Loop Compensation

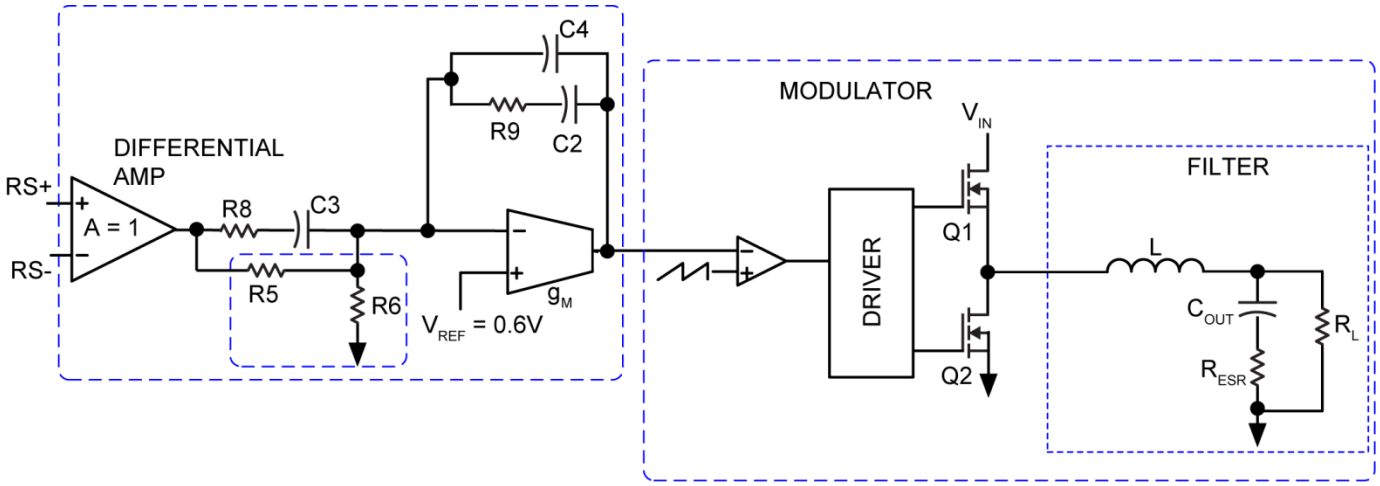


Figure 16. Voltage Mode Loop Compensation

Equation 22 assumes crossover frequency to be much less than half of the switching frequency. There is a sampling effect at the half switching frequency which introduces the double pole. For high crossover applications, it is recommended to run a bode plot to optimize the transient response.

Voltage Mode (Type III Method)

The MIC2111B provides an internal transconductance amplifier with the inverting input (FB) and the output (COMP) available for external frequency compensation. The flexibility of external compensation allows for a wide selection of output filtering components, especially the output capacitor. The use of high-ESR aluminum electrolytic capacitors is recommended for cost sensitive applications. Use low-ESR POSCAPs or ceramic capacitors at the output for size sensitive applications. The high switching frequency of the MIC2111B allows the use of ceramic capacitors at the output. Choose all passive power components to meet the output ripple, component size, and component cost requirements. Choose the compensation components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin.

To choose the appropriate compensation network type, the power supply poles and zeroes, the zero crossover frequency, and the type of the output capacitor must be determined first.

In a buck converter, the LC filter in the output stage introduces a pair of complex poles at the following frequency:

$$f_{PO} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} \quad \text{Eq. 19}$$

The output capacitor introduces a zero at:

$$f_{ZO} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad \text{Eq. 20}$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

The loop-gain crossover frequency (f_O), where the loop gain equals 1 (0dB) should be set below 1/10th of the switching frequency as in:

$$f_O \leq \frac{f_{SW}}{10} \quad \text{Eq. 21}$$

Choosing a lower cross-over frequency reduces the effects of noise pick-up into the feedback loop, such as jitter duty cycle.

In order to maintain a stable system, two stability criteria must be met:

1. The phase shift at the cross-over frequency (f_O,) must be less than 180°. In other words, the phase margin of the loop must be greater than zero.
2. The gain at the frequency where the phase shift is −180° (gain margin) must be less than 1.

Maintain a phase margin of around 60° to achieve a robust loop stability and well-behaved transient response.

When using an electrolytic or large-ESR POSCAP output capacitor the capacitor ESR zero (f_{ZO}) typically occurs between the LC poles and the crossover frequency f_O ($f_{PO} < f_{ZO} < f_O$). Choose Type II Proportional and Integral (PI) compensation network as previously specified.

When using a ceramic or low-ESR tantalum output capacitor the capacitor ESR zero typically occurs above the desired crossover frequency f_O ($f_{PO} < f_{ZO} < f_O$). Choose Type III proportional, integral, and derivative (PID) compensation network.

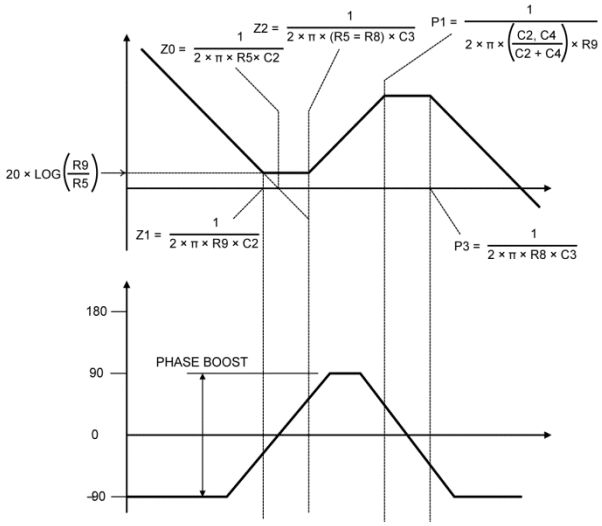


Figure 17. Type III Compensation Pole and Zero Locations

Ensure that $R_2 > /g_m$ and the parallel resistance of R_1, R_3, and R_4 is greater than $1/g_M$. Otherwise, a 180° phase shift is introduced to the response making the loop unstable. Use the following compensation procedures:

1. With $R_9 \geq 10k\Omega$, place the first zero (f_{Z1}) at $0.8 \times f_{PO}$:

$$f_{Z1} = \frac{1}{2\pi \times R9 \times C2} = 0.8 \times f_{PO} \quad \text{Eq. 22}$$

So,

$$C_2 = \frac{1}{2\pi \times R9 \times 0.8 \times f_{PO}} \quad \text{Eq. 23}$$

2. The gain of the modulator (A_{MOD}), comprises the pulse width modulator, LC filter, feedback divider, and associated circuitry at cross-over frequency is:

$$A_{MOD} = \frac{V_{IN}}{V_{RAMP}} \times \frac{1}{(2\pi \times f_O)^2 \times L_{OUT} \times C_{OUT}} \quad \text{Eq. 24}$$

The gain of the error amplifier (A_{EA}) in mid-band frequencies is:

$$A_{EA} = 2\pi \times f_O \times C3 \times R_9 \quad \text{Eq. 25}$$

The total loop gain as the product of the modulator gain and the error amplifier gain at f_O is 1:

$$A_{MOD} \times A_{EA} = 1 \quad \text{Eq. 26}$$

So,

$$\frac{V_{IN}}{V_{RAMP}} \times \frac{1}{(2\pi \times f_O)^2 \times C_{OUT} \times L} \times 2\pi f_O \times C_3 \times R9 = 1 \quad \text{Eq. 27}$$

Solving for C3:

$$C_3 = \frac{V_{RAMP} \times (2\pi \times f_O \times L \times C_{OUT})}{V_{IN} \times R_9} \quad \text{Eq. 28}$$

3. Use the second pole (f_{P2}) to cancel f_{ZO} when $f_{PO} < f_O < f_{ZO} < f_{SW}/2$. The frequency response of the loop gain does not flatten out soon after the 0dB crossover, and maintains –20dB/decade slope up to 1/2 of the switching frequency. This is likely to occur if the output capacitor is a low-ESR tantalum. Set $f_{P2} = f_{ZO}$.

When using a ceramic capacitor the capacitor ESR zero f_{ZO} is likely to be located even above one half of the switching frequency, $f_{PO} < f_O < f_{SW}/2 < f_{ZO}$. In this case, place the frequency of the second pole (f_{P2}) high enough in order not to erode significantly the phase margin at the crossover frequency. For example, set f_{P2} at $5 \times f_O$ so that the contribution to phase loss at the crossover frequency f_O is only about 11°:

$$f_{P2} = 5 \times f_O \quad \text{Eq. 29}$$

Once f_{P2} is known, calculate R_1:

$$R_8 = \frac{1}{2\pi \times f_{P2} \times C_3} \quad \text{Eq. 30}$$

4. Place the second zero (f_{Z2}) at $0.2 \times f_O$ or at f_{PO}, whichever is lower and calculate R_1 using the following equation:

$$R_5 = \frac{1}{2\pi \times f_{Z2} \times C_3} - R_8 \quad \text{Eq. 31}$$

5. Place the third pole (f_{P3}) at 1/2 the switching frequency and calculate C_{CF}:

$$C4 = \frac{C_2}{(2\pi \times 0.5 \times f_{SW} \times R_9 \times C_2) - 1} \quad \text{Eq. 32}$$

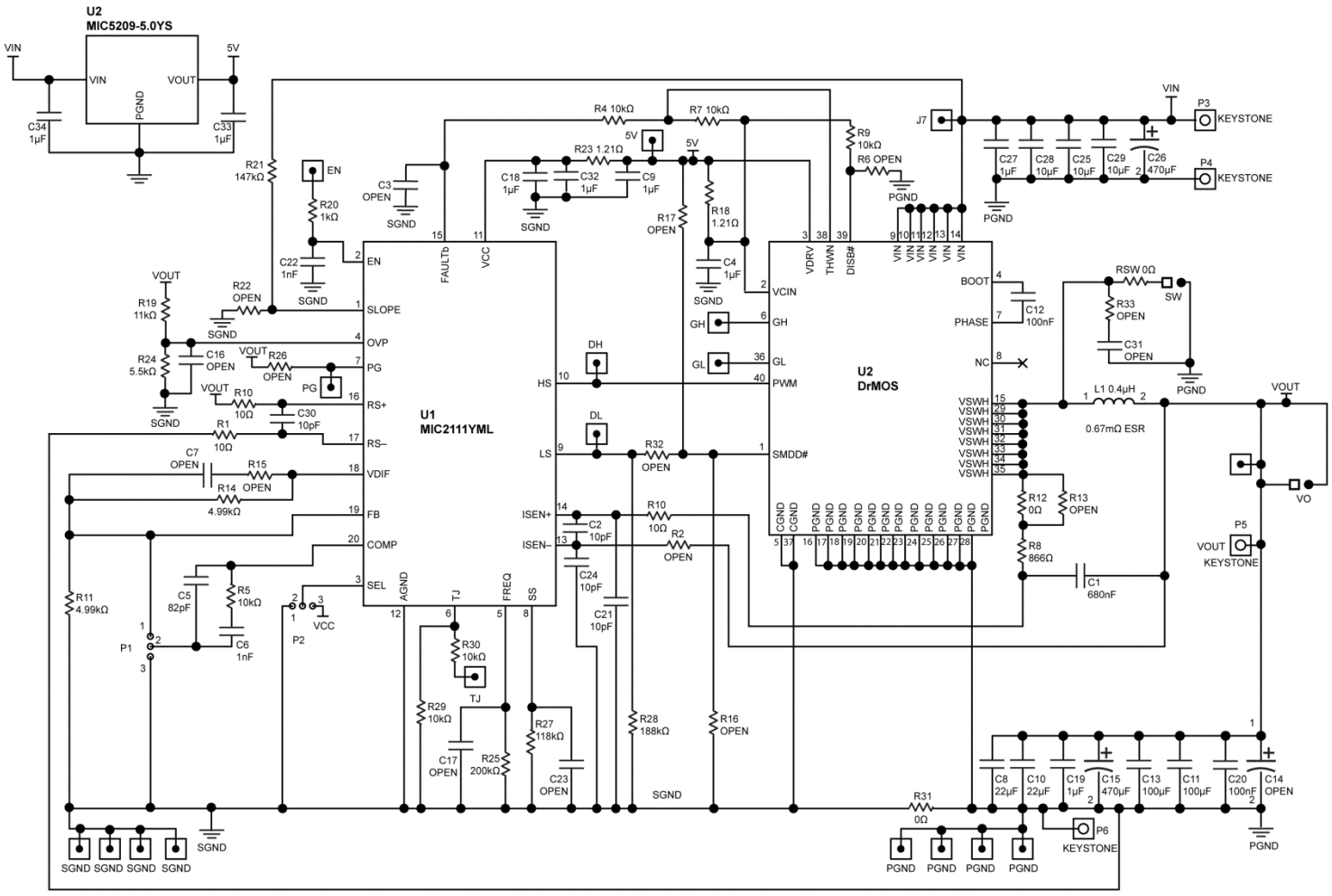
6. Calculate R_2 as:

$$R_6 = \frac{V_{FB}}{V_{OUT} - V_{FB}} - R5 \quad \text{Eq. 33}$$

Design and Layout Checklist

- Ceramic capacitor placed between the VIN and PGND close to power module input.
- Output ceramic capacitors should be placed next to inductor output node for high-frequency decoupling.
- The signal and power ground planes must be separated to prevent high current and fast switching signals from interfering with the low level, noise sensitive analog signals. These planes should be connected at only 1 point.
- The following signals and their components should be decoupled or referenced to the power ground plane:
  - VIN, VCC, PGND
- These analog signals should be referenced or decoupled to the analog ground plane:
  - VCC, SS, PG, COMP, FB, VOUT, and AGND
- Place the current-sense lines in differential way. The trace coming from the switch node to this resistor has high dv/dt and should be routed away from other noise sensitive components and traces.
- The remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, and other high dv/dt or di/dt sources.

Typical Application Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1608X7R1C684K080AC	TDK[6]	0.68µF Ceramic Capacitor, X7R, 0603 Size, 16V	1
C2, C21, C24, C30	C1608C0G1H100D	TDK	10pF Ceramic Capacitor, COG, 0603 Size, 50V	4
C3, C7, C16, C17, C23, C31, R2, R6, R13, R15, R16, R17, R22, R26	OPEN			
C4, C9, C18, C19, C27, C32, C33, C34	C1608X5R1E105K	TDK	1µF Ceramic Capacitor, X5R, 0603 Size, 25V	8
C5	C1608C0G1H820J	TDK	82pF Ceramic Capacitor, COG, 0603 Size, 50V	1
C6, C22	C1608C0G1H102J	TDK	1nF Ceramic Capacitor, COG, 0603 Size, 50V	2

Note:

6. TDK: www.tdk.com.

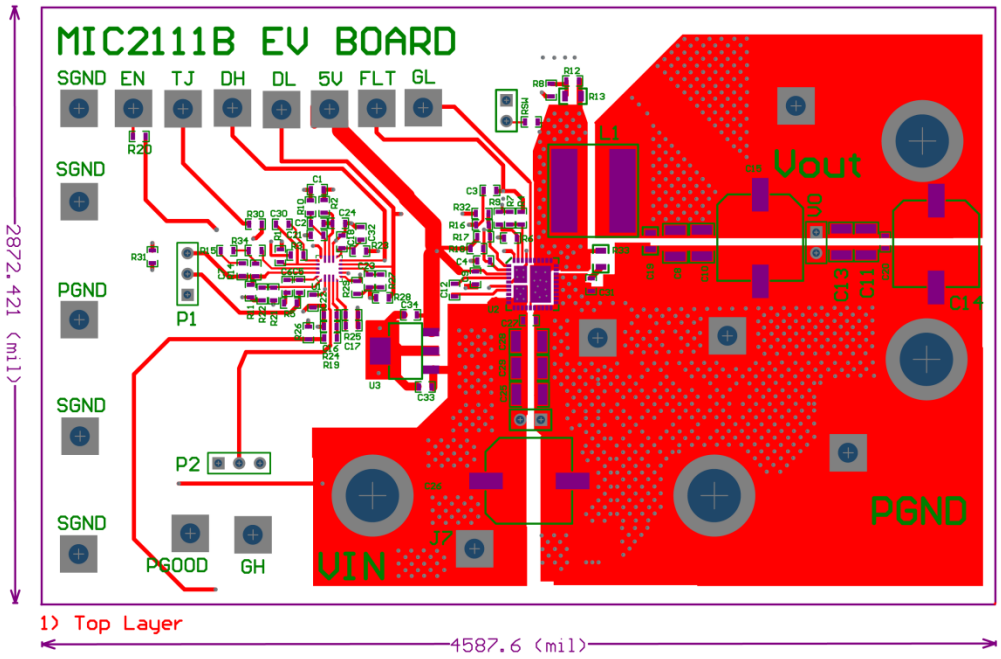
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
C8, C10	C3225X5R0J226M/1.60	TDK	22µF Ceramic Capacitor, X5R,1210 Size,6.3V	2
C11, C13	C3225X5R0J107M	TDK	100µF Ceramic Capacitor, X5R,1210 Size,6.3V	2
C12, C20	C1608X7R1E104K	TDK	100nF Ceramic Capacitor, X7R,0603 Size,25V	2
C15	6SVP470MX	Panasonic[7]	470µF OS-CON Capacitor, 6.3V	1
C25, C28, C29	C3225X5R1E106M	TDK	10µF Ceramic Capacitor, X5R,1210 Size, 25V	2
C26	EEEFP1E471AP	Panasonic	470µF Aluminum Capacitor, 25V	1
L1	744325040	Wurth Electric[8]	0.4µH Inductor, 37A Saturation Current	1
R1, R2, R3, R10	CRCW060310R0FKEA	Vishay Dale[9]	10Ω Resistor, 0603 Size, 1%	4
R4, R5, R7, R9, R29, R30	CRCW060310K0FKEA	Vishay Dale	10kΩ Resistor, 0603 Size, 1%	4
R8	CRCW0603866RFKEA	Vishay Dale	866Ω Resistor, 0603 Size, 1%	1
R11, R14	CRCW06034K99FKEA	Vishay Dale	4.99kΩ Resistor, 0603 Size, 1%	2
R12, R31, RSW	CRCW06030000Z0EA	Vishay Dale	0Ω Resistor, 0603 Size, 1%	3
R18, R23	CRCW06031R21FKEA	Vishay Dale	1.21Ω Resistor, 0603 Size, 1%	2
R19	CRCW060311K0FKEA	Vishay Dale	11kΩ Resistor, 0603 Size, 1%	1
R20	CRCW06031K00FKEA	Vishay Dale	1kΩ Resistor, 0603 Size, 1%	1
R21	CRCW0603147KFKEA	Vishay Dale	147kΩ Resistor, 0603 Size, 1%	1
R24	CRCW06035K49FKEA	Vishay Dale	5.5kΩ Resistor, 0603 Size, 1%	1
R25	CRCW0603200KFKEA	Vishay Dale	200kΩ Resistor, 0603 Size, 1%	1
R27	CRCW0603118KFKEA	Vishay Dale	118kΩ Resistor, 0603 Size, 1%	1
R28	CRCW0603188KFKEA	Vishay Dale	188kΩ Resistor, 0603 Size, 1%	1
U1	**MIC2111B**	**Micrel, Inc.[10]**	**High-Performance, Multi-Mode, Step-Down Controller**	**1**
U2	SiC769ACD	Vishay Dale	35A, DrMOS Module	1
U3	**MIC5209-5.0YS**	**Micrel Inc.**	**500mA, Low-Noise LDO Regulator**	**1**

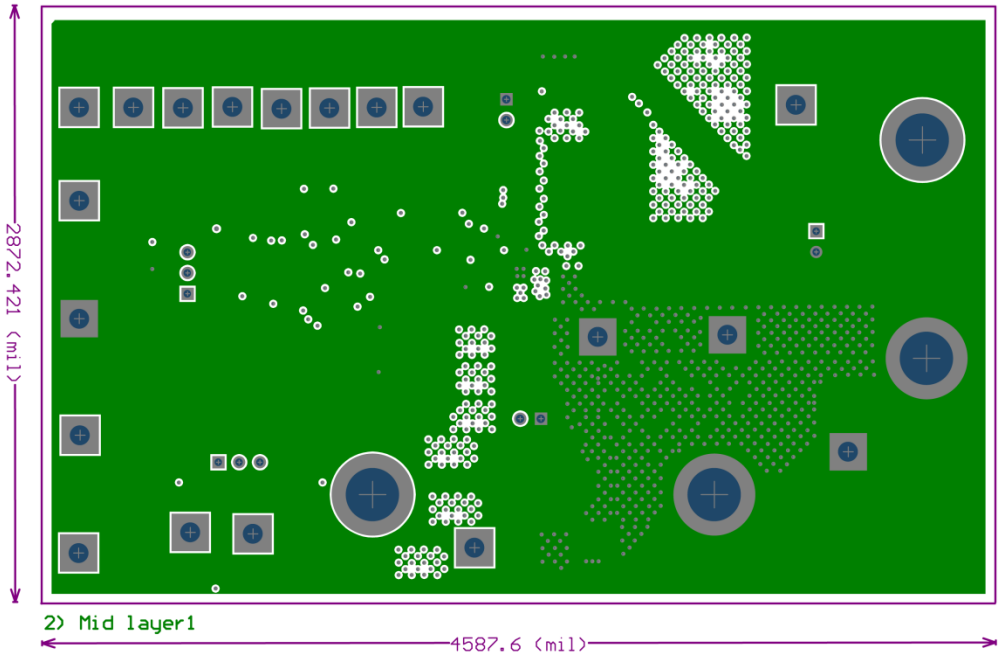
Notes:

7. Panasonic: www.industrial.panasonic.com.
8. Wurth Electric: www.we-online.com.
9. Vishay Dale: www.vishay.com.
10. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

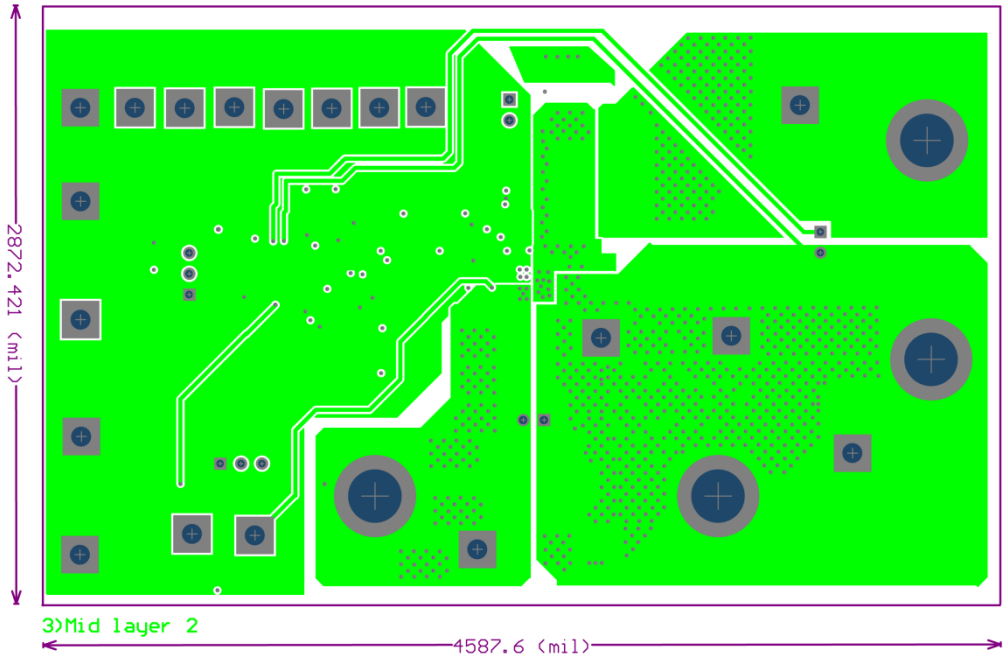


Top Layer

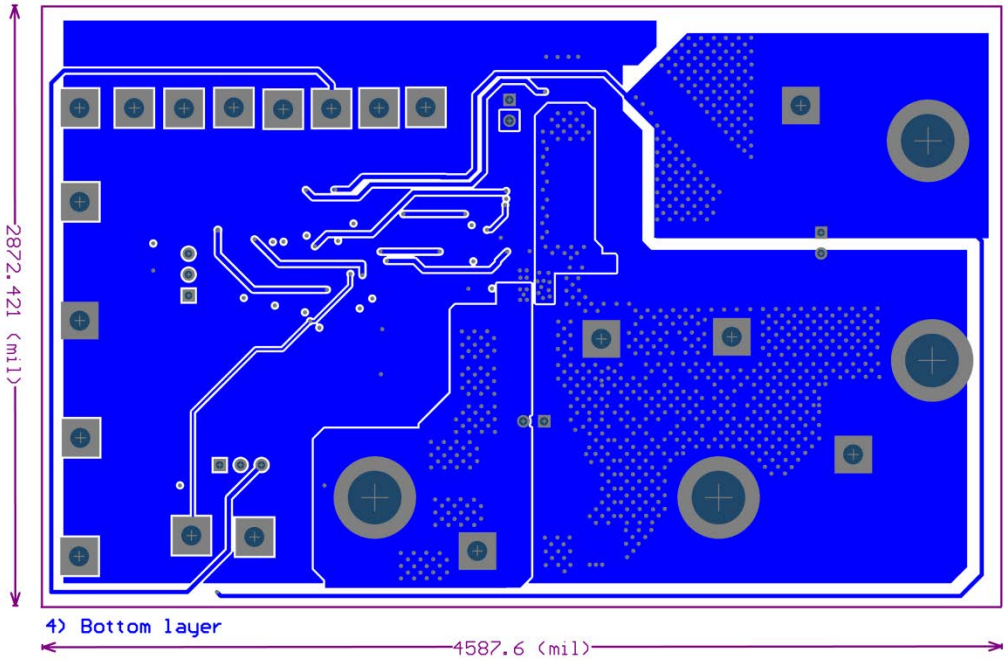


Mid Layer 1

PCB Layout Recommendations (Continued)

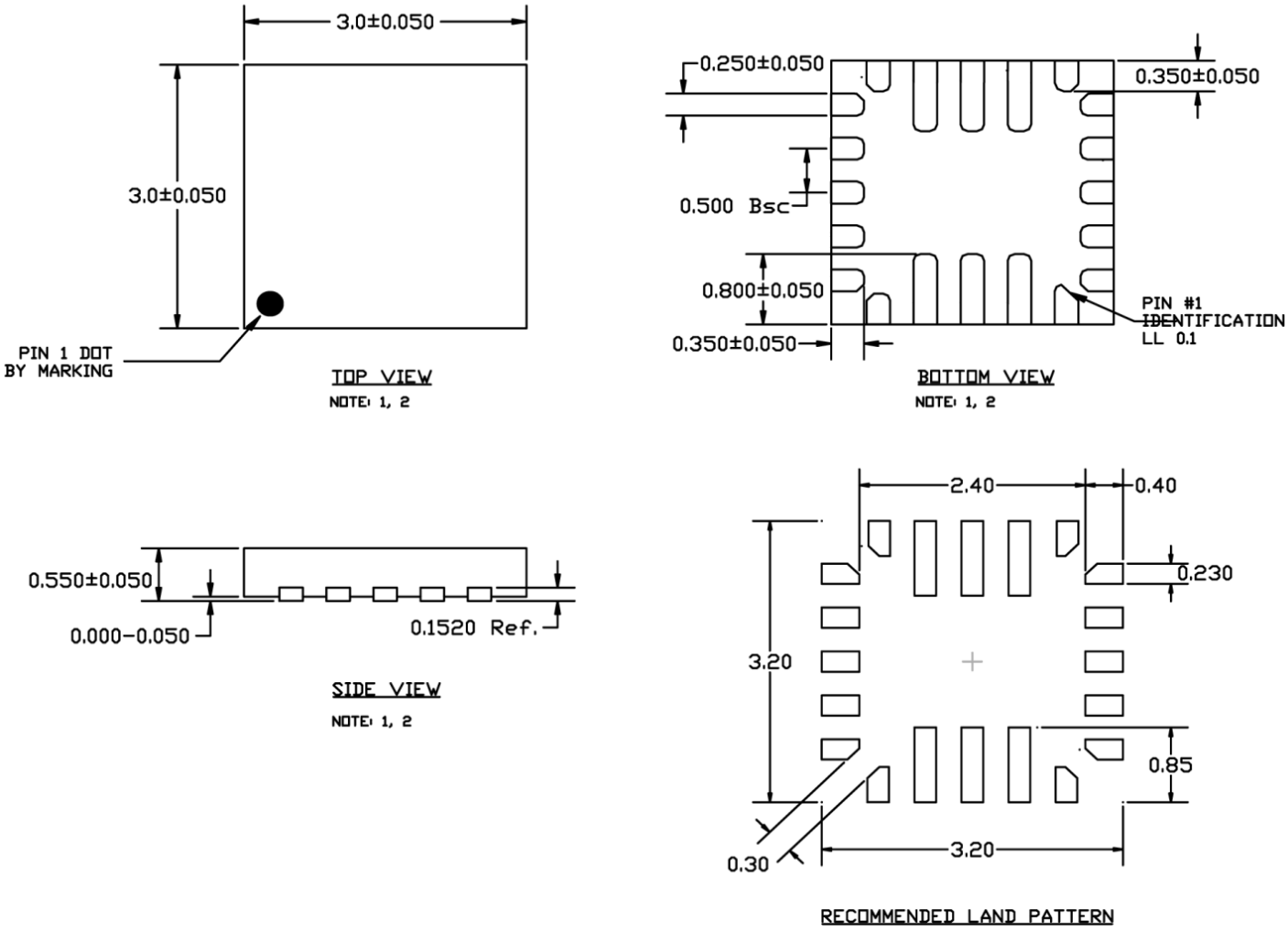


Mid Layer 2



Bottom Layer 1

Package Information and Recommended Land Pattern[11]



20-Pin 3mm × 3mm TQFN (MT)

Note:

11. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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