

Brief Description

The ZSPM4121 battery management load switch can be used to protect a battery from excessive discharge. It actively monitors the battery voltage and disconnects the battery from the load if the battery drops below a set voltage threshold. When the input battery voltage reaches 500mV above the set voltage threshold, the load switch turns on and connects the battery to the load. The 500mV hysteresis between the Off Mode and the On Mode prevents intermittent operation.

The voltage threshold (V_{THRESH}) can be programmed at manufacturing to a customer-selected set point in the voltage range of 1.2V to 4.2V in 100mV increments to support a wide range of applications in consumer, medical, portable, and industrial applications.

This device has ultra-low quiescent current, which makes it ideal for battery-powered applications. Typical quiescent current is 100pA in the Off Mode and 70nA in the On Mode.

The ZSPM4121 includes a slew rate control P-channel load switch, over-current protection, and an open-drain power indicator pin (NPG). The slew-rate controlled turn-on characteristic prevents inrush current and voltage droop on the voltage. The over-current limit protects the device in case of an overload, short-circuit, or ground fault event.

Benefits

- Best-in-class ultra-low quiescent current in Off Mode: 100pA (typical)
- Ultra-low quiescent current in On Mode: 70nA (typical)
- Accurate on/off voltage threshold
- Low $R_{ds(on)}$: 175m Ω (typical) @ 5V

Features

- Threshold voltage options of 1.2V to 4.2V in 100mV steps (factory programmed)
- Wide input voltage range: 1.2V to 5.5V
- Supervisory over-current limit shutdown: (3A)
- Low drop-out disconnect from VCC to loads
- Controlled turn-on slew rate
- 500mV Off Mode to On Mode hysteresis

Related IDT Smart Power Products

- ZSPM4141 Ultra-Low-Power Linear Regulator

Available Support

- Evaluation Kit
- Support Documentation

Physical Characteristics

- Package: 8-pin DFN (2mm x 2mm)

ZSPM4121 Block Diagram



Typical Application Circuit



Ordering Information

| Ordering Code* | Description | Package |
|-----------------|--|----------------------------|
| ZSPM4121AI1 W17 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 1.7V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W21 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 2.1V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W23 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 2.3V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W24 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 2.4V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W25 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 2.5V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W26 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 2.6V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W28 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 2.8V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121AI1 W30 | ZSPM4121 Under-Voltage Load Switch— V_{THRESH} factory set to 3.0V | 8-pin DFN / 7" Reel (2500) |
| ZSPM4121KIT | ZSPM4121 Evaluation Kit | |

* For a 13" reel (3300 parts), replace the W in the ordering code with an R. Custom V_{THRESH} values are also available: 1.2V to 4.2V (typical) in 100mV increments.



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1 ZSPM4121 Characteristics

Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those recommended under “Recommended Operating Conditions” (section 1.3) is not implied. Exposure to absolute–maximum conditions for extended periods may affect device reliability.

1.1. Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted. All voltage values are with respect to network ground terminal.

Table 1.1 Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------|-------------|------|
| Maximum voltage applied to the VCC, VOUT, and NPG pins | | -0.3 to 6.0 | V |
| Electrostatic Discharge – Human Body Model, according to the respective JESD22 JEDEC standard | | 2 | kV |
| Electrostatic Discharge – Charged Device Model, according to the respective JESD22-C101 JEDEC standard | | 500 | V |
| Operating Junction Temperature Range | T_J | -20 to 85 | °C |
| Storage Temperature Range | T_{stg} | -65 to 150 | °C |
| Lead Temperature (soldering, 10 seconds) | | 260 | °C |

1.2. Thermal Characteristics

Table 1.2 Thermal Characteristics for 8-Pin DFN (2mm x 2mm) Package

| θ_{JA} (°C/W) ¹⁾ | θ_{JC} (°C/W) ²⁾ |
|--|------------------------------------|
| 73.1 | 10.7 |
| 1) This rating assumes a FR4 board only. 2) This rating assumes a 1oz. copper JEDEC standard board with thermal vias. See section 6.1 for more information. | |

1.3. Recommended Operating Conditions

Table 1.3 Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------|-----|-----|-----|------|
| Unregulated Supply Input at VCC Pin | V_{CC} | 1.2 | | 5.5 | V |
| Operating Ambient Temperature ¹⁾ | T_A | -20 | | 55 | °C |
| Operating Junction Temperature | T_J | -20 | | 85 | °C |
| 1) Operating ambient temperature is only intended as a guideline. The operating junction temperature requirements must not be exceeded. | | | | | |

1.4. Electrical Characteristics

Electrical characteristics for $V_{CC} = 1.2V$ to $5.5V$ (unless otherwise noted). Minimum and maximum characteristics are tested at $T_J = 25^\circ C$.

Table 1.4 Electrical Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|----------------|--|---------------------|--------------|---------------------|-----------|
| Input Supply | | | | | | |
| Input Supply Voltage at VCC pin | V_{CC} | | 1.2 | | 5.5 | V |
| Quiescent Current: On Mode | I_{q-ON} | $V_{CC} = 5.0V$, no load | | 70 | 150 | nA |
| Quiescent Current: Off Mode | I_{q-OFF} | $V_{CC} < V_{THRESH}$, no load | | 100 | | pA |
| Load Switch | | | | | | |
| Over-Current Shutdown | I_{OC} | $V_{CC} = 5.0V$ | | 3 | | A |
| Over-Current Retry Period | t_{OC} | $V_{CC} = 5.0V$ | | 1.7 | | ms |
| Output Switch Leakage Current | $I_{LEAK-SW}$ | $V_{CC} < V_{THRESH}$; V_{OUT} grounded | | 100 | | pA |
| Switch ON-Resistance | Rds-on | $V_{CC} = 5.0V$ | | 175 | | $m\Omega$ |
| | | $V_{CC} = 3.3V$ | | 200 | | $m\Omega$ |
| | | $V_{CC} = 1.8V$ | | 350 | | $m\Omega$ |
| Transition Times | | | | | | |
| Transition Delay: On Mode to Off Mode | t_{d1} | $V_{OFF} = 2.0V$, $V_{CC} = 3.0V \rightarrow 1.5V$ | | 650 | | μs |
| Transition Delay: Off Mode to On Mode | t_{d2} | $V_{OFF} = 2.0V$, $V_{CC} = 1.5V \rightarrow 3.0V$ | | 1.7 | | ms |
| Output Turn-on Rise Time | t_{ON} | $V_{CC} = 2.5V$, $R_{LOAD} = 50\Omega$ | | 200 | | μs |
| NPG Output | | | | | | |
| Output Leakage | $I_{LEAK-NPG}$ | $V_{CC} = 5.0V$, $V_{NPG} = 5.5V$ | | | 100 | nA |
| Low-Level Output Voltage | V_{OL-NPG} | $I_{NPG} = 5\text{ mA}$ | | | 0.4 | V |
| Off Thresholds | | | | | | |
| Off Threshold | V_{OFF} | V_{THRESH} = customer-selected threshold voltage in the range of 1.2V to 4.2V with 100mV steps between options programmed at manufacturing | $0.95 * V_{THRESH}$ | V_{THRESH} | $1.05 * V_{THRESH}$ | V |
| Off Mode to On Mode Hysteresis | V_{Hys} | Rising Transition: Off Mode to On Mode | | 500 | | mV |

2 Typical Performance Characteristics

T = 25°C (unless otherwise noted)

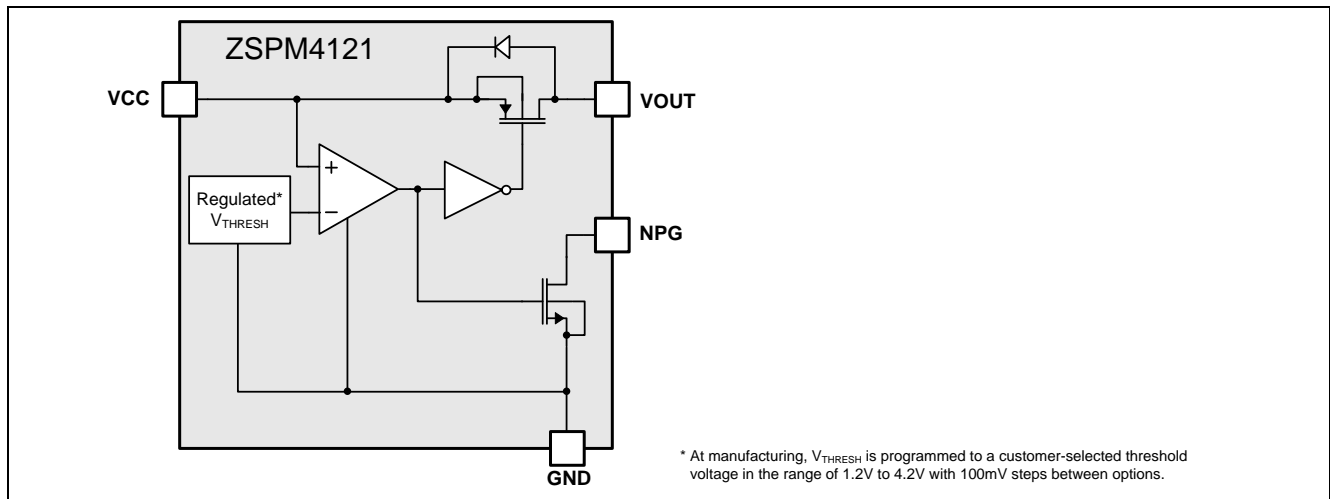




3 Description of Circuit

The ZSPM4121 battery management load switch includes an internally generated threshold voltage, comparator with hysteresis, slew rate control for the load switch, a P-channel load switch, and an open-drain indicator pin. When the input battery voltage rises to 500mV above the threshold, the load switch turns on (the On Mode). When the input battery voltage falls to the threshold voltage or below, the load switch is off (the Off Mode), and the quiescent current draw on the battery is in the order of 100pA (typical). The ZSPM4121 threshold voltage is programmed at manufacturing to an option in the range of 1.2V to 4.2V with 100mV steps between options. The 500mV hysteresis between the Off Mode and the On Mode prevents intermittent operation. The ZSPM4121 also provides over-current protection.

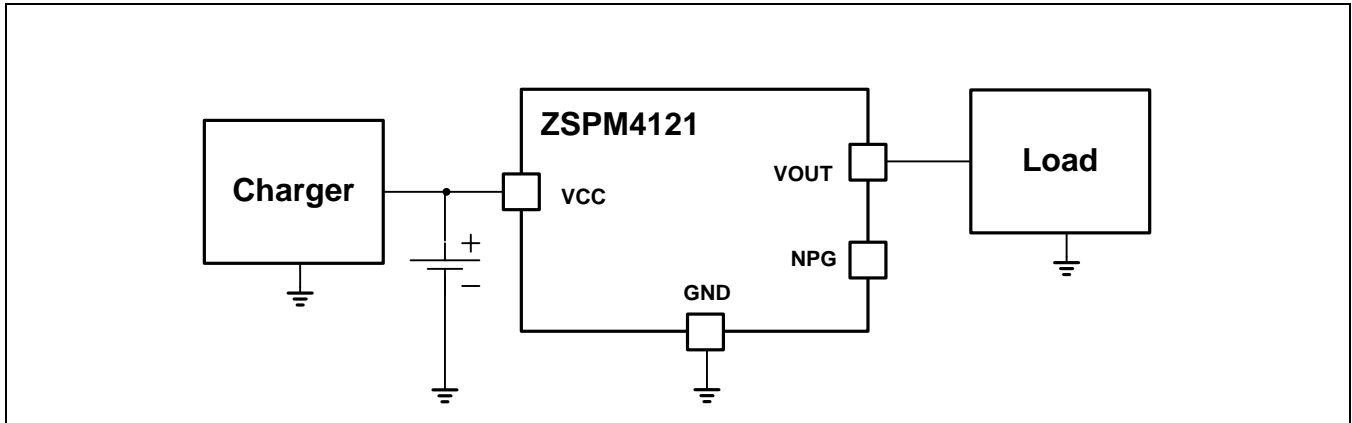
Figure 3.1 ZSPM4121 Block Diagram



4 Application Circuit

4.1. Typical Application Circuit

Figure 4.1 Application Circuit for Disconnecting the Load



5 Pin Configuration and Package

5.1. Package Dimensions and Marking Diagram

Figure 5.1 ZSPM4121 Package Drawing



5.2. Pin Description for 8-Pin DFN (2x2 mm)

Figure 5.2 ZSPM4121 Pin Assignments (top view)



Table 5.1 Pin Description, 8-Pin DFN (2x2)

| Pin # | Name | Function | Description |
|-------|------|----------|--|
| 1 | GND | Ground | GND |
| 2 | VOUT | Output | Output to system load |
| 3 | NC | | No connection (connect to GND or float) |
| 4 | NC | | No connection (connect to GND or float) |
| 5 | NC | | No connection (connect to GND or float) |
| 6 | VCC | Supply | Supply input (connect to pin 7 and VCC supply rail) |
| 7 | VCC | Supply | Supply input (connect to pin 6 and VCC supply rail) |
| 8 | NPG | Output | Open-drain N-channel output (low indicates "Power Good") |

6 Layout and Soldering Requirements

To maximize the efficiency of this package for applications on a single layer or multi-layer printed circuit board (PCB), certain guidelines must be followed when laying out this part on the PCB.

6.1. Recommended Landing Pattern for PCBs

Figure 6.1 Recommended Landing Pattern for 8-Pin DFN



6.2. Multi-Layer PCB Layout

The following are guidelines for mounting the exposed pad ZSPM4121 on a multi-Layer PCB with ground a plane. In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, and thickness of copper, etc.

Figure 6.2 Package and PCB Land Configuration for Multi-Layer PCB



Figure 6.3 JEDEC Standard FR4 Multi-Layer Board – Cross-Sectional View



Figure 6.4 is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations, and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating of the linear regulators might need to be de-rated for higher ambient temperatures. The de-rated value will depend on the calculated worst-case power dissipation and the thermal management implementation in the application.

Figure 6.4 Conducting Heat Away from the Die using an Exposed Pad Package



6.3. Single-Layer PCB Layout

Layout recommendations for a single-layer PCB: Utilize as much copper area for power management as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low thermal impedance attachment method (solder paste or thermal conductive epoxy). In both of the methods mentioned above, it is advisable to use as much copper trace as possible to dissipate the heat.

Important: If the attachment method is NOT implemented correctly, the functionality of the product is NOT guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

Figure 6.5 Application Using a Single-Layer PCB



7 Ordering Information

| Ordering Code* | Description | Package |
|----------------|--|----------------------------|
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| ZSPM4121KIT | ZSPM4121 Evaluation Kit | |

* For a 13" reel (3300 parts), replace the W in the ordering code with an R. Custom V_{THRESH} values are also available: 1.2V to 4.2V (typical) in 100mV increments.

8 Related Documents

| Document |
|---|
| <i>ZSPM4121 Feature Sheet</i> |
| <i>ZSPM4121 Evaluation Kit Description</i> |
| <i>ZSPM4121 Application Note—Low Power Battery Control and Voltage Regulator Solutions for Remote Sensor Networks</i> |

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

9 Glossary

| Term | Description |
|------|---|
| PG | Power Good (NPG = Power Good, active low) |
| RFID | Radio Frequency Identification |
| SPM | Smart Power Management |

10 Document Revision History

| Revision | Date | Description |
|----------|------------------|---|
| 1.00 | April 30, 2012 | First release |
| 1.01 | February 7, 2013 | Addition of “Electrostatic Discharge – Charged Device Model” specification in section 1.1. Update for block diagram. Updates for V designation in marking codes in section 5. Edits for clarity. Update to IDT contact information. |
| | January 29, 2016 | Changed to IDT branding. |



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