PRELIMINARY

# CY2DP818-2

## 1:8 Clock Fanout Buffer

## Features

- Low voltage operation $V_{DD}$ = 3.3V
- 1:8 fanout
- Single-input configurable for LVDS, LVPECL, or LVTTL
- 8 pairs of LVPECL outputs with enable and disable
- Drives a 50 ohm load
- Low input capacitance
- Low output skew
- Low propagation delay typical (tpd < 4 ns)
- Industrial versions available
- Package available include: TSSOP
- Does not exceed Bellcore 802.3 standards
- Operation up to 350 MHz and 700 Mbps

## Description

This Cypress series of network circuits is produced using advanced 0.35 micron CMOS technology, achieving the industry's fastest logic.

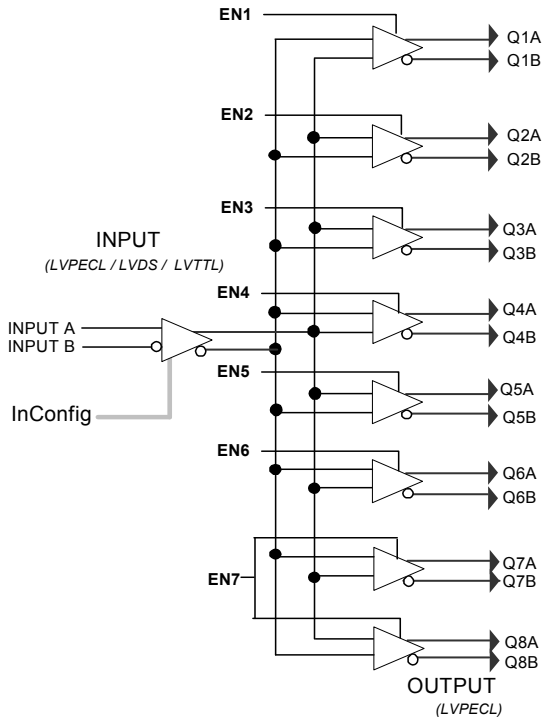
The Cypress CY2DP818-2 fanout buffer features a single LVDS or a single-ended LVTTL compatible input and eight LVPECL output pairs.

Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

The CY2DP818-2 is ideal for both level translations from single-ended to LVPECL and for the distribution of LVPECL based clock signals.

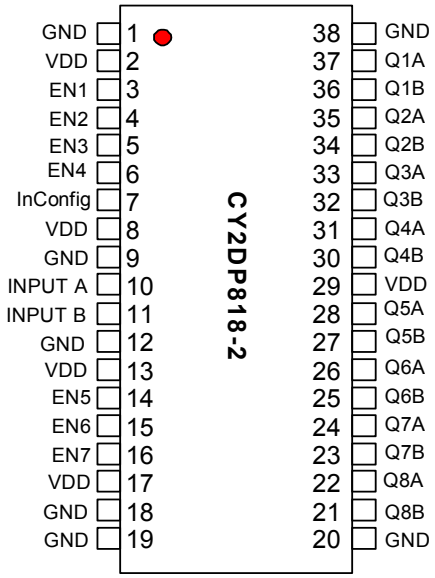
The Cypress CY2DP818-2 has configurable input functions. The input is user configurable through the Inconfig pin for single ended or differential input.

## Logic Block Diagram



## Pin Configuration

**Figure 1. Pin Diagram - 38-Pin TSSOP**




## Pin Description

| Pin Number | Pin Name | Pin Standard Interface | Description |
|---|---|---|---|
| 1, 9,12,18,19,20,38 | GND | POWER | **Ground.** |
| 2,8,13,29,17 | VDD | POWER | **Power supply.** |
| 3,4,5,6,14,15,16 | EN(1:7) | LVTTL/LVCMOS | **The respective outputs are enabled when these pins are pulled high**. Outputs are disabled when connected to GND. EN7 controls both Q7(A,B) and Q8(A,B) |
| 10,11 | Input A, Input B | Default: LVPECL/LDVS Optional: LVTTL/LVCMOS single pin | **Differential input pair or single line**. LVPECL/LVDS default. See InConfig, below. |
| 37, 36,35,34, 33,32,31, 30, 28,27,26,25, 24,23,22,21 | Q1(A,B), Q2(A,B) Q3(A,B), Q4(A,B) Q5(A,B), Q6(A,B) Q7(A,B), Q8(A,B) | LVPECL | **Differential outputs.** |
| 7 | InConfig | LVTTL/LVCMOS | **Converts inputs from the default LVPECL/LVDS (logic = 0) to LVTTL/LVCMOS (logic = 1)** See Input Receiver Configuration for Differential or LVTTL/LVCMOS table, Figure 6 and Figure 7 for additional information |



[+] Feedback

## Power Supply Characteristics

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ICCD | Dynamic Power Supply Current | $V_{DD}$ = Max.<br>Input toggling 50% Duty Cycle, Outputs Open | | 1.5 | 2.0 | mA/ MHz |
| IC | Total Power Supply Current | $V_{DD}$ = Max.<br>Input toggling 50% Duty Cycle, Outputs 50 ohms, fL=100 MHz | | | 350 | mA |
| IC Core | Core Current when Output Loads are Disabled | $V_{DD}$ = Max.<br>Input toggling 50% Duty Cycle, Outputs Disabled, not connected to VTT fL = 100 MHz | | | 50 | mA |

## Input Receiver Configuration for Differential or LVTTL/LVCMOS

| INCONFIG Pin 7 Binary Value | Input Receiver Family | Input Receiver Type |
|---|---|---|
| 1 | LVTTL in LVCMOS | Single ended, non inverting, inverting, void of bias resistors |
| 0 | LVDS | Low voltage differential signaling |
| | LVPECL | Low voltage pseudo (positive) emitter coupled logic |

## Function Control of the TTL Input Logic used to Accept or Invert the Input Signal

| LVTTL/LVCMOS Input Logic | | | |
|---|---|---|---|
| Input Condition | | Input Logic | Output Logic Q Pins, Q1A or Q1 |
| Ground | Input B (–) Pin 11 | | |
| | Input A (+) Pin 10 | Input | True |
| $V_{DD}$ | Input B (–) Pin 11 | | |
| | Input A (+) Pin 10 | Input | Invert |
| Ground | Input A (+) Pin 10 | | |
| | Input B (–) Pin 11 | Input | Invert |
| $V_{DD}$ | Input A (+) Pin 10 | | |
| | Input B (–) Pin 11 | Input | True |



[+] Feedback

## Absolute Maximum Conditions

| Parameter | Description | | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | | Inputs and $V_{CC}$ | –0.3 | 4.6 | V |
| $V_{DD}$ | DC Operating Voltage | | Outputs | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{IN}$ | DC Input Voltage | | Relative to $V_{SS}$, with or $V_{DD}$ applied | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | | Relative to $V_{SS}$ | –0.3 | $V_{DD}$ + 0.9 | V |
| $V_{TT}$ | Output Termination Voltage | | | – | $V_{DD} \div 2$ | V |
| $T_S$ | Temperature, Storage | | Non Functional | –65 | +150 | °C |
| $T_A$ | Temperature, Operating Ambient | Commercial | Functional | 0 | 70 | °C |
| | | Industrial | Functional | –40 | +85 | |
| **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required. | | | | | | |

## DC Electrical Specifications

3.3V – LVDS Input at $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C or –40°C to 85°C

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ID}$ | Magnitude of Differential Input Voltage | | | 100 | | 600 | mV |
| $V_{IC}$ | Common Mode of Differential Input Voltage\|$V_{ID}$\| (minimum and maximum) | | | \|VID\|/2 | 2.4–(\|VID\|/2) | | V |
| $I_{IH}$ | Input High Current | $V_{DD}$ = Max. | $V_{IN} = V_{DD}$ | – | ±10 | ± 20 | µA |
| $I_{IL}$ | Input Low Current | $V_{DD}$ = Max. | $V_{IN} = V_{SS}$ | – | ±10 | ± 20 | µA |

3.3V – LVPECL Input at $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C or –40°C to 85°C

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ID}$ | Differential Input Voltage p-p | Guaranteed Logic High Level | | 400 | – | 2600 | mV |
| $V_{IH}$ | Input High Voltage | Guaranteed Logic High Level | | 2.15 | – | 2.4 | V |
| $V_{IL}$ | Input Low Voltage | Guaranteed Logic Low Level | | 1.5 | – | 1.8 | V |
| $I_{IH}$ | Input High Current | $V_{DD}$ = Max. | $V_{IN} = V_{DD}$ | – | ±10 | ±20 | µA |
| $I_{IL}$ | Input Low Current | $V_{DD}$ = Max. | $V_{IN} = V_{SS}$ | – | ±10 | ±20 | µA |
| $V_{CM}$ | Common-mode Voltage | | | 1650 | – | 2250 | mV |

3.3V – LVTTL/LVCMOS Input at $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C or –40°C to 85°C

| Parameter | Description | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | Guaranteed Logic High Level | | 2 | – | – | V |
| $V_{IL}$ | Input Low Voltage | Guaranteed Logic Low Level | | – | – | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{DD}$ = Max | $V_{IN}$ = 2.7V | – | – | 1 | µA |
| $I_{IL}$ | Input Low Current | $V_{DD}$ = Max | $V_{IN}$ = 0.5V | – | – | –1 | µA |
| $I_I$ | Input High Current | $V_{DD}$ = Max, $V_{IN} = V_{DD}$ (Max) | | | | | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$ = Min, $I_{IN}$ = –18 mA | | – | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis[1] | | | – | 80 | | mV |

**Note**
1. Guaranteed but not tested.



[+] Feedback

3.3V – LVPECL Output at $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C or –40°C to 85°C

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Driver Differential Output Voltage p-p | $V_{DD}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | RL = 50 ohm | 1000 | – | 3600 | mV |
| $\Delta V_{OC}$ | Driver common-Mode Variation p-p | $V_{DD}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | RL = 50 ohm | – | – | 300 | mV |
| Rise Time | Differential 20% to 80% | CL–10 pF RL and CL to GND | RL = 50 ohm | 300 | | 1200 | ps |
| Fall Time | | | | | | | |
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –12 mA | 2.1 | – | 3.0 | V |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ User-defined by VTT RTT. | | 0.8 | – | 1.3 | V |
| $I_{OS}$ | Short Circuit Current | $V_{DD}$ = Max, $V_{OUT}$ = GND | | – | – | –150 | mA |

## AC Switching Characteristics

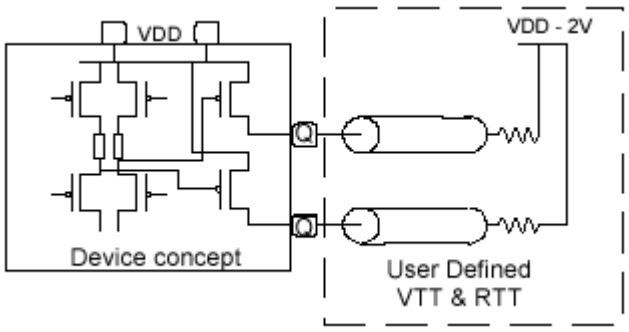
(at $V_{DD}$ = 3.3V ± 5%, $T_A$ = 0°C to 70°C or –40°C to 85°C)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay – Low to High | $V_{OD}$ = 100 mV | 3 | 4 | 5 | ns |
| $t_{PHL}$ | Propagation Delay – High to Low | | 3 | 4 | 5 | ns |
| $T_{PE}$ | Enable (EN) to Functional Operation | | – | – | 6 | ns |
| $T_{PD}$ | Functional Operation to Disable | | – | – | 5 | ns |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase) | | – | – | 0.2 | ns |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL}$–$t_{PLH}$) | | – | 0.2 | | ns |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature, and package type. Same input signal level and output load. | $V_{ID}$ = 100 mV | – | – | 1 | ns |

## High Frequency Parametrics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fmax | Maximum Frequency<br>$V_{DD}$ = 3.3V | 45% to 55% duty cycle<br>Standard load circuit | – | – | 350 | MHz |

**Figure 2. Driver Design**






[+] Feedback

**Figure 3. Differential Receiver to Driver Propagation Delay and Driver Transition Time[2,3,4,5]**

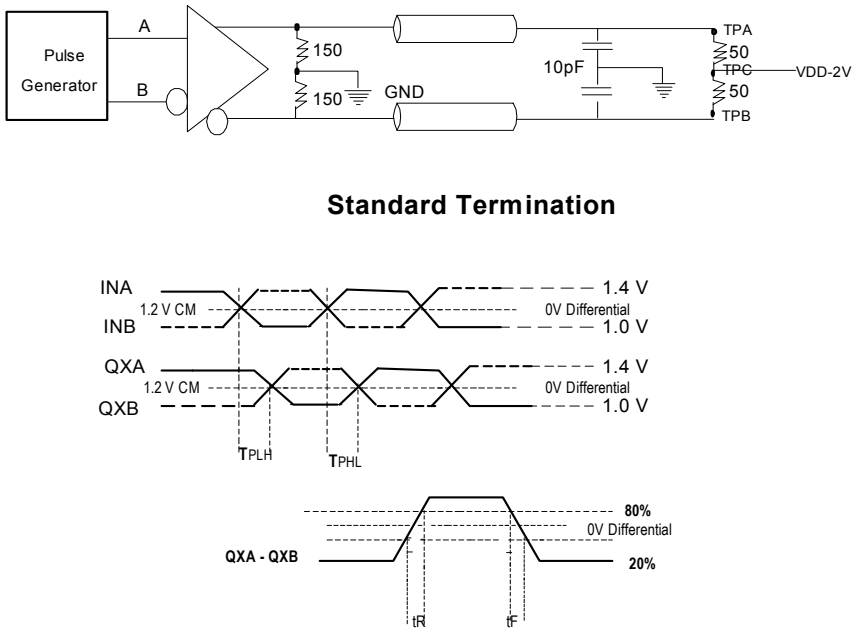
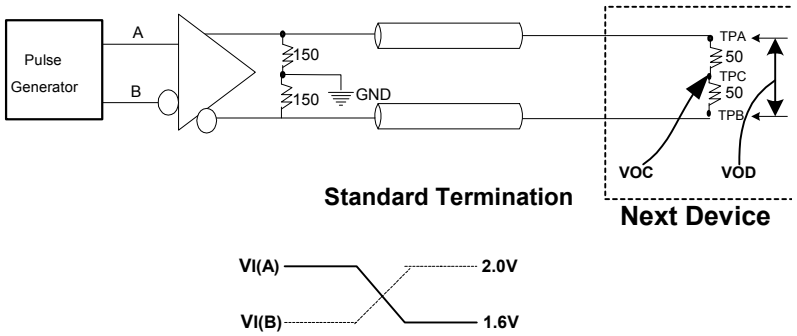



**Figure 4. Test Circuit and Voltage Definitions for the Driver Common-Mode Output Voltage[2,3,4,5]**



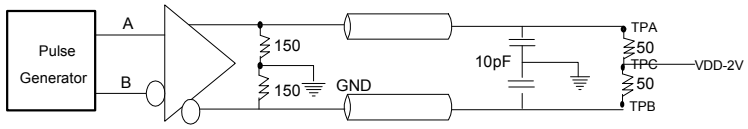

**Notes**

2. All input pulses are supplied by a frequency generator with the following characteristics: $t_R$ and $t_F \leq 1$ ns; pulse rerate = 50 Mpps; pulse width = 10 ± 0.2 ns.
3. RL = 50 ohm ± 1%; Zline = 50 ohm 6".
4. CL includes instrumentation and fixture capacitance within 6" of the DUT.
5. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to $V_{DD}$ – 2.

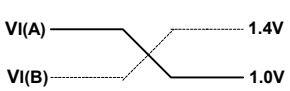


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**Figure 5. Test Circuit and Voltage Definitions for the Differential Output Signal[2,3,4,5]**




**Standard Termination**



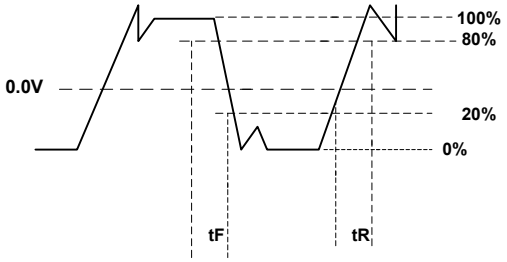
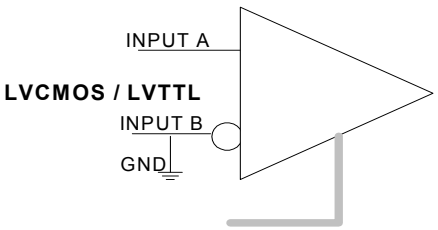
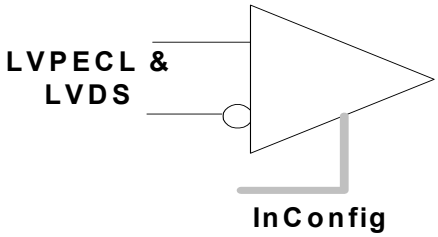




**Figure 6. LVTTL/LVCMOS[6]**




| | |
|---|---|
| 1 | LVTTL/LVCMOS |

**Figure 7. LVDS/LVPECL[6]**




| | |
|---|---|
| 0 | LVDS/LVPECL |

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY2DP818ZI-2 | 38-Pin TSSOP | Industrial, –40° to 85°C |
| CY2DP818ZI-2T | 38-Pin TSSOP–Tape and Reel | Industrial, –40° to 85°C |
| CY2DP818ZC-2 | 38-Pin TSSOP | Commercial, 0°C to 70°C |
| CY2DP818ZC-2T | 38-Pin TSSOP–Tape and Reel | Commercial, 0°C to 70°C |
| **Pb Free Devices** | | |
| CY2DP818ZXI-2 | 38-Pin TSSOP | Industrial, –40° to 85°C |
| CY2DP818ZXI-2T | 38-Pin TSSOP–Tape and Reel | Industrial, –40° to 85°C |
| CY2DP818ZXC-2 | 38-Pin TSSOP | Commercial, 0°C to 70°C |
| CY2DP818ZXC-2T | 38-Pin TSSOP–Tape and Reel | Commercial, 0°C to 70°C |

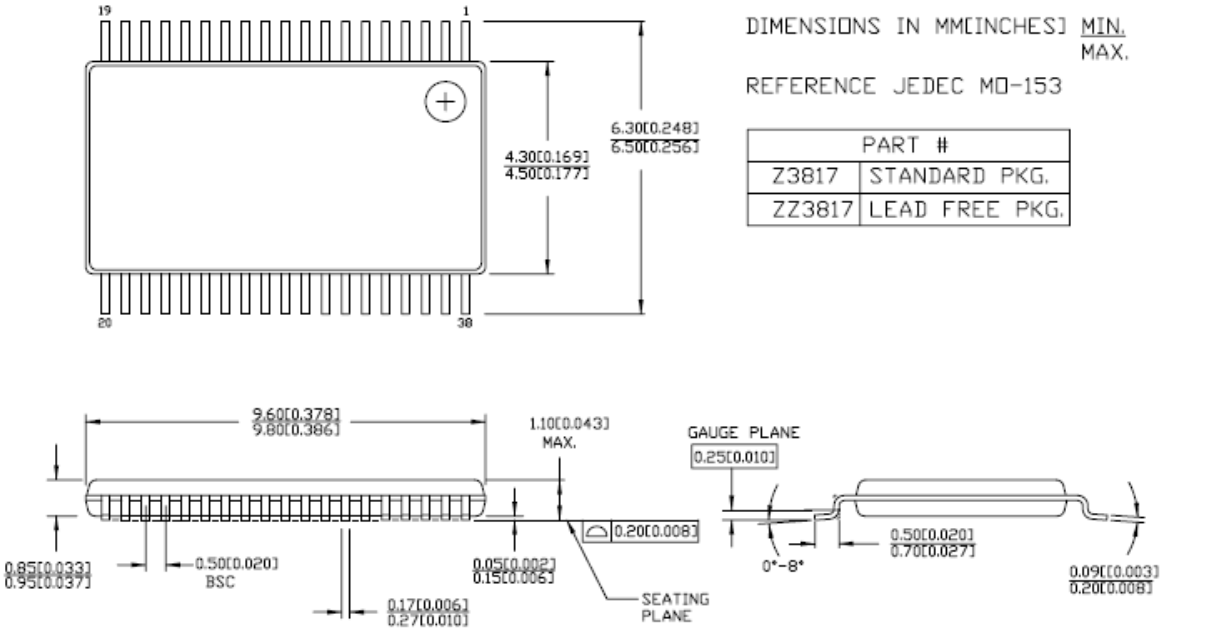
**Note**
6. LVPECL or LVDS differential input value.



[+] Feedback

## Package Drawing and Dimensions

**Figure 8. 38-Pin TSSOP (4.40 mm Body) Z38**




51-85151-*A



[+] Feedback

## Document History Page

| Document Title: CY2DP818-2 1:8 Clock Fanout Buffer<br>Document Number: 38-07588 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 129879 | 11/07/03 | RGL | New Data Sheet |
| *A | 2595534 | 10/23/08 | CXQ/PYRS | Removed “Preliminary”, added Pb-free devices to Ordering Information |

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