ANALOG DEVICES

81 GHz to 86 GHz, E-Band I/Q Upconverter

Data Sheet **HMC8119**

FEATURES

Conversion loss: 10 dB typical
Sideband rejection: 22 dBc typical
Input power for 1 dB compression (P1dB): 16 dBm typical
Input third-order intercept (IP3): 24 dBm typical
Input second-order intercept (IP2): −5 dBm typical
6× local oscillator (LO) leakage at RFOUT: −23 dBm typical
RF return loss: 12 dB typical
LO return loss: 20 dB typical
Die size: 3.601 mm × 1.609 mm × 0.05 mm

APPLICATIONS

E-band communication systems
High capacity wireless backhaul
Test and measurement

GENERAL DESCRIPTION

The HMC8119 is an integrated E-band gallium arsenide (GaAs) pseudomorphic (pHEMT) monolithic microwave integrated circuit (MMIC), in-phase/quadrature (I/Q) upconverter chip that operates from 81 GHz to 86 GHz. The HMC8119 provides a small signal conversion loss of 10 dB with 22 dBc of sideband rejection across the frequency band. The device uses an image rejection mixer that is driven by a 6× LO multiplier. Differential I and Q mixer inputs are provided. The inputs can be driven with differential I and Q baseband waveforms for direct conversion applications. Alternatively, the inputs can be driven using an external 90° hybrid and two external 180° hybrids for single-sideband applications. All data includes the effect of a 1 mil gold wire wedge bond on the intermediate frequency (IF) ports.

FUNCTIONAL BLOCK DIAGRAM

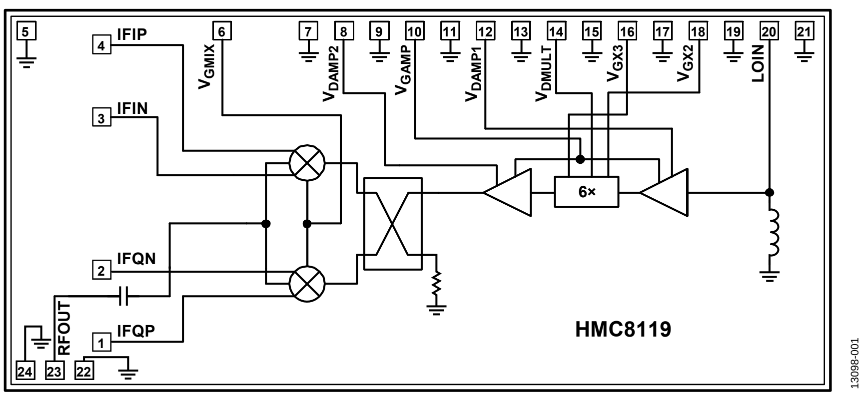

Figure 1.

Rev. A Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

2/16—Revision A: Initial Version

SPECIFICATIONS

T_A = 25°C, IF = 500 MHz, V_{GMIX} = −1 V, V_{DAMPx} = 4 V, V_{DMULT} = 1.5 V, LO = 2 dBm, upper sideband selected (USB). Measurements performed as an upconverter with external 90° and 180° hybrids at the IF ports, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
RF Frequency Range		81		86	GHz
LO Frequency Range		11.83		14.33	GHz
IF Frequency Range		0		10	GHz
LO Drive Range		2		8	dBm
PERFORMANCE					
Conversion Loss			10	13	dB
Sideband Rejection			22		dBc
Input Power for 1 dB Compression (P1dB)			16		dBm
Input Third-Order Intercept (IP3)			24		dBm
Input Second-Order Intercept (IP2)			−5		dBm
6× LO Leakage at RFOUT			−23	−19	dBm
RF Return Loss			12		dB
LO Return Loss			20		dB
IF Return Loss			25		dB
POWER SUPPLY					
Supply Current					
I_{DAMP}[1]			175		mA
I_{DMULT}[2]	Under LO drive		80		mA

[1] Adjust V_{GAMP} from −2 V to 0 V to achieve the total quiescent current, I_{DAMP} = I_{DAMP1} + I_{DAMP2} = 175 mA.
[2] Adjust V_{GX2} and V_{GX3} from −2 V to 0 V to achieve the quiescent current, I_{DMULT} = 1 mA to 2 mA. Refer to the Applications Information section for more information.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage	
V_{DAMP1}, V_{DAMP2}	4.5 V
V_{DMULT}	3 V
Gate Bias Voltage	
V_{GAMP}	−3 V to 0 V
V_{GX2}, V_{GX3}	−3 V to 0 V
V_{GMIX}	−3 V to 0 V
LO Input Power	10 dBm
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
24-Pad Bare Die [CHIP]	73.7	°C/W

[1] Based on ABLEBOND® 84-1LMIT as die attach epoxy with thermal conductivity of 3.6 W/mK.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

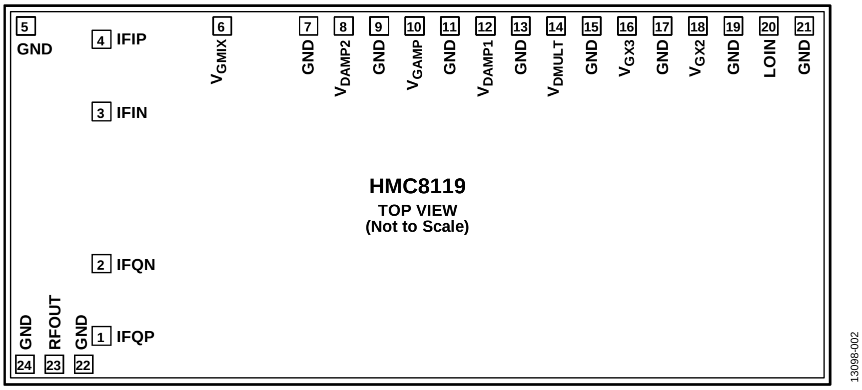

Figure 2. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 2	IFQP, IFQN	Positive and Negative IF Q Inputs. These pads are dc-coupled. When operation to dc is not required, block these pads externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, these pads must not source or sink more than 3 mA of current or die malfunction and die failure may result (see Figure 3).
3, 4	IFIN, IFIP	Negative and Positive IF I Inputs. These pads are dc-coupled. When operation to dc is not required, block these pads externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, these pads must not source or sink more than 3 mA of current or die malfunction and die failure may result (see Figure 3).
5, 7, 9, 11, 13, 15, 17, 19, 21, 22, 24	GND	Ground Connect (See Figure 4).
6	V_{GMIX}	Gate Voltage for the FET Mixer (See Figure 5).
8, 12	V_{DAMP2}, V_{DAMP1}	Power Supply Voltage for the First and the Second Stage LO Amplifier (See Figure 5).
10	V_{GAMP}	Gate Voltage for the First and the Second Stage LO Amplifier (See Figure 5).
14	V_{DMULT}	Power Supply Voltage for the Multiplier (See Figure 5).
16, 18	V_{GX3}, V_{GX2}	Gate Voltage for the Multiplier (See Figure 5).
20	LOIN	Local Oscillator Input. This pad is dc-coupled and matched to 50 Ω (see Figure 6).
23	RFOUT	RF Output. This pad is ac-coupled and matched to 50 Ω (see Figure 7).
Die Bottom	GND	Ground. The die bottom must be connected to RF/dc ground (see Figure 4).

INTERFACE SCHEMATICS

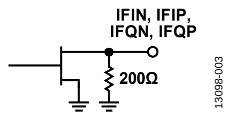

Figure 3. IFIP, IFIN, IFQN, IFQP Interface

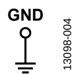

Figure 4. GND Interface

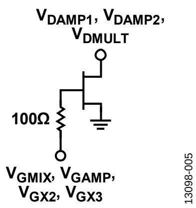

Figure 5. V_{GMIX}, V_{DAMP1}, V_{DAMP2}, V_{DMULT}, V_{GAMP}, V_{GX2}, V_{GX3} Interface

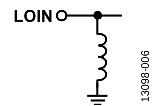

Figure 6. LOIN Interface

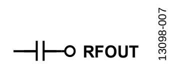

Figure 7. RFOUT Interface

TYPICAL PERFORMANCE CHARACTERISTICS

UPPER SIDEBAND (USB) SELECTED, IF = 500 MHz

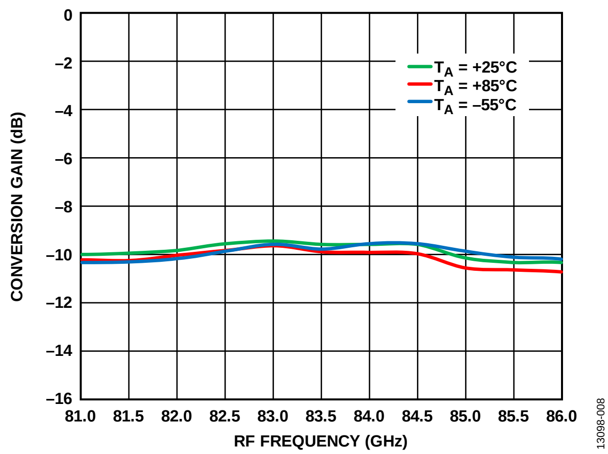

Figure 8. Conversion Gain vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 500 MHz, USB

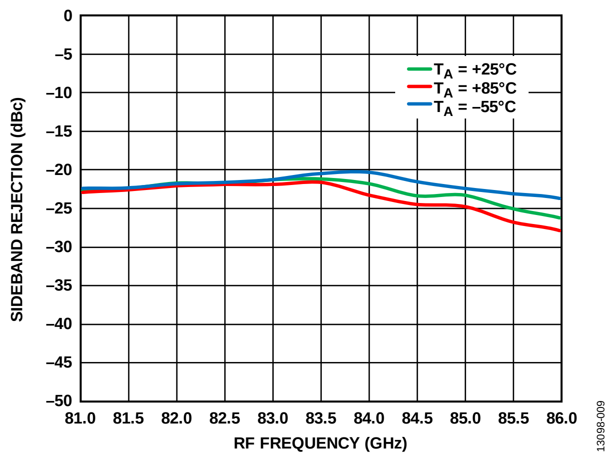

Figure 9. Sideband Rejection vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 500 MHz, USB

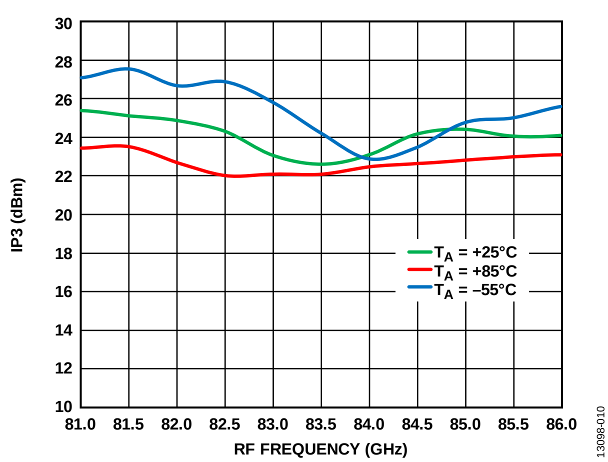

Figure 10. Input IP3 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 500 MHz, USB

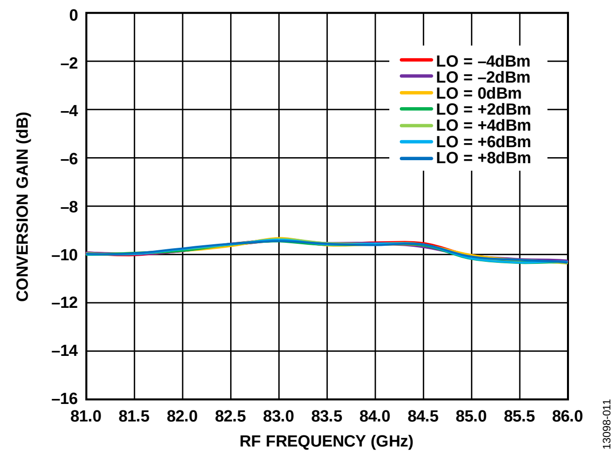

Figure 11. Conversion Gain vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 500 MHz, USB

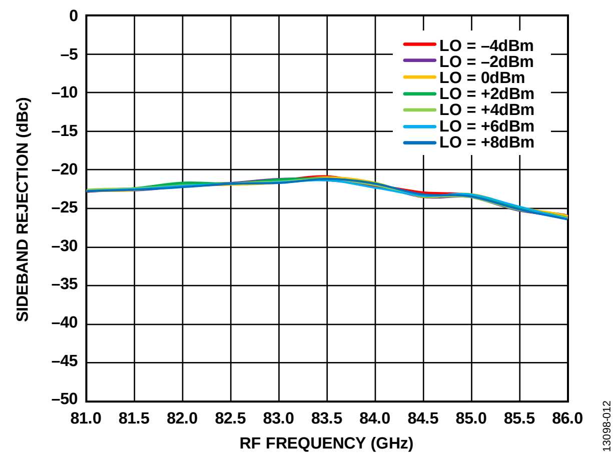

Figure 12. Sideband Rejection vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 500 MHz, USB

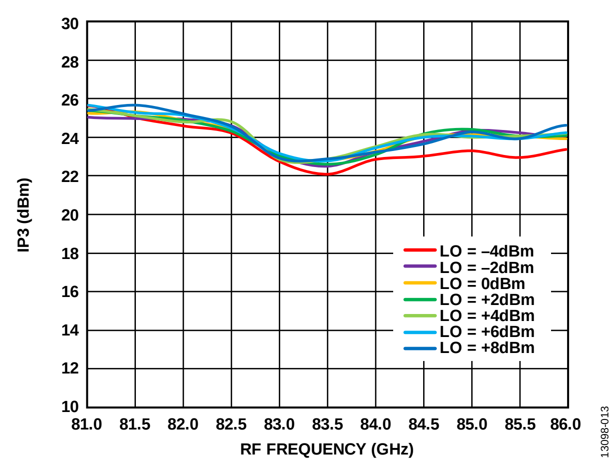

Figure 13. Input IP3 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 500 MHz, USB

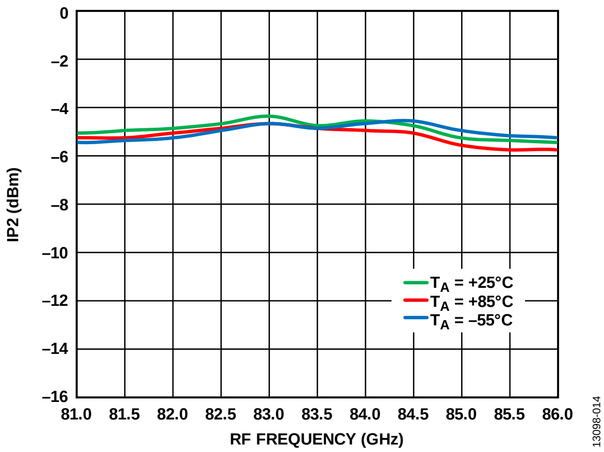

Figure 14. Input IP2 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 500 MHz, USB

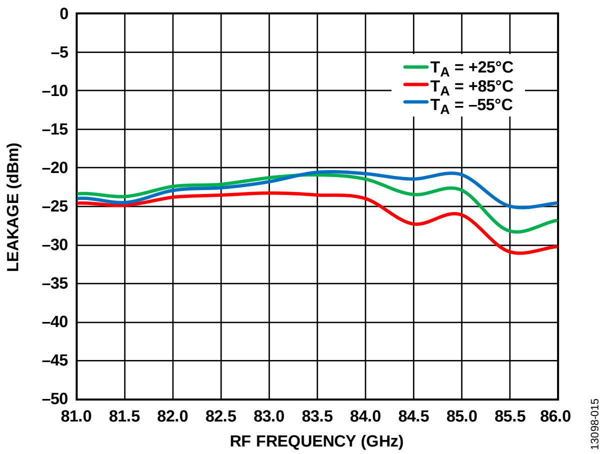

Figure 15. 6× LO Leakage at RFOUT vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO= 2 dBm, IF = 500 MHz, USB

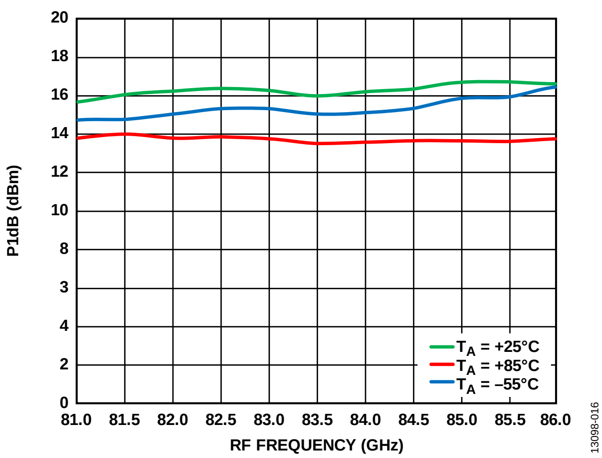

Figure 16. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, IF = 500 MHz, USB

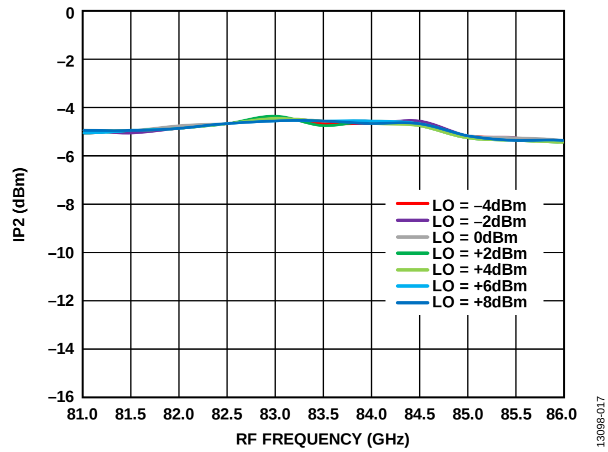

Figure 17. Input IP2 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 500 MHz, USB

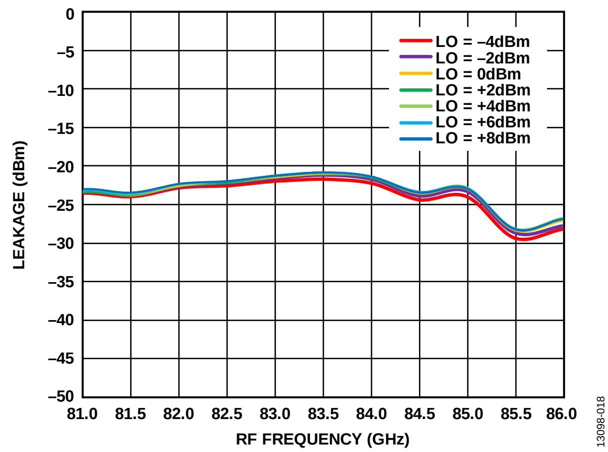

Figure 18. 6× LO Leakage at RFOUT vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 500 MHz, USB

RETURN LOSS PERFORMANCE

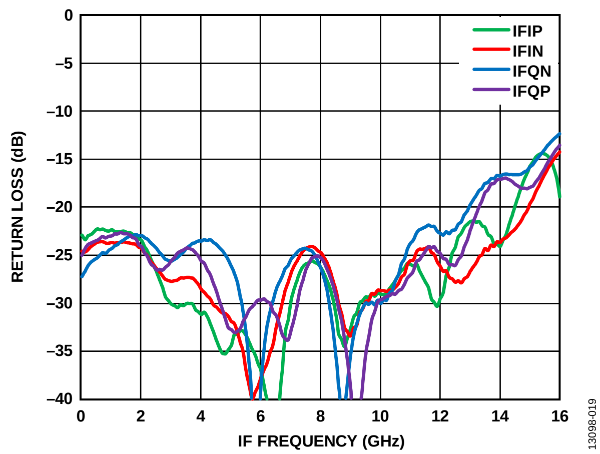

Figure 19. IF Return Loss vs. IF Frequency, LO = 2 dBm at 12 GHz

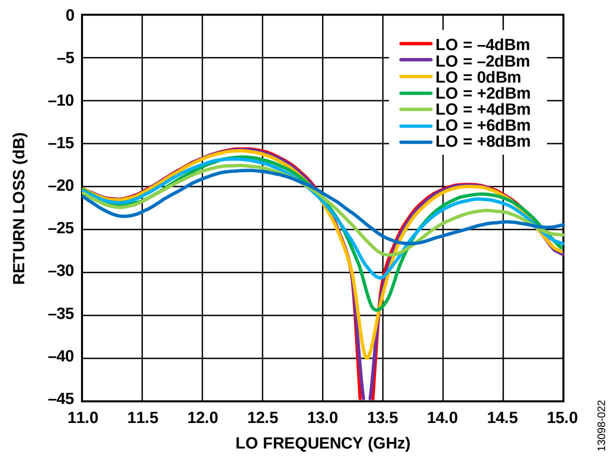

Figure 22. LO Return Loss vs. LO Frequency at Various LO Powers

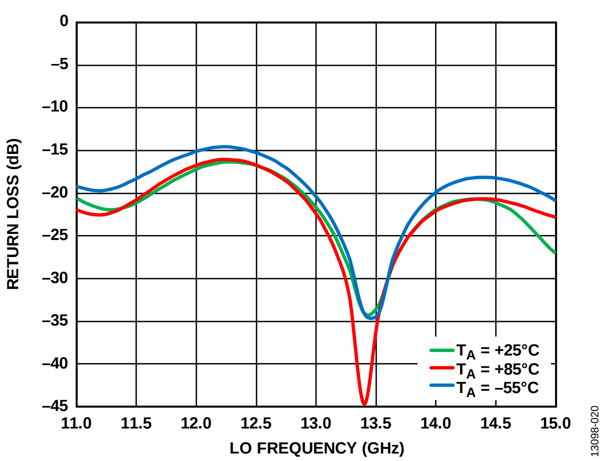

Figure 20. LO Return Loss vs. LO Frequency at Various Temperatures, LO = 2 dBm

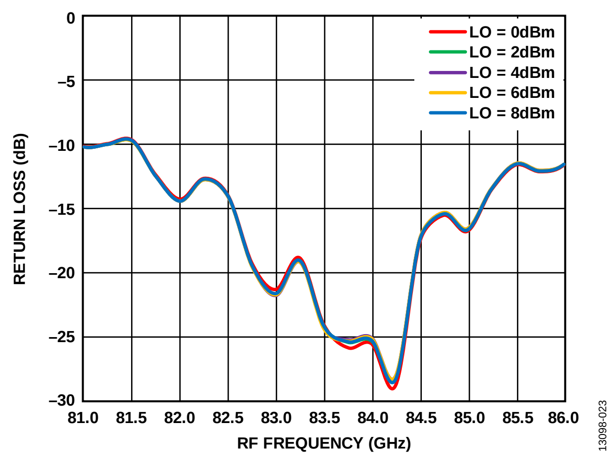

Figure 23. RF Return Loss vs. RF Frequency at Various LO Powers, RFIN = −10 dBm

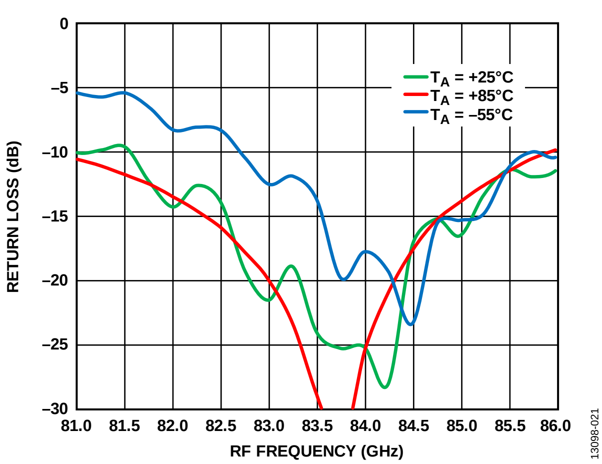

Figure 21. RF Return Loss vs. RF Frequency at Various Temperatures, RFIN = −10 dBm, LO = 2 dBm at 12 GHz

UPPER SIDEBAND (USB) SELECTED, IF = 1000 MHz

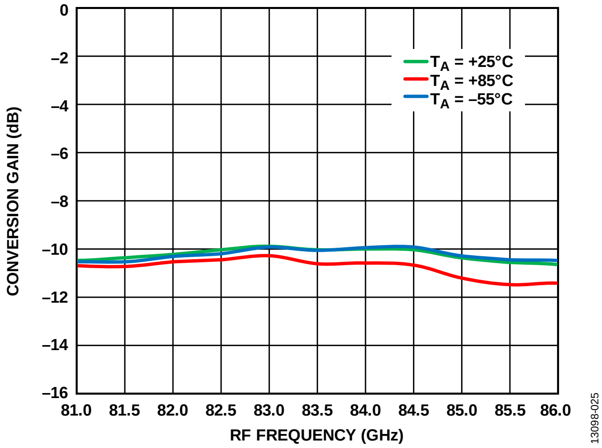

Figure 24. Conversion Gain vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 1000 MHz, USB

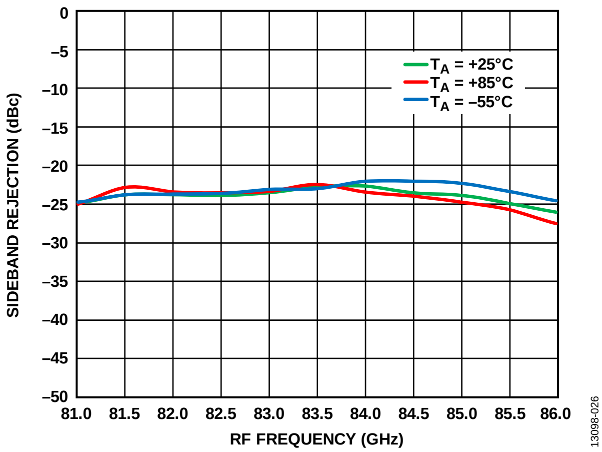

Figure 25. Sideband Rejection vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 1000 MHz, USB

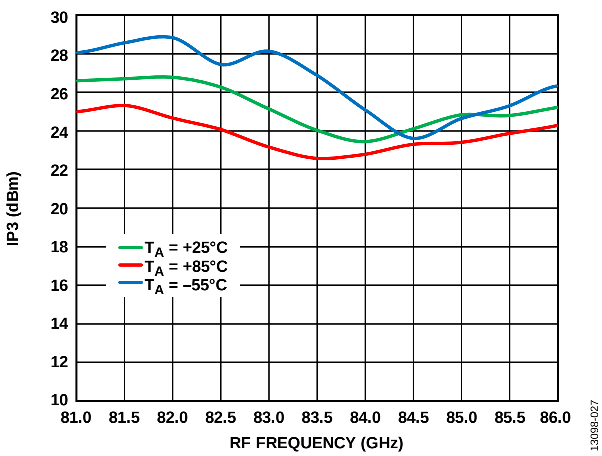

Figure 26. Input IP3 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 1000 MHz, USB

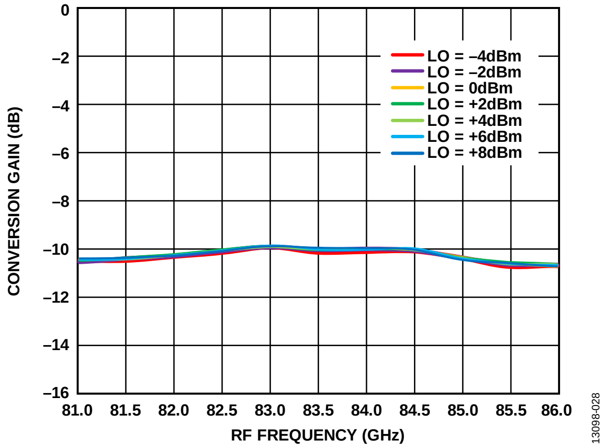

Figure 27. Conversion Gain vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 1000 MHz, USB

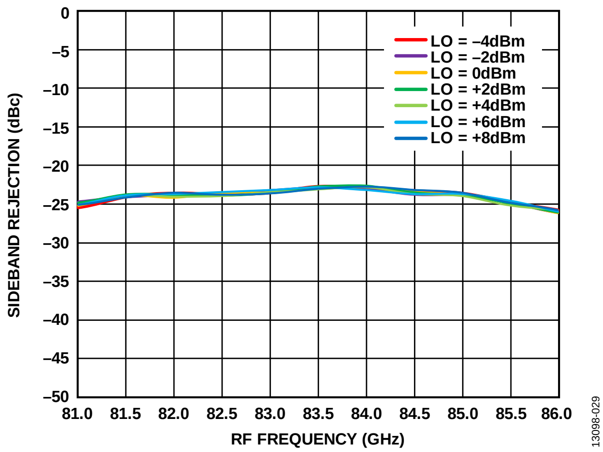

Figure 28. Sideband Rejection vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 1000 MHz, USB

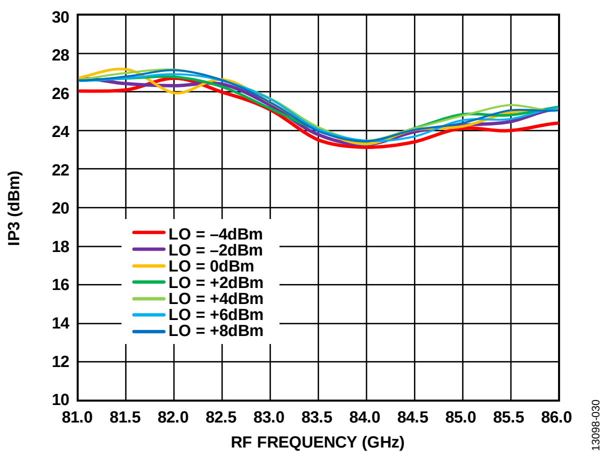

Figure 29. Input IP3 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, USB

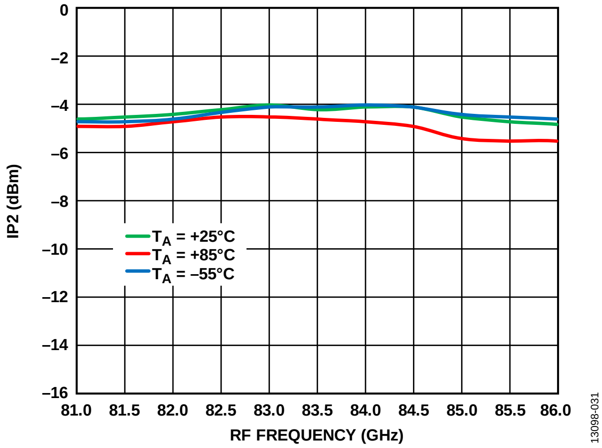

Figure 30. Input IP2 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 1000 MHz, USB

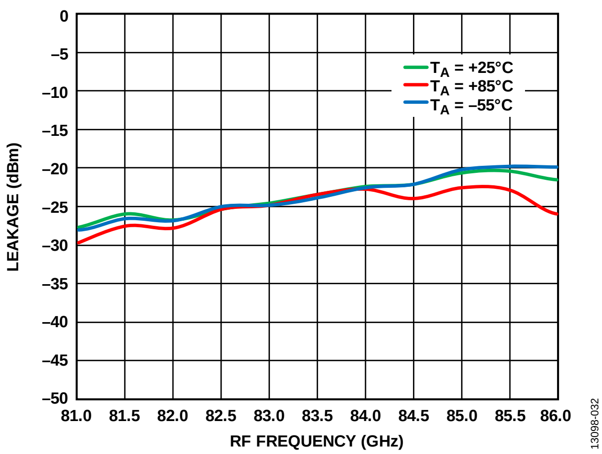

Figure 31. 6× LO Leakage at RFOUT vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 1000 MHz, USB

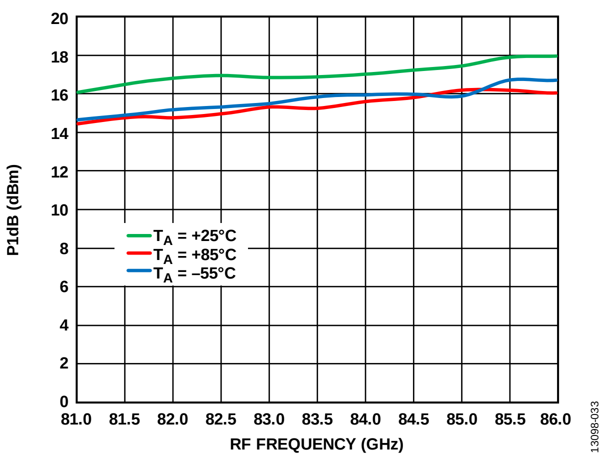

Figure 32. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, IF = 1000 MHz, USB

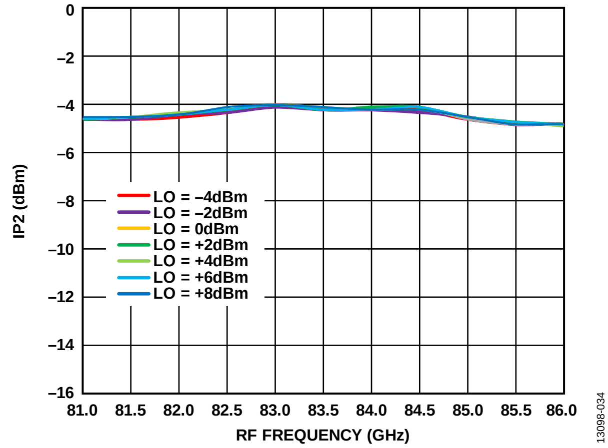

Figure 33. Input IP2 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, USB

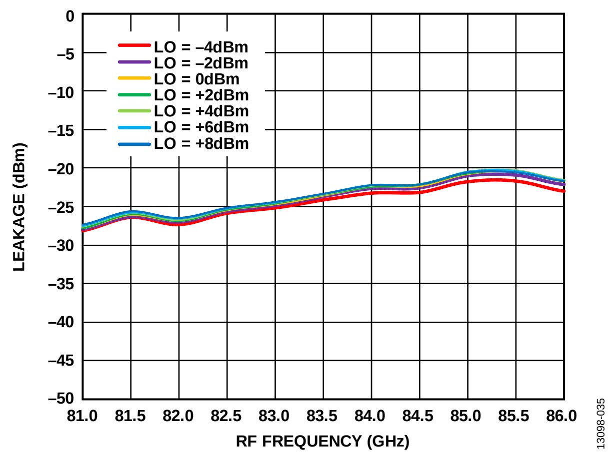

Figure 34. 6× LO Leakage at RFOUT vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, USB

UPPER SIDEBAND (USB) SELECTED, IF = 2000 MHz

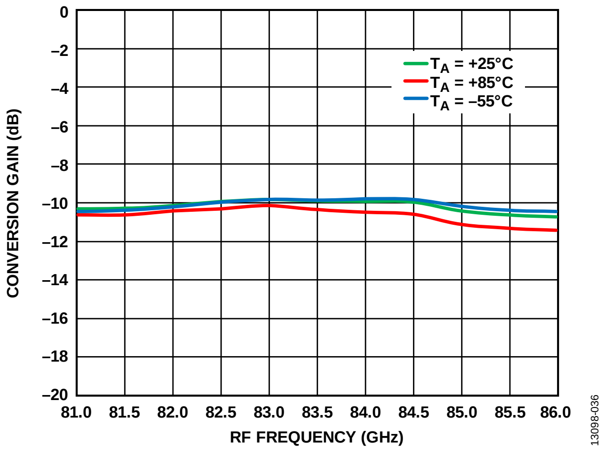

Figure 35. Conversion Gain vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 2000 MHz, USB

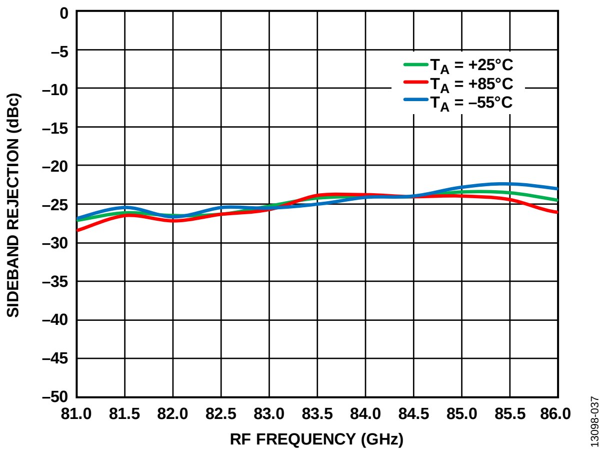

Figure 36. Sideband Rejection vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 2000 MHz, USB

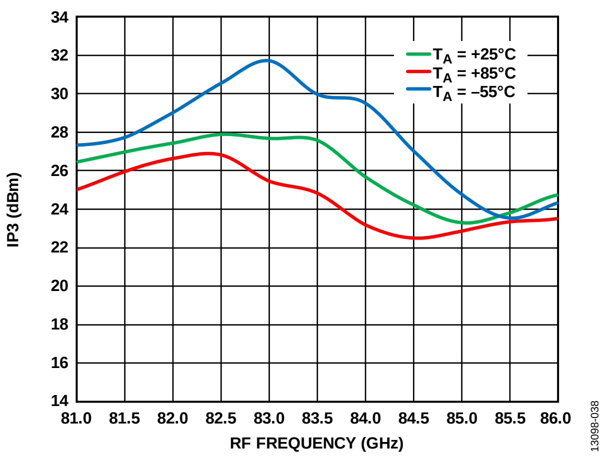

Figure 37. Input IP3 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 2000 MHz, USB

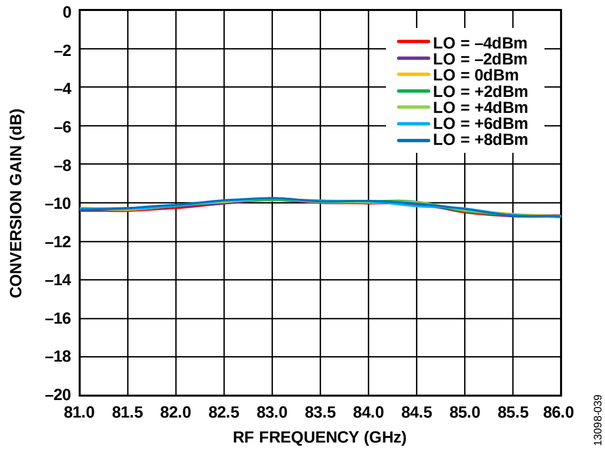

Figure 38. Conversion Gain vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 2000 MHz, USB

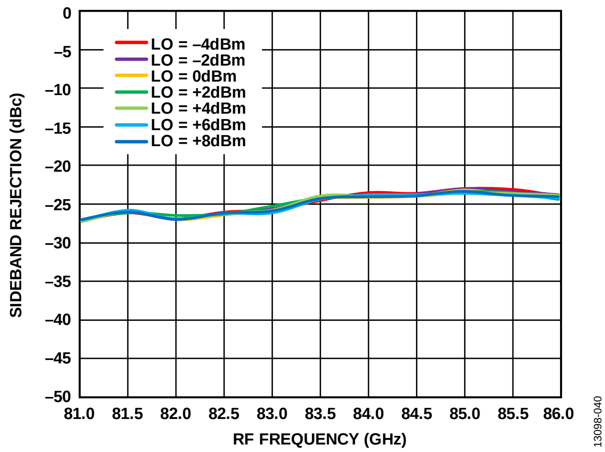

Figure 39. Sideband Rejection vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 2000 MHz, USB

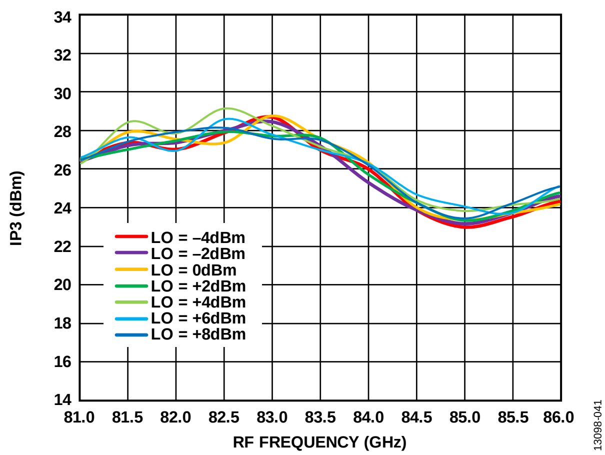

Figure 40. Input IP3 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 2000 MHz, USB

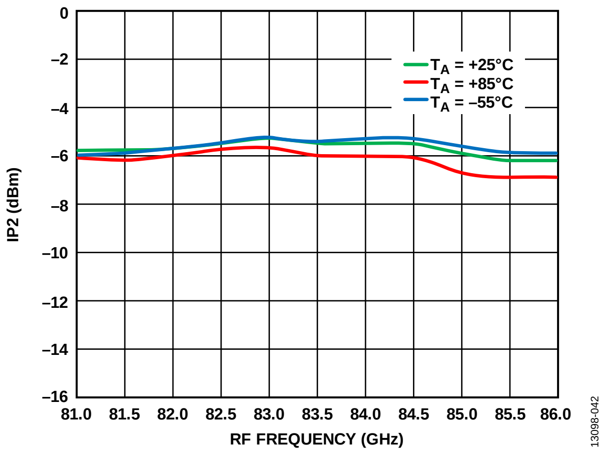

Figure 41. Input IP2 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 2000 MHz, USB

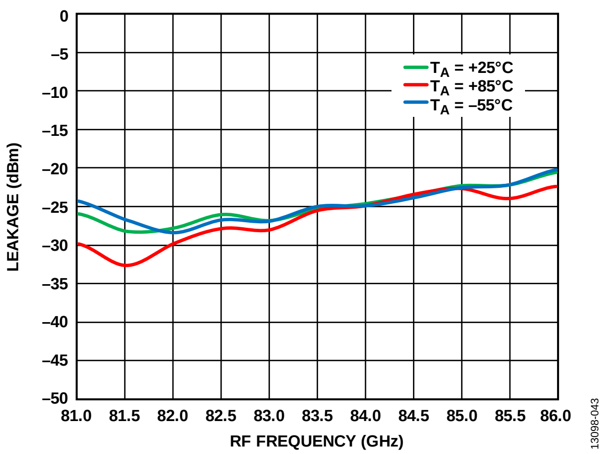

Figure 42. 6× LO Leakage at RFOUT vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 2000 MHz, USB

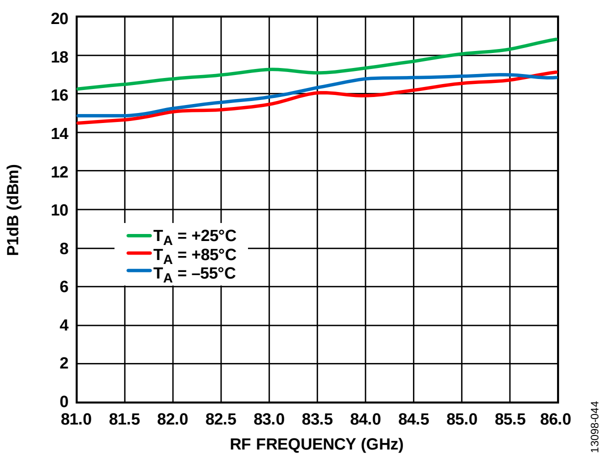

Figure 43. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, IF = 2000 MHz, USB

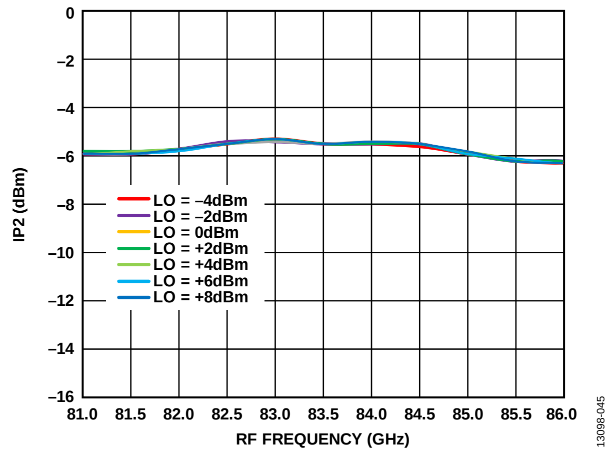

Figure 44. Input IP2 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 2000 MHz, USB

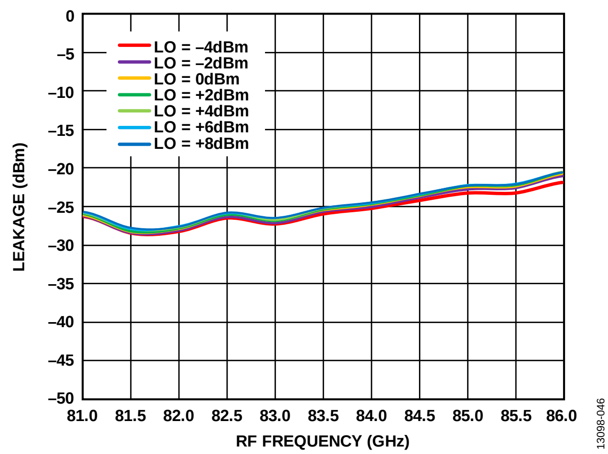

Figure 45. 6× LO Leakage at RFOUT vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, USB

LOWER SIDEBAND (LSB) SELECTED, IF = 500 MHz

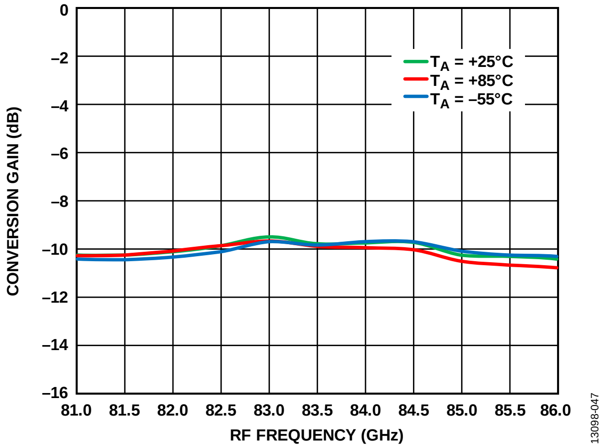

Figure 46. Conversion Gain vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 500 MHz, LSB

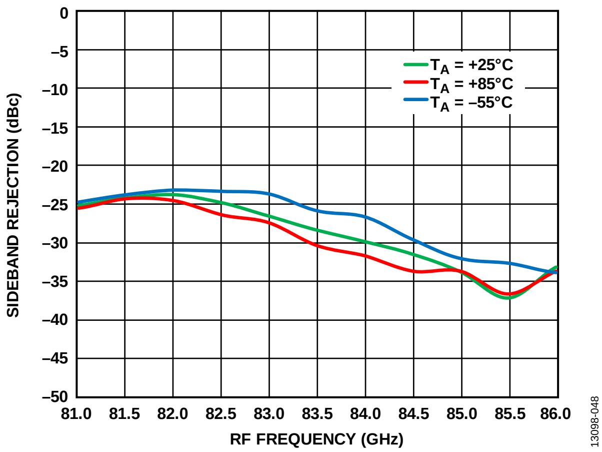

Figure 47. Sideband Rejection vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 500 MHz, LSB

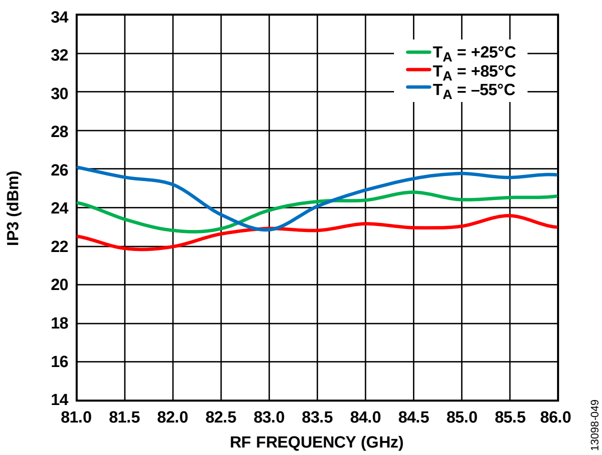

Figure 48. Input IP3 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 500 MHz, LSB

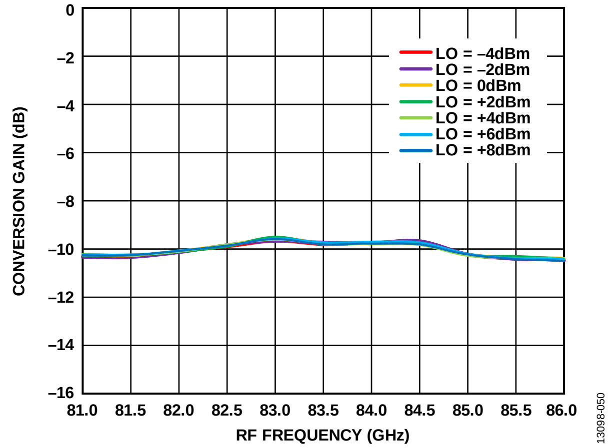

Figure 49. Conversion Gain vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 500 MHz, LSB

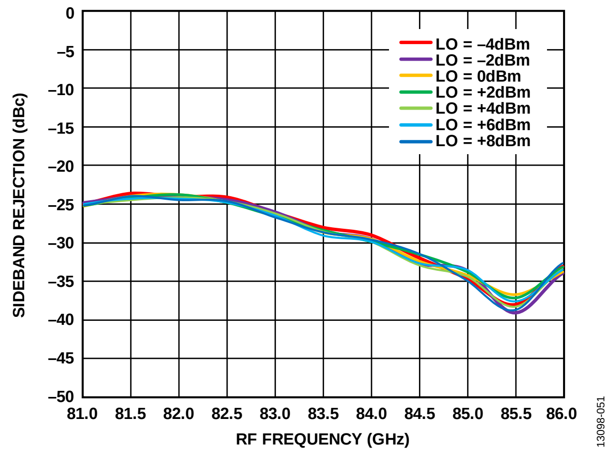

Figure 50. Sideband Rejection vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 500 MHz, LSB

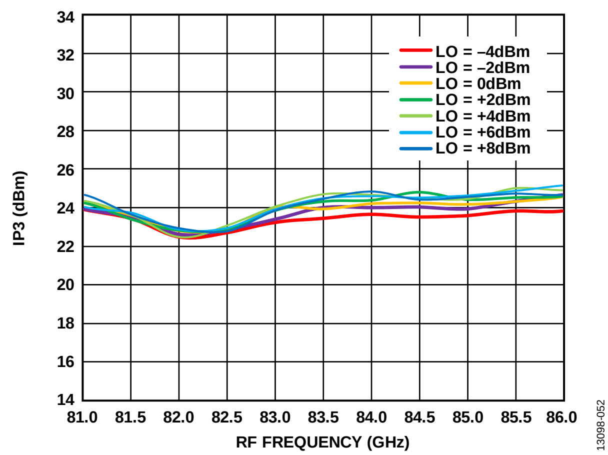

Figure 51. Input IP3 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 500 MHz, LSB

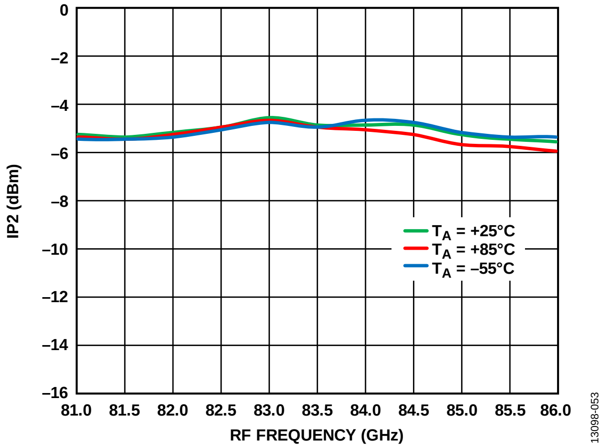

Figure 52. Input IP2 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 500 MHz, LSB

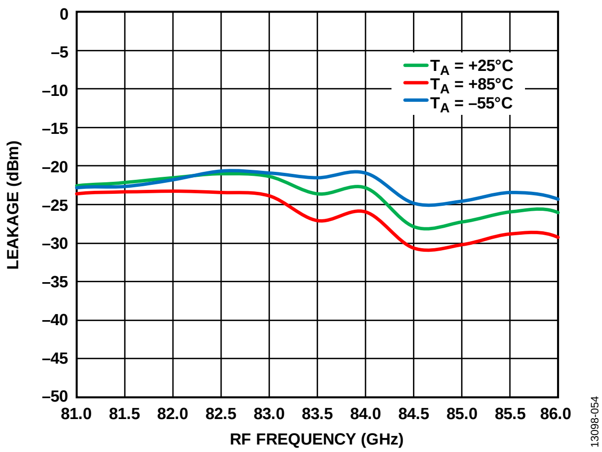

Figure 53. 6× LO Leakage at RFOUT vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, IF = 500 MHz, LSB

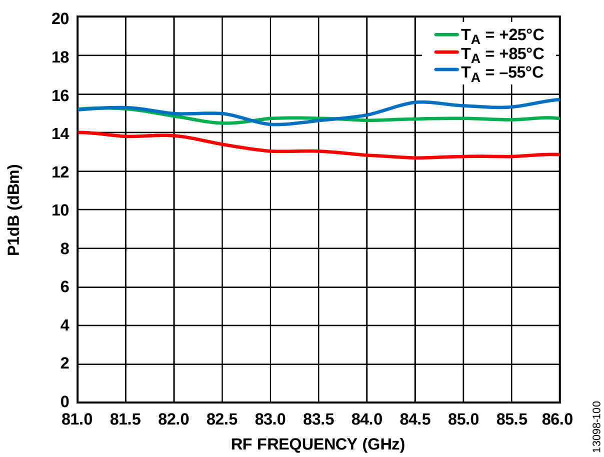

Figure 54. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, IF = 500 MHz, LSB

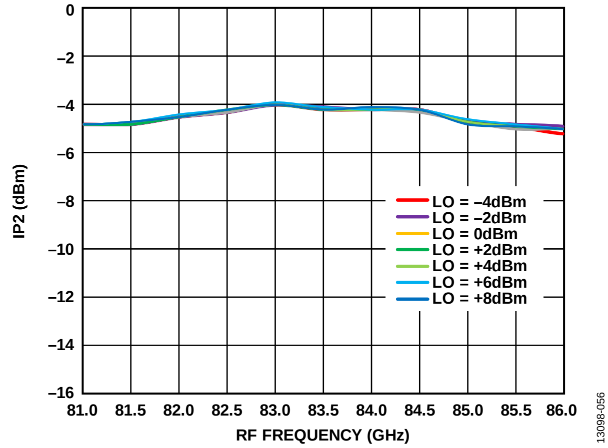

Figure 55. Input IP2 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 500 MHz, LSB

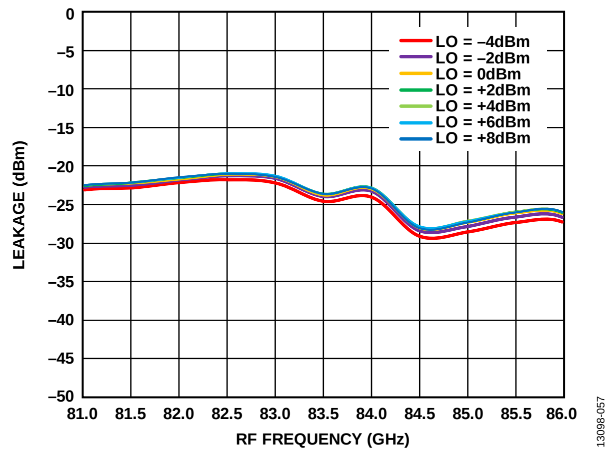

Figure 56. 6× LO Leakage at RFOUT vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 500 MHz, LSB

LOWER SIDEBAND (LSB) SELECTED, IF = 1000 MHz

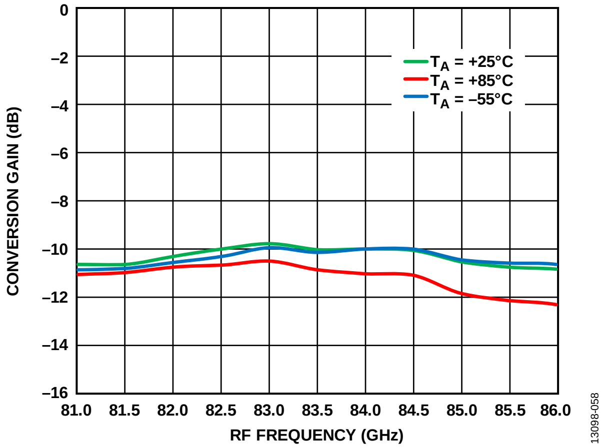

Figure 57. Conversion Gain vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 1000 MHz, LSB

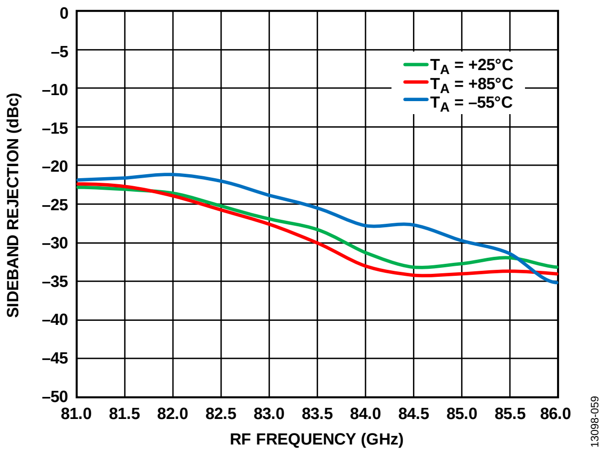

Figure 58. Sideband Rejection vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 1000 MHz, LSB

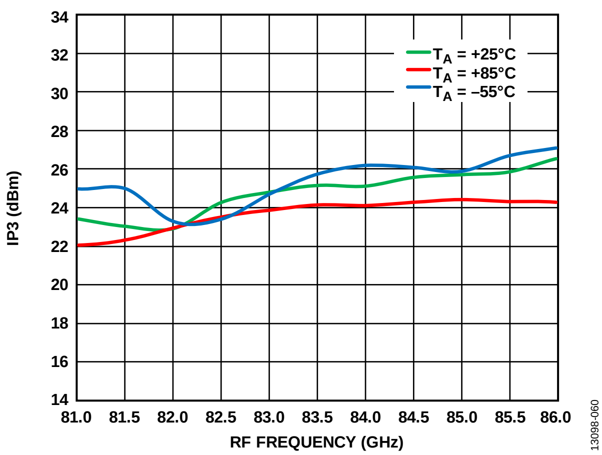

Figure 59. Input IP3 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 1000 MHz, LSB

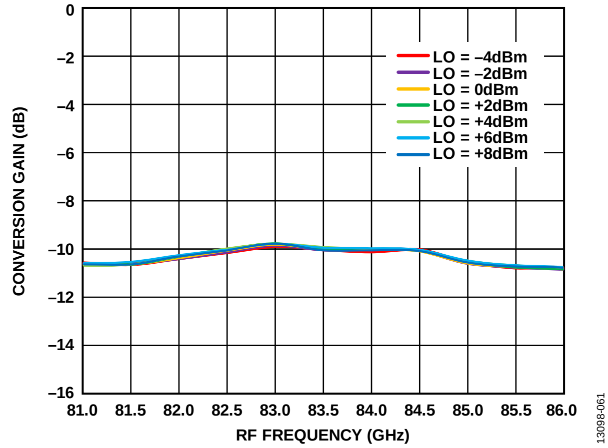

Figure 60. Conversion Gain vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 1000 MHz, LSB

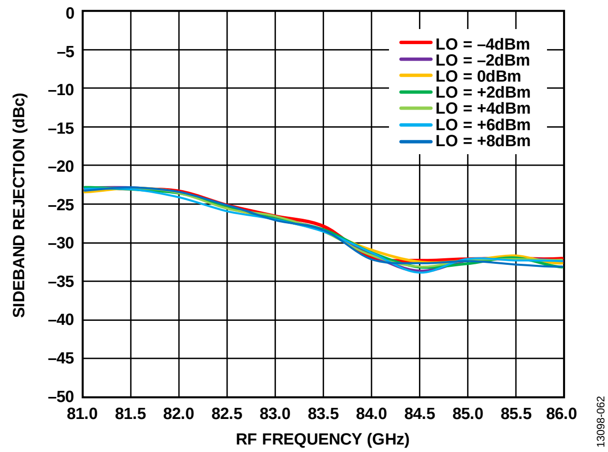

Figure 61. Sideband Rejection vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 1000 MHz, LSB

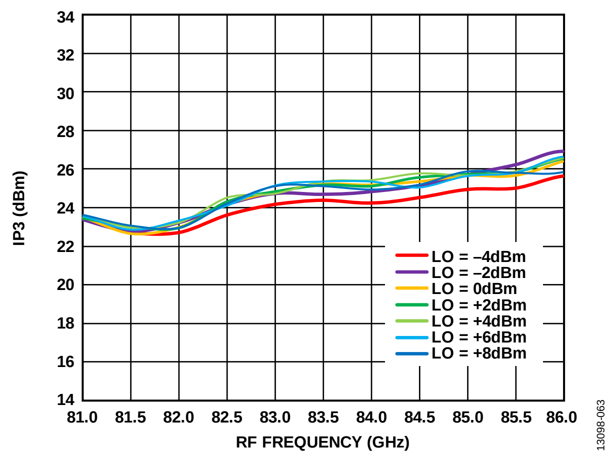

Figure 62. Input IP3 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, LSB

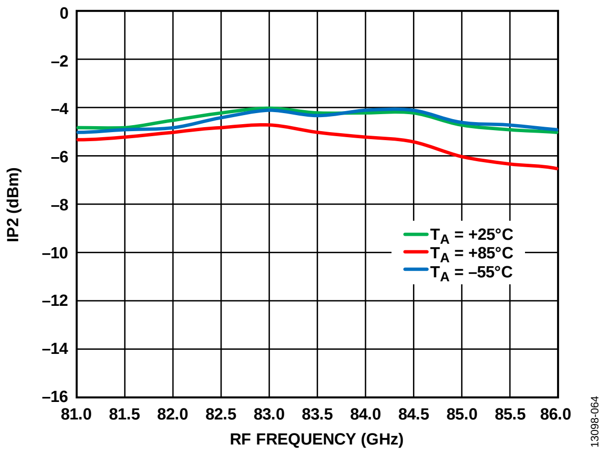

Figure 63. Input IP2 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 1000 MHz, LSB

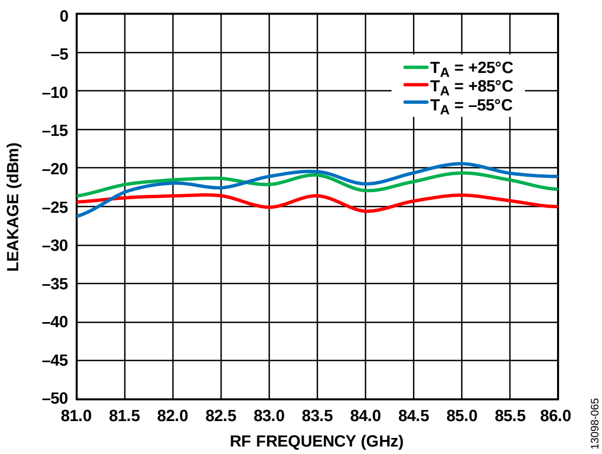

Figure 64. 6× LO Leakage at RFOUT vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 1000 MHz, LSB

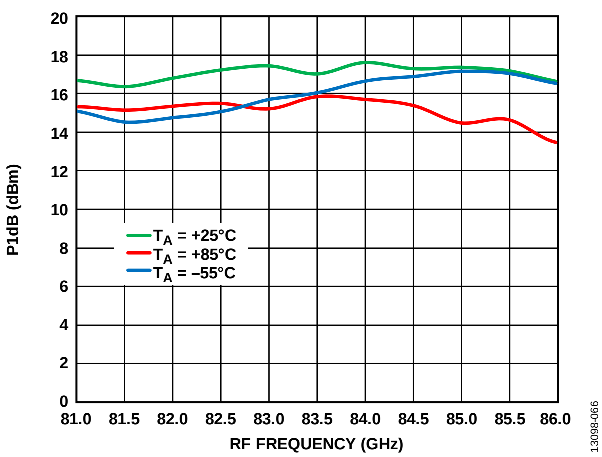

Figure 65. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, IF = 1000 MHz, LSB

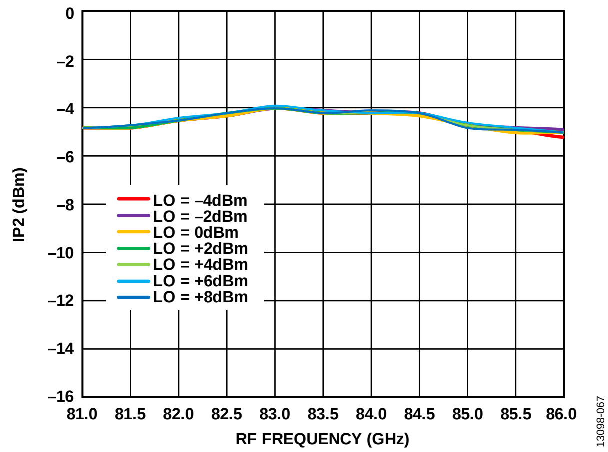

Figure 66. Input IP2 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, LSB

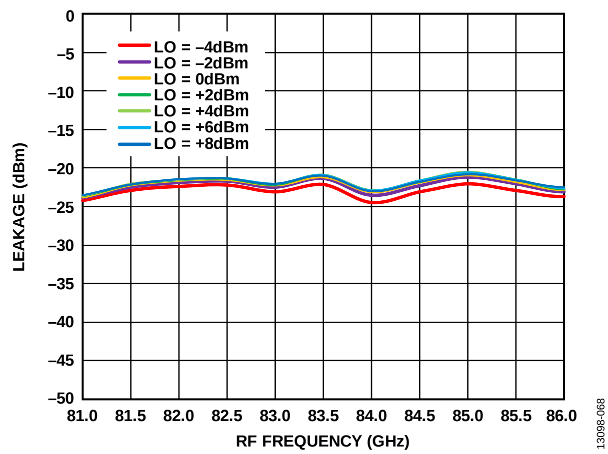

Figure 67. 6× LO Leakage at RFOUT vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 1000 MHz, LSB

LOWER SIDEBAND (LSB) SELECTED, IF = 2000 MHz

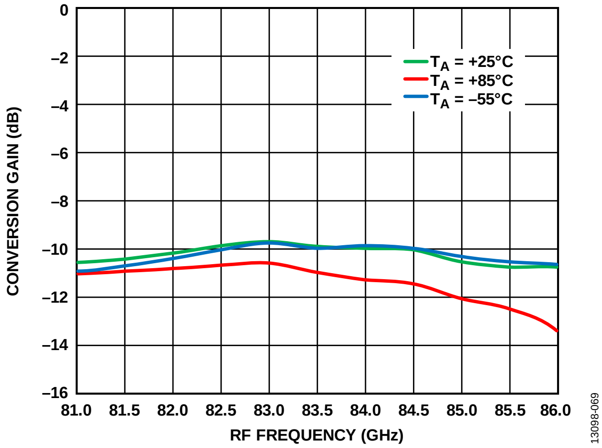

Figure 68. Conversion Gain vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 2000 MHz, LSB

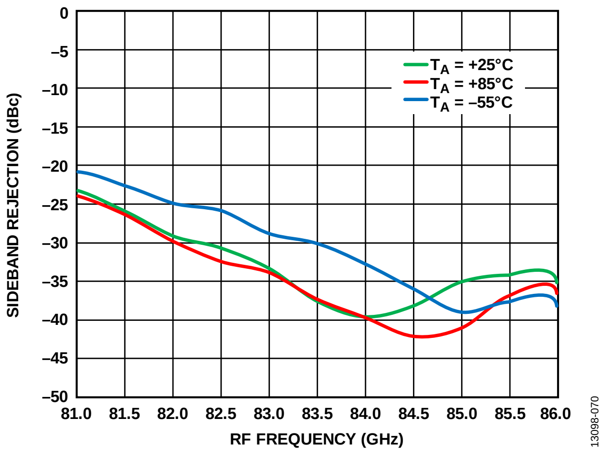

Figure 69. Sideband Rejection vs. RF Frequency at Various Temperatures, IFIN = −8 dBm, LO = 2 dBm, IF = 2000 MHz, LSB

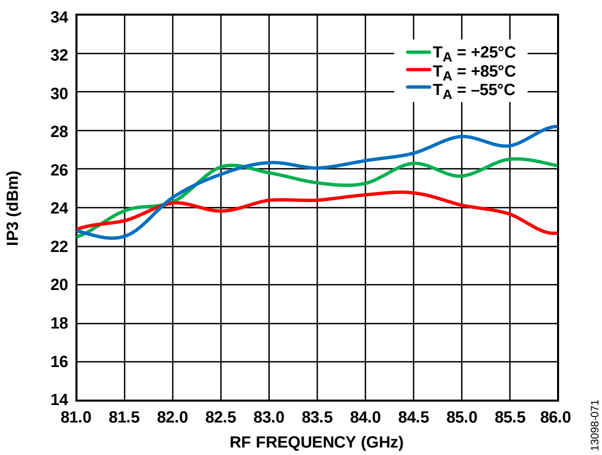

Figure 70. Input IP3 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 2000 MHz, LSB

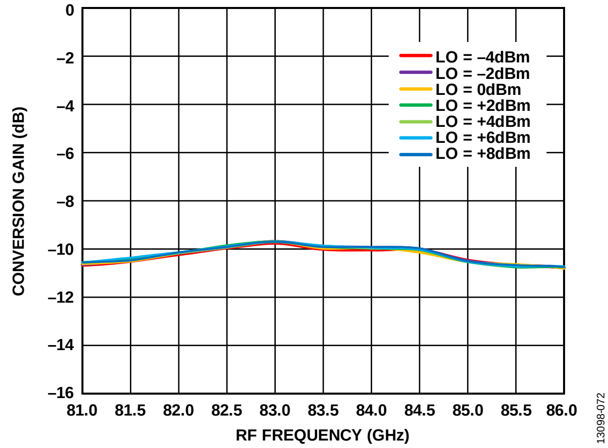

Figure 71. Conversion Gain vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 2000 MHz, LSB

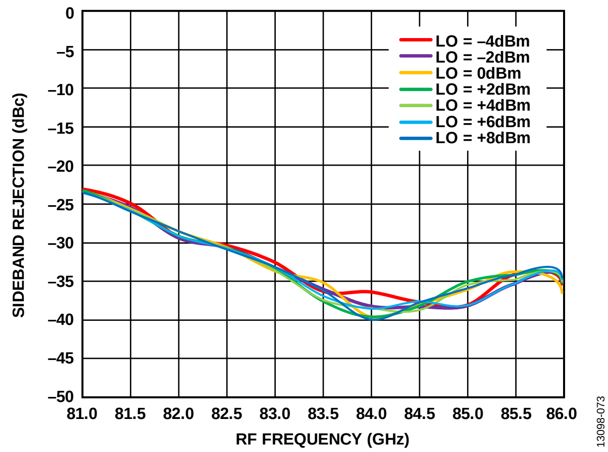

Figure 72. Sideband Rejection vs. RF Frequency at Various LO Powers, IFIN = −8 dBm, IF = 2000 MHz, LSB

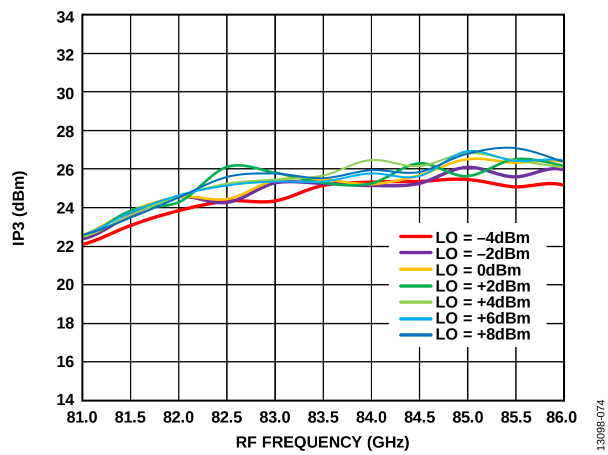

Figure 73. Input IP3 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 2000 MHz, LSB

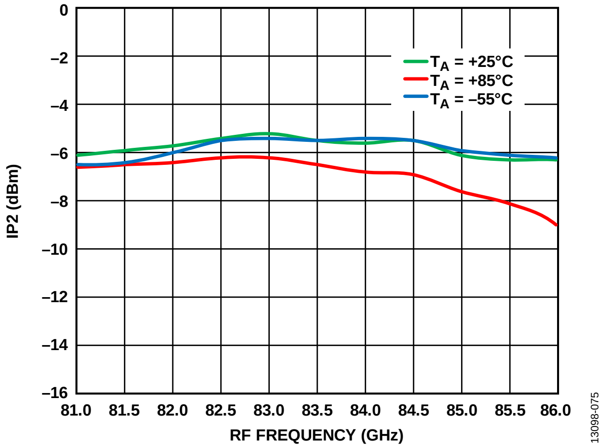

Figure 74. Input IP2 vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, LO = 2 dBm, IF = 2000 MHz, LSB

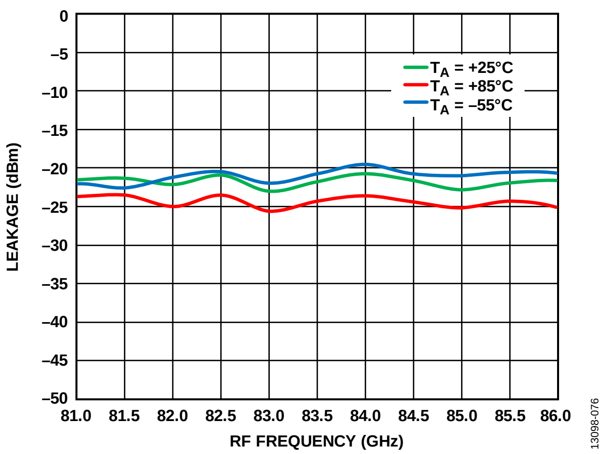

Figure 75. 6× LO Leakage at RFOUT vs. RF Frequency at Various Temperatures, IFIN = 5 dBm, IF = 2000 MHz, LSB

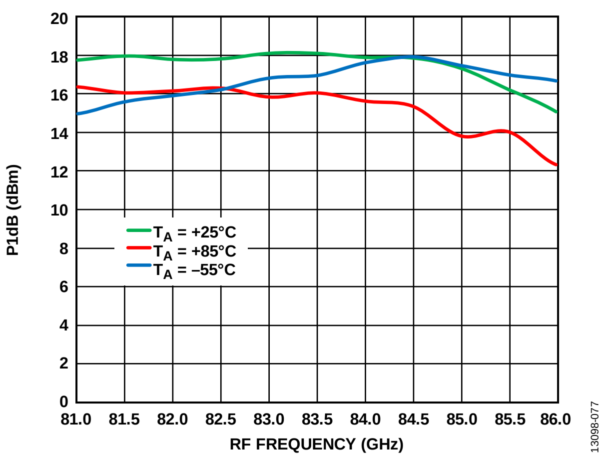

Figure 76. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, IF = 2000 MHz, LSB

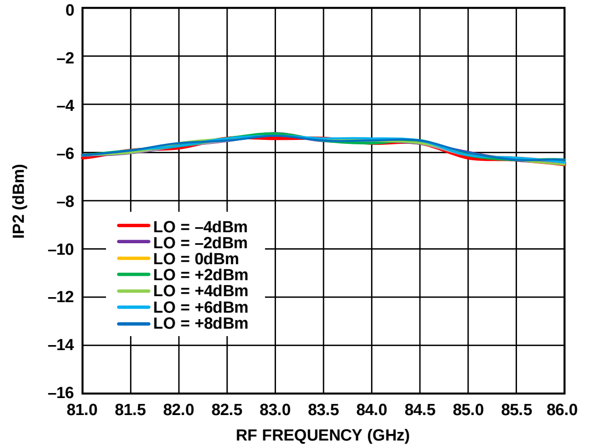

Figure 77. Input IP2 vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 2000 MHz, LSB

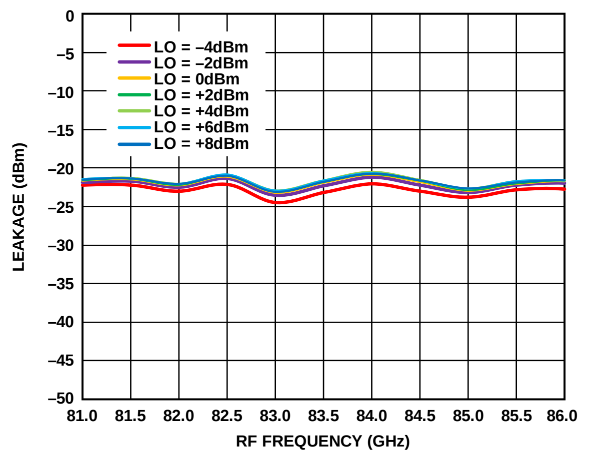

Figure 78. 6× LO Leakage at RFOUT vs. RF Frequency at Various LO Powers, IFIN = 5 dBm, IF = 2000 MHz, LSB

SPURIOUS PERFORMANCE, USB

T_A = 25°C, V_{GMIX} = −1 V, V_{DAMPx} = 4 V, V_{DMULT} = 1.5 V, LO = 2 dBm.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) + (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 82 GHz

IF = 500 MHz at IFIN = 5 dBm, LO = 13.583 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	22.1
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	37.7
	3	N/A	N/A	N/A	N/A	N/A	N/A	54.5
	4	N/A	N/A	N/A	N/A	N/A	N/A	59.5
	5	N/A	N/A	N/A	N/A	N/A	N/A	58.6

IF = 1000 MHz at IFIN = 5 dBm, LO = 13.5 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	22.8
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	31.6
	3	N/A	N/A	N/A	N/A	N/A	N/A	32.5
	4	N/A	N/A	N/A	N/A	N/A	N/A	32.1
	5	N/A	N/A	N/A	N/A	N/A	N/A	31.6

IF = 2000 MHz at IFIN = 5 dBm, LO = 13.333 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	29.7
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	31.5
	3	N/A	N/A	N/A	N/A	N/A	N/A	30.5
	4	N/A	N/A	N/A	N/A	N/A	N/A	29.5
	5	N/A	N/A	N/A	N/A	N/A	N/A	28.9

M × N Spurious Output, RF = 85 GHz

IF = 500 MHz at IFIN = 5 dBm, LO = 14.083 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	15.8
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	38.3
	3	N/A	N/A	N/A	N/A	N/A	N/A	60.5
	4	N/A	N/A	N/A	N/A	N/A	N/A	59.7
	5	N/A	N/A	N/A	N/A	N/A	N/A	60.8

IF = 1000 MHz at IFIN = 5 dBm, LO = 14 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	15.7
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	32.5
	3	N/A	N/A	N/A	N/A	N/A	N/A	31.7
	4	N/A	N/A	N/A	N/A	N/A	N/A	29.7
	5	N/A	N/A	N/A	N/A	N/A	N/A	30.2

IF = 2000 MHz at IFIN = 5 dBm, LO = 13.833 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	17.2
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	30.4
	3	N/A	N/A	N/A	N/A	N/A	N/A	29.7
	4	N/A	N/A	N/A	N/A	N/A	N/A	30
	5	N/A	N/A	N/A	N/A	N/A	N/A	28.6

SPURIOUS PERFORMANCE, LSB

T_A = 25°C, V_{GMIX} = −1 V, V_{DAMPx} = 4 V, V_{DMULT} = 1.5 V, LO = 2 dBm.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) − (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 82 GHz

IF = 500 MHz at IFIN = 5 dBm, LO = 13.75 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	64.4	N/A	54.2	N/A	N/A	19.4
	1	63.4	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	38.4
	3	N/A	N/A	N/A	N/A	N/A	N/A	59
	4	N/A	N/A	N/A	N/A	N/A	N/A	61.3
	5	N/A	N/A	N/A	N/A	N/A	N/A	61.4

IF = 1000 MHz at IFIN = 5 dBm, LO = 13.833 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	17.2
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	42.2
	3	N/A	N/A	N/A	N/A	N/A	N/A	60.1
	4	N/A	N/A	N/A	N/A	N/A	N/A	62
	5	N/A	N/A	N/A	N/A	N/A	N/A	58.7

IF = 2000 MHz at IFIN = 5 dBm, LO = 14 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	17.2
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	49.3
	3	N/A	N/A	N/A	N/A	N/A	N/A	55.9
	4	N/A	N/A	N/A	N/A	N/A	N/A	65.2
	5	N/A	N/A	N/A	N/A	N/A	N/A	64.4

M × N Spurious Outputs, RF = 85 GHz

IF = 500 MHz at IFIN = 5 dBm, LO = 14.25 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	56.9	N/A	57.3	N/A	N/A	19.5
	1	63.45	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	38.8
	3	N/A	N/A	N/A	N/A	N/A	N/A	61.4
	4	N/A	N/A	N/A	N/A	N/A	N/A	61.8
	5	N/A	N/A	N/A	N/A	N/A	N/A	59.2

IF = 1000 MHz at IFIN = 5 dBm, LO = 14.333 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	17.1
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	42.5
	3	N/A	N/A	N/A	N/A	N/A	N/A	59.6
	4	N/A	N/A	N/A	N/A	N/A	N/A	58.9
	5	N/A	N/A	N/A	N/A	N/A	N/A	59.9

IF = 2000 MHz at IFIN = 5 dBm, LO = 14.5 GHz at LOIN = 2 dBm.

		N × LO						
		0	1	2	3	4	5	6
M × IF	0	N/A	N/A	N/A	N/A	N/A	N/A	18.7
	1	N/A	N/A	N/A	N/A	N/A	N/A	0.00
	2	N/A	N/A	N/A	N/A	N/A	N/A	49.7
	3	N/A	N/A	N/A	N/A	N/A	N/A	60.2
	4	N/A	N/A	N/A	N/A	N/A	N/A	60.6
	5	N/A	N/A	N/A	N/A	N/A	N/A	63.2

THEORY OF OPERATION

The HMC8119 is a GaAs I/Q upconverter with an integrated LO buffer and 6× multiplier. See Figure 79 for a functional block diagram of the circuit architecture. The 6× multiplier allows the use of a lower frequency range LO input signal, typically between 11.83 GHz and 14.33 GHz. The 6× multiplier is implemented using a cascade of 3× and 2× multipliers. LO buffer amplifiers are included on chip to allow a typical LO drive level of only 2 dBm for full performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the I and Q mixer cores. The mixer cores comprise singly balanced passive mixers. The RF outputs of the I and Q mixers are then summed through an on-chip Wilkinson power combiner and reactively matched to provide a single-ended 50 Ω output signal at the RFOUT pad.

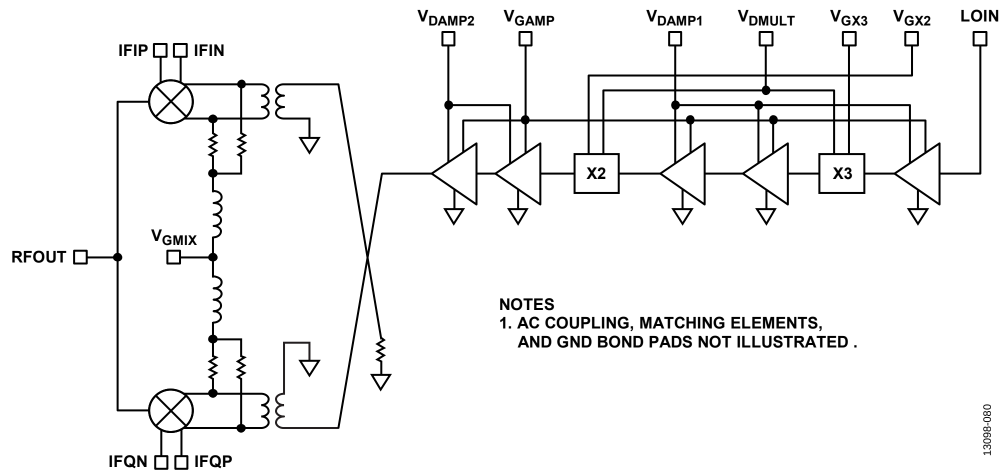

Figure 79. Upconverter Circuit Architecture

APPLICATIONS INFORMATION

BIASING SEQUENCE

The HMC8119 uses several amplifier and multiplier stages in the LO signal path. The active stages all use depletion mode pseudomorphic high electron mobility transistors (pHEMTs). To ensure transistor damage does not occur, use the following power-up bias sequence:

1. Apply a −2 V bias to V_{GAMP}, V_{GX2}, and V_{GX3}.
2. Apply a −1 V bias to V_{GMIX}.
3. Apply 4 V to V_{DAMP1} and V_{DAMP2}, and apply 1.5 V to V_{DMULT}.
4. Adjust V_{GAMP} between −2 V and 0 V to achieve a total amplifier drain current (I_{DAMP1} + I_{DAMP2}) of 175 mA.
5. Apply a LO input signal and adjust V_{GX2} and V_{GX3} between −2 V and 0 V to achieve 80 mA of drain current on V_{DMULT}.

To power down the HMC8119, follow the reverse procedure.

For additional guidance on general bias sequencing, see the *MMIC Amplifier Biasing Procedure* application note.

SINGLE SIDEBAND UPCONVERSION

A typical single-sideband upconversion circuit is shown in Figure 80. For single-sideband upconversions, an external 90° hybrid splits the IF signal into quadrature terms. Then 180° hybrids or baluns transfer differential signals to the I and Q input pairs. Use an optional bias tee network to allow the application of small dc offsets on the IFIP, IFIN, IFQP, and IFQN input pads. By applying dc offsets to the I/Q mixer cores, the 6× LO to RF leakage can be somewhat improved. However, it is important to current limit the applied dc bias to avoid sourcing or sinking more than ±3 mA of bias current. Depending on the bias sources used, it may be prudent to add series resistance to ensure the applied bias current does not exceed ±3 mA. For applications not requiring enhanced LO suppression, omit the bias tee and then dc couple the I/Q inputs to the 180° hybrids.

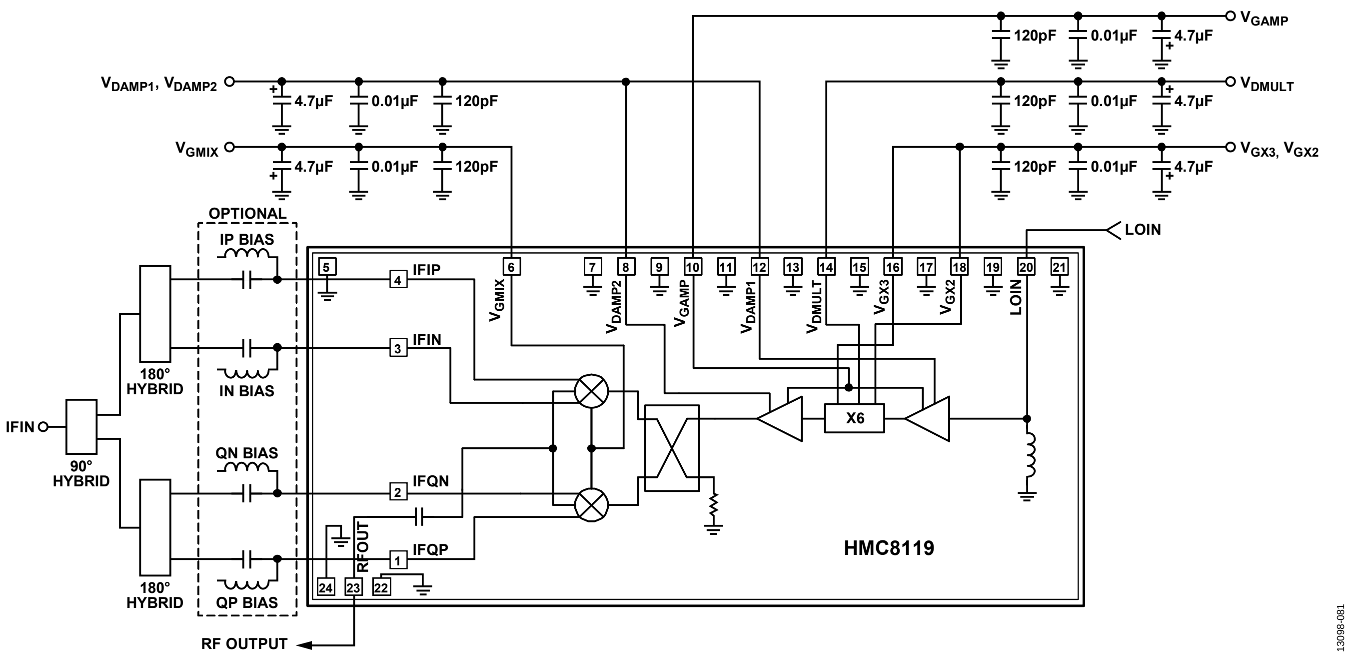

Figure 80. Single-Sideband Upconversion Configuration with Optional DC Bias Tee Network for Enhanced LO Suppression

Zero IF Direct Conversion

A zero IF direct conversion application circuit is shown in Figure 81. An optional bias tee network is included for applications requiring additional LO suppression correction. When omitting the bias tee configuration, it is still important to ac couple the IFIP, IFIN, IFQP, and IFQN pads to the DAC outputs. Most DACs are designed to operate with a common-mode voltage that is above ground. The HMC8119 I/Q inputs are ground referenced and dc coupling to a differential signal source with a common-mode output voltage other than 0 V may cause degraded RF performance and possible device damage from electrical overstress.

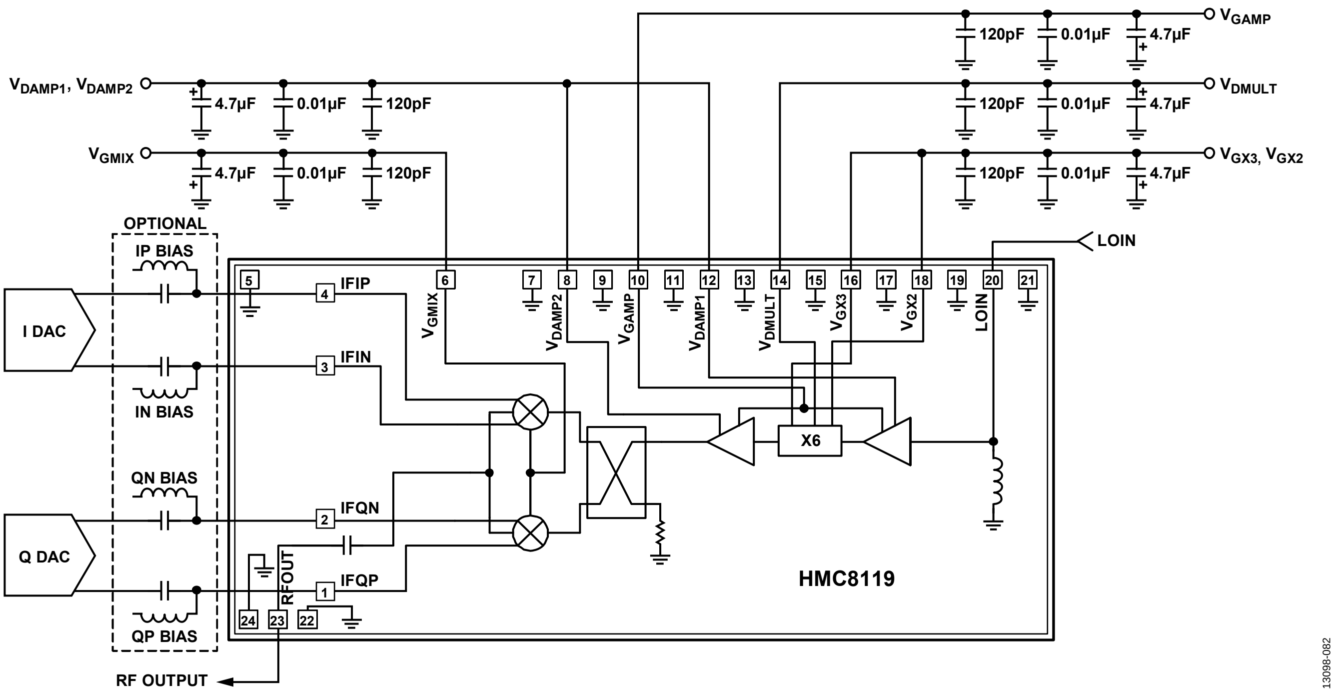

Figure 81. Zero IF Direct Conversion Application Circuit with Optional Bias Tee Network for Enhanced LO Suppression

ASSEMBLY DIAGRAM

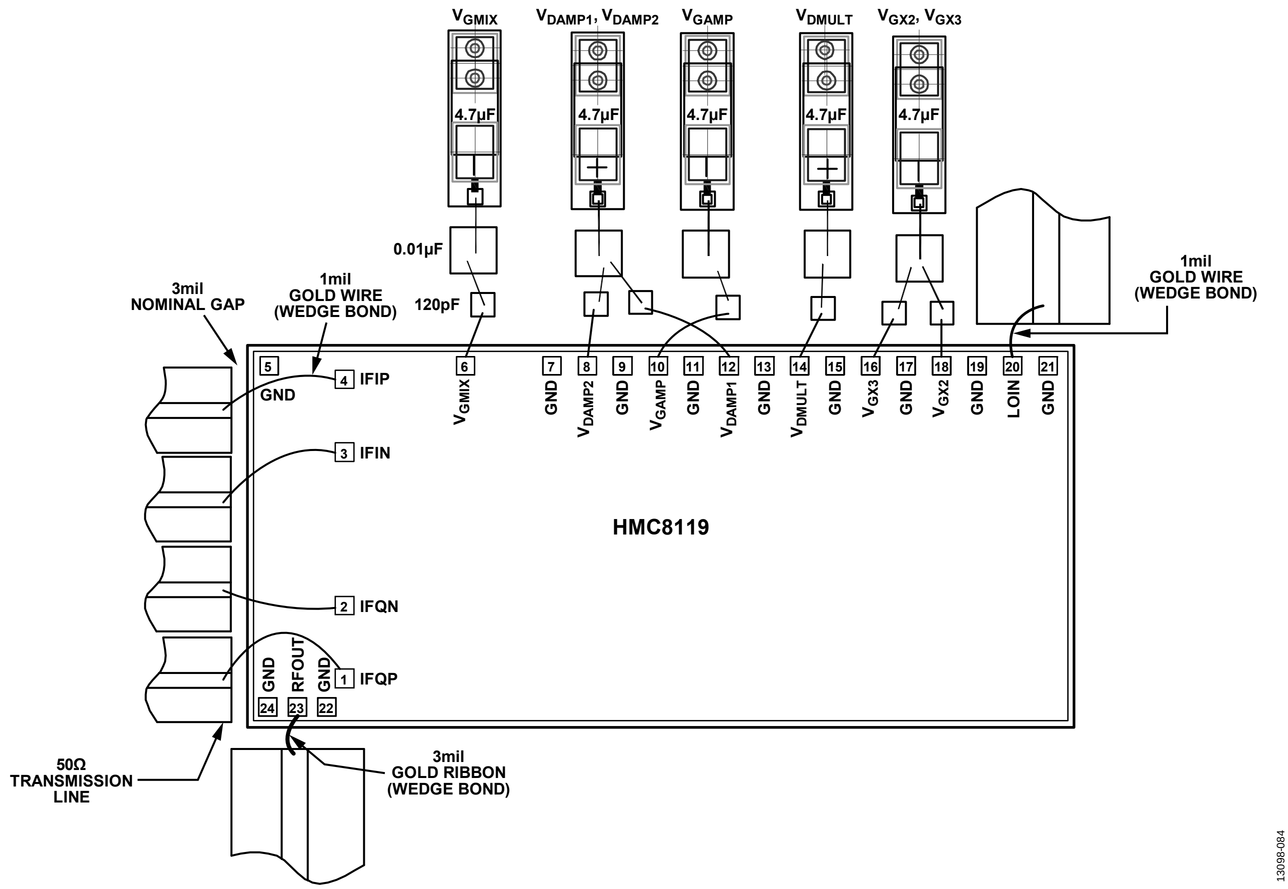

Figure 82. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 83).

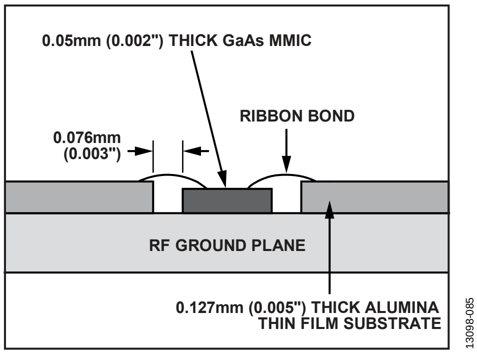

Figure 83. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the following storage, cleanliness, static sensitivity, transients, and general handling precautions.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80%/20% gold/tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90%/10% nitrogen/hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

ABLEBOND 84-1LMIT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 0.003 in. × 0.0005 in. gold ribbon are recommended for the RF port, and wedge bonds with 0.025 mm (1 mil) diameter gold wire are recommended for the IF and LO ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 0.001 in. (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

OUTLINE DIMENSIONS

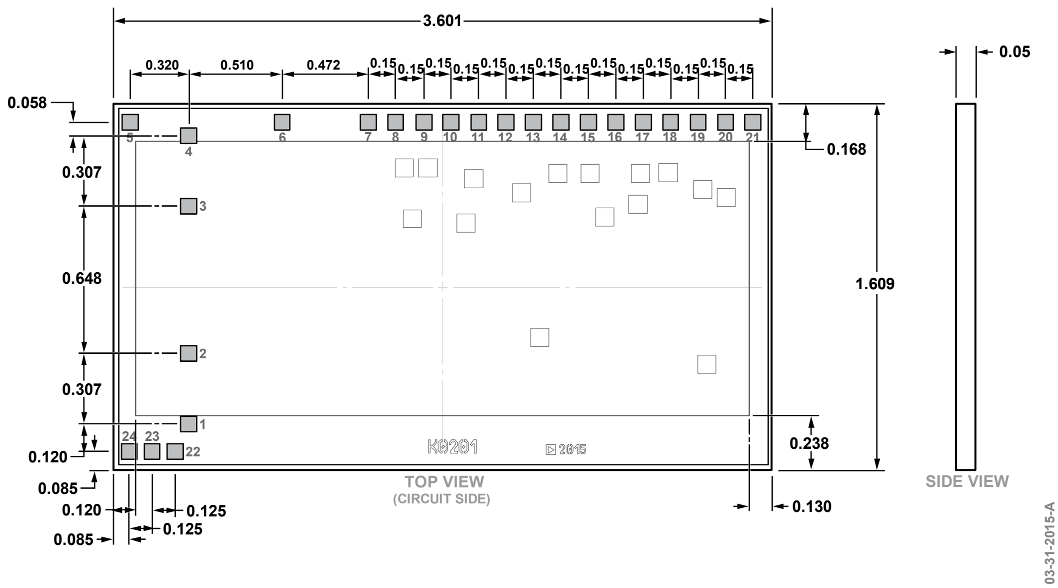

Figure 84. 24-Pad Bare Die [CHIP]
(C-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
HMC8119	−55°C to +85°C	24-Pad Bare Die [CHIP]	C-24-3
HMC8119-SX	−55°C to +85°C	24-Pad Bare Die [CHIP]	C-24-3

[1] The HMC8119-SX is two pairs of the die in a gel pack for the sample orders.
[2] This is a waffle pack option; contact Analog Devices, Inc., for additional packaging options.

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