

IS62C5128BL, IS65C5128BL

512K x 8 HIGH-SPEED CMOS STATIC RAM

JULY 2011

FEATURES

- High-speed access time: 45ns
- Low Active Power: 50 mW (typical)
- Low Standby Power: 10 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single 5V \pm 10% power supply
- Fully static operation: no clock or refresh required
- Available in 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

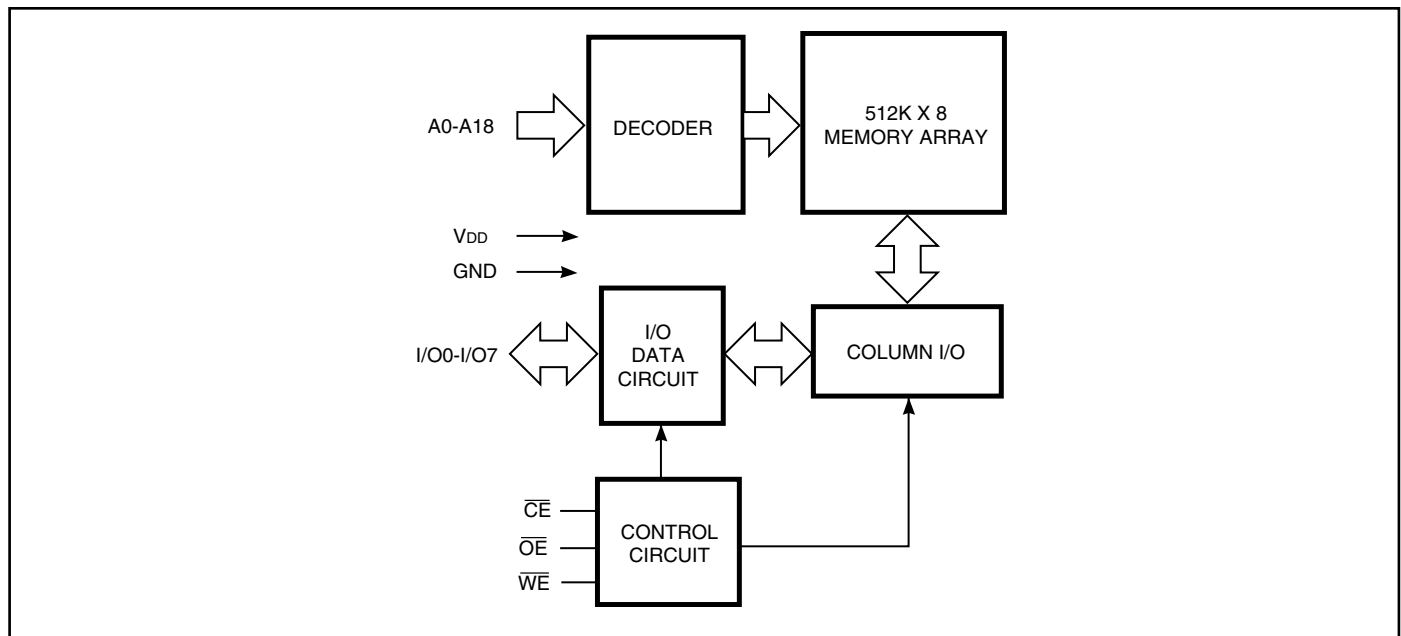
The *ISSI* IS62C5128BL and IS65C5128BL are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 45ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS62C5128BL and IS65C5128BL are packaged in the JEDEC standard 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages

FUNCTIONAL BLOCK DIAGRAM



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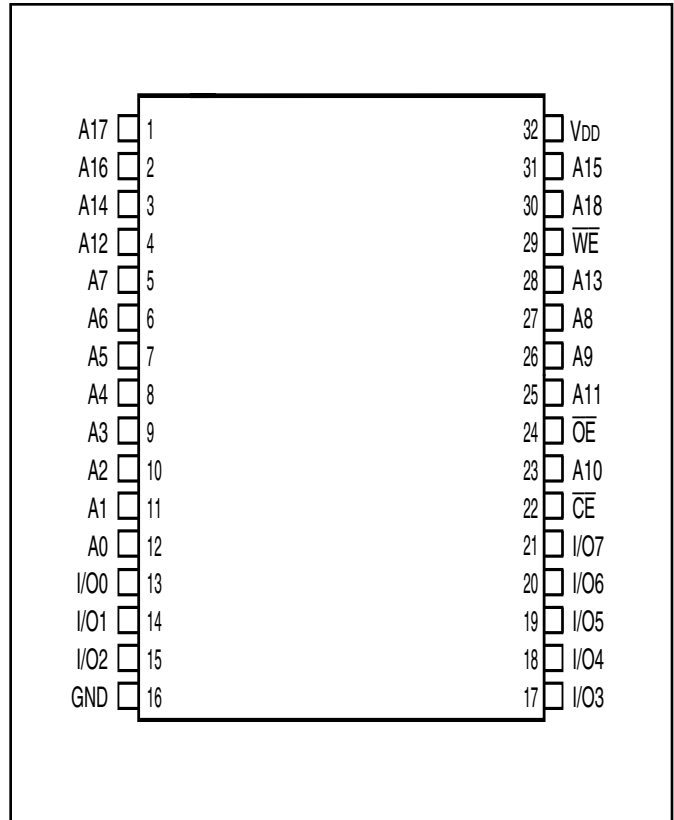
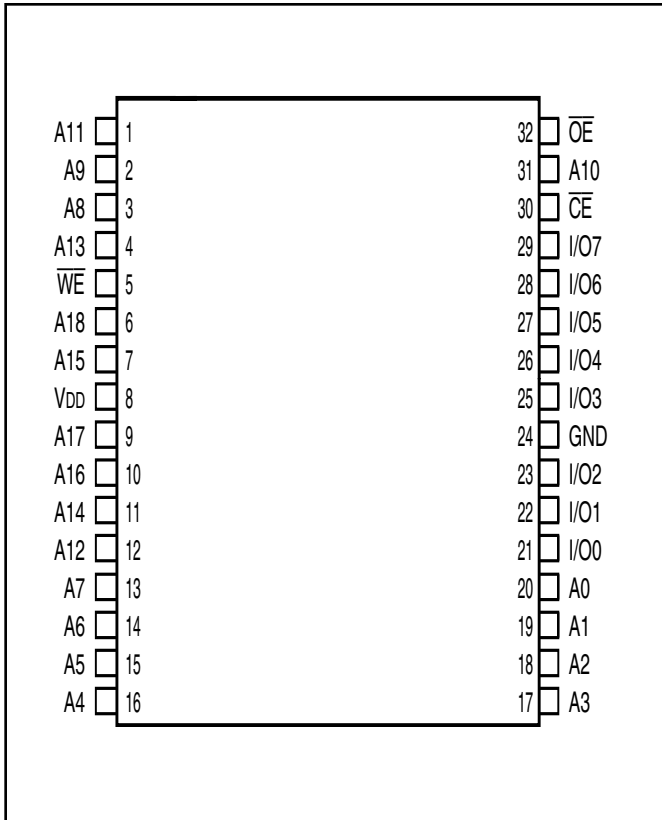
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATION

32-pin sTSOP (TYPE I)

**32-pin SOP
32-pin TSOP (TYPE II)**



PIN DESCRIPTIONS

| | |
|-----------|---------------------|
| A0-A18 | Address Inputs |
| CE | Chip Enable 1 Input |
| OE | Output Enable Input |
| WE | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| VDD | Power |
| GND | Ground |

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | I/O0-I/O7 | I/O PIN |
|-----------------|-----------------|-----------------|-----------------|------------------|-------------------------------------|
| | | | | | V _{DD} Current |
| Not Selected | X | H | X | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | High-Z | I _{CC1} , I _{CC2} |
| Read | H | L | L | D _{OUT} | I _{CC1} , I _{CC2} |
| Write | L | L | X | D _{IN} | I _{CC1} , I _{CC2} |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|--------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.5 | W |
| I _{OUT} | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit | |
|-----------------|-----------------------------------|--|-----------------------|-----------------------|-------------|----|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1.0 mA | 2.4 | — | V | |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 2.1 mA | — | 0.4 | V | |
| V _{IH} | Input HIGH Voltage ⁽¹⁾ | | 2.2 | V _{DD} + 0.5 | V | |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V | |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | Com. Ind. Auto. | -1 -2 -5 | 1 2 5 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} Outputs Disabled | Com. Ind. Auto. | -1 -2 -5 | 1 2 5 | μA |

Note:

1. V_{ILL} (min) = -2.0V AC (pulse width <10 ns). Not 100% tested.
V_{IHH} (max) = V_{DD} + 2.0V AC (pulse width <10 ns). Not 100% tested.

OPERATING RANGE

| Range | Ambient Temperature | V _{DD} | Speed (ns) |
|------------|---------------------|-----------------|------------|
| Commercial | 0°C to +70°C | 5V ± 10% | 45 |
| Industrial | -40°C to +85°C | 5V ± 10% | 45 |
| Automotive | -40°C to +125°C | 5V ± 10% | 45 |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -45 ns | | Unit |
|------------------|--|---|---------------------|--------|------|------|
| | | | | Min. | Max. | |
| I _{CC} | Average operating Current | $\overline{CE} = V_{IL}, V_{DD} = \text{Max.}$ $I_{OUT} = 0 \text{ mA}, f = 0$ | Com. | — | 10 | mA |
| | | | Ind. | — | 10 | |
| | | | Auto. | — | 10 | |
| I _{CC1} | V _{DD} Dynamic Operating Supply Current | $V_{DD} = \text{Max.}, \overline{CE} = V_{IL}$ $I_{OUT} = 0 \text{ mA}, f = f_{MAX}$ | Com. | — | 15 | mA |
| | | | Ind. | — | 20 | |
| | | | Auto. | — | 25 | |
| | | | typ. ⁽²⁾ | | 10 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | $V_{DD} = \text{Max.},$ $V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH},$ $f = 0$ | Com. | — | 1 | mA |
| | | | Ind. | — | 1.5 | |
| | | | Auto. | — | 2 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | $V_{DD} = \text{Max.},$ $\overline{CE} \geq V_{DD} - 0.2V,$ $V_{IN} \geq V_{DD} - 0.2V,$ or $V_{IN} \leq V_{SS} + 0.2V, f = 0$ | Com. | — | 10 | μA |
| | | | Ind. | — | 15 | |
| | | | Auto. | — | 35 | |
| | | | typ. | | 4 | |

Note:

- At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, $f = 0$ means no input lines change.
- Typical values are measured at $V_{DD} = 5V, T_A = 25^\circ\text{C}$ and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -45 | | Unit |
|---------------------------------|----------------------------------|------|------|------|
| | | Min. | Max. | |
| t _{RC} | Read Cycle Time | 45 | — | ns |
| t _{AA} | Address Access Time | — | 45 | ns |
| t _{OHA} | Output Hold Time | 3 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 45 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 20 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | 0 | 15 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 5 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 15 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 5 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

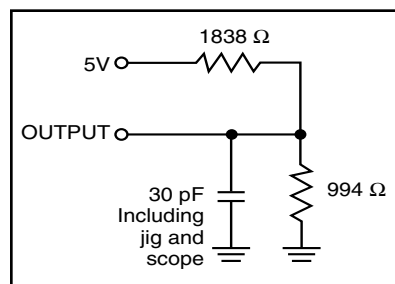
AC TEST LOADS


Figure 1

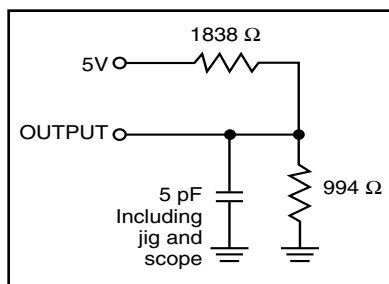
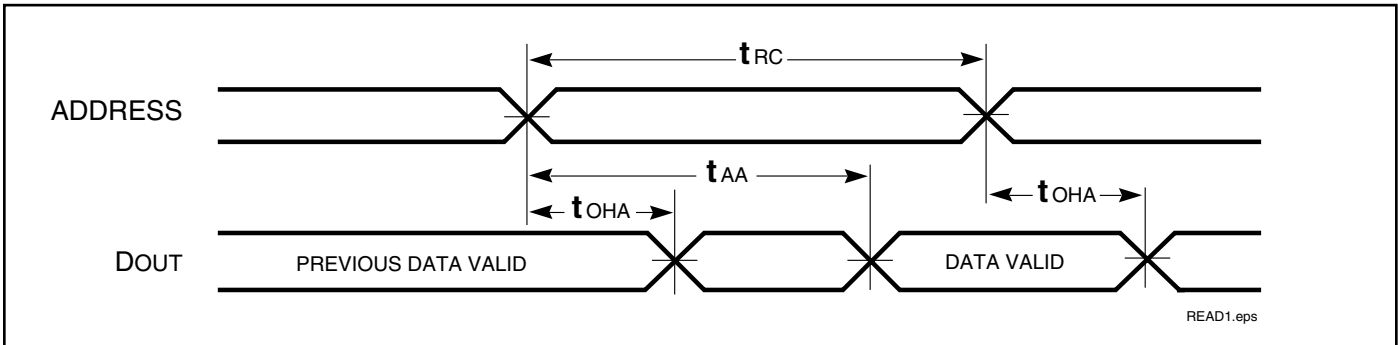
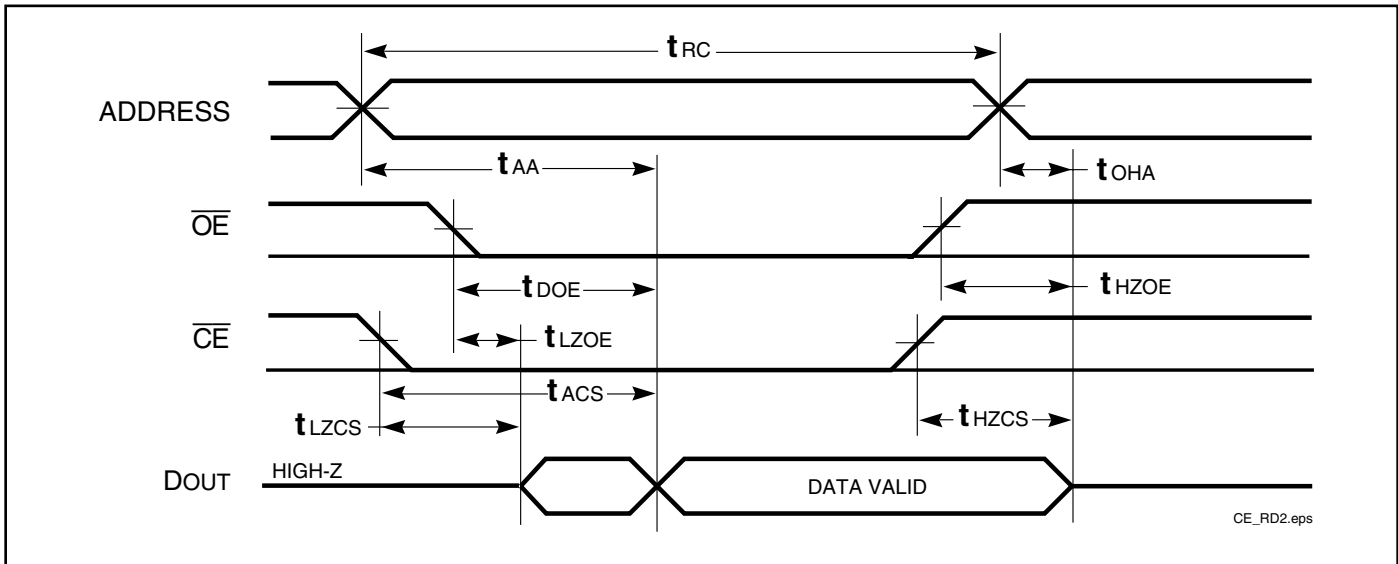


Figure 2

AC WAVEFORMS
READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

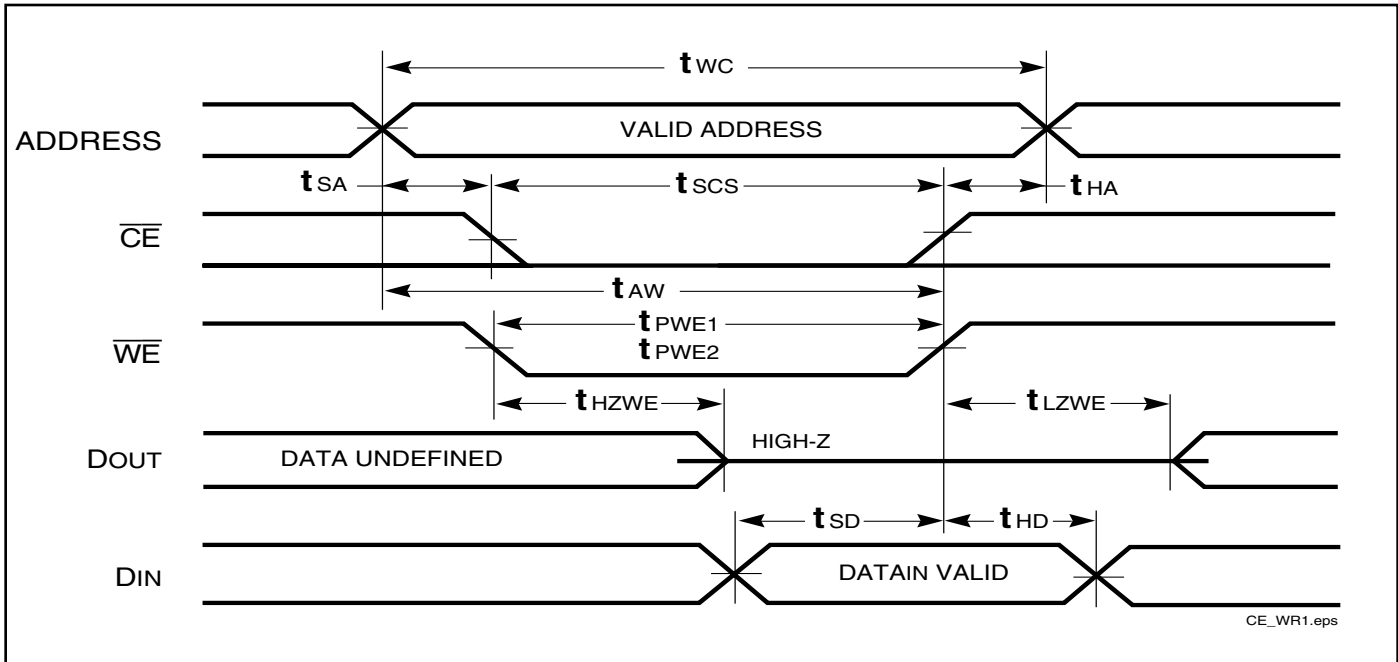
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -45 | | Unit |
|---------------------------------|--|------|------|------|
| | | Min. | Max. | |
| t _{WC} | Write Cycle Time | 45 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 35 | — | ns |
| t _{AW} | Address Setup Time to Write End | 35 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} =High) | 35 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} =Low) | 35 | — | ns |
| t _{SD} | Data Setup to Write End | 25 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 15 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 5 | — | ns |

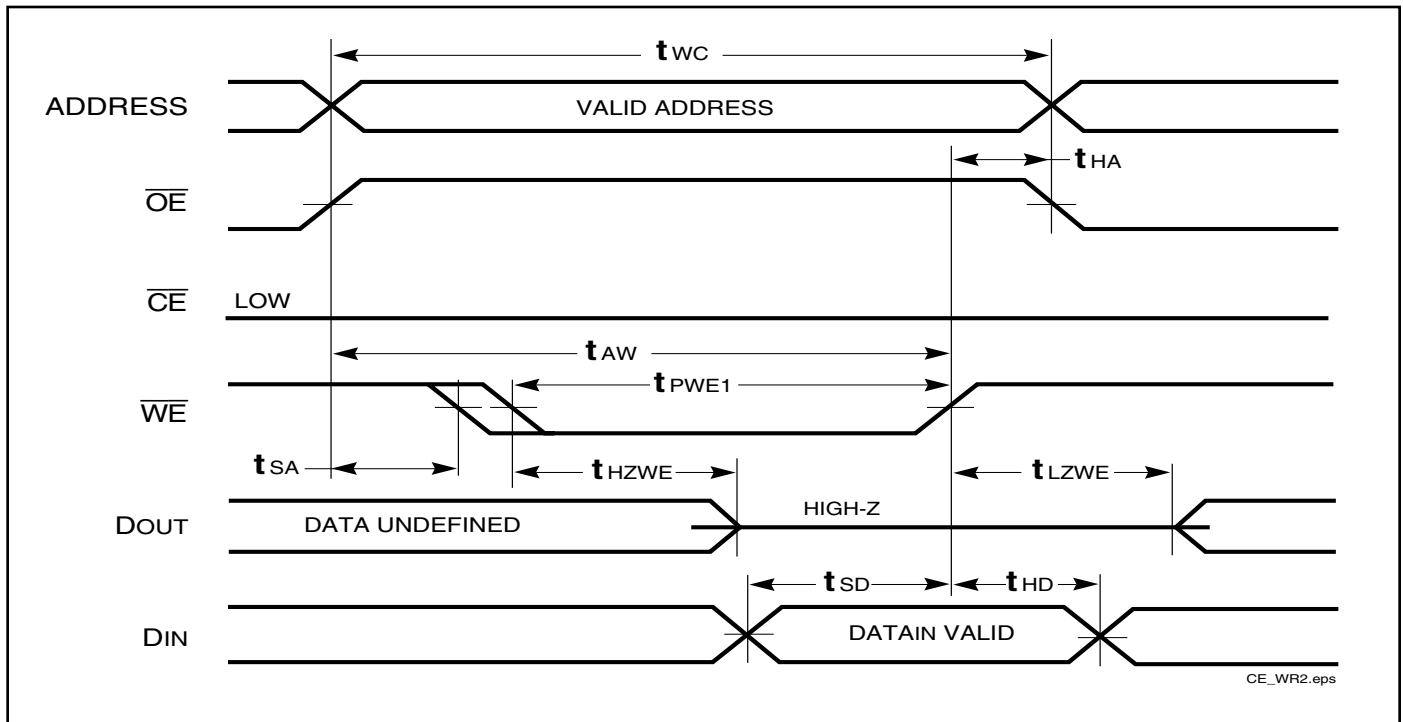
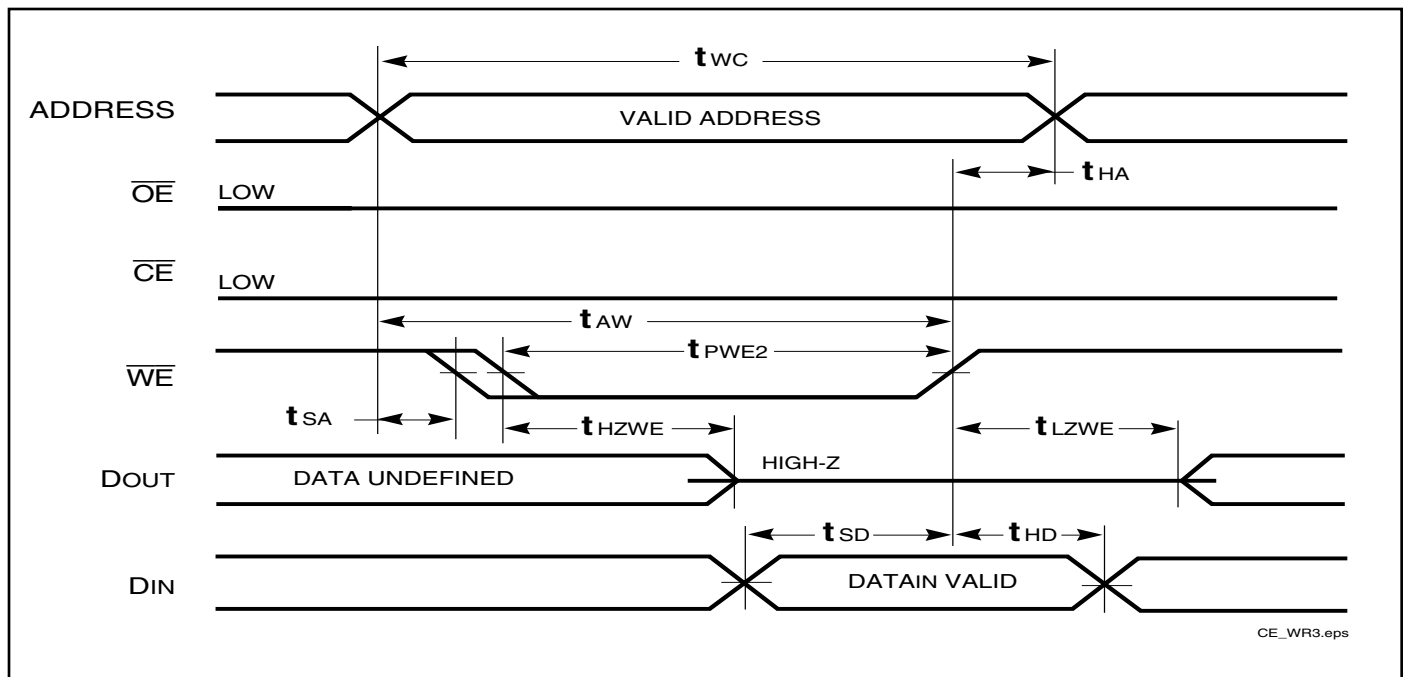
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)**Notes:**

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)

WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾

Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

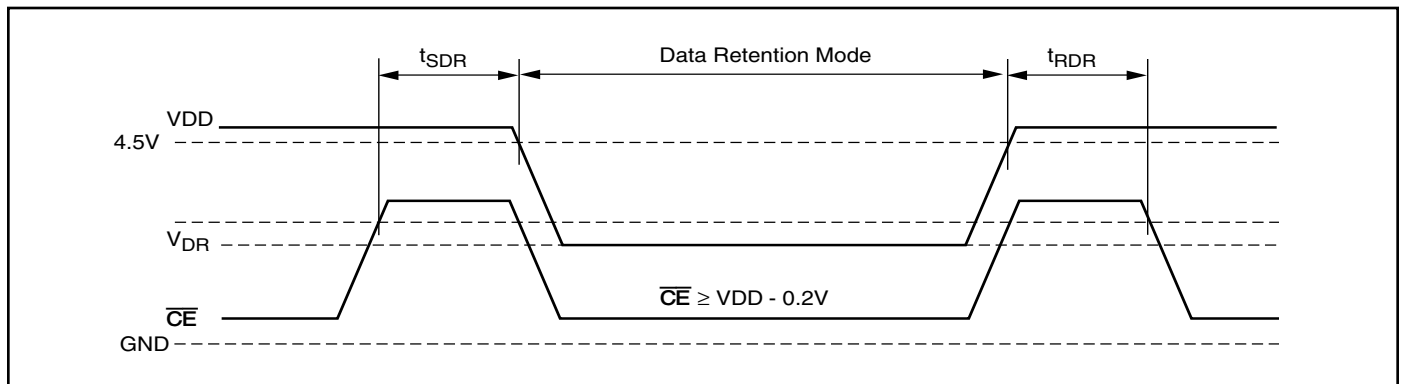
DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Max. | Unit | |
|------------------|------------------------------------|--|------------------------------|------|------|---------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 2.0 | 5.5 | V | |
| I _{DR} | Data Retention Current | V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. | — | 10 | μA |
| | | V _{IN} $\geq V_{DD} - 0.2V$, or V _{IN} $\leq V_{SS} + 0.2V$ | Ind. | — | 15 | |
| | | | Auto. typ. ⁽¹⁾ | — | 35 | |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | — | ns | |
| t _{RDR} | Recovery Time | See Data Retention Waveform | t _{RC} | — | ns | |

Note:

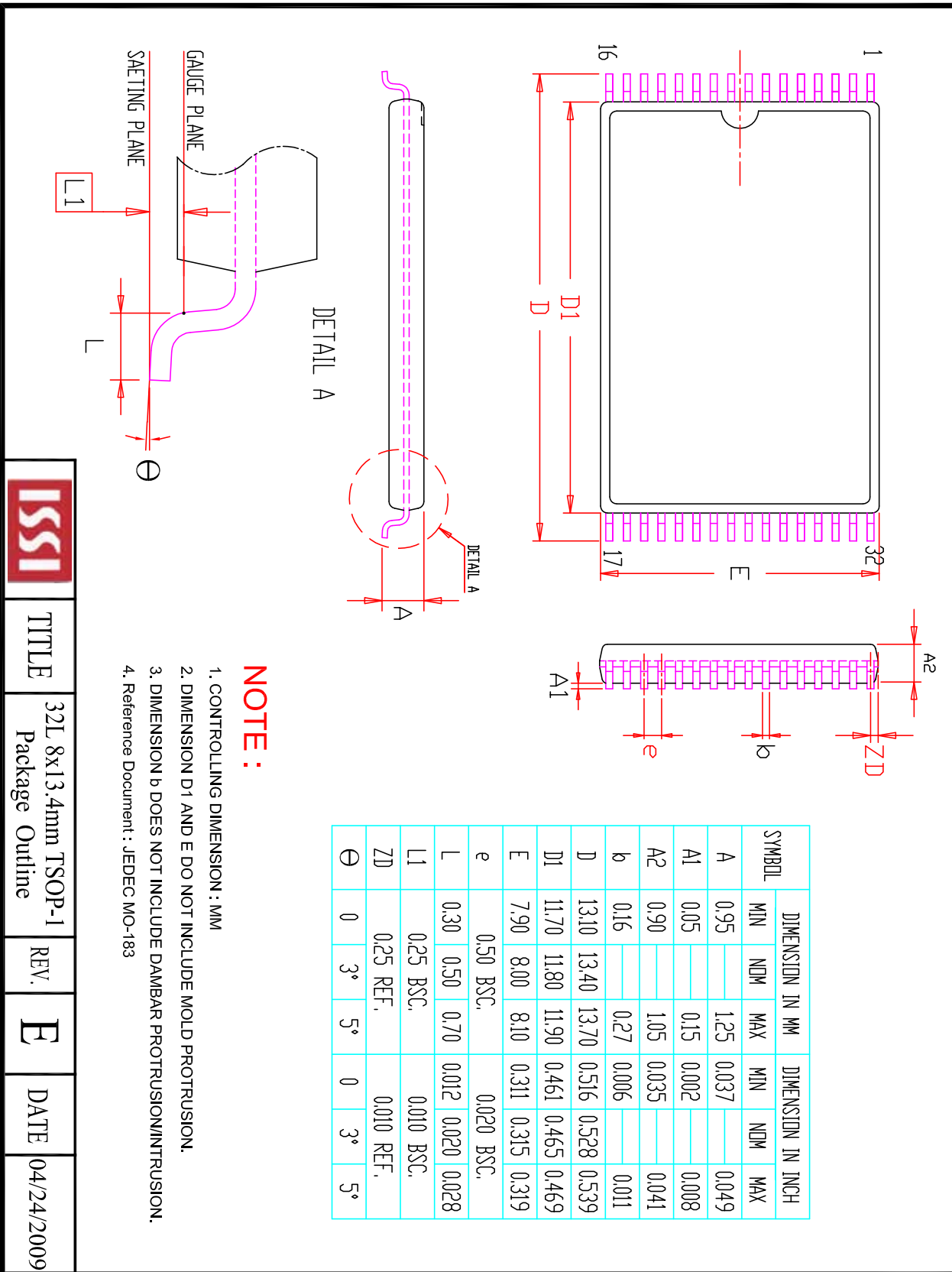
1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

| Speed (ns) | Order Part No. | Package |
|-------------------|-----------------------|--------------------------------|
| 45 | IS62C5128BL-45QI | 450-mil Plastic SOP |
| | IS62C5128BL-45QLI | 450-mil Plastic SOP, Lead-free |
| | IS62C5128BL-45HI | 32-pin STSOP-I |
| | IS62C5128BL-45HLI | 32-pin STSOP-I, Lead-free |
| | IS62C5128BL-45TI | 32-pin TSOP-II |
| | IS62C5128BL-45TLI | 32-pin TSOP-II, Lead-free |



TITLE

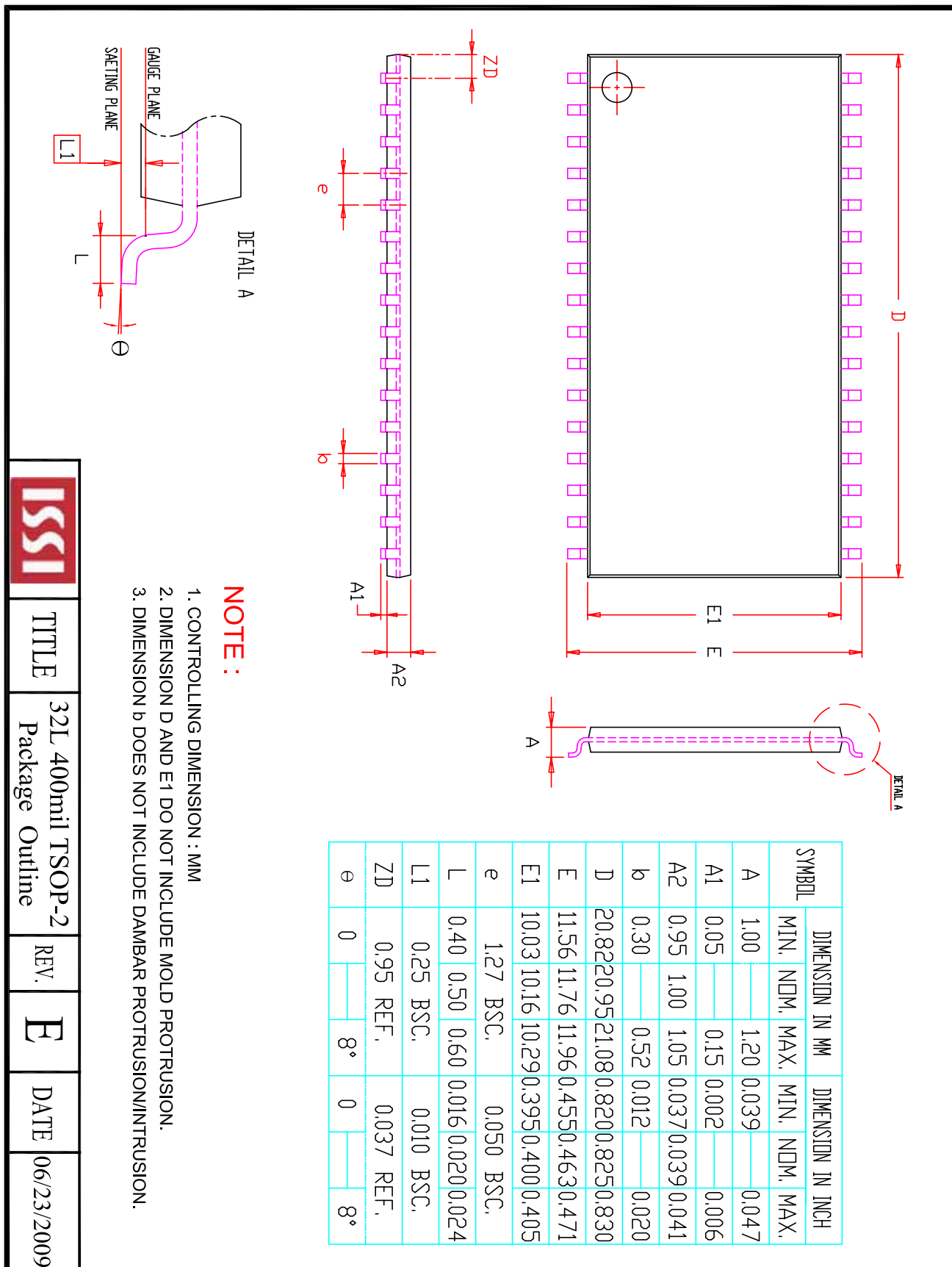
32L 8x13.4mm TSOP-1
Package Outline

REV.

E

DATE

04/24/2009



TITLE

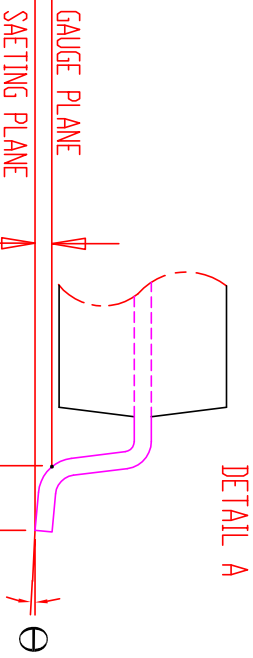
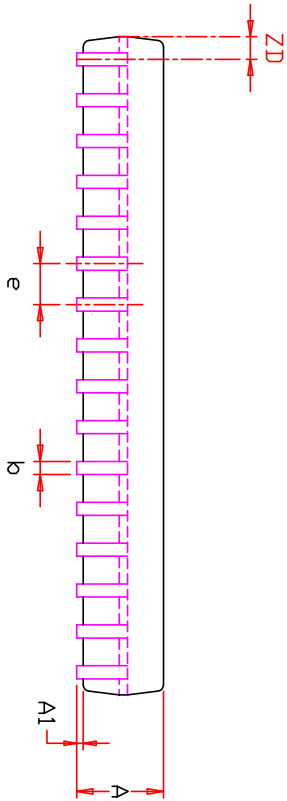
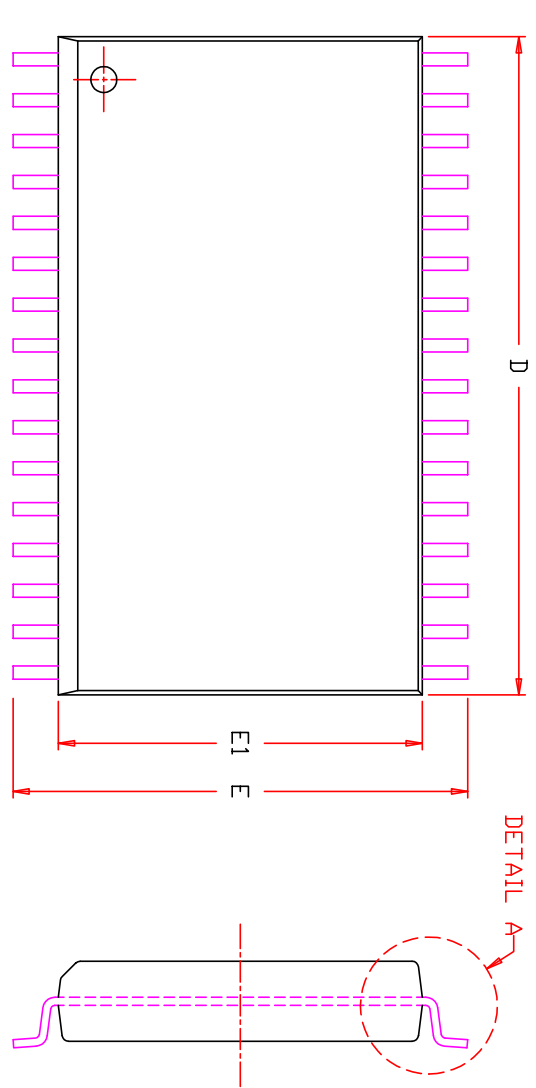
32L 400mil TSOP-2
Package Outline

REV.

E

DATE

06/23/2009



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|------|------------|-------------------|------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 2.62 | | 3.12 | 0.103 | | 0.123 |
| A1 | 0.05 | | 0.30 | 0.002 | | 0.012 |
| b | 0.33 | | 0.51 | 0.013 | | 0.020 |
| D | 20.24 | | 20.750,797 | | | 0.817 |
| E | 13.79 | | 14.450,543 | | | 0.569 |
| E1 | 11.18 | | 11.43 | 0.440 | | 0.450 |
| e | 1.27 | BSC. | | 0.050 | BSC. | |
| L | 0.38 | | 1.27 | 0.015 | | 0.050 |
| L1 | 0.25 | BSC. | | 0.010 | BSC. | |
| ZD | 0.725 | REF. | | 0.029 | REF. | |
| ϕ | 0 | | 8° | 0 | | 8° |



TITLE

32L 450mil SOP
Package Outline

REV.

D

DATE

04/20/2009

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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