

# Micropower 8-Bit Current Output D/A Converter

## **FEATURES**

#### Guaranteed Precision Full-Scale DAC Output Current at 25°C:

LTC1329A-50 50μA ±1% LTC1329-10 10μA ±3% LTC1329-50 50μA ±3%

- Wide Output Voltage DC Compliance: -15V to 2.5V
- Wide Supply Range:  $2.7V \le V_{CC} \le 6.5V$
- Supply Current in Shutdown: 0.2µA
- Low Supply Current: 75μA for LTC1329-10, 95μA for LTC1329-50/LTC1329A-50
- Available in 8-Pin SO
- Triple Mode<sup>™</sup> Interface Modes
  - 1. Standard 3-Wire Mode
  - 2. Pulse Mode 1-Wire Interface: Increment-Only
  - 3. Pulse Mode 2-Wire Interface: Increment/Decrement
- Can Read Back the 8-Bit DAC Value in 3-Wire Mode
- DAC Powers Up at Midrange
- DAC Contents Are Retained in Shutdown

## **APPLICATIONS**

- LCD Contrast Control
- Backlight Brightness Control
- Battery Charger Current/Voltage Adjustment
- Power Supply Voltage Adjustment
- Trimmer Pot Elimination

### DESCRIPTION

The LTC  $^{\odot}$ 1329-10/LTC1329-50/LTC1329A-50 are micropower 8-bit current output D/A converters (DACs) with an output range of  $0\mu$ A to  $10\mu$ A for the LTC1329-10 and  $0\mu$ A to  $50\mu$ A for the LTC1329-50/LTC1329A-50. The DAC current output can be biased from -15V to 2V or -15V to 2.5V in 3.3V and 5V systems, respectively. Supply current is only  $95\mu$ A for the LTC1329-50/LTC1329A-50 and  $75\mu$ A for LTC1329-10. A shutdown mode drops the supply current to  $0.2\mu$ A.

The LTC1329 can communicate with external circuitry by using one of three interface modes: standard 3-wire serial mode and two pulse modes. Upon power-up, the internal counter resets to 1000 0000B, the DAC output assumes midrange and the chip is configured in 3-wire or pulse mode depending on the signal level at  $\overline{\text{CS}}$ .

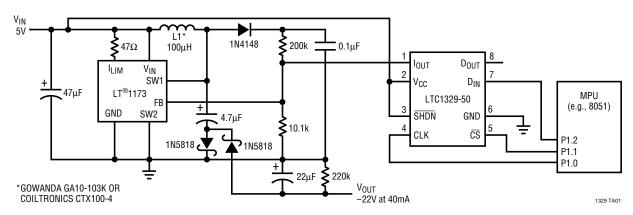
In 3-wire mode, the system MPU can serially transfer 8-bit data to and from the LTC1329. In pulse mode, the upper six bits of the DAC output can be programmed for increment-only (1-wire interface) or increment/decrement (2-wire interface) operation depending on the signal level at  $D_{\text{IN}}$ .

#### LTC1329 is available in 8-pin SO packages.

(7), LTC and LT are registered trademarks of Linear Technology Corporation. Triple Mode is a trademark of Linear Technology Corporation.

## TYPICAL APPLICATION

#### **Digitally Controlled LCD Bias Generator**

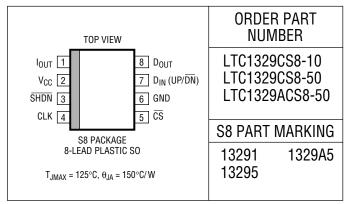




## **ABSOLUTE MAXIMUM RATINGS**

# 

## PACKAGE/ORDER INFORMATION



Consult factory for Industrial and Military grade parts.

## **ELECTRICAL CHARACTERISTICS** $V_{CC} = 3.3V$ , $T_A = 25^{\circ}C$ , unless otherwise specified.

SYMBOL	. PARAMETER	CONDITIONS		LTC1329-10 Min Typ Max		LTC1329-50/LTC1329A-50 MIN TYP MAX			UNITS	
V <sub>CC</sub>	TAHAMETEH	CONDITIONS		2.7	111	6.5	2.7	- 1111	6.5	V
ICC	Supply Current	$V_{\overline{SHDN}} = V_{DIN} = V_{\overline{CS}} = V_{CC}, V_{CLK} = 0V,$ $D_{OUT} = NC, I_{OUT} = NC$	•	<u> </u>	75	130	E.I	95	150	μА
		Shutdown	•		0.2	5		0.2	5	μΑ
	DAC Resolution				8			8		Bits
	DAC Full-Scale Current	Output Voltage at I <sub>OUT</sub> = 0.45V, T <sub>A</sub> = 25°C (LTC1329-10, LTC1329-50)	•	9.7 9.5	10 10	10.3 10.5	48.5 47.5	50 50	51.5 52.5	μA μA
		Output Voltage at $I_{OUT} = 0.45V$ , $T_A = 25^{\circ}C$ (LTC1329A-50)	•				49.5 49.0	50 50	50.5 51.0	μA μA
	DAC Zero-Scale Current	Output Voltage at I <sub>OUT</sub> = 0.45V	•			200			200	nA
	DAC Differential Nonlinearity	Monotonicity Guaranteed	•		±0.3	±0.9			±0.9	LSB
	Supply Voltage Rejection	V <sub>CC</sub> = 3V to 5.5V, I <sub>OUT</sub> = Full Scale, Output Voltage at I <sub>OUT</sub> = 0.45V	•		±1	±2		±1	±2	LSB
		V <sub>CC</sub> = 2.7V to 6.5V, Full Scale, Output Voltage at I <sub>OUT</sub> = 0.45V	•		±2.5	±4		±2.5	±4	LSB
	Output Voltage Rejection	V <sub>CC</sub> = 5V, I <sub>OUT</sub> = Full Scale, Output Voltage at I <sub>OUT</sub> = -15V to 0V	•		±0.25	±1			±0.25	LSB
		V <sub>CC</sub> = 5V, I <sub>OUT</sub> = Full Scale, Output Voltage at I <sub>OUT</sub> = 0V to 2.5V	•			±1.5			±1.5	LSB
I <sub>IH</sub> , I <sub>IL</sub>	Logic Input Current	$0V \le V_{IN} \le V_{CC}$	•			±1			±1	μΑ
V <sub>IH</sub>	High Level Input Voltage	V <sub>CC</sub> = 5V V <sub>CC</sub> = 3.3V	•	2.0 1.9			2.0 1.9			V
V <sub>IL</sub>	Low Level Input Voltage	V <sub>CC</sub> = 5V V <sub>CC</sub> = 3.3V	•			0.80 0.45			0.80 0.45	V
V <sub>OH</sub>	High Level Output Voltage	$V_{CC} = 5V, I_0 = 400\mu A$ $V_{CC} = 3.3V, I_0 = 400\mu A$	•	2.4 2.1			2.4 2.1			V
$\overline{V_{0L}}$	Low Level Output Voltage	$V_{CC} = 5V, I_0 = 2mA$ $V_{CC} = 3.3V, I_0 = 1mA$	•			0.4 0.4			0.4 0.4	V
I <sub>OZ</sub>	Three-State Output Leakage	$V_{\overline{CS}} = V_{CC}$	•			±5			±5	μА

# **RECOMMENDED OPERATING CONDITIONS** $V_{CC} = 3.3V$ , unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Int	Serial Interface						
f <sub>CLK</sub>	Clock Frequency		•			2	MHz
t <sub>CKS</sub>	Setup Time, CLK↓ Before $\overline{\text{CS}}$ ↓		•	150			ns
tcss	Setup Time, <del>CS</del> ↓ Before CLK↑		•	400			ns
$t_{DV}$	CS↓ to D <sub>OUT</sub> Valid	See Test Circuits	•	150			ns
t <sub>DS</sub>	D <sub>IN</sub> Setup Time Before CLK↑		•	150			ns
t <sub>DH</sub>	D <sub>IN</sub> Hold Time After CLK↑		•	150			ns
t <sub>DO</sub>	CLK↓ to D <sub>OUT</sub> Valid	See Test Circuits	•	150			ns
t <sub>CKHI</sub>	CLK High Time		•	200			ns
t <sub>CKLO</sub>	CLK Low Time		•	250			ns
tcsh	CLK↓ Before CS↑		•	150			ns
$t_{DZ}$	CS↑ to D <sub>OUT</sub> in Hi-Z	See Test Circuits	•			400	ns
t <sub>CKH</sub>	CS↑ Before CLK↑		•			400	ns
tcslo	CS Low Time	f <sub>CLK</sub> = 2MHz (Note 4)	•	4550			ns
		V <sub>CLK</sub> = 0V	•	400			ns
t <sub>cshi</sub>	CS High Time		•	400	·	·	ns

The ● denotes specifications which apply over the full operating temperature range.

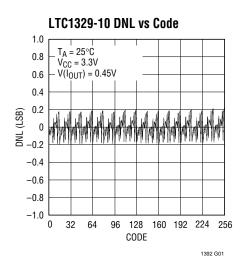
**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

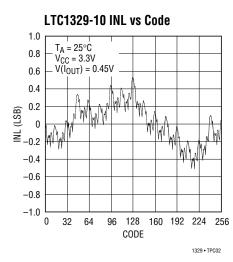
**Note 2:** Timing for all input signals is measured at 0.8V for a High-to-Low transition and at 2V for a Low-to-High transition.

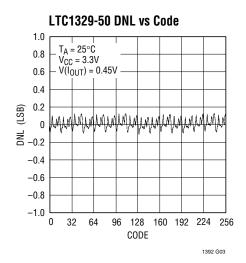
**Note 3:** Timing specification are guaranteed but not tested.

Note 4: This is the minimum time required for valid data transfer.

## TYPICAL PERFORMANCE CHARACTERISTICS

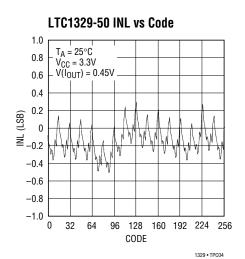


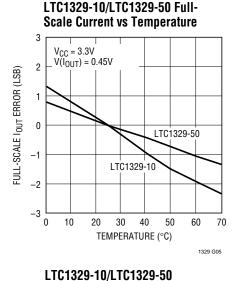


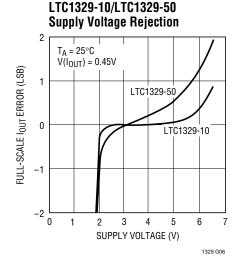




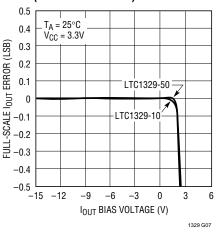
### TYPICAL PERFORMANCE CHARACTERISTICS

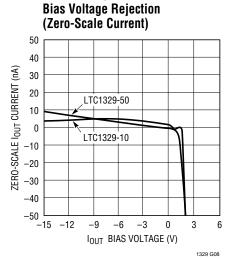


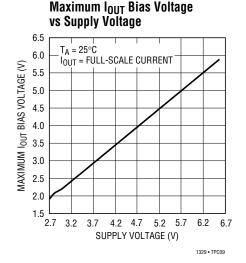




LTC1329-10/LTC1329-50 Bias Voltage Rejection (Full-Scale Current)







## PIN FUNCTIONS

 $I_{OUT}$  (Pin 1): DAC Current Output. In 3.3V or 5V systems, the DAC current output can be biased from -15V to 2V or -15V to 2.5V respectively.

 $V_{CC}$  (Pin 2): Voltage Supply (2.7V  $\leq$  V<sub>CC</sub>  $\leq$  6.5V). This supply must be kept free from noise and ripple by bypassing directly to the ground plane.

**SHDN (Pin 3):** Shutdown. A logic low puts the chip into Shutdown mode. The digital setting for the DAC is retained.

**CLK (Pin 4):** Shift Clock. This clock synchronizes the serial data in 3-wire mode. This pin has a Schmitt trigger input.

**CS** (**Pin 5**): Chip Select Input. In 3-wire mode, a logic low on this  $\overline{CS}$  pin enables the LTC1329. Upon power-up, a logic high at  $\overline{CS}$  puts the chip into pulse mode. If  $\overline{CS}$  ever goes low, the chip is configured in 3-wire mode until the next power is cycled.

**GND (Pin 6):** Ground. Ground should be tied directly to a ground plane.

 $D_{IN}$  (UP/ $\overline{DN}$ )(Pin 7): Data Input. In 3-wire mode, the DAC data is shifted into  $D_{IN}$  on the rising edge of CLK. In pulse mode, upon power-up a logic high at  $D_{IN}$  puts the counter into increment-only mode. If  $D_{IN}$  ever goes low, the

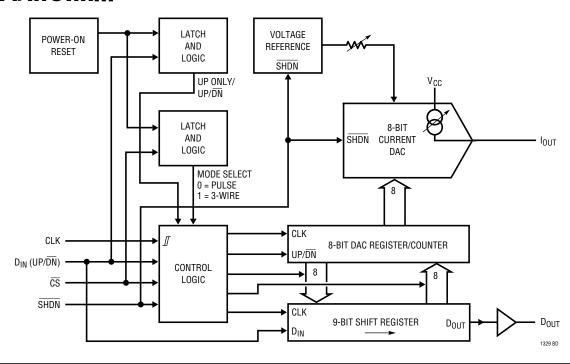
4

## PIN FUNCTIONS

counter is configured in increment/decrement mode until the power is cycled.

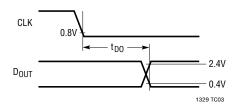
 $\mathbf{D_{OUT}}$  (Pin 8): Data Output. In 3-wire mode, on every conversion  $\mathbf{D_{OUT}}$  serially outputs the previous 8-bit DAC data. In pulse mode,  $\mathbf{D_{OUT}}$  is three-stated.

## **BLOCK DIAGRAM**

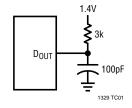


## **TEST CIRCUITS**

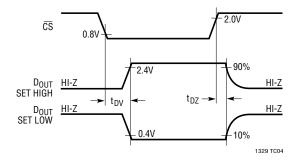
#### Voltage Waveforms for tpo



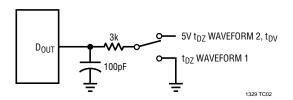
### Load Circuit for t<sub>DO</sub>



### Voltage Waveforms for t<sub>DZ</sub>, t<sub>DV</sub>



### Load Circuit for t<sub>DZ</sub>, t<sub>DV</sub>





# SERIAL I/O OPERATING SEQUENCE

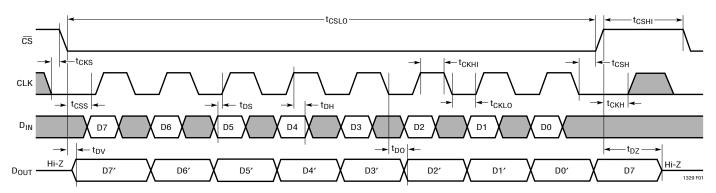


Figure 1. 3-Wire Interface Timing Specification

### APPLICATIONS INFORMATION

#### **8-BIT CURRENT OUTPUT DAC**

The LTC1329-10/LTC1329-50/LTC1329A-50 are 8-bit. current output digital-to-analog (DAC) converters. For each part, the 8-bit DAC output is guaranteed monotonic and is digitally adjustable in 256 equal steps. Upon power up, the internal DAC register resets to 10000000B and the DAC output assumes midrange. The current output  $(I_{OUT})$ can be biased from -15V to 2V or -15V to 2.5V in 3.3V and 5V systems, respectively. The LTC1329-10 features a fullscale output of  $10\mu A$  trimmed to  $\pm 3\%$  at room temperature ( $\pm 5\%$  over temperature), while the LTC1329-50 features a 50 $\mu$ A full scale and two accuracy grades;  $\pm 1\%$ at room temperature ( $\pm 2\%$  over temperature) for the LTC1329A-50 and  $\pm 3\%$  at room temperature ( $\pm 5\%$  over temperature) for the LTC1329-50. All versions include a flexible serial digital interface which allows easy interconnection to a variety of digital systems.

#### DIGITAL INTERFACE

#### **Automatic Mode Selection**

The LTC1329 family includes a serial interface capable of communicating with the host system using one of three protocols; standard 3-wire mode, a 2-wire up/down pulse mode and a 1-wire increment-only pulse mode. The LTC1329 family is designed to auto-configure itself depending on the way data is presented to it. A diagram illustrating this auto detection behavior is shown in Figure 2. At power-up, the interface is set to 1-wire pulse mode.

If the CS line ever goes low (as it will at the beginning of a valid 3-wire serial transfer) the chip immediately reconfigures itself into 3-wire mode and remains in this mode until the next time the power is cycled. If  $\overline{CS}$  stays high, the LTC1329 family stays in pulse mode and watches the UP/DN pin to determine whether to switch to 2-wire mode. If UP/DN ever goes low (as it will the first time a "down" command is given) the chip switches into 2-wire pulse mode and remains in this mode until the next time the power is cycled. In a properly configured 1-wire system.  $\overline{CS}$  and  $\overline{UP}/\overline{DN}$  will stay high continuously and the LTC1329-10/LTC1329-50/LTC1329A-50 will remain in 1wire pulse mode. 2-wire pulse mode systems should give a single "down" pulse sometime before the first data pulses are sent to prevent the LTC1329 family from staying in 1-wire mode if the first several pulses happen to be "ups".

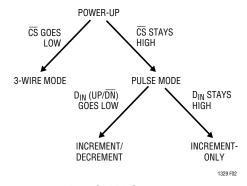


Figure 2. LTC1329 Operating Modes



### APPLICATIONS INFORMATION

#### Standard 3-Wire Mode (Figure 3)

Refer to the Serial Interface Operating Sequence in Figure 1. When operating in 3-wire mode, the LTC1329-10/LTC1329-50/LTC1329A-50 will interface directly with most standard 3- or 4-wire serial interface systems. The clock (CLK) input synchronizes the data transfer with each input bit captured at the rising edge of CLK and each output data bit shifted out through  $D_{OUT}$  at the falling edge. A falling edge at  $\overline{CS}$  initiates the data transfer and brings the  $D_{OUT}$  pin out of three-state. The serial 8-bit data representing the new DAC setting is shifted into the  $D_{IN}$  pin. Simultaneously, the previous DAC setting is shifted out of the  $D_{OUT}$  pin. After the new data is shifted in, a rising edge at  $\overline{CS}$  transfers the data from the input shift register into the DAC register. The DAC output assumes the new value and the  $D_{OUT}$  pin returns to a high-impedance state.

I<sub>OUT</sub> = (B7 B6 B5 B4 B3 B2 B1 B0)I<sub>FULLSCALE</sub>/255

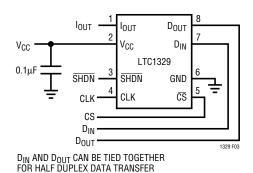


Figure 3. 3-Wire Mode; Serial Interface

## 1-Wire Interface (Pulse Mode, Figure 4)

In 1-wire pulse mode, each rising edge at CLK increments the upper six bits of the DAC register by one count. When incramented beyond 11111100B, the counter rolls over and sets the DAC to the minimum value (00000000B). In this way, a single pulse applied to CLK increases the DAC output by a single 4-LSB step and 63 pulses decrease the DAC output by one step. The last two LSBs are always zero in pulse mode.

(3-Wire Control by CS, CLK and D<sub>IN</sub>)

I<sub>OUT</sub> = (B7 B6 B5 B4 B3 B2 0 0)I<sub>FULLSCALF</sub>/255

To configure the LTC1329-10/LTC1329-50/LTC1329A-50 in 1-wire pulse mode, tie both the  $\overline{CS}$  and D IN pins to V CC.

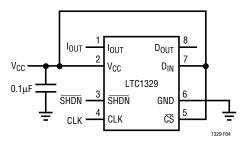


Figure 4. Pulse Mode: Increment Only (1-Wire Control by CLK)

### 2-Wire Interface (Pulse Mode, Figure 5)

In 2-wire pulse mode, a logic HIGH at  $UP/\overline{DN}$  programs the DAC register to increment and each rising edge at CLK increments the upper six bits of the register by one count. Similarly, a logic LOW at  $UP/\overline{DN}$  set the DAC register to decrement and a rising edge at CLK decrements the upper six bits of the register by one count. Each count in 2-wire mode changes the DAC output by a single four LSB step. The DAC register stops incramenting at 11111100B and stops decrementing at 00000000B and will not roll over in 2-wire pulse mode. The last two LSBs are always zero in pulse mode.

 $I_{OUT} = (B7 B6 B5 B4 B3 B2 0 0)I_{FULLSCALE}/255$ 

To configure the LTC1329-10/LTC1329-50/LTC1329A-50 in 2-wire pulse mode, tie  $\overline{\text{CS}}$  to  $V_{\text{CC}}$  and bring the UP/ $\overline{\text{DN}}$  pin low at least once during power-up.

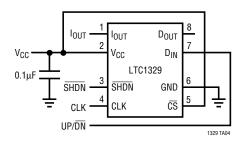
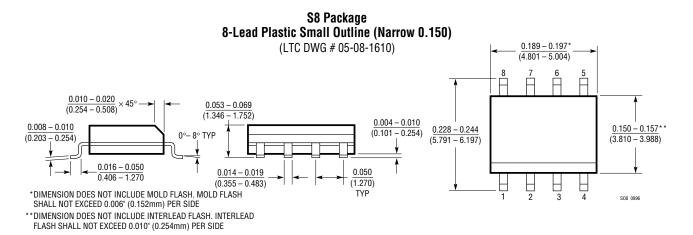


Figure 5. Pulse Mode; Increment/Decrement (2-Wire Control by CLK and UP/DN)

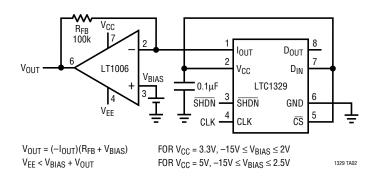


# PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

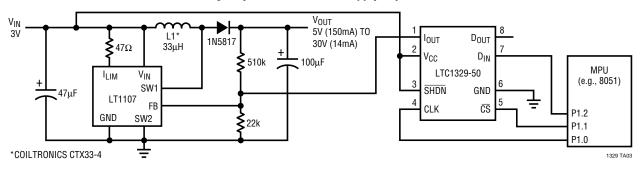


## TYPICAL APPLICATIONS

#### Pulse Mode: Increment-Only (1-Wire Control by CLK) with Voltage Output



### **Digitally Controlled Power Supply Adjustment**



## **RELATED PARTS**

PART NUMBER	DESCRIPTION	COMMENTS
LTC1451	12-Bit Micropower Serial Input V <sub>OUT</sub> DAC	Higher Resolution, 8-Pin SO
LTC1452	12-Bit Multiplying Serial Input V <sub>OUT</sub> DAC	Higher Resolution, 8-Pin SO
LTC8043	12-Bit Multiplying Serial Input I <sub>OUT</sub> DAC	Higher Resolution, 8-Pin SO

### **ПОСТАВКА** ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

# Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

#### http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

#### Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru\_6 moschip.ru 4 moschip.ru 9