# **Dual Matched General Purpose Transistor**

# **NPN Matched Pair**

These transistors are housed in an ultra-small SOT-363 package ideally suited for portable products. They are assembled to create a pair of devices highly matched in all parameters, eliminating the need for costly trimming. Applications are Current Mirrors; Differential, Sense and Balanced Amplifiers; Mixers; Detectors and Limiters. Complementary PNP equivalent NST65010MW6T1G is available.

#### **Features**

- Current Gain Matching to 10%
- Base-Emitter Voltage Matched to 2 mV
- Drop-In Replacement for Standard Device
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V <sub>CEO</sub>	65	V
Collector - Base Voltage	V <sub>CBO</sub>	80	V
Emitter-Base Voltage	V <sub>EBO</sub>	6.0	V
Collector Current – Continuous	I <sub>C</sub>	100	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation Per Device FR-5 Board (Note 1) $T_{\Delta} = 25^{\circ}C$	P <sub>D</sub>	380 250	mW
Derate Above 25°C		3.0	mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	328	°C/W
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

1.  $FR-5 = 1.0 \times 0.75 \times 0.062$  in

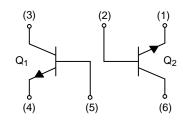


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SOT-363 CASE 419B STYLE 1



# **MARKING DIAGRAMS**



2G = Device Code M = Date Code

= Pb–Free Package

(Note: Microdot may be in either location)

# ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NST65011MW6T1G	SOT-363 (Pb-Free)	3,000 / Tape & Reel
NSVT65011MW6T1G	SOT-363 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Min	Тур	Max	Unit
V <sub>(BR)CEO</sub>	65	_	-	V
V <sub>(BR)CES</sub>	80	_	_	V
V <sub>(BR)CBO</sub>	80	_	_	V
V <sub>(BR)EBO</sub>	6.0	_	_	V
I <sub>CBO</sub>	_ _	_ _	15 5.0	nA μA
h <sub>FE</sub>	150 200 0.9	- 300 1.0	- 500 1.1	_
V <sub>CE(sat)</sub>	_ _	_ _	250 600	mV
V <sub>BE(sat)</sub>	700 850	750 890	800 950	mV
V <sub>BE(0n)</sub> V <sub>BE(1) -</sub> V <sub>BE(2)</sub>	580 - -	660 _ 1.0	700 770 2.0	mV
f <sub>T</sub>	100	-	-	MHz
C <sub>ob</sub>	-	-	4.5	pF
NF	_	-	10	dB
	V(BR)CEO V(BR)CES V(BR)CBO V(BR)EBO ICBO  hFE hFE(1)/hFE(2) VCE(sat)  VBE(on) VBE(1) - VBE(2)	V(BR)CEO   65     V(BR)CES   80     V(BR)CBO   80     V(BR)EBO   6.0     ICBO   -     -     hFE	V(BR)CEO   65	V(BR)CEO         65         -         -           V(BR)CES         80         -         -           V(BR)CBO         80         -         -           V(BR)EBO         6.0         -         -           ICBO         -         -         15           -         -         -         5.0    PRE 150

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2.  $h_{FE(1)}/h_{FE(2)}$  is the ratio of one transistor compared to the other transistor within the same package. The smaller  $h_{FE}$  is used as numerator.

3.  $V_{BE(1)} - V_{BE(2)}$  is the absolute difference of one transistor compared to the other transistor within the same package.

## **TYPICAL CHARACTERISTICS**

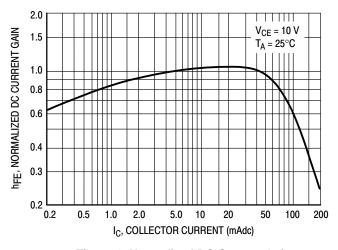


Figure 1. Normalized DC Current Gain

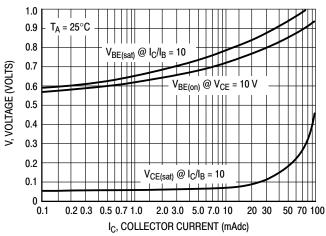


Figure 2. "Saturation" and "On" Voltages

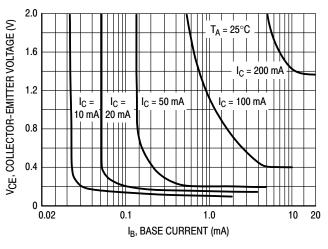


Figure 3. Collector Saturation Region

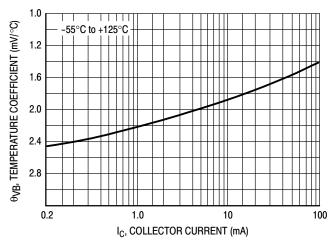


Figure 4. Base-Emitter Temperature Coefficient

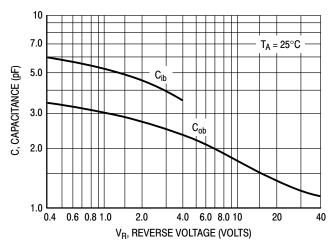


Figure 5. Capacitances

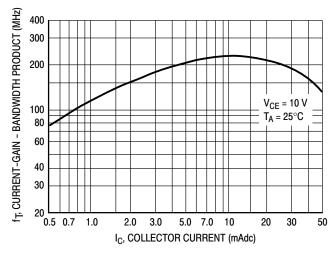


Figure 6. Current-Gain - Bandwidth Product

# **TYPICAL CHARACTERISTICS**

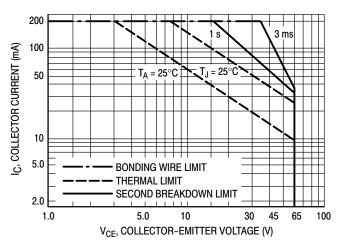


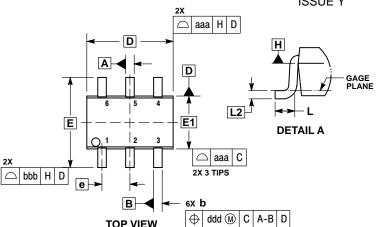
Figure 7. Active Region Safe Operating Area

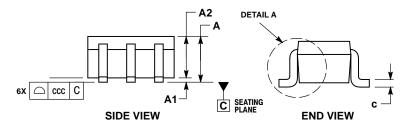
The safe operating area curves indicate  $I_C$ – $V_{CE}$  limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 7 is based upon  $T_{J(pk)} = 150$ °C;  $T_{C}$  or  $T_{A}$  is variable depending upon conditions.

#### PACKAGE DIMENSIONS

## SC-88 (SOT-363) CASE 419B-02 **ISSUE Y**





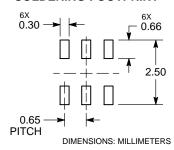
#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
  DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRU-SIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.

- DATUMS A AND B ARE DETERMINED AT DATUM H.
  DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
- ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDI-TION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α			1.10			0.043	
A1	0.00		0.10	0.000		0.004	
A2	0.70	0.90	1.00	0.027	0.035	0.039	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С	0.08	0.15	0.22	0.003	0.006	0.009	
D	1.80	2.00	2.20	0.070	0.078	0.086	
E	2.00	2.10	2.20	0.078	0.082	0.086	
E1	1.15	1.25	1.35	0.045	0.049	0.053	
е	0.65 BSC			0.026 BSC			
L	0.26	0.36	0.46	0.010	0.014	0.018	
L2	0.15 BSC			0.006 BSC			
aaa	0.15			0.006			
bbb	0.30			0.012			
ccc	0.10			0.004			
ddd	0.10			0.004			

#### RECOMMENDED **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. EMITTER 2 2 BASE 2
  - COLLECTOR 1 EMITTER 1

  - COLLECTOR 2

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